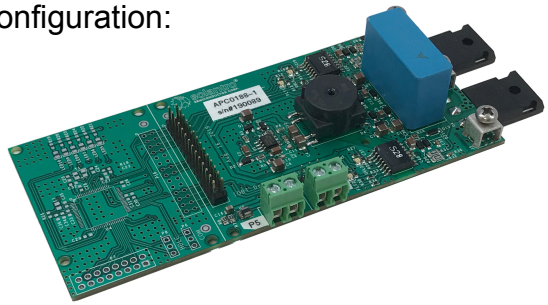
SA6880-S – Isolated 3.5 A / 1200 V IGBT Driver Evaluation Board

1. Introduction

The SA6880-S is a high performance isolated IGBT/MOSFET driver IC with 3.5 A peak output current capability. The SA6880-S evaluation board is designed to allow testing of two SA6880-S drivers in either a half bridge or a DC/DC synchronous buck configuration. For synchronous buck testing 1200 V / 380 V, a 15 mH inductor and 4.6 µF capacitor should be populated. The design was tested as described in this document. It has not been qualified to operate over a wide temperature range. The evaluation board is provided for functional testing and evaluation purposes only.

Evaluation board specifications for a synchronous buck configuration:

- Input voltage: 1200 V
- Output voltage: 380 V
- Output current: 0.4 A
- Operation frequency; 20 kHz
- Duty cycle: 0.34



2. SA6880-S – Features and Specifications

- Single-channel 1200 V isolated driver optimized for industrial and automotive applications.
- 3.5 A peak output current
- 3.75 kV_{RMS} input to output isolation voltage
- High common-mode transient immunity (CMTI): greater than 50 kV/µs
- Less than 115 ns propagation delay
- Less than ±20 ns pulse width distortion
- Integrated IGBT protection functions: Soft turn-off; Desaturation detection; Active Miller-Current clamp; High Side Under voltage lockout protection with feedback; Fault sensing/reporting to system controller (DESAT & UVLO)
- TTL compatible inputs
- Automotive temperature range: - 40° C to +125° C
- Bipolar or unipolar supply operation
- Wide 30 V output supply range
- UL1577 certified to V_{ISO} = 3750 V_{RMS} for 60 seconds.
- IEC60747-17 and VDE 0884-10 compliant

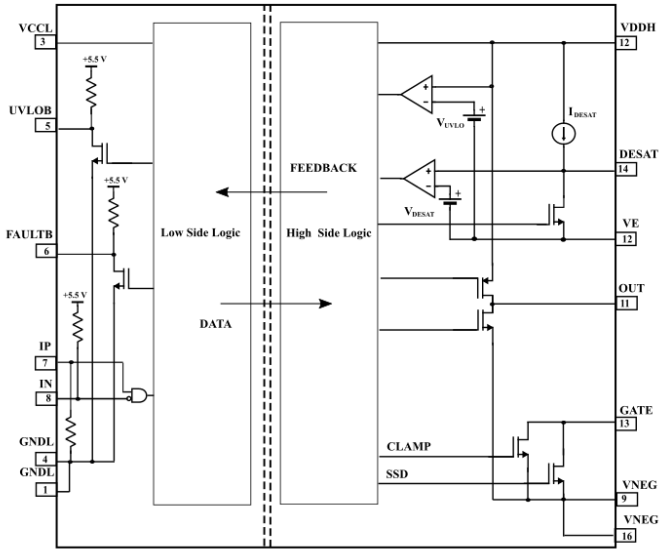


Figure 1 - Simplified block diagram of SA6880-S and pin descriptions

PIN	Name	Description
1	GNDL	Low side (LS) ground return
2	NC	No connect – (note: ***Connect to GND*** *to prevent damage to the IC.*)
3	VCCL	Low side (LS) power supply
4	NC or GNDL	This pin should either be left No connect or tied to Low Side (LS) ground return
5	UVLO	Under voltage lock-out. Open drain active LOW output
6	FAULTB	Desaturation (Over-current protection) Fault. Open Drain active LOW output
7	IP	Non-inverting driver input. The IP input controls signal for the driver output while IN is set to low. The IGBT/MOSFET is turned on when IP is set to high and IN is set to low, otherwise it is turned off. A minimum pulse width is required to suppress glitches while controlling the IGBT/MOSFET. An internal pull-down resistor ensures that the IGBT/MOSFET is kept in off-state if terminal IP is left unconnected.
8	IN	Inverting driver input. IN- control signals for the driver output while IP is set to high. The IGBT/MOSFET is turned on when IN- is set to low, and is turned off when IN- is set to high, while IN is kept high.
9	VNEG	High side (HS) negative supply voltage (Ref. VNEG）
10	GATE	Gate connection for Miller current clamp and SSD (soft-shutdown) pull down
11	OUT	Driver output
12	VDDH	High side (HS) positive supply
13	VE	Connected to IGBT emitter /MOSFET source
14	DESAT	Desaturation over-current sensing input
15	NC	No connect. For factory test only

16	VNEG	High side negative supply voltage (Ref. VNEG)

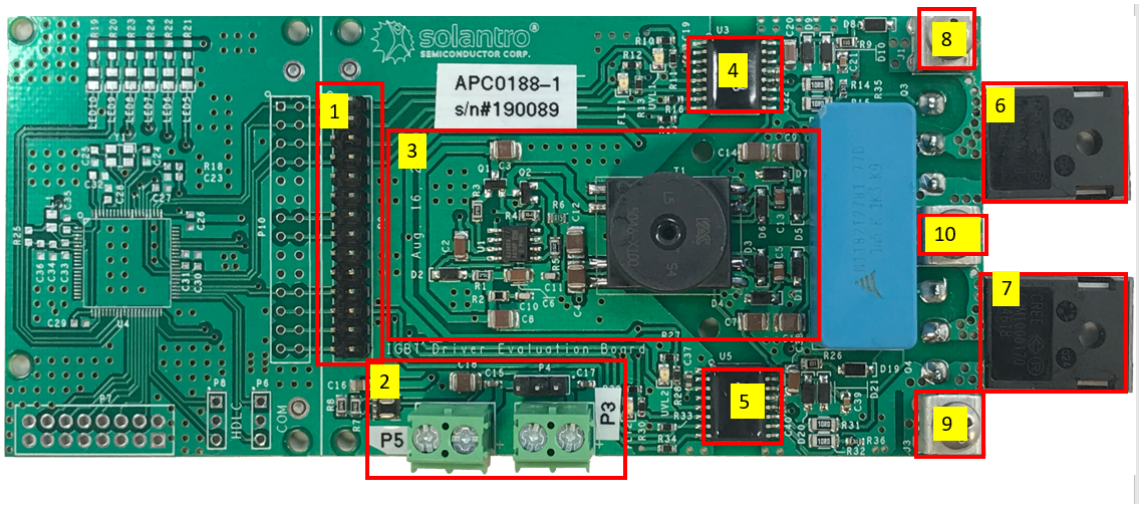
Warnings

There are exposed, high voltages on the SA6880-S evaluation board. It should only be operated by experienced power supply professionals. The SA6880-S evaluation board surfaces may be hot during operation. Do not touch. To evaluate this board as safely as possible, the following test configuration must be used:

- Follow the power-up and test procedure below.
- Only use isolated oscilloscope probes.
- Use isolated test equipment for the high side, with appropriate overcurrent and overvoltage protection.

3. Setting up the SA6880-S evaluation board

Before using the SA6880-S evaluation board, make a visual inspection to ensure that the board is in good condition, with no visible damage. See Figure 2 for a picture of the SA6880-S evaluation board and major blocks.



1	Driver control signals	6	HS IGBT[1] or SiC MOSFET[2]
2	Power supply connectors	7	LS IGBT[1] or SiC MOSFET[2]
3	Isolated power supplies	8	High voltage DC(+) power supply connector
4	HS driver	9	High voltage DC(-) power supply connector
5	LS driver	10	Jumper for an inductor

Figure 2 - SA6880-S evaluation board

Note:

1. IGBT switch: IGBT 1200V 80A 483W TO247-3
   https://www.infineon.com/dgdl/IKW40N120H3_Rev1_2G.pdf?folderId=db3a30431c69a49d011c6f86019b00a1&fileId=db3a304325305e6d012591d4832f7032
2. SiC MOSFET N-CH 1700V 4.9A TO247
   https://www.wolfspeed.com/downloads/dl/file/id/173/product/13/c2m1000170d.pdf

3.1 Power connection

To power the SA6880-S evaluation board, connect a 12 V DC power supply with 0.20 mA current limit to connector P3. Short pins 1 and 2 of jumper P4 (be careful with the polarity of the power supply).

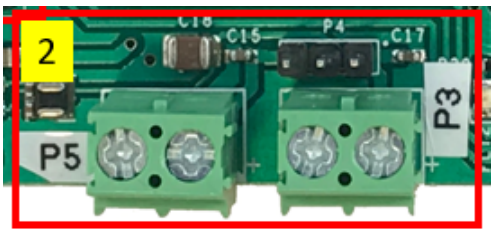


Figure 3 - 12 V power supply connection

The 12 V supply is connected to the low side of the two drivers (pins VCCL). It also provides power for the following power rails:

- 3.3 V for powering the LED showing the drivers FAOLT and UVLO signals;
- two -8 V for supplying isolated voltages to drivers' high side VNEG (negative supply voltage).
- two 17 V for supplying isolated voltages to drivers' high side VDDH (positive supply voltage).

3.2 Drivers' IP and IN inputs and UNLOB and FAULTB outputs

The inputs, IN and IP, and the outputs, UVLOB and FAULTB, for the LS drivers are connected to the dual pin header connector P9. The connector P9 is shown in *Figure 4*.

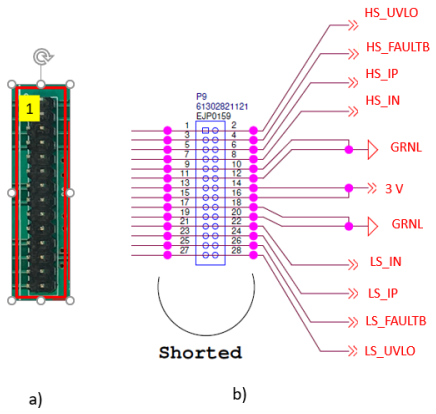


Figure 4 - Connector P9: a) picture b) schematic

The drivers' input signals are TTL signals and can be from a signal generator, microcontroller, or FPGA.

3.3 Power for the half bridge

Figure 5 shows the half bridge of the SA6880-S evaluation board. The half bridge can be supplied up to 1200 V. The power supply DC(+) must be connected to J1(8 in the picture) and the supply DC(-) to J3(9 in the picture). The switching node is J23(10 in the picture).

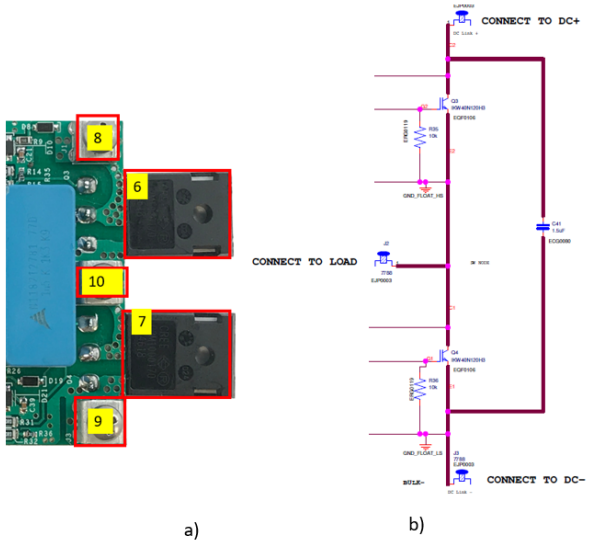


Figure 5 - Half bridge: a) picture b) circuit

4. External Components - Design Considerations

Figure 6 shows a SA6880-S recommended application circuit. Capacitors C1 and C2 are decoupling capacitors (recommended value = 1 µF). Capacitors C3 and C4 are decoupling capacitors (recommended

value = 10 µF). Pull-up resistors, R3 and R4 (recommended value = 3.3 kΩ) ensure the low side outputs are high when no faults are detected.

Gate resistor R_G limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The DESAT circuit (overcurrent protection) includes a high voltage diode D1, resistor R1, capacitor C5 and diode D2.

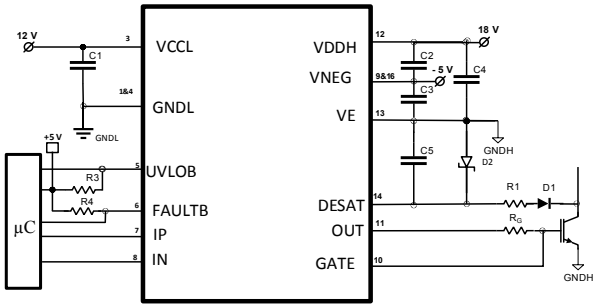


Figure 6 - SA6880-S recommended application circuit

4.1 Gate resistor design

The gate resistor R_G is located between the driver output and the gate of the power device (IGBT or SiC MOSFET). It plays a critical role in limiting the noise, ringing and oscillations in the gate drive loop due to parasitic inductance and capacitance. Figure 7 shows a simplified circuit of the gate drive loop. The resistance R'_G combines the internal turn ON (OFF) resistance R_{DS_ON} (R_{DS_OFF}), the external gate resistance R_G, and the switch internal gate resistance R_{IG}.

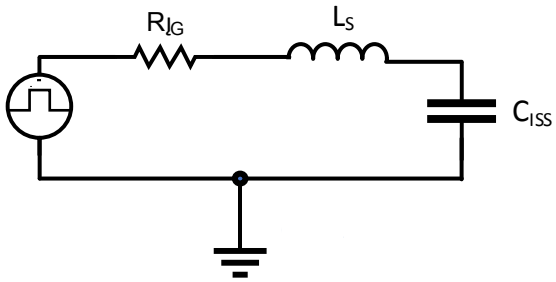


Figure 7- Simplified circuit of the gate drive loop.

The gate resistor has two major roles. Firstly, to limit the peak source/sink driver output currents turning the switching device (IGBT / SiC MOSFET) ON/OFF. Secondly, to limit the slew rate (rise/fall times) of the IGBT / SiC MOSFET output current and voltage. This is done by limiting the currents charging and discharging the power device's input capacitance which influence the power device's switching speed. Too small gate resistance R_G results in an overshoot in the gate drive voltage waveform, while a higher resistor value overdamps the oscillation and slows down the power device turn ON and OFF. The smaller the R_G, the faster rise and fall times are. Selecting the right value for R_G depends on the device being driven (IGBT or SiC MOSFET). A recommended value for the external gate resistance R_G is between 5 and 10 Ω depending on the switching device.

4.2 Desaturation circuit design

The DESAT fault detection circuit aims to indirectly detect overcurrent in the power switch by sensing the voltage across the device (V_{CE} for IGBT or V_{DS} for SiC MOSFET). In the case of IGBT, the voltage across the device (V_{CE}) when fully ON is approximately $V_{CE\ SAT}$ (typically 2 V). In a fault condition (over-current, short-circuit), V_{CE} increases and desaturation occurs. A preset limit can be set as a trip point to shut down the IGBT prior to damage occurring due to DESAT. The default internal reference voltage for DESAT in the SA6880 is 6.5 V. This means, if the voltage at the DESAT pin exceeds 6.5 V, the driver output turns OFF instantaneously with a soft shutdown. A FAULT feedback is triggered with a short delay to alert the microcontroller to take further actions.

In the DESAT circuit, resistor R1 (recommended value = 1 kΩ) and diode D1 limit the current flowing in and out of the DESAT pin. The breakdown voltage of diode D1 should be the same as the IGBT or MOSFET. When the IGBT is turned ON, a current source inside the driver starts charging the blanking capacitor C5. During normal operation, the IGBT's forward voltage is smaller than the DESAT threshold voltage and the capacitor is clamped at the forward voltage. When a short circuit occurs, the capacitor voltage starts to increase to the DESAT threshold voltage which triggers a shutdown of the IGBT. The time for charging the capacitor to the DESAT threshold voltage, V_{DESAT}, is called the blanking time, t_{BLANK}. The blanking time is set by the value of blanking capacitor C5, the charging current I_{CHARGE} and the DESAT threshold voltage V_{DESAT_TR}

$$t_{BLANK} = C5\frac{V_{DESAT\_TR}}{I_{CHARGE}}$$

The blanking time can be controlled by C5 capacitance. A recommended value for the blanking capacitor for IGBTs is 220 pF, but can be adjusted according to the switching device being used.

When using a SiC MOSFET the designer should design the DESAT circuit with a shorter blanking time in order to protect the MOSFET due to the fast fall time during turn ON. In addition, the designer should find out the acceptable MOSFET DESAT voltage, V_{DESAT_MOSFET}, which indicates the overcurrent in the MOSFET. If it is smaller than V_{DESAT_TR}, additional diodes in in series with D1 can be added for compensation:

$$V_{DESAT\_TR} = V_{DESAT\_MOSFET} + nV_F + R_{DESAT} \times I_{CHARGE}$$

where *n* is the diode number and V_F is the forward diode voltage drop.

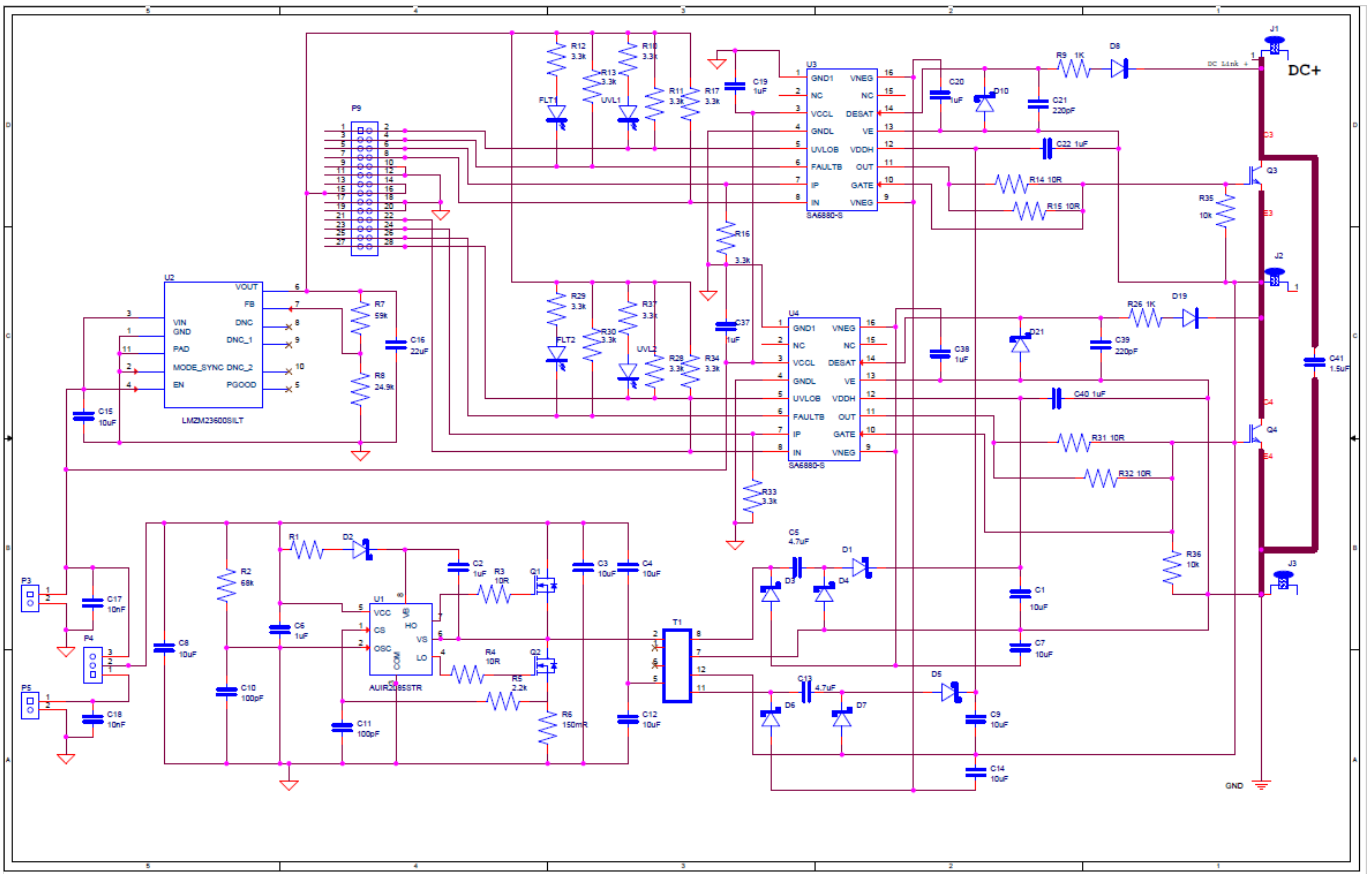
$$V_{DESAT\_MOSFET} = R_{DS\ ON} \times I_{D\ overcurrent}$$

Diode D2 prevents the voltage on the DESAT pin from falling 0.4 V below the voltage on VE pin.

5. Schematics, Assembly Drawing and Bill of Materials

The schematics, Assembly Drawing and Bill of Materials are included in the sections below.

5.1 SA6880-S evaluation board - schematic



5.2 SA6880-S evaluation board - assembly drawing