

CCM-PFC

ICE1PCS01

ICE1PCS01G

Standalone Power Factor
Correction (PFC) Controller in
Continuous Conduction Mode
(CCM)

Power Management & Supply



Never stop thinking.

CCM-PFC**Revision History:****2007-02-06**Datasheet

Previous Version: V1.2

Page	Subjects (major changes since last revision)
	Update package information

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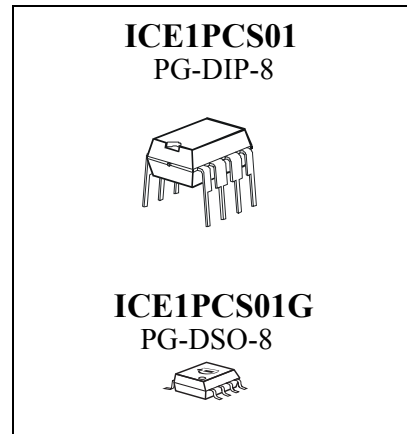
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Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

Product Highlights

- Wide Input Range
- Output Power Controllable by External Sense Resistor
- Programmable Operating Frequency
- Output Under-Voltage Detection
- Fast Output Dynamic Response during LoadJumps
- Pb-free lead plating; RoHS compliant



Features

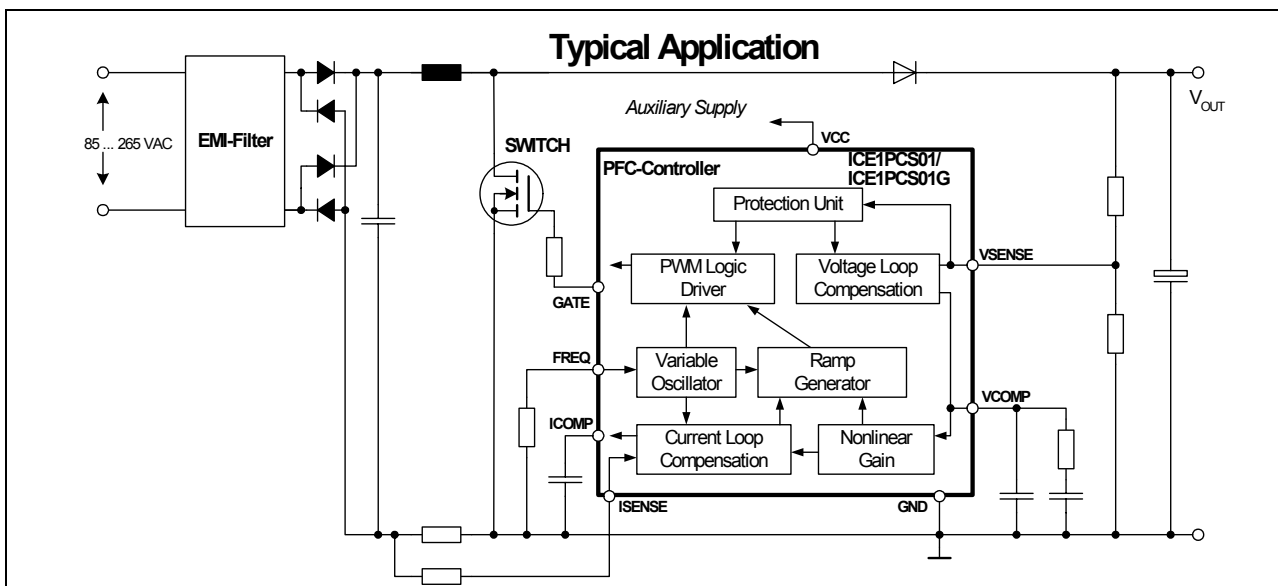
- Ease of Use with Few External Components
- Supports Wide Range
- Average Current Control
- External Current and Voltage Loop Compensation for Greater User Flexibility
- Programmable Operating/Switching Frequency (50kHz - 250kHz)
- Max Duty Cycle of 95% (typ) at 125kHz
- Trimmed Internal Reference Voltage (5V±2%)
- VCC Under-Voltage Lockout
- Cycle by Cycle Peak Current Limiting
- Over-Voltage Protection
- Open Loop Detection
- Output Under-Voltage Detection
- Brown-Out Protection
- Enhanced Dynamic Response
- Unique Soft-Start to Limit Start Up Current
- Fulfills Class D Requirements of IEC 1000-3-2

Description

The ICE1PCS01/G is a 8-pin wide input range controller IC for active power factor correction converters. It is designed for converters in boost topology, and requires few external components. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.

The IC operates in the CCM with average current control, and in DCM only under light load condition. The switching frequency is programmable by the resistor at pin 4. Both compensations for the current and voltage loop are external to allow full user control.

There are various protection features incorporated to ensure safe system operation conditions. Examples are peak current limitation, brown-out protection and output under voltage detection. The internal reference is trimmed (5V±2%) to ensure precise protection and control level. The device has a unique soft-start function which limits the start up current thus reducing the stress on the boost diode.



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ICE1PCS01	PG-DIP-8
ICE1PCS01G	PG-DSO-8

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1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	GND	IC Ground
2	ICOMP	Current Loop Compensation
3	ISENSE	Current Sense Input
4	FREQ	Switching Frequency Setting
5	VCOMP	Voltage Loop Compensation
6	VSENSE	V _{OUT} Sense (Feedback) Input
7	VCC	IC Supply Voltage
8	GATE	Gate Drive Output

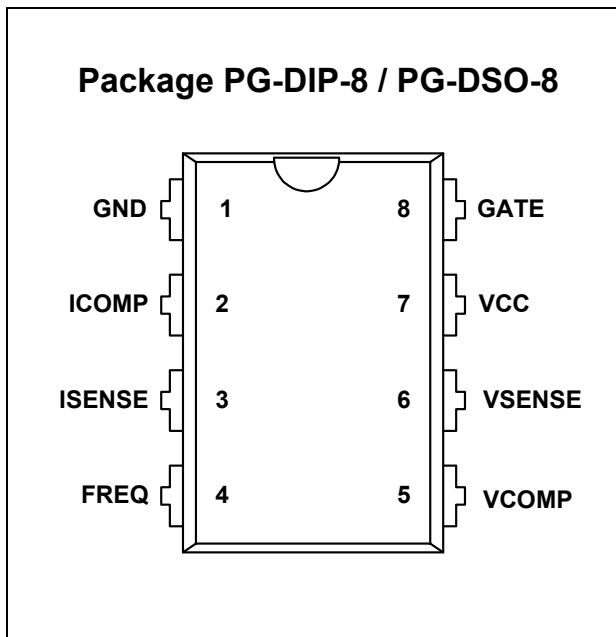


Figure 1 Pin Configuration (top view)

1.2 Pin Functionality

GND (Ground)

The ground potential of the IC.

ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA2 and averages the current sense signal.

ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor (R1). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

During power up time, high inrush currents cause high voltage drop at R1, driving currents into pin 3 which could be beyond the absolute maximum ratings. Therefore a series resistor (R2) of around 220Ω is recommended in order to limit this current into the IC.

FREQ (Frequency Setting)

This pin allows the setting of the operating switching frequency by connecting a resistor to ground. The frequency range is from 50kHz to 250kHz.

VSENSE (Voltage Sense/Feedback)

The output bus voltage is sensed at this pin via a resistive divider. The reference voltage for this pin is 5V.

VCOMP (Voltage Loop Compensation)

This pin provides the compensation of the output voltage loop with a compensation network to ground (see Figure 2). This also gives the soft start function which controls an increasing AC input current during start-up.

VCC (Power Supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply. The operating range is between 10V and 21V. The turn-on threshold is at 11.2V and under voltage occurs at 10.2V. There is no internal clamp for a limitation of the power supply.

GATE

The GATE pin is the output of the internal driver stage, which has a capability of 1.5A source and sink current. Its gate drive voltage is clamped at 11.5V (typically).

2 Representative Block diagram

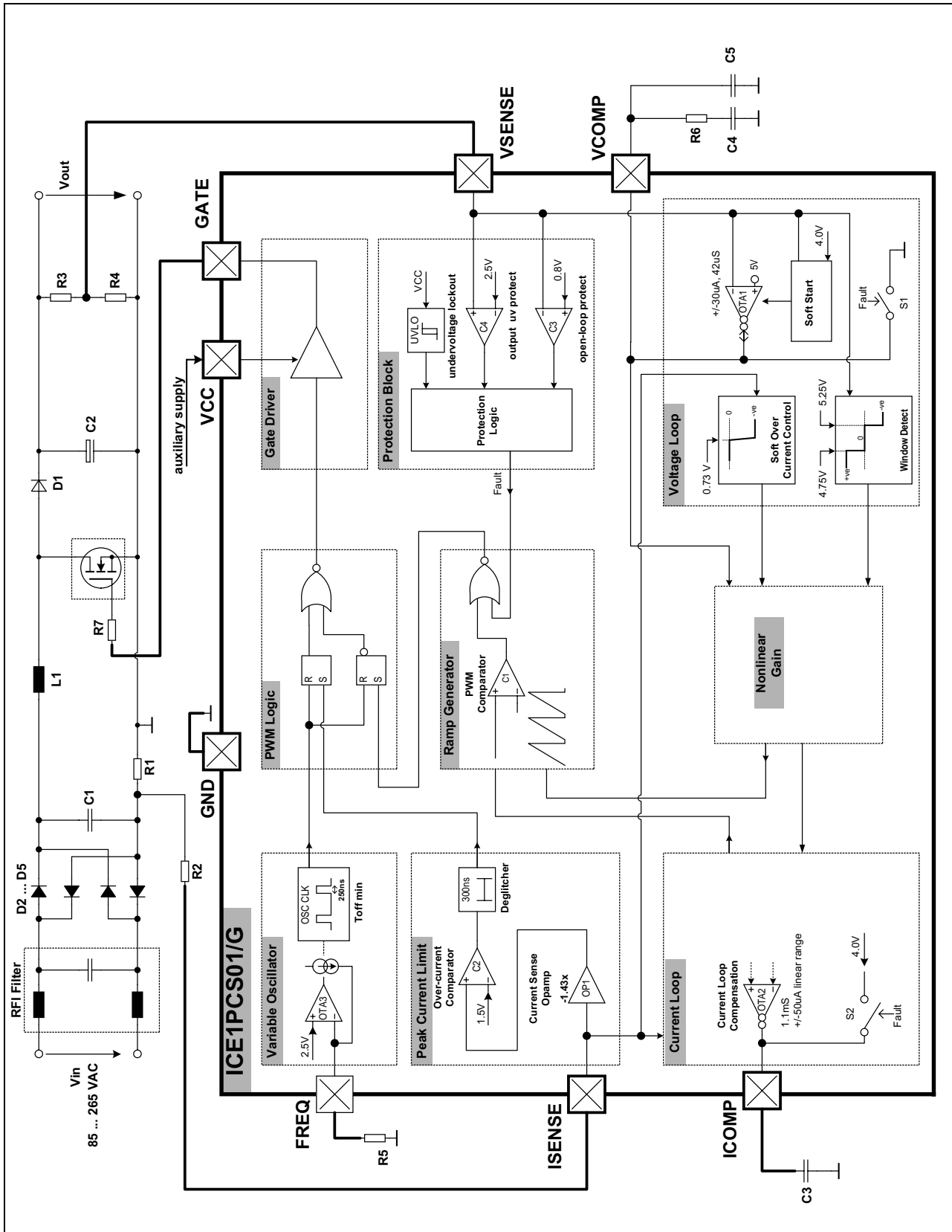


Figure 2 Representative Block diagram

3 Functional Description

3.1 General

The ICE1PCS01/G is a 8 pin control IC for power factor correction converters. It comes in both DIP and DSO packages and is suitable for wide range line input applications from 85 to 265 VAC. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control.

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM). In DCM, the average current waveform will be distorted but the resultant harmonics are still low enough to meet the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bus voltage. Depending on the load condition, OTA1 establishes an appropriate voltage at VCOMP pin which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device. Important protection features are namely Brown-out protection, Current Limitation and Output Under-voltage Protection.

3.2 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 11.2V and the voltage at pin 6 (VSENSE) is >0.8V, the IC begins operating its gate drive and performs its Soft-Start as shown in Figure 3.

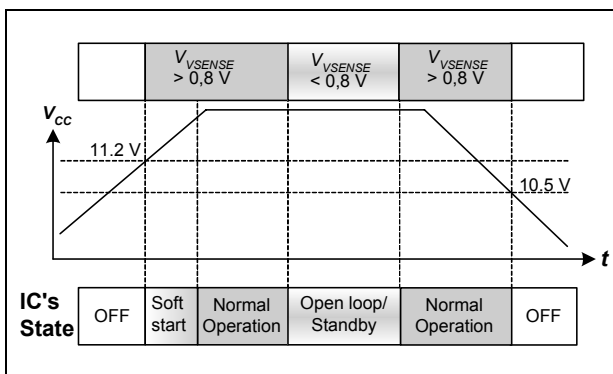


Figure 3 State of Operation respect to VCC

If VCC drops below 10.2V, the IC is off. The IC will then be consuming typically 200µA, whereas consuming 18mA during normal operation.

The IC can be turned off and forced into standby mode by pulling down the voltage at pin 6 (VSENSE) to lower than 0.8V. The current consumption is reduced to 3mA in this mode.

3.3 Start-up (Soft-Start)

Figure 4 and 5 show the operation of OTA1 during startup. It sources a constant 10.8µA into the compensation network at pin 5 (VCOMP). The voltage at this pin rises linearly and so does the amplitude of the input current. As soon as the output voltage V_{OUT} reaches 80% of its rated level, the startup procedure is finished and the normal voltage control takes over. In normal operation, the IC operates with a higher maximum current at OTA1 and therefore with a higher voltage loop gain in order to improve the dynamic behavior of the device.

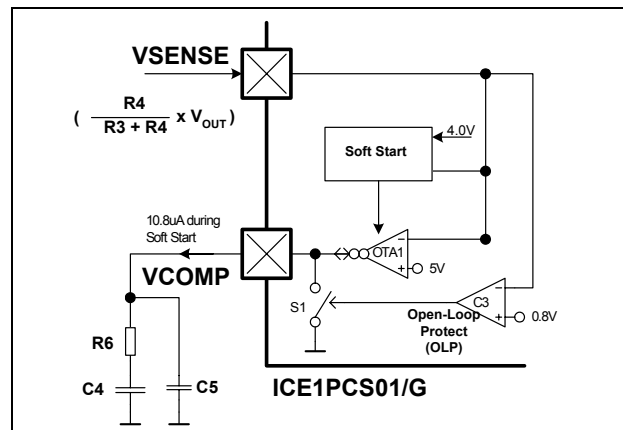


Figure 4 Soft Start Circuit

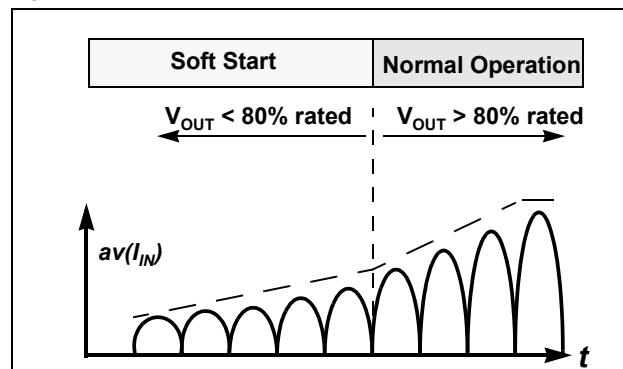


Figure 5 Soft Start with controlled current

The advantage of this technique is a soft-start function with lower stress for the boost diode but without the risk of audible noise.

3.4 System Protection

The IC provides several protection features in order to ensure the PFC system in safe operating range. Depending on the input line voltage (V_{IN}) and output bus voltage (V_{OUT}), Figure 6 and 7 show the conditions when these protections are active.

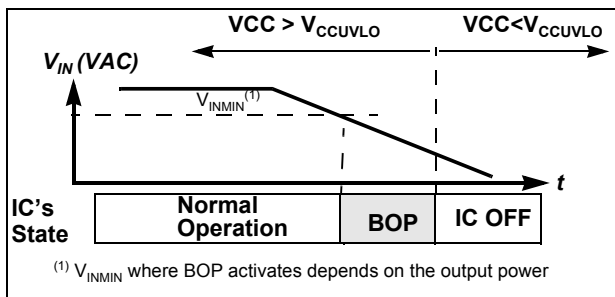


Figure 6 V_{IN} Related Protection Features

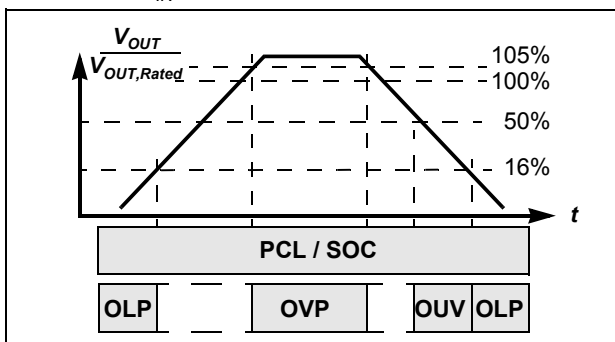


Figure 7 V_{OUT} Related Protection Features

The following sections describe the functionality of these protection features.

3.4.1 Brown-Out Protection (BOP)

Brown-out occurs when the input voltage V_{IN} falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the V_{CCUVLO} level yet. For a system without BOP, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current. The ICE1PCS01/G limits internally the current drawn from the mains and therefore also limits the input power. The difference of input and output power will result in decreasing output voltage. If the condition prolongs, the decreasing V_{OUT} will terminate in output under voltage condition (OUV, 50% of rated), and the IC will be shut down (See section 3.4.5).

Figure 8 shows the occurrence of BOP in respect to the ISENSE voltage.

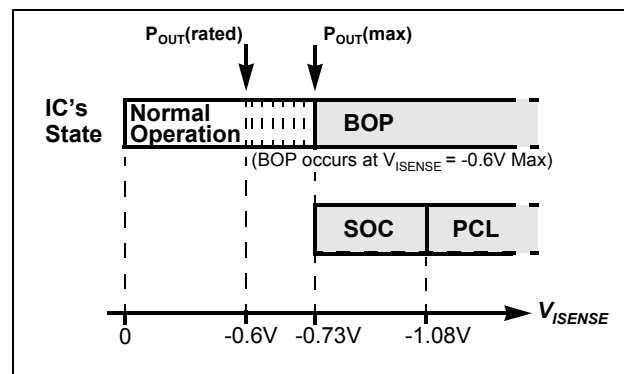


Figure 8 BOP, SOC and PCL Protection as function of V_{ISENSE}

The V_{IN} threshold for BOP to occur is dependent on the voltage at ISENSE and thus the output power. The rated output power with a minimum V_{IN} (V_{INMIN}) is

$$P_{OUT(rated)} = V_{INMIN} \times \frac{0.6}{R1 \cdot \sqrt{2}}$$

Due to the internal parameter tolerance, the maximum power with V_{INMIN} before BOP occurs is

$$P_{OUT(max)} = V_{INMIN} \times \frac{0.73}{R1 \cdot \sqrt{2}}$$

And the BOP takes over the normal operation under rated output power latest at an input voltage of

$$V_{BOPMAX} = P_{OUT(rated)} \times \frac{R1 \cdot \sqrt{2}}{0.73}$$

3.4.2 Soft Over Current Control (SOC)

The IC is designed **not** to support any output power that corresponds to a voltage lower than -0.73V at the ISENSE pin. A further increase in the inductor current, which results in a lower ISENSE voltage, will activate the Soft Over Current Control (SOC). This is a soft control as it does not directly switch off the gate drive like the PCL. It acts on the nonlinear gain block to result in a reduced PWM duty cycle.

3.4.3 Peak Current Limit (PCL)

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 3 (ISENSE) reaches -1.08V. This voltage is amplified by OP1 by a factor of -1.43 and connected to comparator C2 with a reference voltage of 1.5V as shown in Figure 9. A deglitcher with 300ns after the comparator improves noise immunity to the activation of this protection.

Functional Description

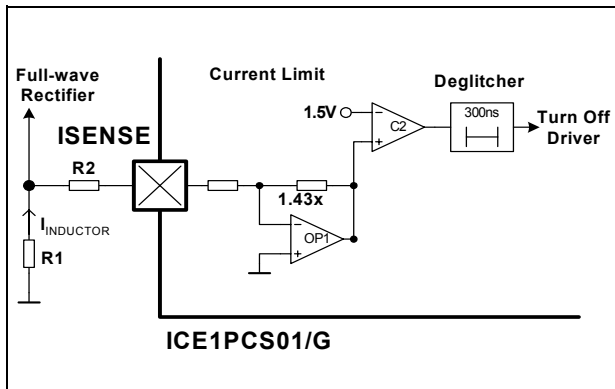


Figure 9 Peak Current Limit (PCL)

3.4.4 Open Loop Protection / Input Under Voltage Protect (OLP)

Whenever VSENSE voltage falls below 0.8V, or equivalently V_{OUT} falls below 16% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage V_{IN} for normal operation. In this case, most of the blocks within the IC will be shutdown. It is implemented using comparator C3 with a threshold of 0.8V as shown in the IC block diagram in Figure 2.

3.4.5 Output Under Voltage Detection (OUV)

In the event of main interrupt or brown-out condition, the PFC system is not able to deliver the rated output power. This will cause the output voltage V_{OUT} to drop below its rated value. The IC provides an output under voltage detection that checks if V_{OUT} is falling below 50% of its rated value. Comparator C4 as shown in the device block diagram (Figure 2) senses the voltage at pin 6 (VSENSE) with a reference of 2.5V. If comparator C4 trips, the IC will be shut down as in OLP. The IC will be ready to restart if there is sufficient V_{IN} to pull V_{OUT} out of OLP.

3.4.6 Over-Voltage Protection (OVP)

Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active as shown in Figure 7. This is implemented by sensing the voltage at pin VSENSE with respect to a reference voltage of 5.25V. A VSENSE voltage higher than 5.25V will immediately reduce the output duty cycle, bypassing the normal voltage loop control. This results in a lower input power to reduce the output voltage V_{OUT}.

3.5 Frequency Setting

The switching frequency of the PFC converter can be set with an external resistor R5 at FREQ pin. The pin voltage V_{FREQ} is typically 2.5V. The corresponding capacitor for the oscillator is integrated in the device and the R5/frequency relationship is given at the

“Electrical Characteristic” section. The recommended operating frequency range is from 50kHz to 250kHz. As an example, a R5 of 33kΩ at pin FREQ will set a switching frequency F_{SW} of 133kHz typically.

3.6 Average Current Control

3.6.1 Complete Current Loop

The complete system current loop is shown in Figure 10.

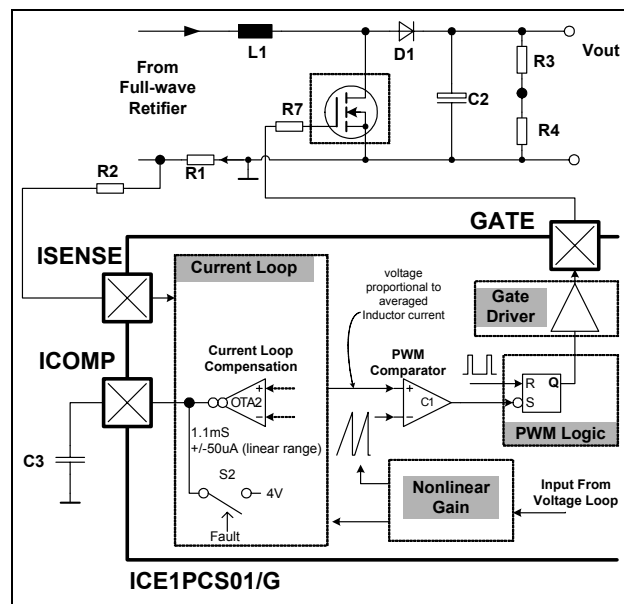


Figure 10 Complete System Current Loop

It consists of the current loop block which averages the voltage at pin ISENSE, resulted from the inductor current flowing across R1. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C1 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

3.6.2 Current Loop Compensation

The compensation of the current loop is done at the ICOMP pin. This is the OTA2 output and a capacitor C3 has to be installed at this node to ground (see Figure 10). Under normal mode of operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 5V in the event of IC shuts down when OLP and UVLO occur.

3.6.3 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction.

Functional Description

Assuming the voltage loop is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to V_{IN} . The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF} , and thus to the input voltage V_{IN} . Figure 11 shows the scheme to achieve the objective.

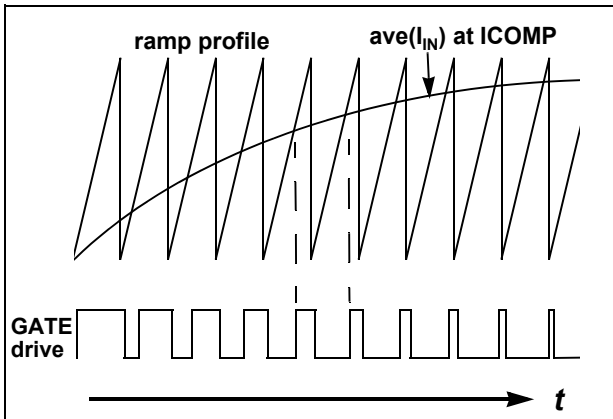


Figure 11 Average Current Control in CCM

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 5 (ICOMP). The PWM cycle starts with the Gate turn off for a duration of T_{OFFMIN} (250ns typ.) and the ramp is kept discharged. The ramp is then allowed to rise after T_{OFFMIN} expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF} .

Figure 12 shows the timing diagrams of T_{OFFMIN} and the PWM waveforms.

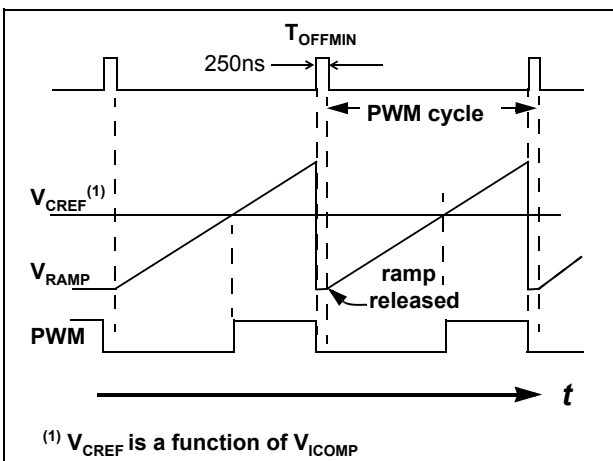


Figure 12 Ramp and PWM waveforms

3.6.4 Nonlinear Gain Block

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the voltage at pin VCOMP. This block has been designed to support the wide input voltage range (85-265VAC).

3.7 PWM Logic

The PWM logic block prioritizes the control input signals and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse T_{OFFMIN} , are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output under 133kHz of operation.

In case of high input currents which result in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal Toffmin resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 13.

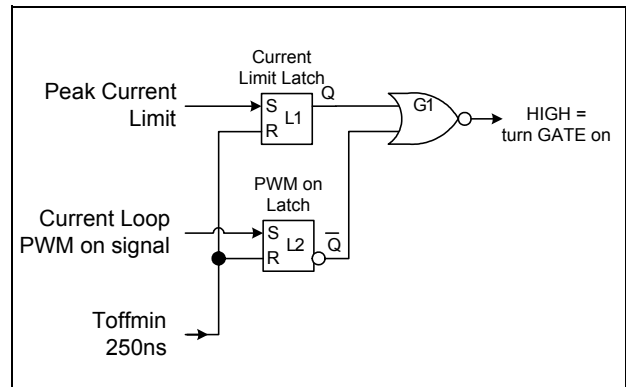


Figure 13 PWM Logic

3.8 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT} . This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from V_{OUT} . The pin VSENSE is the input of OTA1 which has an internal reference of 5V. Figure 14 shows the important blocks of this voltage loop.

3.8.1 Voltage Loop Compensation

The compensation of the voltage loop is installed at the VCOMP pin (see Figure 14). This is the output of OTA1 and the compensation must be connected at this pin to ground. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

Functional Description

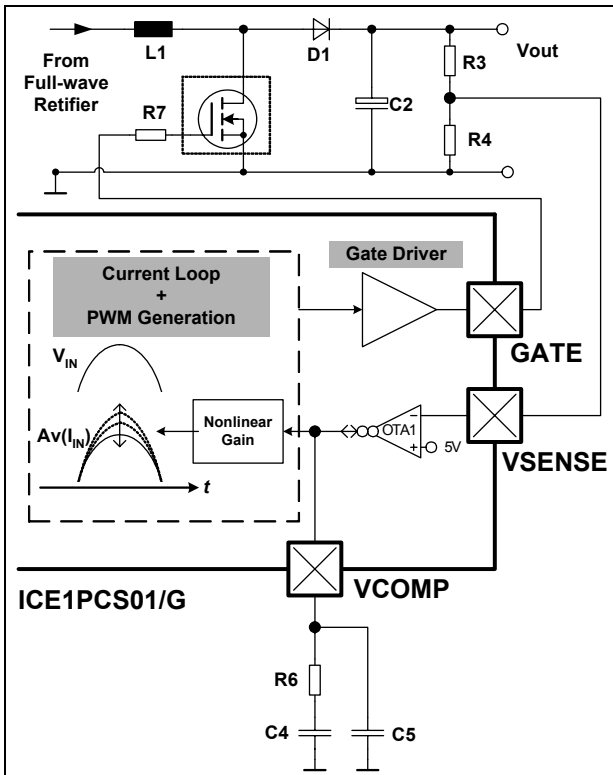


Figure 14 Voltage Loop

3.8.2 Enhanced Dynamic Response

Due to the low frequency bandwidth of the voltage loop, the dynamic response is slow and in the range of about several 10ms. This may cause additional stress to the bus capacitor and the switching transistor of the PFC in the event of heavy load changes.

The IC provides therefore a “window detector” for the feedback voltage V_{VSENSE} at pin 6 (VSENSE). Whenever V_{VSENSE} exceeds the reference value (5V) by $\pm 5\%$, it will act on the nonlinear gain block which in turn affect the gate drive duty cycle directly. This change in duty cycle is bypassing the slow changing VCOMP voltage, thus results in a fast dynamic response of V_{OUT} .

3.9 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 15) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 8 (GATE) is typically clamped at 11.5V.

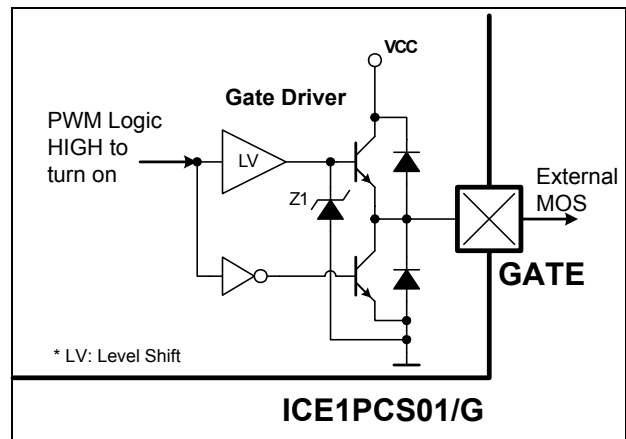


Figure 15 Gate Driver

The output is active HIGH and at VCC voltages below the under voltage lockout threshold V_{CCUVLO} , the gate drive is internally pull low to maintain the off state.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	-0.3	22	V	
FREQ Voltage	V_{FREQ}	-0.3	7	V	
ICOMP Voltage	V_{ICOMP}	-0.3	7	V	
ISENSE Voltage	V_{ISENSE}	-24	7	V	
ISENSE Current	I_{ISENSE}	-1	1	mA	Recommended R2=220Ω
VSENSE Voltage	V_{VSENSE}	-0.3	7	V	
VSENSE Current	I_{VSENSE}	-1	1	mA	R3>400kΩ
VCOMP Voltage	V_{VCOMP}	-0.3	7	V	
GATE Voltage	V_{GATE}	-0.3	22	V	Clamped at 11.5V if driven internally.
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient for DSO-8-3	$R_{thJA}(DSO)$	-	185	K/W	PG-DSO-8-3
Thermal Resistance Junction-Ambient for DIP-8-4	$R_{thJA}(DIP)$	-	90	K/W	PG-DIP-8-4
ESD Protection	V_{ESD}	-	2	kV	Human Body Model ¹⁾

¹⁾ According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	V_{CCUVLO}	21	V	
Junction Temperature	T_{JCon}	-40	125	°C	

Electrical Characteristics
4.3 Characteristics

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_j from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$. Typical values represent the median values, which are related to $25\text{ }^{\circ}\text{C}$. **If not otherwise stated, a supply voltage of $V_{CC} = 15\text{V}$ is assumed for test condition.**

4.3.1 Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Turn-On Threshold	V_{CCon}	10.5	11.2	11.9	V	
VCC Turn-Off Threshold/ Under Voltage Lock Out	V_{CCUVLO}	9.4	10.2	10.8	V	
VCC Turn-On/Off Hysteresis	V_{Cchy}	0.8	1	1.3	V	
Start Up Current Before V_{CCon}	$I_{CCstart}$	50	100	200	μA	$V_{VCC} = V_{VCCon} - 0.1\text{V}$
Operating Current with active GATE	I_{CCHG}	13.5	18	22.5	mA	$R5 = 33\text{k}\Omega$ $C_L = 4.7\text{nF}$
Operating Current during Standby	I_{CCStdy}	2.0	2.6	3.2	mA	$R5 = 33\text{k}\Omega$ $V_{VSENSE} = 0.5\text{V}$

4.3.2 Variable Frequency Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Frequency (Typical)	F_{SWnom}	106	133	161	kHz	$R5 = 33\text{k}\Omega$
Switching Frequency (Min.)	F_{SWmin}	40	56	70	kHz	$R5 = 82\text{k}\Omega$
Switching Frequency (Max.)	F_{SWmax}	200	250	320	kHz	$R5 = 15\text{k}\Omega$
Voltage at FREQ pin	V_{FREQ}	2.40	2.50	2.60	V	

Electrical Characteristics
4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max. Duty Cycle	D_{MAX}	92	95	98	%	$F_{SW} = F_{SWnom}$ ($R5 = 33k\Omega$)
Min. Duty Cycle	D_{MIN}			0	%	$V_{VCOMP} = 0V, V_{VSENSE} = 5V$ $V_{ICOMP} = 6.4V$
Min. Off Time	T_{OFFMIN}	150	250	350	ns	$V_{VCOMP} = 5V, V_{VSENSE} = 5V$ $V_{ISENSE} = 0.1V$

4.3.4 System Protection Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Open Loop Protection (OLP) VSENSE Threshold	V_{OLP}	0.77	0.81	0.86	V	
Peak Current Limitation (PCL) ISENSE Threshold	V_{PCL}	-1.15	-1.08	-1.00	V	
Soft Over Current Control (SOC) ISENSE Threshold	V_{SOC}	-0.79	-0.73	-0.66	V	
Output Under Voltage Detection (OUV) VSENSE Threshold	V_{OUV}	2.45	2.55	2.65	V	
Output Over-Voltage Protection (OVP)	V_{OVP}	5.12	5.25	5.38	V	

Electrical Characteristics
4.3.5 Current Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA2 Transconductance Gain	Gm_{OTA2}	0.9	1.1	1.3	mS	At Temp = 25°C
OTA2 Output Linear Range	I_{OTA2}		+/- 50		μA	Guaranteed by design
ICOMP Voltage during OLP	V_{ICOMP}	3.6	4.0		V	$V_{VSENSE} = 0.5V$

4.3.6 Voltage Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA1 Reference Voltage	V_{OTA1}	4.90	5.00	5.10	V	
OTA1 Transconductance Gain	Gm_{OTA1}	31.5	42	52.5	μS	
OTA1 Max. Source Current Under Normal Operation	I_{OTA1SO}	21	30	38	μA	$V_{VSENSE} = 4.25V$ $V_{VCOMP} = 4V$
OTA1 Max. Sink Current Under Normal Operation	I_{OTA1SK}	21	30	38	μA	$V_{VSENSE} = 6V$ $V_{VCOMP} = 4V$
Soft Start End	V_{SOFT}	3.80	4.00	4.20	V	
OTA1 Source Current Under Soft Start	I_{OTA1SS}	8.0	10.8	13.4	μA	$V_{VSENSE} = 2V$ $V_{VCOMP} = 0V$
Enhanced Dynamic Response VSENSE High Threshold	V_{Hi}	5.12	5.25	5.38	V	
VSENSE Low Threshold	V_{Lo}	4.63	4.75	4.87	V	
VSENSE Input Bias Current at 5V	I_{VSEN5V}	0		1.5	μA	$V_{VSENSE} = 5V$
VSENSE Input Bias Current at 1V	I_{VSEN1V}	0		1	μA	$V_{VSENSE} = 1V$
VCOMP Voltage during OLP	V_{VCOMP}	0	0.2	0.4	V	$V_{VSENSE} = 0.5V$ $I_{VCOMP} = 0.5mA$

Electrical Characteristics
4.3.7 Driver Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	V_{GATEL}	-	-	1.2	V	$V_{CC} = 5V$ $I_{GATE} = 5mA$
		-	-	1.5	V	$V_{CC} = 5V$ $I_{GATE} = 20mA$
		-	0.8	-	V	$I_{GATE} = 0A$
		-	1.6	2.0	V	$I_{GATE} = 20mA$
		-0.2	0.2	-	V	$I_{GATE} = -20mA$
GATE High Voltage	V_{GATEH}	-	11.5	-	V	$V_{CC} = 20V$ $C_L = 4.7nF$
		-	10.5	-	V	$V_{CC} = 11V$ $C_L = 4.7nF$
		-	7.5	-	V	$V_{CC} = V_{VCCoff} + 0.2V$ $C_L = 4.7nF$
GATE Rise Time	t_r	-	20	-	ns	$V_{Gate} = 2V \dots 9V$ $C_L = 4.7nF$
GATE Fall Time	t_f	-	20	-	ns	$V_{Gate} = 9V \dots 2V$ $C_L = 4.7nF$
GATE Current, Peak, Rising Edge	I_{GATE}	-1.5	-	-	A	$C_L = 4.7nF^{1)}$
GATE Current, Peak, Falling Edge	I_{GATE}	-	-	1.5	A	$C_L = 4.7nF^{1)}$

¹⁾ Design characteristics (not meant for production testing)

5 Outline Dimension

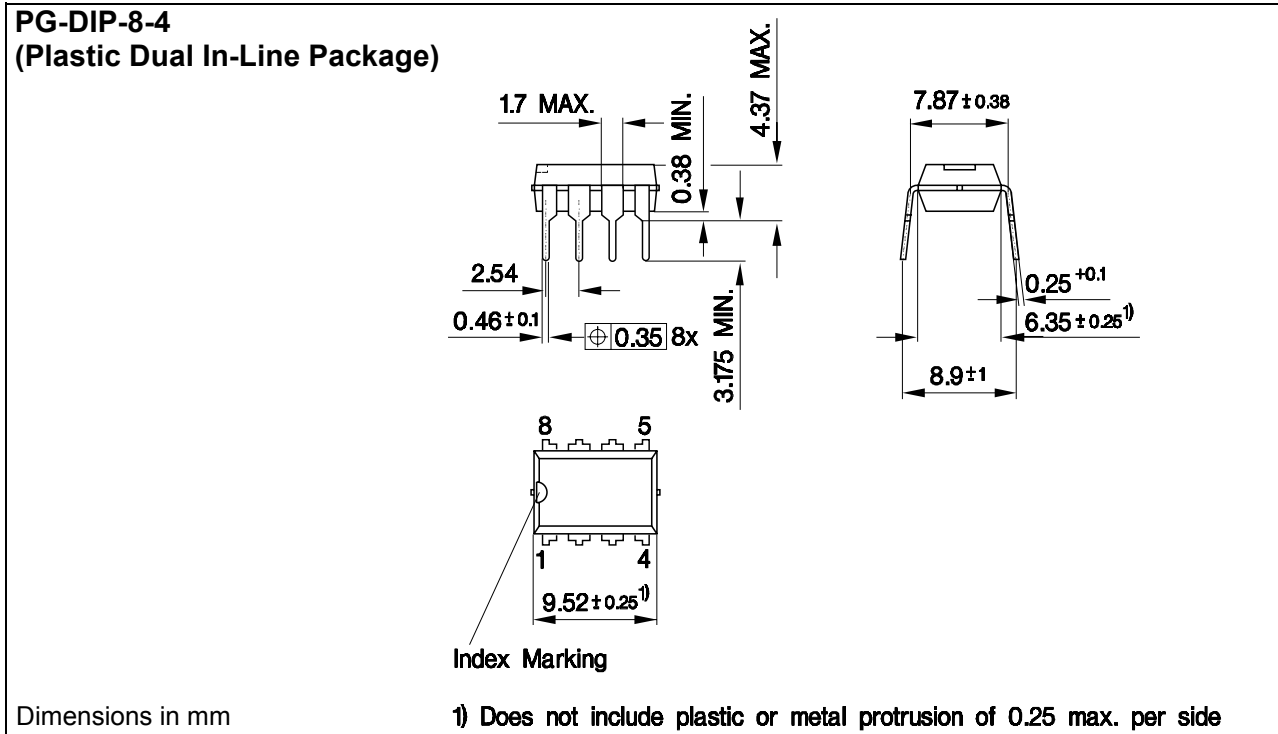


Figure 16 PG-DIP-8-4 Outline Dimension

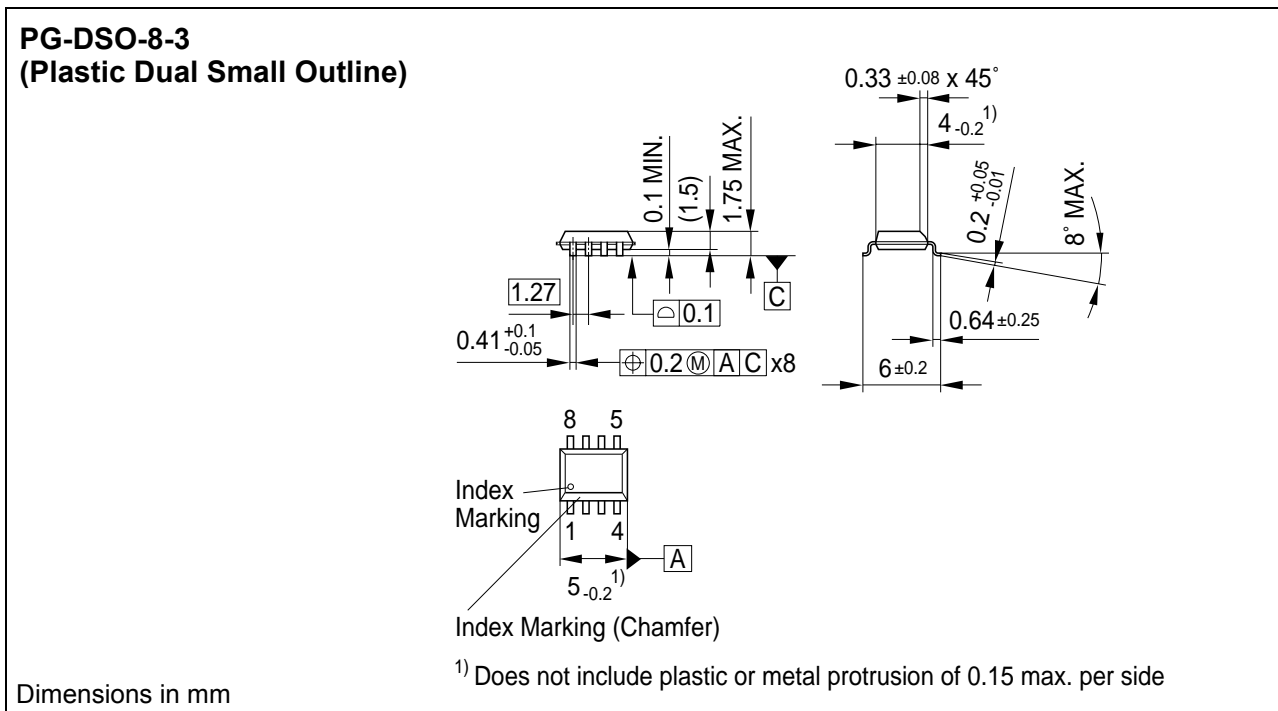


Figure 17 PG-DSO-8-3 Outline Dimension