Version 2.3, 09 November 2019

CCM-PFC

ICE2PCS01

ICE2PCS01G

Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

PowerManagement&Supply

Never stop thinking.

Revision History: **2019-11-09** Datasheet

Previous Version: V 2.2

Page	Subjects (major changes since last revision)
5	Typo error, Vcc maximum voltage should be 25V instead of 26V

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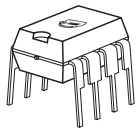
CCM-PFC

ICE2PCS01
ICE2PCS01G

Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

ICE2PCS01
PG-DIP-8



ICE2PCS01G
PG-DSO-8

Product Highlights

- **Leadfree DIP and DSO Package**
- **Wide Input Range**
- **Optimized for applications which require fast Startup**
- **Output Power Controllable by External Sense Resistor**
- **Programmable Operating Frequency**
- **Output Over-Voltage Protection**
- **Fast Output Dynamic Response during Load Jumps**

Features

- Ease of Use with Few External Components
- Supports Wide Range
- Average Current Control
- External Current and Voltage Loop Compensation for Greater User Flexibility
- Programmable Operating/Switching Frequency (50kHz - 250kHz)
- Max Duty Cycle of 95% (at 25°C) at 125kHz
- Trimmed Internal Reference Voltage (3V±2% at 25°C)
- VCC Under-Voltage Lockout
- Cycle by Cycle Peak Current Limiting
- Output Over-Voltage Protection
- Open Loop Detection
- Enhanced Dynamic Response
- Short Startup(SoftStart) duration
- Fulfills Class D Requirements of IEC 1000-3-2
- Soft Overcurrent Protection
-

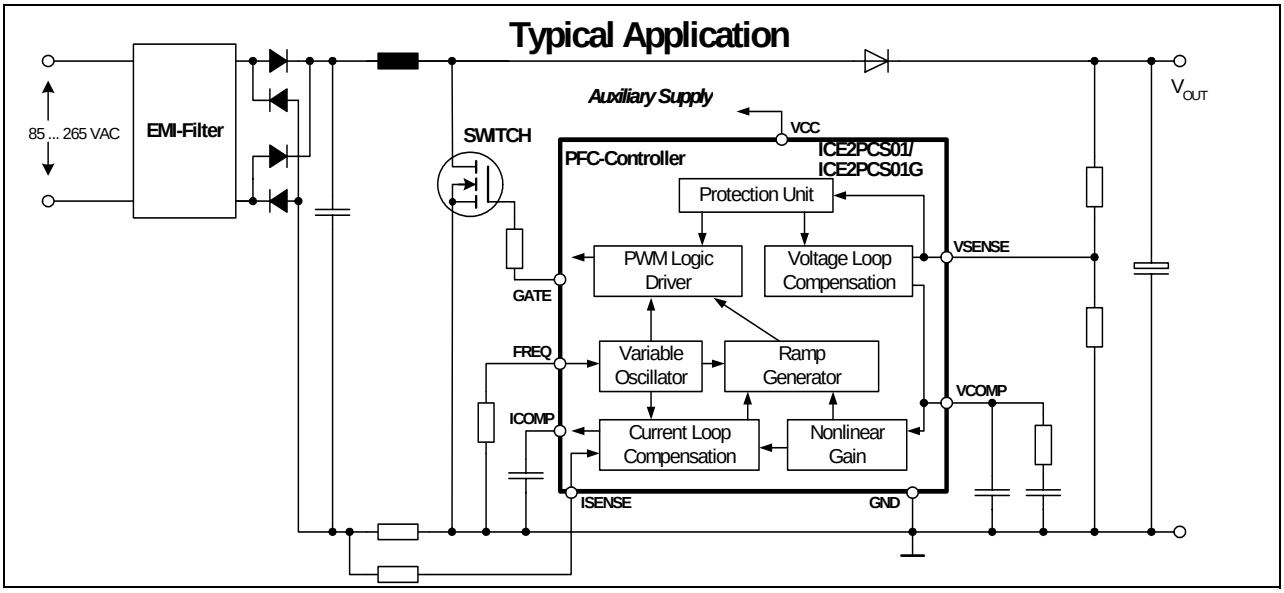
Description

The ICE2PCS01/G is a 8-pin wide input range controller IC for active power factor correction converters. It is designed for converters in boost topology, and requires few external components. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.

The IC operates in the CCM with average current control, and in DCM only under light load condition. The switching frequency is programmable by the resistor at pin 4. Both compensations for the current and voltage loop are external to allow full user control.

There are various protection features incorporated to ensure safe system operation conditions. The internal reference is trimmed (3V±2%) to ensure precise protection and control level. The device has a fast startup time with controlled peak start up current.

Typical Application



Type	Package
ICE2PCS01	PG-DIP-8
ICE2PCS01G	PG-DSO-8

1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	GND	IC Ground
2	ICOMP	Current Loop Compensation
3	ISENSE	Current Sense Input
4	FREQ	Switching Frequency Setting
5	VCOMP	Voltage Loop Compensation
6	VSENSE	V_{OUT} Sense (Feedback) Input
7	VCC	IC Supply Voltage
8	GATE	Gate Drive Output

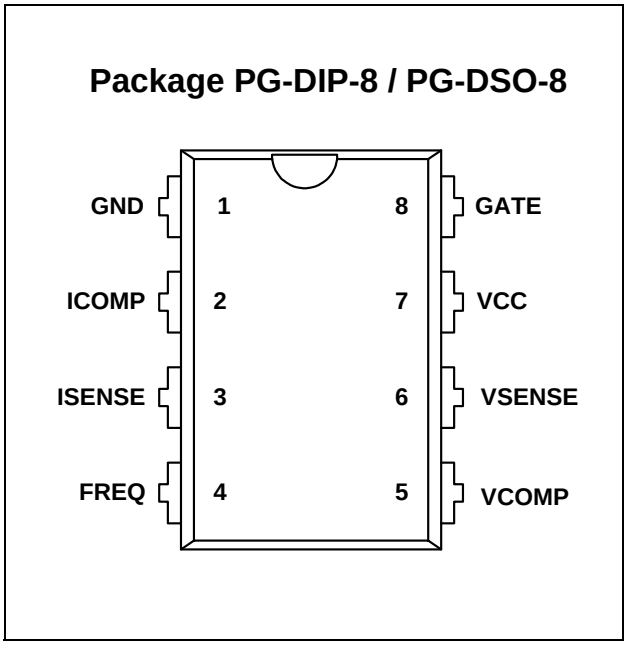


Figure 1 Pin Configuration (top view)

1.2 Pin Functionality

GND (Ground)

The ground potential of the IC.

ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA2 and averages the current sense signal.

ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor (R1). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

During power up time, high inrush currents cause high negative voltage drop at R1, driving currents out of pin 3 which could be beyond the absolute maximum ratings. Therefore a series resistor (R2) of around 220Ω is recommended in order to limit this current into the IC.

FREQ (Frequency Setting)

This pin allows the setting of the operating switching frequency by connecting a resistor to ground. The frequency range is from 50kHz to 250kHz.

VSENSE (Voltage Sense/Feedback)

The output bus voltage is sensed at this pin via a resistive divider. The reference voltage for this pin is 3V.

VCOMP (Voltage Loop Compensation)

This pin provides the compensation of the output voltage loop with a compensation network to ground (see Figure 2). This also gives the soft start function which controls an increasing AC input current during start-up.

VCC (Power Supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply. The operating range is between 11V and 25V. The turn-on threshold is at 11.8V and under voltage occurs at 11V. There is no internal clamp for a limitation of the power supply.

GATE

The GATE pin is the output of the internal driver stage, which has a capability of 1.5A instantaneous source and 2.0A instantaneous sink current.

Its gate drive voltage is clamped at 15V (typically).

2 Representative Block diagram

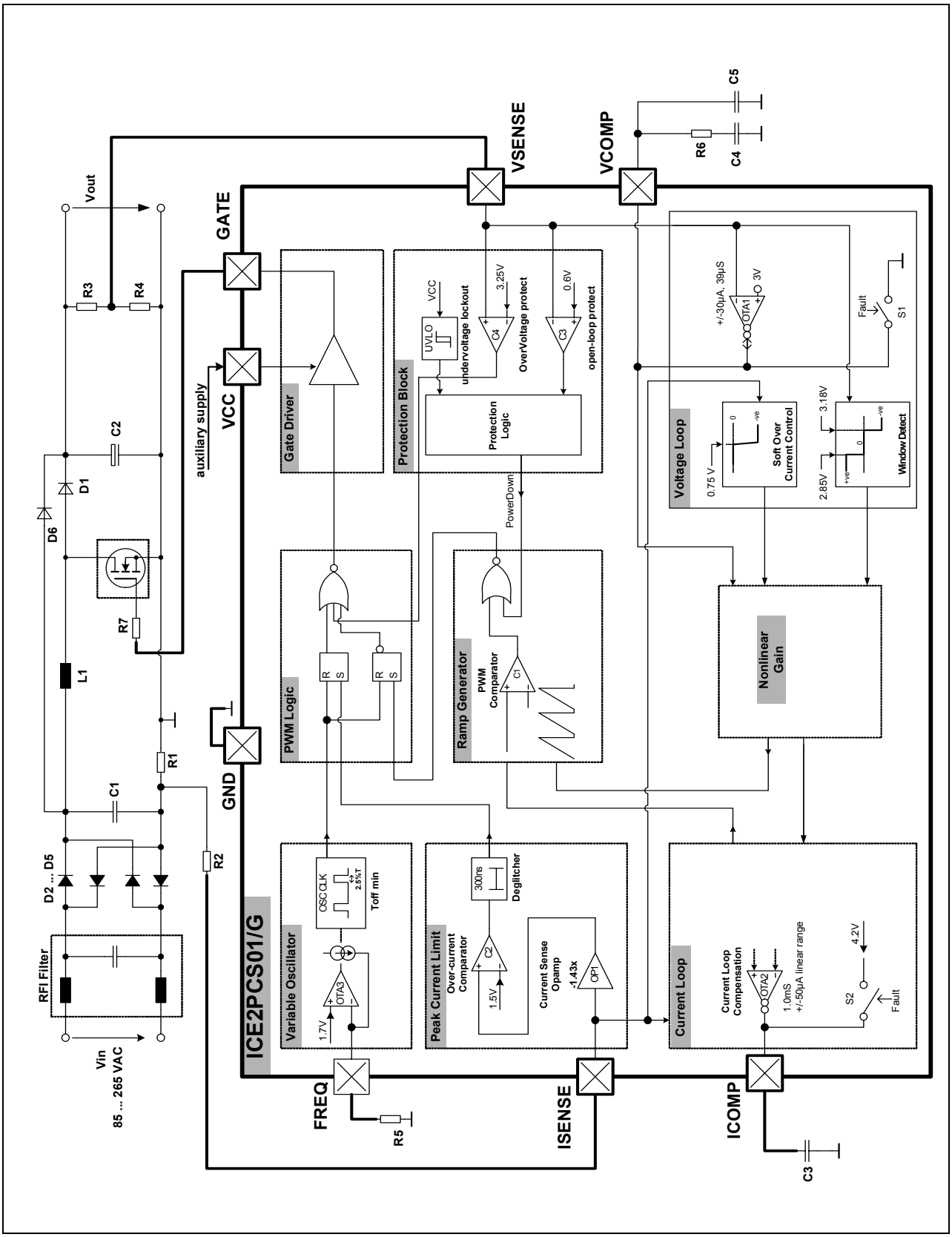


Figure 2 Representative Block diagram

3 Functional Description

3.1 General

The ICE2PCS01/G is a 8 pin control IC for power factor correction converters. It comes in both DIP and DSO packages and is suitable for wide range line input applications from 85 to 265 VAC. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control.

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM). In DCM, the average current waveform will be distorted but the resultant harmonics are still low enough to meet the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bus voltage. Depending on the load condition, OTA1 establishes an appropriate voltage at VCOMP pin which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device. Important protection features are namely Open-Loop protection, Current Limitation and Output Over-voltage Protection.

3.2 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 11.8V and the voltage at pin 6 (VSENSE) is >0.6V, the IC begins operating its gate drive and performs its Startup as shown in Figure 3.

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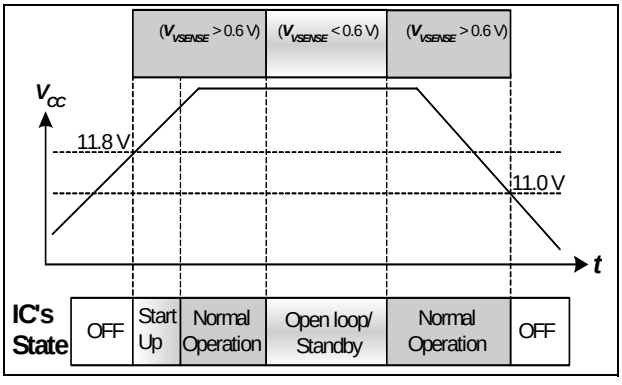

Figure 3 State of Operation respect to VCC

If VCC drops below 11V, the IC is off. The IC will then be consuming typically 300∞A, whereas consuming 13mA during normal operation.

The IC can be turned off and forced into standby mode by pulling down the voltage at pin 6 (VSENSE) to lower than 0.6V. The current consumption is reduced to 300µA in this mode.

3.3 Start-up

Figure 4 shows the operation of voltage loop's OTA1 during startup. The VCOMP pin is pull internally to ground via switch S1 during UVLO and other fault conditions (see later section on "System Protection").

During power up when V_{OUT} is less than 83% of the rated level, OTA1 sources an output current, maximum 30∞A, into the compensation network at pin 5 (VCOMP) causing the voltage at this pin to rise linearly. This results in a controlled linear increase of the input current from 0A thus reducing the stress on the external component.

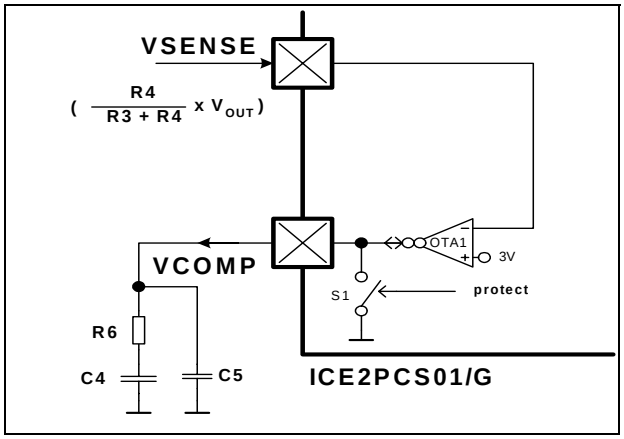

Figure 4 Startup Circuit

As V_{OUT} has not reached within 5% from the rated value, VCOMP voltage is level-shifted by the window detect block as shown in Figure 5, to ensure there is fast boost up of the output voltage.

When V_{OUT} approaches its rated value, OTA1's sourcing current drops and the level shift of the window detect block is removed. The normal voltage loop then takes control.

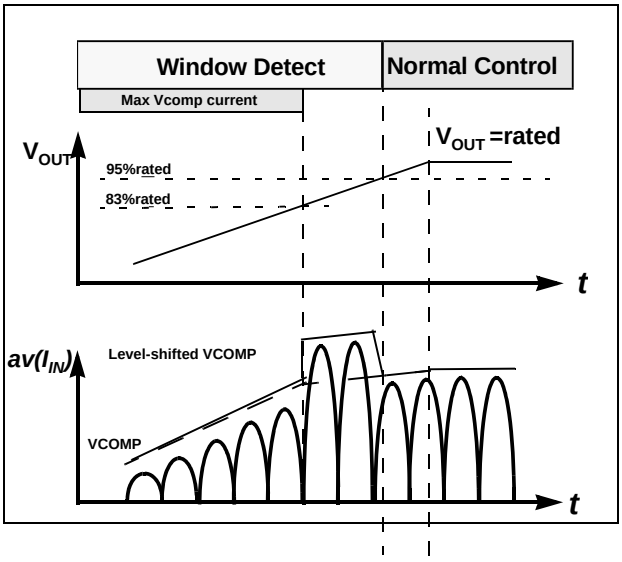

Figure 5 Startup with controlled maximum current

3.4 System Protection

The IC provides several protection features in order to ensure the PFC system in safe operating range. Depending on the input line voltage (V_{IN}) and output bus voltage (V_{OUT}), Figure 7 and 8 show the conditions when these protections are active.

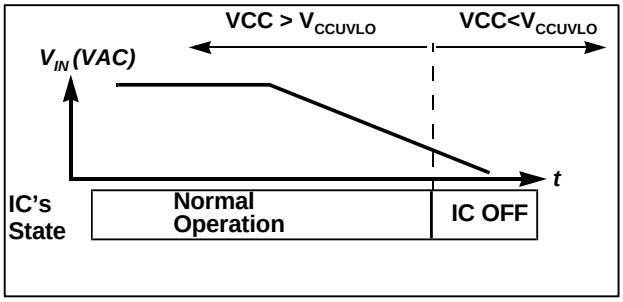

Figure 6 V_{IN} Related Protection Features

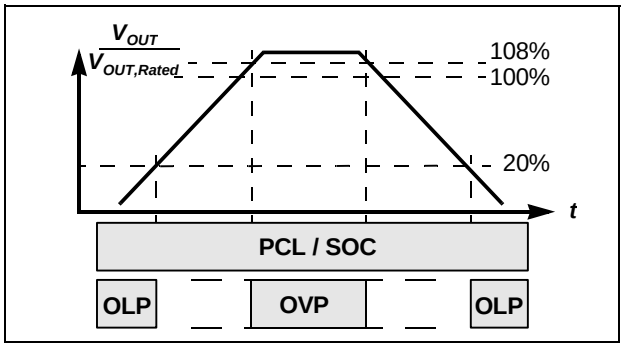

Figure 7 V_{OUT} Related Protection Features

The following sections describe the functionality of these protection features.

3.4.1 Soft Over Current Control (SOC)

The IC is designed **not** to support any output power that corresponds to a voltage lower than -0.75V at the ISENSE pin. A further increase in the inductor current, which results in a lower ISENSE voltage, will activate the Soft Over Current Control (SOC). This is a soft control as it does not directly switch off the gate drive. It acts on the nonlinear gain block to result in a reduced PWM duty cycle.

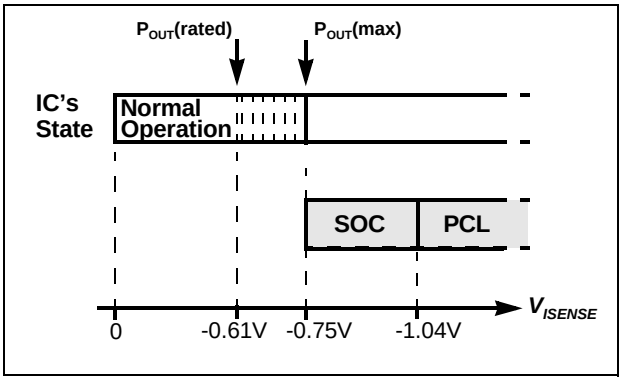

Figure 8 SOC and PCL Protection as function of V_{ISENSE}

The rated output power with a minimum V_{IN} (V_{INMIN}) is

$$P_{OUT}(rated) = V_{INMIN} \cdot \frac{0.61}{R1 \cdot \sqrt{2}}$$

Due to the internal parameter tolerance, the maximum power with V_{INMIN} is

$$P_{OUT}(max) = V_{INMIN} \cdot \frac{0.75}{R1 \cdot \sqrt{2}}$$

3.4.2 Peak Current Limit (PCL)

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 3 (ISENSE) reaches -1.04V. This voltage is amplified by OP1 by a factor of -1.43 and connected to comparator C2 with a reference voltage of 1.5V as shown in Figure 9. A deglitcher with 300ns after the comparator improves noise immunity to the activation of this protection.

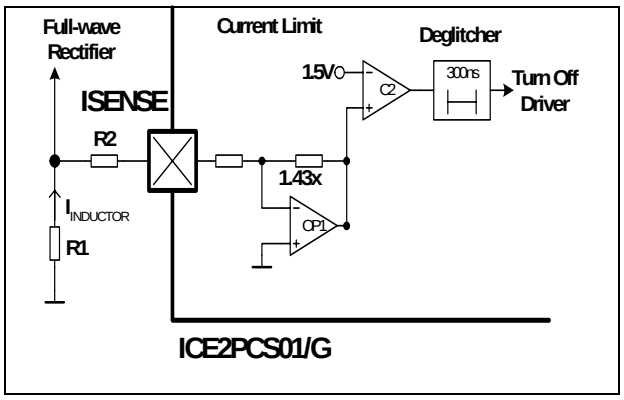

Figure 9 Peak Current Limit (PCL)

3.4.3 Open Loop Protection / Input Under Voltage Protect (OLP)

Whenever VSENSE voltage falls below 0.6V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage V_{IN} for normal operation. In this case, most of the blocks within the IC will be shutdown. It is implemented using comparator C3 with a threshold of 0.6V as shown in the IC block diagram in Figure 2.

3.4.4 Over-Voltage Protection (OVP)

Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active as shown in Figure 6. This is implemented by sensing the voltage at pin VSENSE with respect to a reference voltage of 3.15V. A VSENSE voltage higher than 3.15V will immediately reduce the output duty cycle, bypassing the normal voltage loop control. This results in a lower input power to reduce the output voltage V_{OUT}. A VSENSE voltage higher than 3.25V will immediately turn off the gate, thereby preventing damage to bus capacitor.

3.5 Frequency Setting

The switching frequency of the PFC converter can be set with an external resistor R5 at FREQ pin as shown Figure 10. The pin voltage V_{FREQ} is typically 1.7V. The corresponding capacitor for the oscillator is integrated in the device and the R5/frequency relationship is given at the "**Electrical Characteristic**" section. The recommended operating frequency range is from 50kHz to 250kHz. As an example, a R5 of 33kΩ at pin FREQ will set a switching frequency F_{SW} of 136kHz typically.

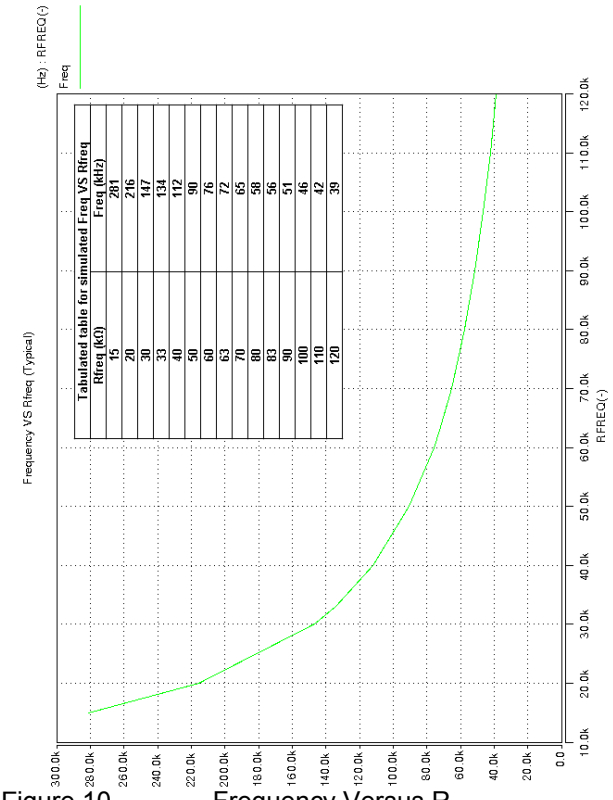

Figure 10 Frequency Versus R_{FREQ}

3.6 Average Current Control

3.6.1 Complete Current Loop

The complete system current loop is shown in Figure 11.

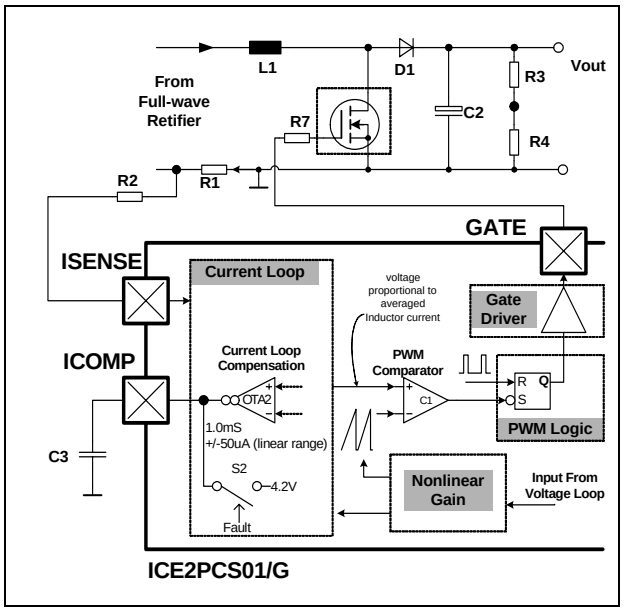

Figure 11 Complete System Current Loop

It consists of the current loop block which averages the voltage at pin ISENSE, resulted from the inductor current flowing across R1. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C1 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

3.6.2 Current Loop Compensation

The compensation of the current loop is done at the ICOMP pin. This is the OTA2 output and a capacitor C3 has to be installed at this node to ground (see Figure 11). Under normal mode of operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 4.2V in the event of IC shuts down when OLP and UVLO occur.

3.6.3 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction.

Assuming the voltage loop is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to V_{IN}. The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF}, and thus to the input voltage V_{IN}. Figure 12 shows the scheme to achieve the objective.

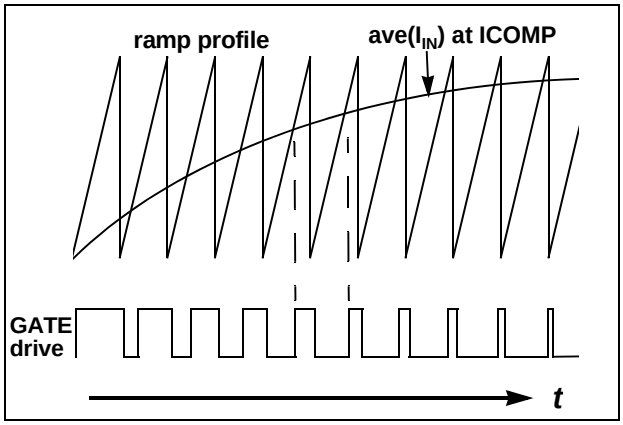

Figure 12 Average Current Control in CCM

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 5 (ICOMP). The PWM cycle starts with the Gate turn off for a duration of T_{OFFMIN} (250ns typ.) and the ramp is kept discharged. The ramp is then allowed to rise after T_{OFFMIN} expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF}.

Figure 13 shows the timing diagrams of T_{OFFMIN} and the PWM waveforms.

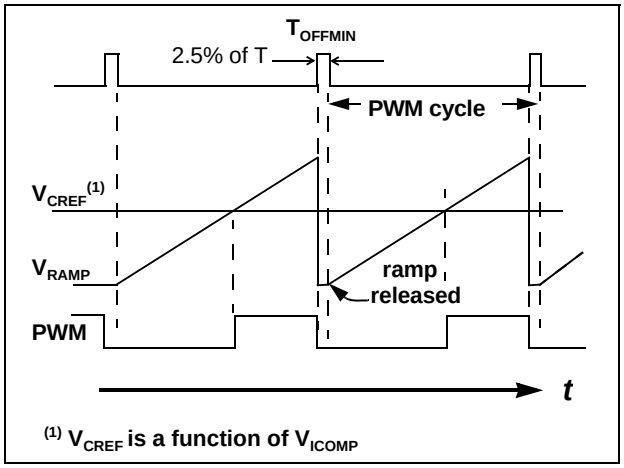

Figure 13 Ramp and PWM waveforms

3.6.4 Nonlinear Gain Block

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the

voltage at pin VCOMP. This block has been designed to support the wide input voltage range (85-265VAC).

3.7 PWM Logic

The PWM logic block prioritizes the control input signals and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse T_{OFFMIN}, are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output under 136kHz of operation.

In case of high input currents which result in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal Toffmin resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 14.

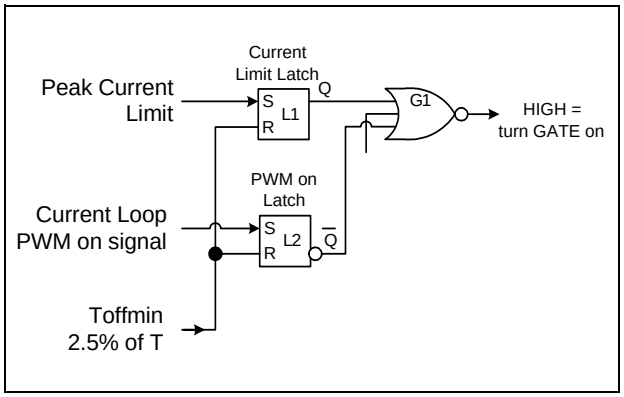

Figure 14 PWM Logic

3.8 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT}. This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from V_{OUT}. The pin VSENSE is the input of OTA1 which has an internal reference of 3V. Figure 15 shows the important blocks of this voltage loop.

3.8.1 Voltage Loop Compensation

The compensation of the voltage loop is installed at the VCOMP pin (see Figure 15). This is the output of OTA1 and the compensation must be connected at this pin to ground. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

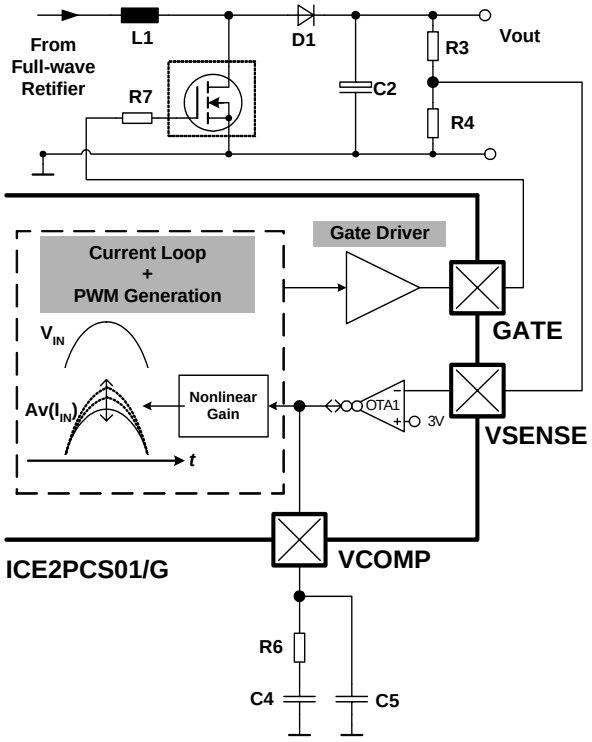

Figure 15 Voltage Loop

3.8.2 Enhanced Dynamic Response

Due to the low frequency bandwidth of the voltage loop, the dynamic response is slow and in the range of about several 10ms. This may cause additional stress to the bus capacitor and the switching transistor of the PFC in the event of heavy load changes.

The IC provides therefore a “window detector” for the feedback voltage V_{VSENSE} at pin 6 (VSENSE). Whenever V_{VSENSE} exceeds the reference value (3V) by ±5%, it will act on the nonlinear gain block which in turn affect the gate drive duty cycle directly. This change in duty cycle is bypassing the slow changing VCOMP voltage, thus results in a fast dynamic response of V_{OUT}.

3.9 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 16) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 8 (GATE) is typically clamped at 15V.

The output is active HIGH and at VCC voltages below the under voltage lockout threshold V_{CCUVLO}, the gate drive is internally pull low to maintain the off state.

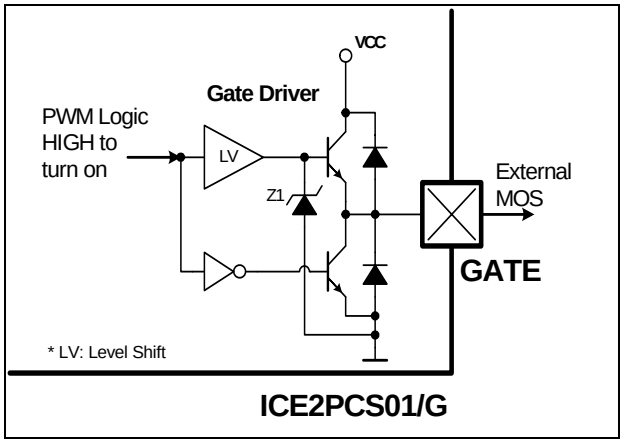

Figure 16 Gate Driver

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	-0.3	25	V	
FREQ Voltage	V_{FREQ}	-0.3	5	V	
ICOMP Voltage	V_{ICOMP}	-0.3	5	V	
ISENSE Voltage	V_{ISENSE}	-20	5	V	2)
ISENSE Current	I_{ISENSE}	-1	1	mA	Recommended R2=220Ω
VSENSE Voltage	V_{VSENSE}	-0.3	5	V	
VSENSE Current	I_{VSENSE}	-1	1	mA	R3>400kΩ
VCOMP Voltage	V_{VCOMP}	-0.3	5	V	
GATE Voltage	V_{GATE}	-0.3	17	V	Clamped at 15V if driven internally.
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient for DSO-8-13	$R_{thJA}(DSO)$	-	185	K/W	PG-DSO-8-13
Thermal Resistance Junction-Ambient for DIP-8-4	$R_{thJA}(DIP)$	-	90	K/W	PG-DIP-8-4
ESD Protection	V_{ESD}	-	2	kV	Human Body Model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

2) Absolute ISENSE current should not be exceeded

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	V_{CCUVLO}	25	V	
Junction Temperature	T_{JCon}	-40	125	°C	

4.3 Characteristics

Note: ***The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40 °C to 125°C.Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} =18V is assumed for test condition.***

4.3.1 Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Turn-On Threshold	V_{CCon}	11.4	11.8	12.7	V	
VCC Turn-Off Threshold/ Under Voltage Lock Out	V_{CCUVLO}	10.4	11.0	11.7	V	
VCC Turn-On/Off Hysteresis	V_{CChy}	0.65	0.8	1.4	V	
Start Up Current Before V_{CCon}	$I_{CCstart}$	-	450	1100	∝A	V_{VCC}=V_{VCCon} -0.1V
Operating Current with active GATE	I_{CCHG}	-	15	20	mA	R5 = 33kΩ C_L= 4.7nF
Operating Current during Standby	$I_{CCStdby}$	-	700	1300	∝A	V_{VSENSE}= 0.5V V_{ICOMP}= 4V

4.3.2 Variable Frequency Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Frequency (Typical)	F_{SWnom}	124	136	147	kHz	R5 = 33kΩ
Switching Frequency (Min.)	F_{SWmin}	50	56	62	kHz	R5 = 82kΩ
Switching Frequency (Max.)	F_{SWmax}	250	285	315	kHz	R5 = 15kΩ
Voltage at FREQ pin	V_{FREQ}	1.65	1.70	1.76	V	

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max. Duty Cycle	D_{MAX}	92	95	98.5	%	$F_{SW} = F_{SWnom}$ (R5 = 33kΩ)
Min. Duty Cycle	D_{MIN}			0	%	V_{VCOMP}= 0V, V_{VSENSE}= 3V V_{ICOMP}= 4.3V
Min. Off Time	T_{OFFMIN}	100	250	580	ns	V_{VSENSE}= 3V V_{ISENSE}= 0.1V (R5 = 33kΩ)

The parameter is not subject to production test - verified by design/characterization

4.3.4 System Protection Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Open Loop Protection (OLP) VSENSE Threshold	V_{OLP}	0.55	0.6	0.65	V	
Peak Current Limitation (PCL) ISENSE Threshold	V_{PCL}	-1.16	-1.04	-0.95	V	
Soft Over Current Control (SOC) ISENSE Threshold	V_{SOC}	-0.75	-0.68	-0.61	V	
Output Over-Voltage Protection (OVP)	V_{OVP}	3.1	3.25	3.4	V	

4.3.5 Current Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA2 Transconductance Gain	Gm_{OTA2}	0.8	1.0	1.3	mS	At Temp = 25°C
OTA2 Output Linear Range[1)]	I_{OTA2}	-	± 50	-	∝A	
ICOMP Voltage during OLP	V_{ICOMPF}	3.9	4.2	-	V	V_{VSENSE}= 0.5V

4.3.6 Voltage Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA1 Reference Voltage	V_{OTA1}	2.92	3.00	3.08	V	measured at VSENSE
OTA1 Transconductance Gain	Gm_{OTA1}	26	39	51	∝S	
OTA1 Max. Source Current Under Normal Operation	I_{OTA1SO}	18	30	38	∝A	V_{VSENSE}= 2V V_{VCOMP}= 3V
OTA1 Max. Sink Current Under Normal Operation	I_{OTA1SK}	21	30	41	∝A	V_{VSENSE}= 4V V_{VCOMP}= 3V
Enhanced Dynamic Response VSENSE High Threshold VSENSE Low Threshold	 V_{Hi} V_{Lo}	 3.09 2.76	 3.18 2.85	 3.26 2.94	 V V	
VSENSE Input Bias Current at 3V	I_{VSEN3V}	0	-	1.5	∝A	V_{VSENSE}= 3V
VSENSE Input Bias Current at 1V	I_{VSEN1V}	0	-	1	∝A	V_{VSENSE}= 1V
VCOMP Voltage during OLP	V_{VCOMPF}	0	0.2	0.4	V	V_{VSENSE}= 0.5V I_{VCOMP}= 0.5mA

4.3.7 Driver Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	V_{GATEL}	-	-	1.2	V	V_{CC} =***10V*** I_{GATE} = 5 mA
		-		1.5	V	V_{CC} =***10V*** I_{GATE} =20 mA
		-	0.4	-	V	I_{GATE} = 0 A
		-	-	1.0	V	I_{GATE} = 20 mA
		-0.2	0	-	V	I_{GATE} = -20 mA
GATE High Voltage	V_{GATEH}	-	14.8	-	V	V_{CC} = 25V C_L = 4.7nF
		-	14.8	-	V	V_{CC} = 19V C_L = 4.7nF
		7.8	9.2	-	V	V_{CC} = V_{VCCoff} + 0.2V C_L = 4.7nF
GATE Rise Time	t_r	-	60	-	ns	V_{Gate} = 2V ...12V C_L = 4.7nF
GATE Fall Time	t_f	-	50	-	ns	V_{Gate} = 12V ...2V C_L = 4.7nF
GATE Current, Peak, Rising Edge	I_{GATE}	-1.5	-	-	A	C_L = 4.7nF[1)]
GATE Current, Peak, Falling Edge	I_{GATE}	-	-	2.0	A	C_L = 4.7nF[1)]

[1)] Design characteristics (not meant for production testing)

5 Outline Dimension

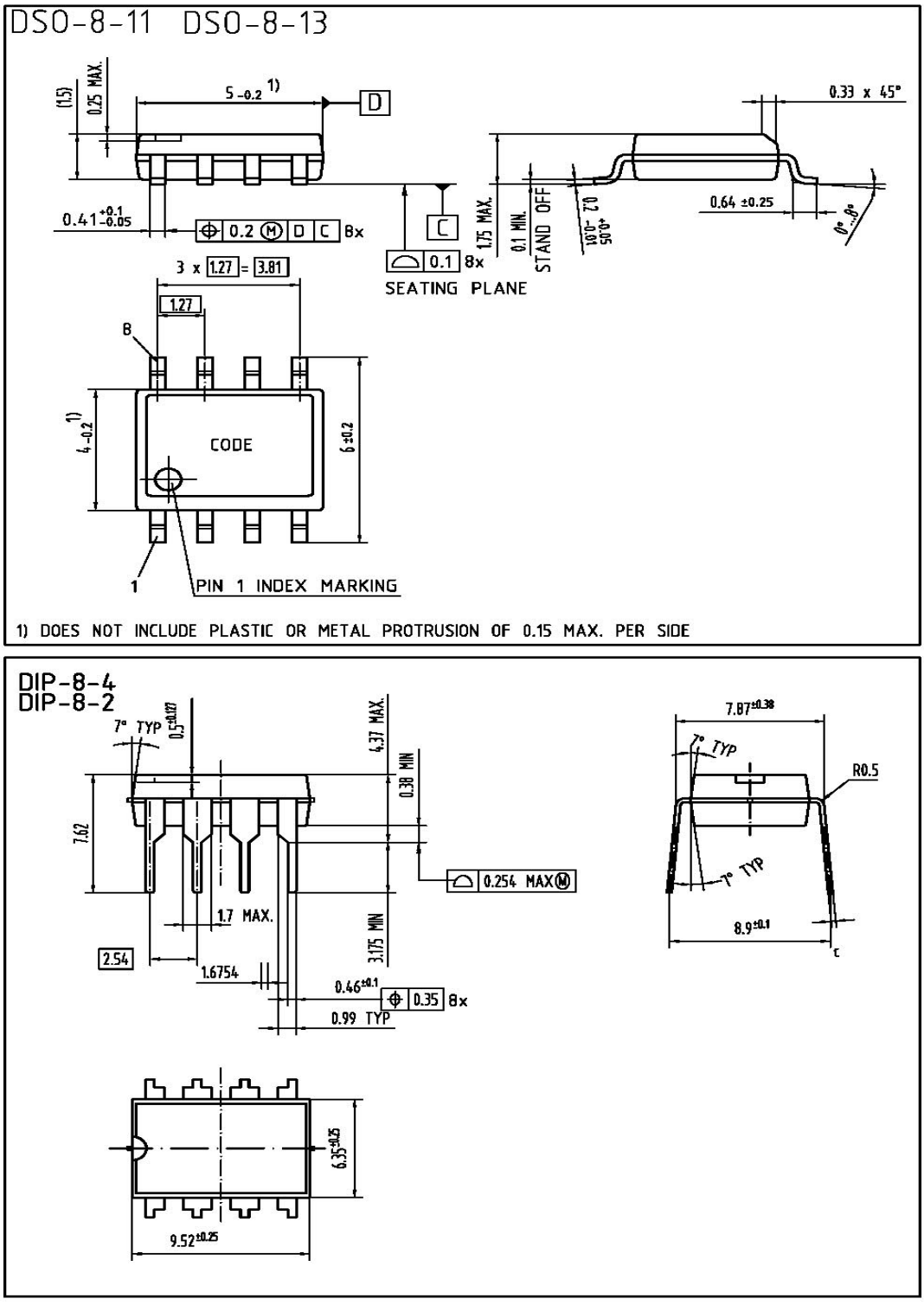

Figure 17 PG-DSO-8 and PG-DIP-8 Outline Dimension