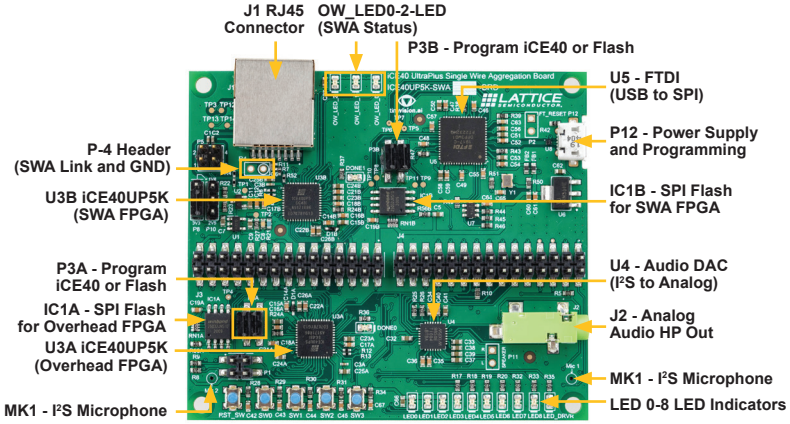
QuickSTART

Single-Wire Aggregation Evaluation Board

This document provides a brief introduction to the Single-Wire Evaluation Kit.



1 Check Kit Contents

The Single-Wire Aggregation (SWA) Evaluation Kit contains the following items:

- Two SWA Evaluation Boards
- Two Jumper Wires
- Two Micro-USB Cables
- Quick Start Guide

2 Using the SWA Evaluation Kit

The Board contains two iCE40UP5K FPGA devices:

- SWA FPGA - for the actual Single-Wire Aggregation
- Overhead FPGA - for I²C, I²S and GPIO signal generation and verification.

3 Installing the Software

The SWA Evaluation Board is pre-programmed with the Single-Wire Aggregation Demo.

Other ready-to-use SWA configurations are available for demonstration and evaluation at www.latticesemi.com/singlewire.

4 Powering the Board and Observing the Demo Program

Connect the micro-USB cable to the board. Connect the single-wire link and common ground on the two SWA Evaluation Board through J4 using the two jumper wires. Upon boot up, the SWA demonstration is loaded from SPI Flash to the iCE40UP and starts running. This aggregates the I²C, I²S and GPIO signals.

To run the SWA demo:

1. Press and hold the RST_SW buttons of both Master and Slave SWA board.
2. Release the button of each SWA board. This resets the SWA FPGA.
3. Simultaneously press the SWS3 buttons of each board. This resets the Overhead FPGA.

Note the following after resetting Overhead FPGA.

- GPIO Signal Aggregation
  - Overhead FPGAs on Master and Slave SWA Board start sending 6-bit counter GPIO signals to the SWA FPGA for aggregation. It is then de-aggregated by the receiving SWA FPGA. The de-aggregated signals are sent to the receiving Overhead FPGA and LED for verification.
  - LED[8:3] blinks like a 6-bit counter on both SWA boards.
  - LED2 blinks on both SWA boards, indicating that the SWA board is receiving 6-bit counter GPIO signals.
  - Pressing SW1 resets GPIO generation and verification. Pressing SW1 on the transmitting SWA board causes LED2 of the receiving board to turn off because it interrupts the expected 6-bit counter GPIO signals. Pressing SW1 on the receiving SWA board resets the GPIO verification. After this, the LED2 blinks again.
- I^2C Signal Aggregation
  - At Master SWA Board, Press SW0. The Master Overhead FPGA generates nine I^2C commands to set-up, enable DAC on the Slave SWA Board.
  - 1 kHz single tone or audio coming from the I^2S microphone of the Master SWA board is observed on the audio receiver connected on the Slave SWA board's audio jack.
  - Pressing SW0 again generates I^2C command to mute and unmute the DAC.
- I^2S Signal Aggregation
  - Master SWA FPGA acts as the I^2S controllers generating the I^2S clock and I^2S WS for the I^2S microphone and Master Overhead FPGA. I^2S sampling rate is at ~48 kHz.
  - Master Overhead FPGA generate I^2S data. I^2S data sent to Master SWA FPGA are either a 1 kHz single tone or I^2S data coming from I^2S microphone. Pressing or switching SW2 at Master SWA board selects the I^2S data sent to Master SWA FPGA.
  - De-aggregated I^2S data from Slave SWA board are sent to Slave Overhead FPGA to verify if it is receiving a 1 kHz single tone. Same signals are sent to DAC so that you can verify the received audio through audio jack. LED0 on Slave SWA FPGA indicates the status of I^2S data verification. Blinking LED0 means it is receiving expected single tone data.
  - Switching SW2 at Slave SWA board resets I^2S verification being done by Slave Overhead FPGA.
  - I^2S Signals also feedback to Master Overhead FPGA. After resetting Master Overhead FPGA, Master SWA LED0 blinks, which indicates that it is sending 1 kHz single tone signal to SWA FPGA.
  - Switching Slave SWA Board – SW2 resets I^2S verification.

5 Doing More with the Single Wire Evaluation Kit

Check the Lattice website at www.latticesemi.com/single-wire to download the full User's Guide, PC-based software tools to interact with the demonstration program, and other resources.

Technical Support

www.latticesemi.com/support

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