ICL3207E

±15kV ESD Protected, +3V to +5.5V, Low Power, 250kbps, RS-232 Transmitter/Receiver

The ICL3207E is a 3V to 5.5V powered RS-232 transmitter/receiver that meets EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. The ICL3207E features five transmitters and three receivers. It provides ±15kV ESD protection (IEC61000-4-2 Air Gap) and ±15kV Human Body Model protection on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are ISDN Terminal Adapters (TAs), PDAs, Palmtops, peripherals, and notebook and laptop computers where the low operational power consumption and even lower standby power consumption is critical. Small footprint packaging and the use of small, low value capacitors ensure board space savings. Data rates greater than 250kbps are ensured at worst case load conditions. The ICL3207E is fully compatible with 3.3V only systems, mixed 3.3V and 5V systems, and 5V only systems. The ICL3207E is a lower power, pin-for-pin replacement for the MAX207E, HIN207E, and HIN237E.

Table 1 summarizes the features of the ICL3207E. AN9863 summarizes the features of each device in the ICL32xxE 3V family.

Related Literature

For a full list of related documents, visit our website:

- ICL3207E device page

Features

- Pb-free (RoHS compliant)
- ESD protection for RS-232 I/O pins to ±15kV (IEC61000)
- 5V lower power replacement for MAX207E, HIN207E, and HIN237E
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- Latch-up free
- On-chip voltage converters require only four external 0.1µF capacitors
- RS-232 compatible with V_{CC} = 2.7V
- Receiver hysteresis for improved noise immunity
- Ensured minimum data rate: 250kbps
- Ensured minimum slew rate: 6V/µs
- Wide power supply range: Single +3V to +5.5V

Applications

- Battery powered, hand-held, and portable equipment
- Laptop computers, notebooks, and Palmtops
- Modems, printers, and other peripherals
- ISDN Terminal Adapters (TAs) and set top boxes

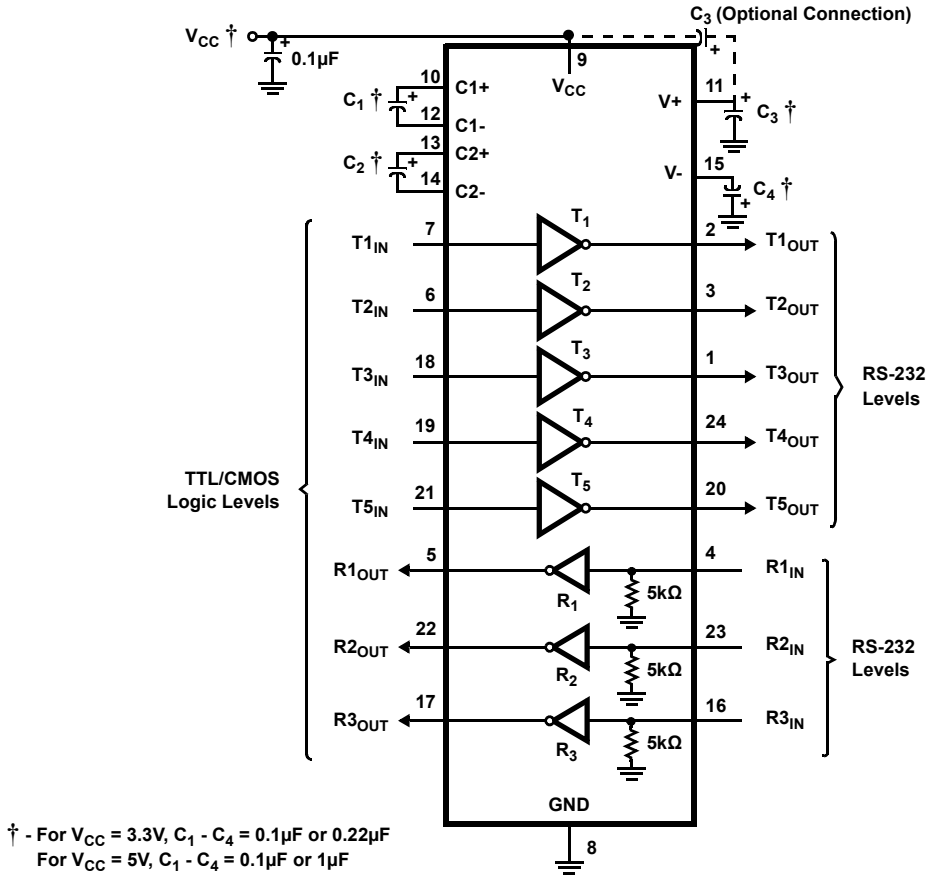
Table 1. Summary of Features

Part Number	No. of Tx	No. of Rx	No. of Monitor Rx (R_{OUTB})	Data Rate (kbps)	Rx Enable Function?	Manual Powerdown?	Automatic Powerdown Function?
ICL3207E	5	3	0	250	No	No	No

Contents

1. Overview

1.1 Typical Operating Circuit



1.2 Ordering Information

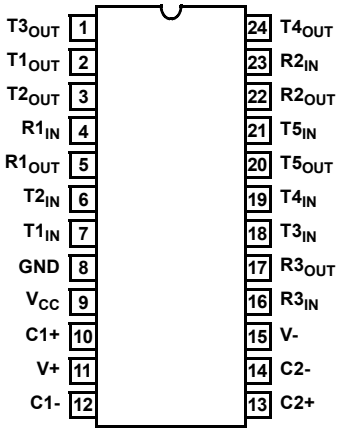
Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3207ECAZ	ICL 3207ECAZ	0 to +70	-	24 Ld SSOP	M24.209
ICL3207ECAZ-T	ICL 3207ECAZ	0 to +70	1k	24 Ld SSOP	M24.209
ICL3207ECBZ	ICL3207ECBZ	0 to +70	-	24 Ld SOIC	M24.3
ICL3207ECBZ-T	ICL3207ECBZ	0 to +70	1k	24 Ld SOIC	M24.3

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ICL3207E device page. For more information about MSL, see TB363.

1.3 Pinout

24 Ld SOIC, SSOP
Top View



1.4 Pin Descriptions

Pin	Function
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
$T1_{IN}$, $T2_{IN}$, $T3_{IN}$, $T4_{IN}$, $T5_{IN}$	TTL/CMOS compatible transmitter inputs.
$T1_{OUT}$, $T2_{OUT}$, $T3_{OUT}$, $T4_{OUT}$, $T5_{OUT}$	±15kV ESD protected, RS-232 level (nominally ±5.5V) transmitter outputs.
$R1_{IN}$, $R2_{IN}$, $R3_{IN}$	±15kV ESD protected, RS-232 compatible receiver inputs.
$R1_{OUT}$, $R2_{OUT}$, $R3_{OUT}$	TTL/CMOS level receiver outputs.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{CC} to GND	-0.3	+6	V
V+ to GND	-0.3	+7	V
V- to GND	+0.3	-7	V
V+ to V-		+14	V
Input Voltages			
T_{IN}	-0.3	+6	V
R_{IN}		±25	V
Output Voltages			
T_{OUT}		±13.2	V
R_{OUT}	-0.3	V_{CC} + 0.3	V
Short-Circuit Duration			
T_{OUT}	Continuous		
ESD Rating	See "ESD Performance" on page 6		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical) (Note 4)	θ_{JA} (°C/W)
24 Ld SOIC Package	75
24 Ld SSOP Package	100

Note:
4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range			
ICL3207ECx	0	+70	°C

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = 25°C

Parameter	Test Conditions		Temp (°C)	Min	Typ	Max	Unit
DC Characteristics							
Supply Current	All Outputs Unloaded		25	-	0.3	1.0	mA
Transmitter Inputs and Receiver Outputs							
Input Logic Threshold Low	T_{IN}		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Input Leakage Current	T_{IN}		Full	-	±0.01	±1.0	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	V_{CC} - 0.1	-	V
Receiver Inputs							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.3	-	V
Input Resistance			25	3	5	7	kΩ
Transmitter Outputs							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	W
Output Short-Circuit Current			Full	-	±35	±60	mA
Timing Characteristics							
Maximum Data Rate (One Transmitter Switching)	V_{CC} = 3.15V, C_1 - C_4 = 0.1µF, R_L = 3kΩ, C_L = 1000pF		Full	250	500	-	kbps
	V_{CC} = 3.0V, C_1 - C_4 = 0.22µF, R_L = 3kΩ, C_L = 1000pF		Full	250	286	-	kbps
	V_{CC} ≥ 4.5V, C_1 - C_4 = 0.1µF, R_L = 3kΩ, C_L = 1000pF		Full	250	310	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.3	-	µs
		t_{PLH}	25	-	0.3	-	µs
Transmitter Skew	t_{PHL} - t_{PLH}		Full	-	200	1000	ns
Receiver Skew	t_{PHL} - t_{PLH}		Full	-	100	500	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured From +3V to -3V or -3V to +3V	C_L = 200pF to 2500pF	25	4	15	30	V/µs
		C_L = 200pF to 1000pF	25	6	15	30	V/µs
ESD Performance							
RS-232 Pins (T_{OUT}, R_{IN})	IEC61000-4-2, Air-Gap Discharge Method		25	-	±15	-	kV
	IEC61000-4-2, Contact Discharge Method		25	-	±8	-	kV
	Human Body Model		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

3. Typical Performance Curves

V_{CC} = 3.3V, T_A = 25°C

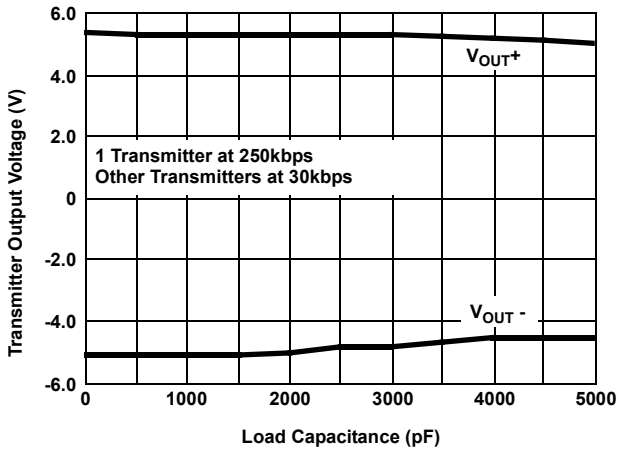


Figure 1. Transmitter Output Voltage vs Load Capacitance

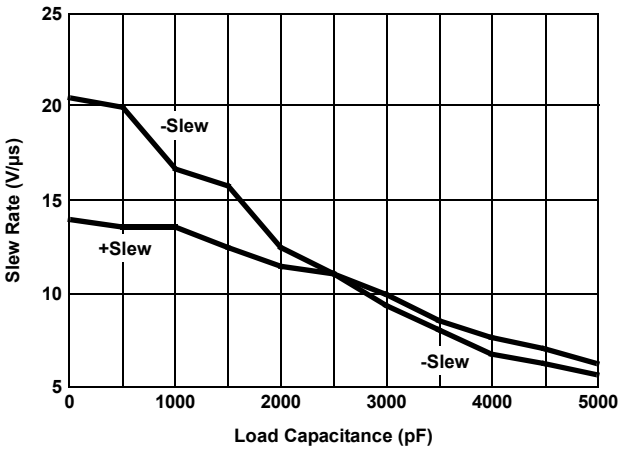


Figure 2. Slew Rate vs Load Capacitance

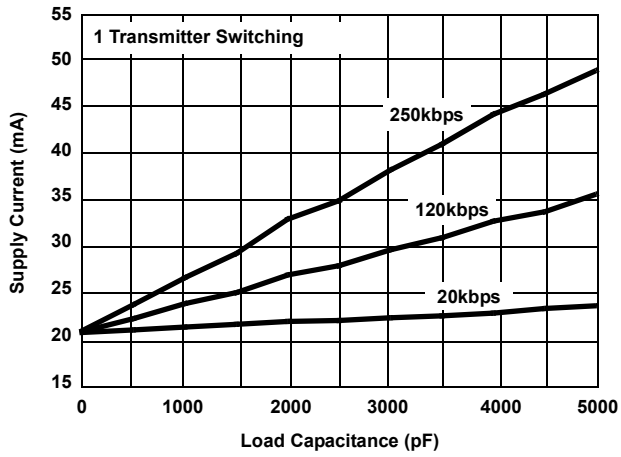


Figure 3. Supply Current vs Load Capacitance When Transmitting Data

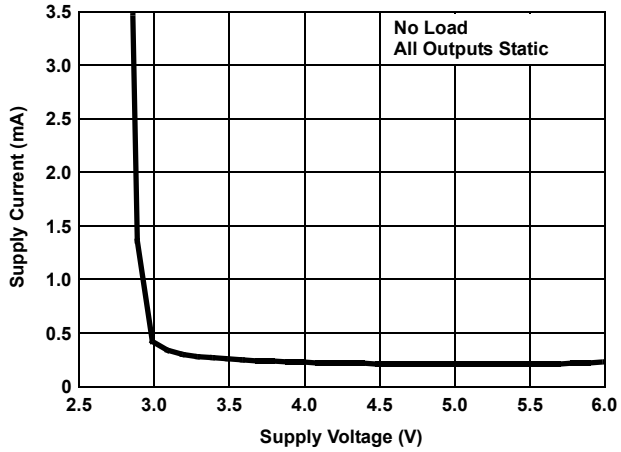


Figure 4. Supply Current vs Supply Voltage

4. Application Information

The ICL3207E operates from a single +3V to +5.5V power supply, ensures a 250kbps minimum data rate, requires only four small external 0.1µF capacitors, features low power consumption, and meets all EIA RS-232C and V.28 specifications.

4.1 Charge Pump

The ICL3207E uses regulated on-chip dual charge pumps as voltage doublers. It uses voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3V. The charge pumps allow the ICL3207E to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See "Capacitor Selection" on page 10 and Table 5 on page 10 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (turning off as soon as the V+ and V- supplies are pumped up to the nominal values) and provide significant power savings.

4.1.1 Charge Pump Abs Max Ratings

The ICL3207E is fully characterized for 3.0V to 3.6V operation, and at critical points for 4.5V to 5.5V operation. Furthermore, load conditions were favorable using static logic states only.

The specified maximum values for V+ and V- are +7V and -7V, respectively. These limits apply for V_{CC} values set to 3.0V and 3.6V (see Table 2). For V_{CC} values set to 4.5V and 5.5V, the maximum values for V+ and V- can approach +9V and -7V, respectively (Table 3 on page 9). The breakdown characteristics for V+ and V- were measured with ±13V.

Table 2. V+ and V- Values for V_{CC} = 3.0V to 3.6V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	$T1_{IN}$ (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 3.0V	V_{CC} = 3.6V	V_{CC} = 3.0V	V_{CC} = 3.6V
0.1	0.1	Open	H	5.80	6.56	-5.60	-5.88
			L	5.80	6.56	-5.60	-5.88
			2.4kbps	5.80	6.56	-5.60	-5.88
		3kΩ // 1000pF	H	5.88	6.60	-5.56	-5.92
			L	5.76	6.36	-5.56	-5.76
			2.4kbps	6.00	6.64	-5.64	-5.96
0.047	0.33	Open	H	5.68	6.00	-5.60	-5.60
			L	5.68	6.00	-5.60	-5.60
			2.4kbps	5.68	6.00	-5.60	-5.60
		3kΩ // 1000pF	H	5.76	6.08	-5.64	-5.64
			L	5.68	6.04	-5.60	-5.60
			2.4kbps	5.84	6.16	-5.64	-5.72
1	1	Open	H	5.88	6.24	-5.60	-5.60
			L	5.88	6.28	-5.60	-5.64
			2.4kbps	5.80	6.20	-5.60	-5.60
		3kΩ // 1000pF	H	5.88	6.44	-5.64	-5.72
			L	5.88	6.04	-5.64	-5.64
			2.4kbps	5.92	6.40	-5.64	-5.64

Table 3. V+ and V- Values for V_{CC} = 4.5V to 5.5V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	$T1_{IN}$ (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 4.5V	V_{CC} = 5.5V	V_{CC} = 4.5V	V_{CC} = 5.5V
0.1	0.1	Open	H	7.44	8.48	-6.16	-6.40
			L	7.44	8.48	-6.16	-6.44
			2.4kbps	7.44	8.48	-6.17	-6.44
		3kΩ // 1000pF	H	7.76	8.88	-6.36	-6.72
			L	7.08	8.00	-5.76	-5.76
			2.4kbps	7.76	8.84	-6.40	-6.64
0.047	0.33	Open	H	6.44	6.88	-5.80	-5.88
			L	6.48	6.88	-5.84	-5.88
			2.4kbps	6.44	6.88	-5.80	-5.88
		3kΩ // 1000pF	H	6.64	7.28	-5.92	-6.04
			L	6.24	6.60	-5.52	-5.52
			2.4kbps	6.72	7.16	-5.92	-5.96
1	1	Open	H	6.84	7.60	-5.76	-5.76
			L	6.88	7.60	-5.76	-5.76
			2.4kbps	6.92	7.56	-5.72	-5.76
		3kΩ // 1000pF	H	7.28	8.16	-5.80	-5.92
			L	6.44	6.84	-5.64	-6.84
			2.4kbps	7.08	7.76	-5.80	-5.80

The resulting new maximum voltages at V+ and V- are listed in Table 4.

Table 4. New Measured Withstanding Voltages

V+, V- to Ground	±13V
V+ to V-	20V

4.2 Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. The transmitters are coupled with the on-chip ±5.5V supplies to deliver true RS-232 levels across a wide range of single supply system voltages.

The ICL3207E ensures a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 800kbps.

Transmitter inputs float if they are unconnected and can cause I_{CC} increases. Connect unused inputs to GND for the best performance.

4.3 Receivers

The ICL3207E has inverting receivers that convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 5) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

Receivers on the ICL3207E are always active.

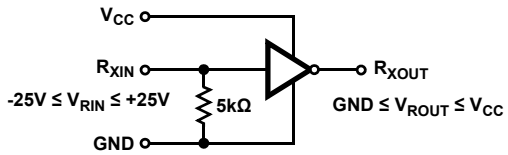


Figure 5. Inverting Receiver Connections

4.4 Low Power Operation

The 3V ICL3207E requires a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation. This supply current is considerably less than the 11mA current required by comparable 5V RS-232 devices and allows you to reduce system power by replacing the old style device with the ICL3207E.

4.4.1 Low Power, Pin Compatible Replacement

Pin compatibility with existing 5V products (such as the MAX207E), coupled with the wide operating supply range, makes the ICL3207E a potential lower power, higher performance drop-in replacement for existing 5V applications. As long as the ±5V RS-232 output swings are acceptable, the ICL3207E works in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown in the "Typical Operating Circuit" on page 3. Terminate C_3 to GND if possible, as slightly better performance results from this configuration.

4.5 Capacitor Selection

The charge pumps require 0.1µF or greater capacitors for 3.3V operation. With 0.1µF capacitors, 5% tolerance supplies (3.14V minimum) deliver greater than ±5V transmitter swings at full data rate. 10% tolerance supplies (2.97V minimum) deliver ±4.95V transmitter swings. If greater than ±5V transmitter swings are required with a 10% tolerance 3.3V supply, 0.22µF capacitors are recommended (see Table 5). Existing 5V applications typically use either 0.1µF or 1µF capacitors, and the ICL3207E works well with either value. New 5V designs should use 0.22µF capacitors for the best results. For other supply voltages, see Table 5 for capacitor values. Do not use values smaller than those listed in Table 5. Increasing the capacitor values (by a factor of two) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value; however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's Equivalent Series Resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Table 5. Required Capacitor Values

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.15 to 3.6	0.1	0.1
3.0 to 3.6	0.22	0.22
4.5 to 5.5	0.1 to 1.0	0.1 to 1.0
3.0 to 5.5	0.22	0.22

4.6 Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

4.7 Operation Down to 2.7V

The ICL3207E transmitter outputs meet RS-562 levels (±3.7V) with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

4.8 High Data Rates

The ICL3207E maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 6 shows a transmitter loopback test circuit, and Figure 7 shows the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 8 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

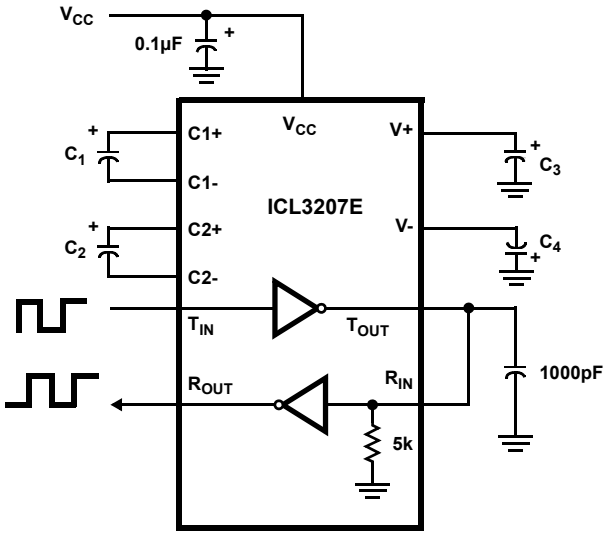


Figure 6. Transmitter Loopback Test Circuit

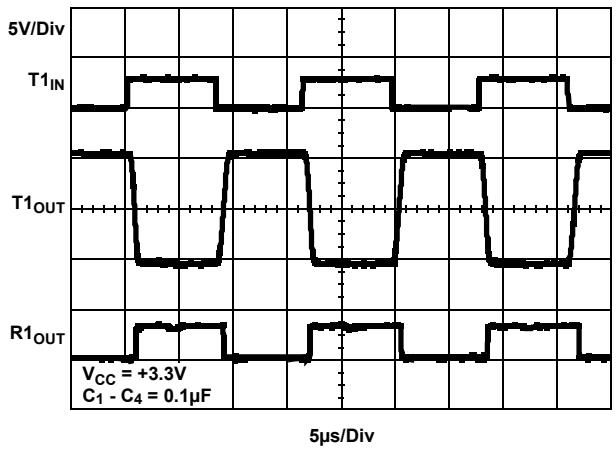


Figure 7. Loopback Test at 120kbps

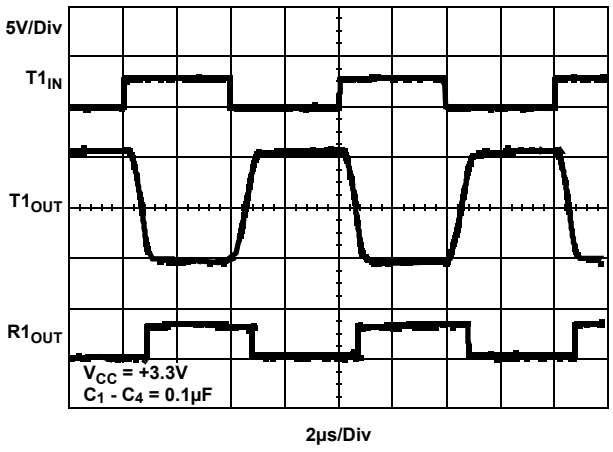


Figure 8. Loopback Test at 250kbps

4.9 Interconnection with 3V and 5V Logic

The ICL3207E directly interfaces with 5V CMOS and TTL logic families. The AC, HC, and CD4000 outputs can drive ICL3207E inputs with the ICL3207E at 3.3V and the logic supply at 5V, but the ICL3207E outputs do not reach the minimum V_{IH} for these logic families. See Table 6 for more information.

Table 6. Logic Family Compatibility With Various Supply Voltages

System Power-Supply Voltage (V)	V_{CC} Supply Voltage (V)	Compatibility
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL3207E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

5. ±15kV ESD Protection

All pins on ICL32xx devices include ESD protection structures, but the ICL32x7E incorporate advanced structures that allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a cable can cause an ESD event that might destroy unprotected ICs. The ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and do not interfere with RS-232 signals as large as ±25V.

5.1 Human Body Model (HBM) Testing

The Human Body Model (HBM) test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, so the test is less severe than the IEC61000 test, which utilizes a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

5.2 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

5.3 Air-Gap Discharge Test Method

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

5.4 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

6. Die Characteristics

Substrate Potential (Powered Up)	GND
Transistor Count	469
Process	Si Gate CMOS

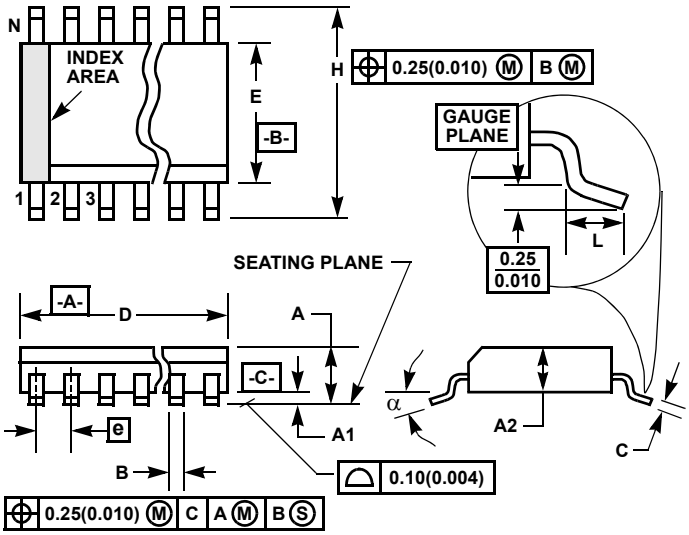
7. Revision History

Revision	Date	Description
FN4914.7	May.20.19	Removed information about the ICL3217E throughout the datasheet. Updated related literature section on page 1. Updated the ordering information table on page 3: -Changed Note 1 and added Note 3 -Added tape and reel column -Added ICL3207ECAZ-T and ICL3207ECBZ-T -Removed the retired ICL3217ECAZ, ICL3217ECBZ, ICL3217EIAZ, and ICL3217EIBZ Added Charge Pump Abs Max Ratings section starting on page 8. Removed About Intersil section. Applied new template. Updated disclaimer.
FN4914.6	Aug.21.15	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing M24.3 to the latest revision updates are as follows: -Revision 0 to Revision 1, Removed µ symbol which is overlapping the alpha symbol in the diagram. -Revision 1 to Revision 2, Updated to new POD standard by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern.

8. Package Outline Drawings

For the most recent package outline drawing, see M24.209.

M24.209 (JEDEC MO-150-AG ISSUE B)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0°	8°	0°	8°	-

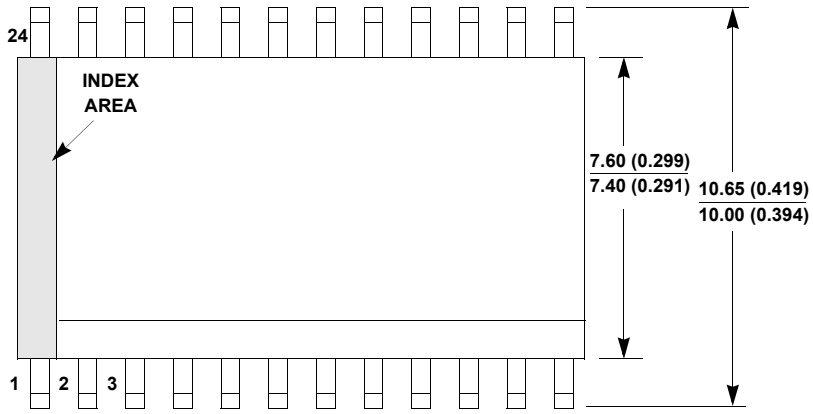
Rev. 1 3/95

NOTES:

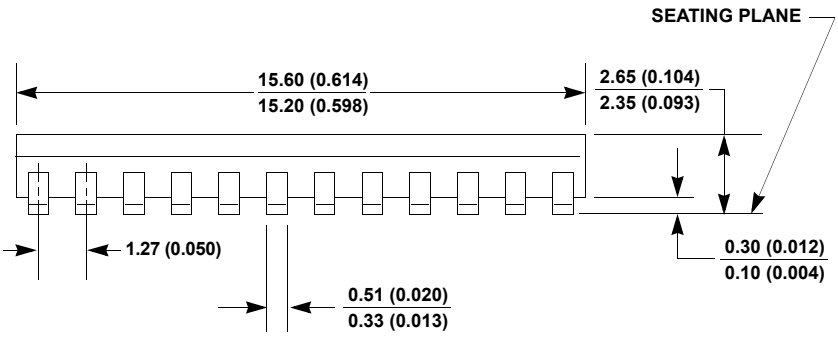
5. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
6. Dimensioning and tolerancing per ANSI Y14.5M-1982.
7. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
8. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
9. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
10. “L” is the length of terminal for soldering to a substrate.
11. “N” is the number of terminal positions.
12. Terminal numbers are shown for reference only.
13. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
14. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)
Rev 2, 3/11

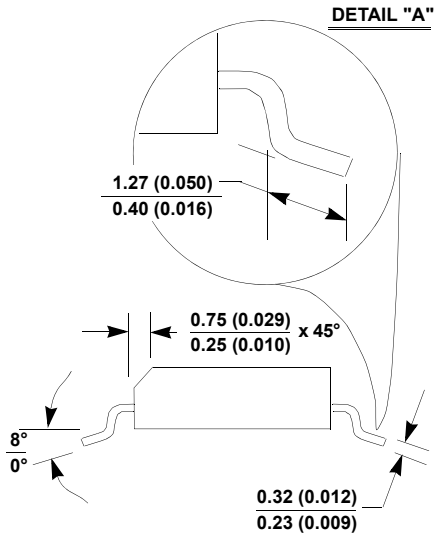
For the most recent package outline drawing, see M24.3.



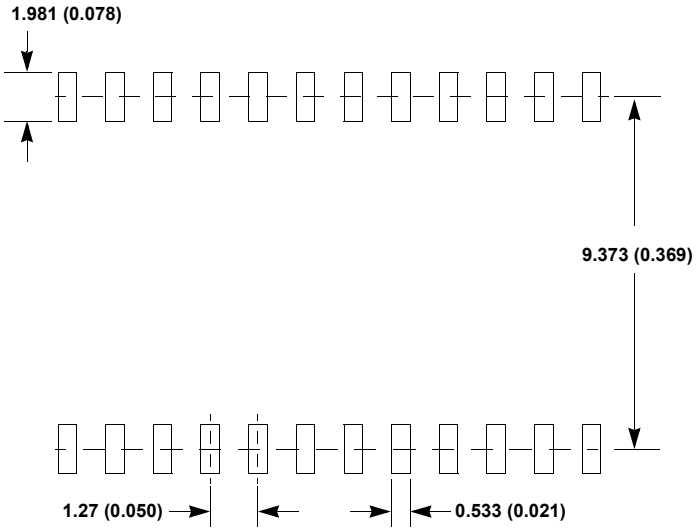
TOP VIEW



SIDE VIEW "A"



SIDE VIEW "B"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

15. Dimensioning and tolerancing per ANSI Y14.5M-1982.
16. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
17. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
18. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
19. Terminal numbers are shown for reference only.
20. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
21. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
22. This outline conforms to JEDEC publication MS-013-AD ISSUE C.