

IF4510 N-Channel JFET

Features

- InterFET [N0450 Geometry](#)
- Low Noise: 1.1 nV/√Hz Typical
- High Gain: 50mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

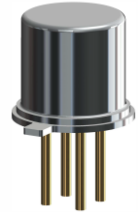
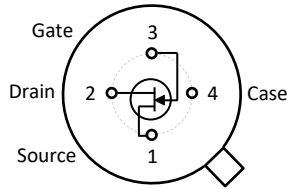
Applications

- Low-Noise, High Gain Amplifiers

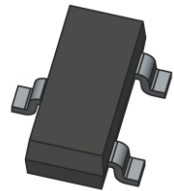
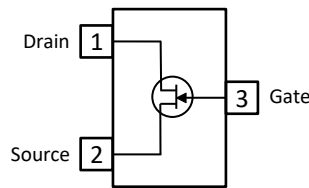
Description

The -40V InterFET IF4510 JFET is targeted for low noise high gain amplifier designs. The IF4510 has a cutoff voltage of less than 1.5V ideal for low voltage applications. The TO-72 package is hermetically sealed and suitable for military applications.

TO-72 Bottom View



SOT23 Top View



Product Summary

Parameters		IF4510 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	V
I_{DSS}	Drain to Source Saturation Current	5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.35	V
G_{FS}	Forward Transconductance	15	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF4510T72	Through-Hole	TO-72	Bulk
IF4510ST3	Surface Mount	SOT23	Bulk
IF4510ST3TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IF4510COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IF4510CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	225	mW
P Power Derating	1.8	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 200	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	Min	Typ	Max	Unit
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-40			V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -30V, V_{DS} = 0V$			-0.1	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 15V, I_D = 0.5nA$	-0.35		-1.5	V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	5	20		mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	Min	Typ	Max	Unit
G_{FS} Forward Transconductance	$V_{DS} = 15V, I_D = 5mA, f = 1kHz$	15	50		mS
C_{iss} Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1MHz$			35	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1MHz$			8	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 4V, I_D = 5mA, f = 1kHz$		1.1		nV/ $\sqrt{\text{Hz}}$

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.