

IFN3954, IFN3955, IFN3956 Dual Matched N-Channel JFET

Features

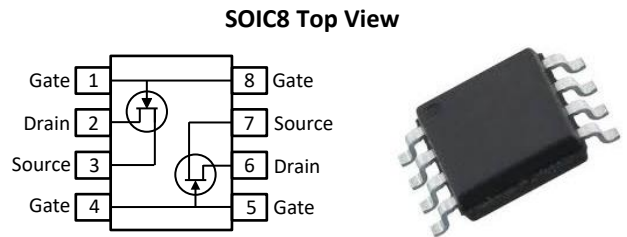
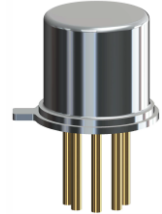
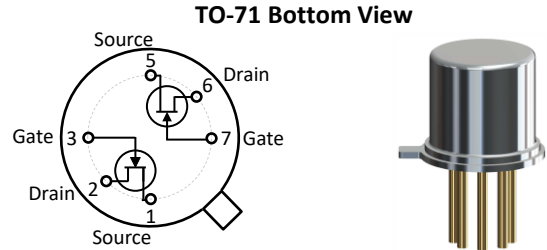
- InterFET [N0016H Geometry](#)
- Typical Noise: 6 nV/√Hz
- Low Ciss: 3.5pF Typical
- High Input Impedance
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- Differential Amplifiers
- Low Noise Pre-Amplifier
- High Impedance Amplifier

Description

The -50V InterFET IFN3954, IFN3955, and IFN3956 matched pair JFET's are targeted for high input impedance applications for mid to high frequency designs. Gate leakages are typically 10pA at room temperatures. Parts are matched down to 5mV. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



Product Summary

| Parameters | IFN3954 Min | IFN3955 Min | IFN3956 Min | Unit |
|---|-------------|-------------|-------------|------|
| BV _{GSS} Gate to Source Breakdown Voltage | -50 | -50 | -50 | V |
| I _{DSS} Drain to Source Saturation Current | 0.5 | 0.5 | 0.5 | mA |
| V _{GS(off)} Gate to Source Cutoff Voltage | -1 | -1 | -1 | V |
| G _{FS} Forward Transconductance | 1000 | 1000 | 1000 | μS |

Ordering Information Custom Part and Binning Options Available

| Part Number | Description | Case | Packaging |
|---|---|-------|-------------------------------------|
| IFN3954; IFN3955; IFN3956 | Through-Hole | TO-71 | Bulk |
| SMP3954; SMP3955; SMP3956 | Surface Mount | SOIC8 | Bulk |
| SMP3954TR; SMP3955TR; SMP3956TR | 7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces | SOIC8 | Minimum 500 Pieces Tape and Reel |
| IFN3954COT; IFN3955COT; IFN3956COT * | Chip Orientated Tray (COT Waffle Pack) | COT | 70/Waffle Pack |
| IFN3954CFT; IFN3955CFT; IFN3956CFT * | Chip Face-up Tray (CFT Waffle Pack) | CFT | 70/Waffle Pack |

* Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

| Parameters | Value | Unit |
|--|------------|----------------------|
| V_{RGS} Reverse Gate Source and Gate Drain Voltage | -50 | V |
| I_{FG} Continuous Forward Gate Current | 50 | mA |
| P_D Continuous Device Power Dissipation | 250 | mW |
| P Power Derating | 4.3 | mW/ $^\circ\text{C}$ |
| T_J Operating Junction Temperature | -55 to 150 | $^\circ\text{C}$ |
| T_{STG} Storage Temperature | -65 to 175 | $^\circ\text{C}$ |

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

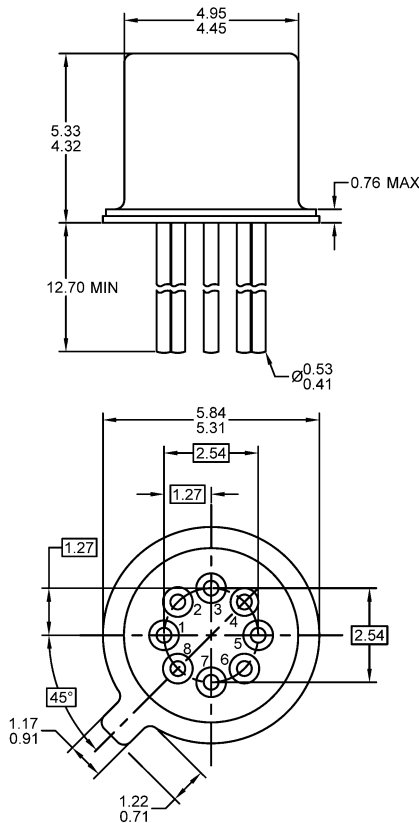
| Parameters | Conditions | IFN3954, IFN3955, IFN3956 | | | Unit |
|--|---|---------------------------|-----|--------------|----------|
| | | Min | Typ | Max | |
| $V_{(BR)GSS}$ Gate to Source Breakdown Voltage | $I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$ | -50 | | | V |
| I_{GSS} Gate to Source Reverse Current | $V_{GS} = -30\text{V}, V_{DS} = 0\text{V}, T_A = 25^\circ\text{C}$ $V_{GS} = -30\text{V}, V_{DS} = 0\text{V}, T_A = 125^\circ\text{C}$ | | | -100 -500 | pA nA |
| I_G Gate Operating Current | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, T_A = 25^\circ\text{C}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, T_A = 125^\circ\text{C}$ | | | -50 -250 | pA nA |
| $V_{GS(OFF)}$ Gate to Source Cutoff Voltage | $V_{DS} = -20\text{V}, I_G = 1\text{nA}$ | -1 | | -4.5 | V |
| V_{GS} Gate Source Voltage | $V_{DS} = 20\text{V}, I_D = 50\mu\text{A}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ | -0.5 | | -4.2 -4 | V |
| $V_{GS(F)}$ Gate Source Forward Voltage | $V_{DS} = 0\text{V}, I_G = 1\text{mA}$ | | | 2 | V |
| I_{DSS} Drain to Source Saturation Current | $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$ (Pulsed) | 0.5 | | 5 | mA |

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

| Parameters | Conditions | IFN3954, IFN3955, IFN3956 | | | Unit |
|--|--|---------------------------|-----|---------------|----------------------|
| | | Min | Typ | Max | |
| G_{FS} Forward Transconductance | $V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{kHz}$ $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 200\text{MHz}$ | 1000 1000 | | 3000 | μS |
| G_{OS} Output Conductance | $V_{DS} = 20\text{V}, f = 1\text{kHz}$ | | | 35 | μS |
| C_{ISS} Input Capacitance | $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ | | | 4 | pF |
| C_{RSS} Reverse Capacitance | $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ | | | 1.2 | pF |
| NF Noise Figure | $V_{DS} = 20\text{V}, f = 10\text{Hz}, R_G = 10\text{M}\Omega$ | | | 0.5 | dB |
| $ I_{G1} - I_{G2} $ Differential Gate Current | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, T_A = 125^\circ\text{C}$ | | | 10 | nA |
| I_{DSS1}/I_{DSS2} Saturation Drain Current Ratio | $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$ | 0.95 | | 1 | |
| $ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ | | | 5 10 15 | mV |
| $\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ $T_0 = -55^\circ\text{C} \text{ to } 125^\circ\text{C}$ | | | 1 2.5 5 | mV/ $^\circ\text{C}$ |
| g_{fs1}/g_{fs2} Transconductance Ratio | $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$ | 0.97 | | 1 | |

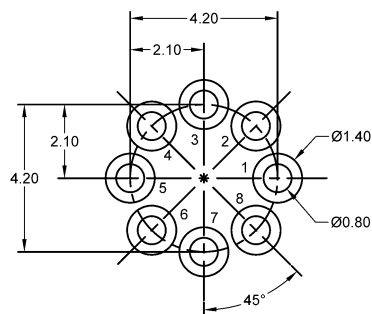
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.