







IFN3957, IFN3958 Dual Matched N-Channel JFET

Features

- InterFET N0016H Geometry
- Typical Noise: 6 nV/VHz
- · Low Ciss: 3.5pF Typical
- · High Input Impedance
- Replacement for 2N3957,8 Parts
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

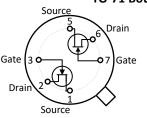
Applications

- · Differential Amplifiers
- · Low Noise Pre-Amplifier
- · High Impedance Amplifier

Description

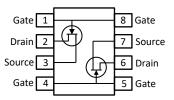
The -50V InterFET IFN3957 and IFN3958 matched pair JFET's are targeted for high input impedance applications for mid to high frequency designs. Gate leakages are typically 10pA at room temperatures. Parts are matched down to 5mV. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

TO-71 Bottom View





SOIC8 Top View





Product Summary

	Parameters	IFN3957 Min	IFN3958 Min	Unit
BV _{GSS}	Gate to Source Breakdown Voltage	-50	-50	V
I _{DSS}	Drain to Source Saturation Current	0.5	0.5	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	-1	-1	V
GFS	Forward Transconductance	1000	1000	μS

Ordering Information Custom Part and Rinning Ontions Available

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Part Number	Description	Case	Packaging			
IFN3957; IFN3958	Through-Hole	TO-72	Bulk			
SMP3957; SMP3958	Surface Mount	SOIC8	Bulk			
	7" Tape and Reel: Max 500 Pieces		Minimum 500 Pieces			
SMP3957TR; SMP3958TR	13" Tape and Reel: Max 2,500 Pieces	SOIC8	Tape and Reel			
IFN3957COT; IFN3958COT *	Chip Orientated Tray (COT Waffle Pack)	СОТ	70/Waffle Pack			
IFN3957CFT; IFN3958CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack			

^{*} Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-50	V
I _{FG}	Continuous Forward Gate Current	50	mA
PD	Continuous Device Power Dissipation	250	mW
Р	Power Derating	4.3	mW/°C
Tı	Operating Junction Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-65 to 175	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			IFN3957, IFN3958			
	Parameters	Conditions	Min	Тур	Max	Unit
V _{(BR)GSS}	Gate to Source Breakdown Voltage	$I_{G} = -1\mu A, V_{DS} = 0V$	-50			V
I _{GSS}	Gate to Source Reverse Current	$V_{GS} = -30V$, $V_{DS} = 0V$, $T_A = 25$ °C $V_{GS} = -30V$, $V_{DS} = 0V$, $T_A = 125$ °C			-100 -500	pA nA
IG	Gate Operating Current	V _{DS} = 20V, I _D = 200μA, T _A = 25°C V _{DS} = 20V, I _D = 200μA, T _A = 125°C			-50 -250	pA nA
V _{GS(OFF)}	Gate to Source Cutoff Voltage	$V_{DS} = -20V, I_G = 1nA$	-1		-4.5	V
V _{GS}	Gate Source Voltage	V _{DS} = 20V, I _D = 50μA V _{DS} = 20V, I _D = 200μA	-0.5		-4.2 -4	V
V _{GS(F)}	Gate Source Forward Voltage	$V_{DS} = 0V$, $I_G = 1mA$			2	
I _{DSS}	Drain to Source Saturation Current	$V_{DS} = 20V, V_{GS} = 0V$ (Pulsed)	0.5		5	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

-				IFN3957, IFN3958			
P	arameters	Conditions		Min	Тур	Max	Unit
GFS	Forward	$V_{DS} = 10V, V_{GS} = 0V, f = 0$	= 1kHz	1000		3000	115
GFS	Transconductance	$V_{DS} = 20V$, $V_{GS} = 0V$, $f = 200MHz$		1000			μS
Gos	Output Conductance	V _{DS} = 20V, f = 1k⊦	lz			35	μS
C _{iss}	Input Capacitance	$V_{DS} = 20V, V_{GS} = 0V, f =$	1MHz			4	pF
C _{rss}	Reverse Capacitance	$V_{DS} = 20V, V_{GS} = 0V, f =$	1MHz			1.2	рF
NF	Noise Figure	V _{DS} = 20V, f = 10Hz, R _G =	= 10MΩ			0.5	dB
$ I_{G1} - I_{G2} $	Differential Gate Current	V _{DS} = 20V, I _D = 200μA, Τ _A	= 125°C			10	nA
I _{DSS1} /I _{DSS2}	Saturation Drain	$V_{DS} = 20V, V_{GS} = 0V$	IFN3957	0.90		1	
IDSS1/IDSS2	Current Ratio	VBS = 20V, VGS = 0V	IFN3958	0.85		1	
 V _{GS1} – V _{GS2}	Differential Gate	V _{DS} = 20V, I _D = 200μA	IFN3957			20	mV
•GS1 - •GS2	Source Voltage	V DS = 20V, ID = 200μA	IFN3958			25	IIIV
 V _{GS1} – V _{GS2}	Differential Gate	V _{DS} = 20V, I _D = 200μA	IFN3957			5	
$\int \frac{ \sqrt{GS1} - \sqrt{GS2} }{\Delta T}$	Source Voltage with	$T_0 = -55^{\circ}\text{C to } 125^{\circ}\text{C}$	IFN3958			5 5	mV/°C
	Temperature	.0 55 6 10 125 6					
gfs1/gfs2	Transconductance	$V_{DS} = 20V$, $I_D = 200 \mu A$,	IFN3957	0.90		1	
P121/ P127	Ratio	f = 1kHz	IFN3958	0.85		1	



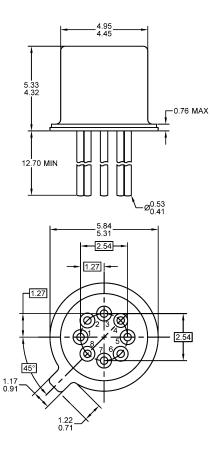






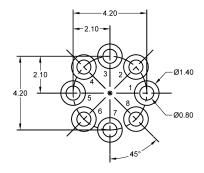
TO-71 Mechanical and Layout Data

Package Outline Data



- 1. All linear dimensions are in millimeters.
- Eight leaded device. Not all leads are shown in drawing views.
- 3. Some package configurations will not populate pin 8 and/or pin 4.
- 4. Package weight approximately 0.35 grams
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- Pads 8 and/or pad 4 can be eliminated for devices with less pins.
- The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.