IFN3993/A, IFN3994/A P-Channel JFET

Features

- InterFET P0099F Geometry
- Typical Noise: 8 nV/√Hz
- Fast Switching
- Replacement for 2N3993,4 Parts
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

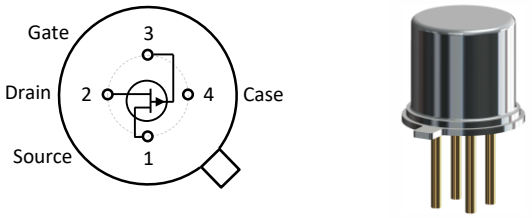
Applications

- Choppers
- High Speed Commutators

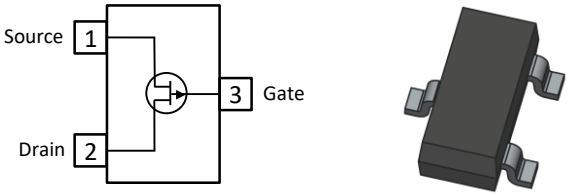
Description

The 25V InterFET IFN3993/A and IFN3994/A are targeted for choppers and high speed commutator designs. The on resistance is typically less than 100 Ohms at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

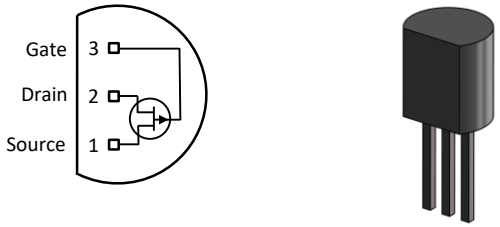
TO-72 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary (Highlighted values = A variant)

Parameters		IFN3993/A Min	IFN3994/A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	25	25	V
I_{DSS}	Drain to Source Saturation Current	-10	-2	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	4	1	V
G_{FS}	Forward Transconductance	6	4	µS
		7	5	

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN3993; IFN3994 IFN3993A; IFN3994A	Through-Hole	TO-72	Bulk
PN3993; PN3994 PN3993A; PN3994A	Through-Hole	TO-92	Bulk
SMP3993; SMP3994 SMP3993A; SMP3994A	Surface Mount	SOT23	Bulk
SMP3993TR; SMP3994TR SMP3993ATR; SMP3994ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFN3993COT; IFN3994COT IFN3993ACOT; IFN3994ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN3993CFT; IFN3994CFT IFN3993ACFT; IFN3994ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	25	V
I_{FG}	Continuous Forward Gate Current	-10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	2.4	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

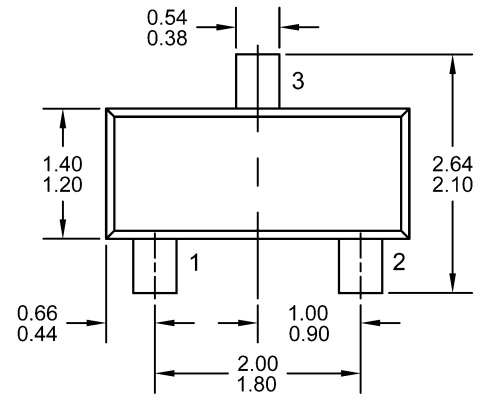
Parameters		Conditions	IFN3993/A		IFN3994/A		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 1µA	25		25		V
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -10V, I_D = -1µA	4	9.5	1	5.5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -10V (Pulsed)	-10		-2		mA
I_{DGO}	Drain Reverse Current	V_{GS} = -15V, I_S = 0A, T_A = 25°C V_{GS} = -15V, I_S = 0A, T_A = 150°C		-1.2		-1.2	nA µA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = -10V, V_{GS} = 10V, T_A = 25°C V_{DS} = -10V, V_{GS} = 10V, T_A = 150°C		-1.2 -1		-1.2 -1	nA µA

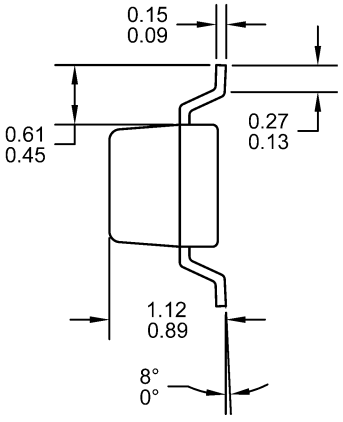
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified, Highlighted values = A variant)

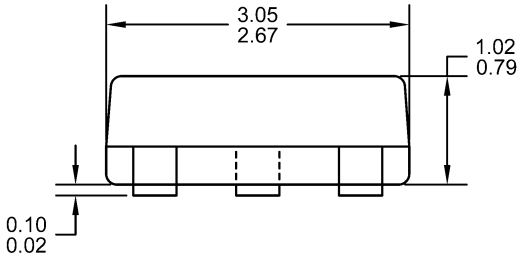
Parameters		Conditions	IFN3993/A		IFN3994/A		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = -10V, V_{GS} = 0V, f = 1kHz	6 7	12 12	4 5	10 10	mS
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		150		300	Ω
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		16 12		16 12	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = 10V, f = 1MHz		4.5 3		5 3.5	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

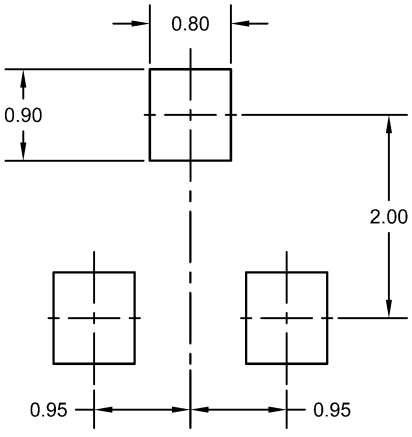






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

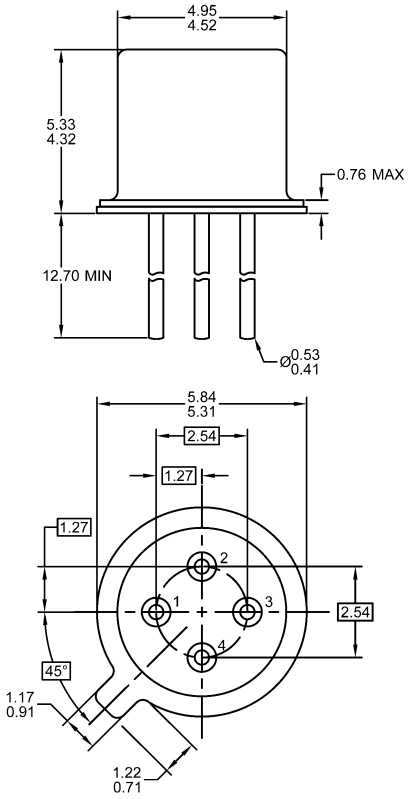
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

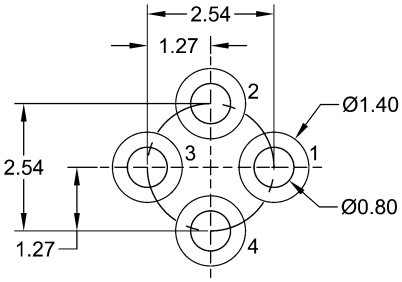
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.