







IFNU401, IFNU402, IFNU403 Dual Matched N-Channel JFET

Features

InterFET <u>N0016H Geometry</u>
 Low Leakage: 10 pA Typical

• Low Input Capacitance: 3.5 pF Typical

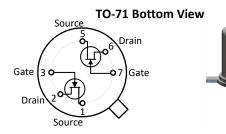
- · High Input Impedance
- Replacement for U401,2,3
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

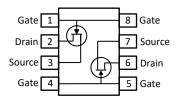
- · Low Noise Differential Amplifier
- · Differential Amplifier
- JFET Input Op-Amps

Description

The -50V InterFET IFNU401, IFNU402, and IFNU403 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



SOIC8 Top View





Product Summary

	Parameters	IFNU401 Min	IFNU402 Min	IFNU403 Min	Unit
BV_GSS	Gate to Source Breakdown Voltage	-50	-50	-50	V
I _{DSS}	Drain to Source Saturation Current	0.5	0.5	0.5	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
G_{FS}	Forward Transconductance	2	2	2	mS

Ordering Information Custom Part and Binning Options Available

Cidering information custom Part and Binning Options Available						
Part Number	Description	Case	Packaging			
IFNU401; IFNU402; IFNU403	Through-Hole	TO-71	Bulk			
SMPU401; SMPU402; SMPU403	Surface Mount	SOIC8	Bulk			
	7" Tape and Reel: Max 500 Pieces		Minimum 500 Pieces			
SMPU401; SMPU402; SMPU403	13" Tape and Reel: Max 2,500 Pieces	SOIC8	Tape and Reel			
IFNU401COT; IFNU402COT;						
IFNU403COT *	Chip Orientated Tray (COT Waffle Pack)	СОТ	70/Waffle Pack			
IFNU401CFT; IFNU402CFT;						
IFNU403CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack			

^{*} Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-50	V
I _{FG}	Continuous Forward Gate Current	50	mA
PD	Continuous Device Power Dissipation	300	mW
Р	Power Derating	2.8	mW/°C
Tı	Operating Junction Temperature	-55 to 125	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			IFNU401, IFNU402, IFNU403			
	Parameters	Conditions	Min	Тур	Max	Unit
V _{(BR)GSS}	Gate to Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0V$	-50			V
I _{GSS}	Gate to Source Reverse Current	$V_{GS} = -30V, V_{DS} = 0V$			-25	pА
IG	Gate Operating Current	$V_{DS} = 15V$, $I_D = 200\mu A$, $T_A = 125 ^{\circ}C$ $V_{DS} = 15V$, $I_D = 200\mu A$, $T_A = 125 ^{\circ}C$			-15 -10	pA nA
V _{GS(OFF)}	Gate to Source Cutoff Voltage	V _{DS} = 20V, I _D = 1nA	-0.5		-2.5	V
V _{GS}	Gate Source Voltage	$V_{DS} = 20V$, $I_D = 200 \mu A$	-0.2		-2.3	V
I _{DSS}	Drain to Source Saturation Current	V_{DS} = 20V, V_{GS} = 0V (Pulsed)	0.5		10	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

				IFNU40	IFNU401, IFNU402, IFNU403		
Parameters		Conditions		Min	Тур	Max	Unit
GFS	Forward Transconductance	$V_{DS} = 10V, V_{GS} = 0V, f = V_{DS} = 15V, I_D = 200\mu A, f$		2 1		7 2	mS
Gos	Output Conductance	$V_{DS} = 10V, V_{GS} = 0V, f = V_{DS} = 15V, I_D = 200\mu A, f$				20 2	μS
C _{iss}	Input Capacitance	V_{DS} = 15V, I_{D} = 200 μ A, f	= 1MHz			8	pF
Crss	Reverse Capacitance	$V_{DS} = 15V$, $I_D = 200\mu A$, f	= 1MHz			3	pF
e _n	Equivalent Circuit Input Noise Voltage	$V_{DS} = 20V$, $I_D = 200\mu A$, f	= 100Hz			20	nV/√Hz
V _{GS1} – V _{GS2}	Differential Gate Source Voltage	V _{DS} = 10V, I _D = -200μA	IFNU401 IFNU402 IFNU403			5 10 10	mV
$\frac{\left V_{GS1}-V_{GS2}\right }{\Delta T}$	Differential Gate Source Voltage with Temperature	V _{DS} = 10V, I _D = 200μA T _A = 25°C, T _B = 85°C	IFNU401 IFNU402 IFNU403			1 2.5 4	mV/°C
CMRR	Common Mode Rejection Ratio	$V_{DD} = 10V \text{ to } 20V,$ $I_D = 200 \mu A$	IFNU401 IFNU402 IFNU403		95 95 95		dB



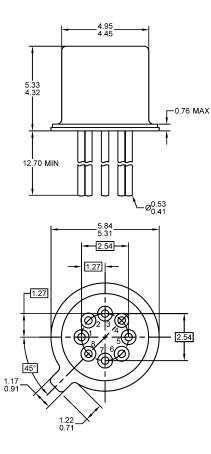






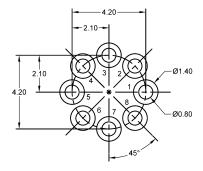
TO-71 Mechanical and Layout Data

Package Outline Data



- 1. All linear dimensions are in millimeters.
- Eight leaded device. Not all leads are shown in drawing views.
- 3. Some package configurations will not populate pin 8 and/or pin 4.
- 4. Package weight approximately 0.35 grams
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- 2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
- The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.