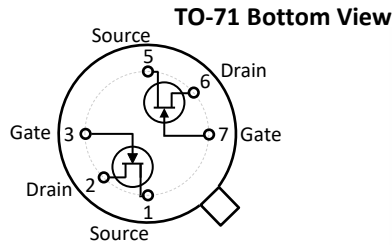


IFNU410, IFNU411, IFNU412 Dual Matched N-Channel JFET

Features

- InterFET [N0016H Geometry](#)
- Low Leakage: 10 pA Typical
- Low Input Capacitance: 3.5 pF Typical
- High Input Impedance
- Replacement for U410, U411, U412
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

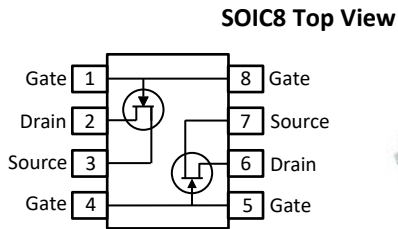


Applications

- Low Noise Differential Amplifier
- Differential Amplifier
- Wide-Band Amplifier

Description

The -40V InterFET IFNU410, IFNU411, and IFNU412 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



Product Summary

Parameters	IFNU410 Min	IFNU411 Min	IFNU412 Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS} Drain to Source Saturation Current	0.5	0.5	0.5	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.5	-0.5	-0.5	V
G_{FS} Forward Transconductance	1 0.6	1 0.6	1 0.6	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFNU410; IFNU411; IFNU412	Through-Hole	TO-71	Bulk
SMPU410; SMPU411; SMPU412	Surface Mount	SOIC8	Bulk
SMPU410; SMPU411; SMPU412	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU410COT; IFNU411COT; IFNU412COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU410CFT; IFNU411CFT; IFNU412CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation	375	mW
P Power Derating	3	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

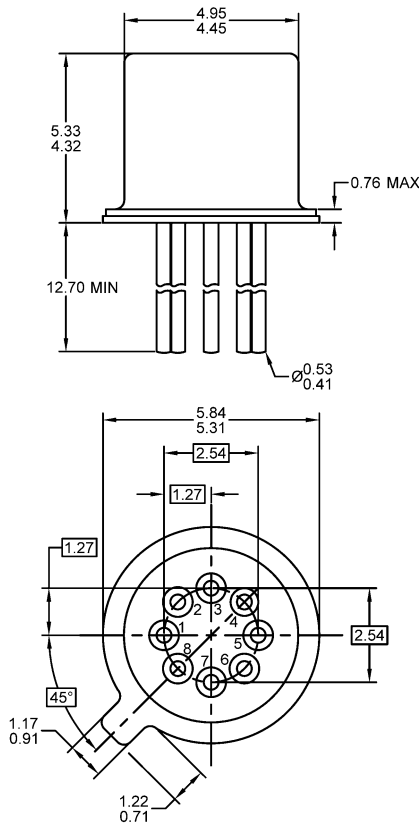
Parameters	Conditions	IFNU410, IFNU411, IFNU412			Unit
		Min	Typ	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$	-40			V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$			-0.2	nA
I_G Gate Operating Current	$V_{DS} = 10\text{V}, I_D = 200\mu\text{A}$			-200	pA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 20\text{V}, I_D = 1\text{nA}$	-0.5		-3.5	V
V_{GS} Gate Source Voltage	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$	-0.2		-3	V
I_{DSS} Drain to Source Saturation Current	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$ (Pulsed)	0.5		5	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFNU410, IFNU411, IFNU412			Unit
		Min	Typ	Max	
G_{FS} Forward Transconductance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{kHz}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$	1 0.6		4 1.2	mS
G_{OS} Output Conductance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{kHz}$ $V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 1\text{kHz}$			20 5	μS
C_{iss} Input Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$			4.5	pF
C_{rss} Reverse Capacitance	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$			1.2	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}, f = 100\text{Hz}$		20	70	nV/ $\sqrt{\text{Hz}}$
$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage	$V_{DS} = 20\text{V}, I_D = -200\mu\text{A}$			10 20 40	mV
$\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature	$V_{DS} = 20\text{V}, I_D = 200\mu\text{A}$ $T_A = 25^\circ\text{C}, T_B = 85^\circ\text{C}$			1 2.5 4	mV/ $^\circ\text{C}$
CMRR Common Mode Rejection Ratio	$V_{DD} = 10\text{V to } 20\text{V},$ $I_D = 200\mu\text{A}$		80 80 70		dB

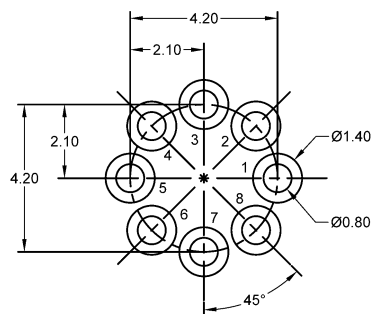
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.