

# INFU424, INFU425, INFU426 Dual Matched N-Channel JFET

## Features

- InterFET [N0001H Geometry](#)
- Low Leakage: 0.25 pA Typical
- Low Input Capacitance: 2.0 pF Typical
- High Input Impedance
- Replacement for U424, U425, U426
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

## Applications

- Low Leakage Input Buffer
- High Frequency Amplifier/Buffer
- Ultrahigh Impedance Pre-Amplifier
- Impedance Converters

## Description

The -40V InterFET IFNU424, IFNU425, and IFNU426 JFET's are targeted for ultra high input impedance applications for differential amplification and impedance matching. Gate leakages are less than 1pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

## Product Summary

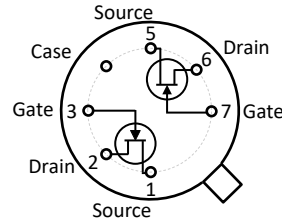
Parameters	INFU424 Min	INFU425 Min	INFU426 Min	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	-40	-40	-40	V
$I_{DSS}$ Drain to Source Saturation Current	60	60	60	$\mu A$
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.4	-0.4	-0.4	V
$G_{FS}$ Forward Transconductance	100	100	100	$\mu S$

## Ordering Information Custom Part and Binning Options Available

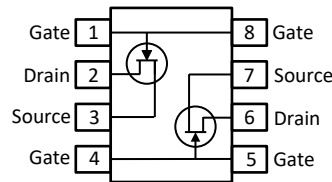
Part Number	Description	Case	Packaging
IFNU424; IFNU425; IFNU426	Through-Hole	TO-78	Bulk
SMPU424; SMPU425; SMPU426;	Surface Mount	SOIC8	Bulk
SMPU424TR; SMPU425TR; SMPU426TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU424COT; IFNU425COT; IFNU426COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU424CFT; IFNU425CFT; IFNU426CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

\* Bare die packaged options are designed for matched specifications but not 100% tested

TO-78 Bottom View



SOIC8 Top View



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V <sub>RGS</sub> Reverse Gate Source and Gate Drain Voltage	-40	V
I <sub>FG</sub> Continuous Forward Gate Current	50	mA
P <sub>D</sub> Continuous Device Power Dissipation	400	mW
P Power Derating	3.2	mW/°C
T <sub>J</sub> Operating Junction Temperature	-55 to 150	°C
T <sub>STG</sub> Storage Temperature	-60 to 200	°C

### Static Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

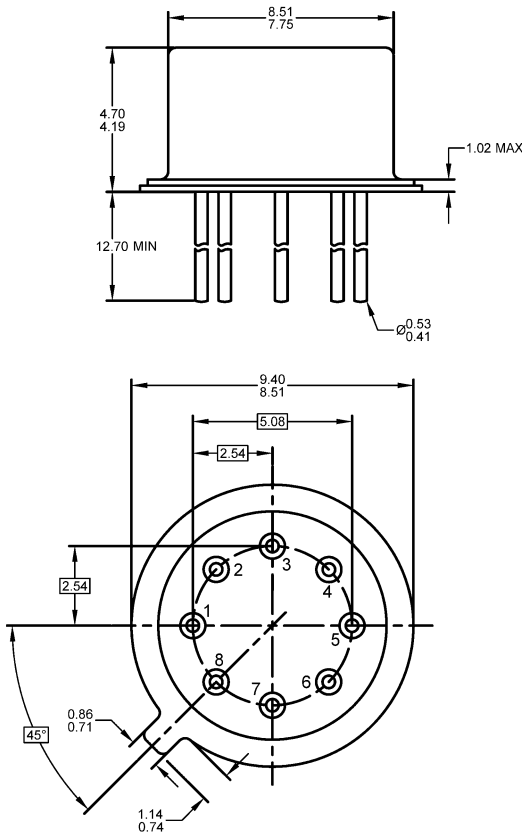
Parameters	Conditions	INFU424, INFU425, INFU426			Unit
		Min	Typ	Max	
V <sub>(BR)GSS</sub> Gate to Source Breakdown Voltage	I <sub>G</sub> = -1μA, V <sub>DS</sub> = 0V	-40	-60		V
BV <sub>G1G2</sub> Gate to Gate Breakdown Voltage	I <sub>G</sub> = -1μA, I <sub>D</sub> = 0A, I <sub>S</sub> = 0A	±40			V
I <sub>GSS</sub> Gate to Source Reverse Current	V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 25°C V <sub>GS</sub> = -20V, V <sub>DS</sub> = 0V, T <sub>A</sub> = 125°C			-3 -3	pA nA
I <sub>G</sub> Gate Operating Current	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA, T <sub>A</sub> = 25°C V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA, T <sub>A</sub> = 125°C			-0.5 -500	pA pA
V <sub>GS(OFF)</sub> Gate to Source Cutoff Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA	-0.4		-3	V
V <sub>GS</sub> Gate Source Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA			-2.9	V
I <sub>DSS</sub> Drain to Source Saturation Current	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V (Pulsed)	60	1800		μA

### Dynamic Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Conditions	INFU424, INFU425, INFU426			Unit
		Min	Typ	Max	
G <sub>FS</sub> Forward Transconductance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1kHz	100		1500	μS
G <sub>OS</sub> Output Conductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA, f = 1kHz			3	μS
C <sub>iss</sub> Input Capacitance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1MHz			3	pF
C <sub>rss</sub> Reverse Capacitance	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1MHz			1.5	pF
e <sub>n</sub> Equivalent Circuit Input Noise Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA, f = 10Hz		20	70	nV/√Hz
NF Noise Figure	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA, f = 10Hz, R <sub>G</sub> = 1MΩ			1	dB
V <sub>GS1</sub> - V <sub>GS2</sub>   Differential Gate Source Voltage	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA			10 15 25	mV
$\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature	V <sub>DS</sub> = 10V, I <sub>D</sub> = 30μA T <sub>A</sub> = -55°C, T <sub>B</sub> = 25°C, T <sub>C</sub> = 125°C			1 2.5 5	mV/°C
CMRR Common Mode Rejection Ratio	V <sub>DD</sub> = 10V to 20V, I <sub>D</sub> = 30μA	90 80 80			dB

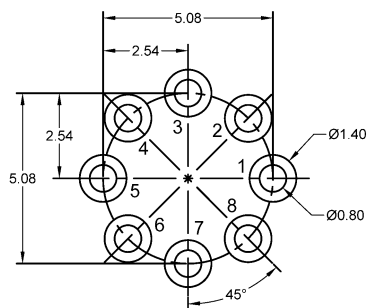
## TO-78 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.