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Data Sheet IHD 260/660

Dual Channel SCALE IGBT Driver Core

A successor to the IHD 215/280/680 dual-gate driver cores for 1200V and 1700V IGBTs

The IHD 260 and IHD 660 (short IHDx60) are highly-integrated dual IGBT driver cores based on CONCEPT's proprietary SCALE technology which has been established on the market as an industrial standard since 1999.

As most customers apply the IHD 215, IHD 280 and IHD 680 drivers in a similar way, the IHDx60 covers a dedicated set of compatible items to give the benefits of optimum performance, optimum reliability and a competitive price.

The driver cores are optimized to match various IGBTs and applications from 25A to 450A and 1200V to 1700V.

Typical applications include half-bridge control of 1700V/75A IGBTs at switching frequencies up to 100kHz and 1700V/450A IGBTs at switching frequencies up to 18.5kHz for the IHD660 version.

Features

- ✓ Direct replacement of IHD 215/280/680
- ✓ Highly approved SCALE technology
- ✓ Non-inverting or optionally inverting inputs
- ✓ Gate drive capability 6A, 1W or 3W each
- ✓ Typical delay time of 315ns
- ✓ Power supply voltage monitoring set to 11.5V
- ✓ Superior EMC (dv/dt > 100V/ns, ESD > 2kV)
- ✓ Direct driving of two independent driver channels
- ✓ Command signal transmitted via transformer interface
- ✓ Fault signal via transformer interface or optional optocoupler
- ✓ 25ms blocking time at fault with custom-specific time options

Applications

- ✓ Driving 1200V and 1700V IGBTs
- ✓ Switching DC to 100 kHz
- ✓ Duty cycle 0 ... 100%
- ✓ Operating temp. -40 ... +85 °C
- ✓ Two-level topologies
- ✓ AC drives, SMPS, etc.
- ✓ Industry, traction, wind power

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Compatibility to IHD 215/280/680 Gate Drivers

The IHDx60 are available with different options covering a dedicated set of compatible items. In this data sheet, the text referring to critical compatible items is underlined.

Option N and Option I select between non-inverting and inverting inputs respectively. It is no longer possible to interchange the IN+ and IN- inputs to invert the logic as could be done with IHD 215/280/680.
On the secondary side, any fault state is extended by a period known as the command blocking time. During this time, the driver is kept in the off-state. The command blocking time is set at the factory to a nominal value of 25ms. Other values upon request. It is no longer possible for the application to adjust the blocking time.

For option T, the signal transformer interface is used to transfer the secondary fault signal to the primary side. This transfer may be performed at each change in the command signal, but only during the blocking time. For option C, an optocoupler is used to transfer the secondary-side fault state to the primary side within a delay of less than several microseconds. The initial creepage distance and the maximum operating voltage are reduced by the optocoupler.

For a summary, refer to the Ordering Information section on the last page.

Block Diagram of IHDx60 Option T

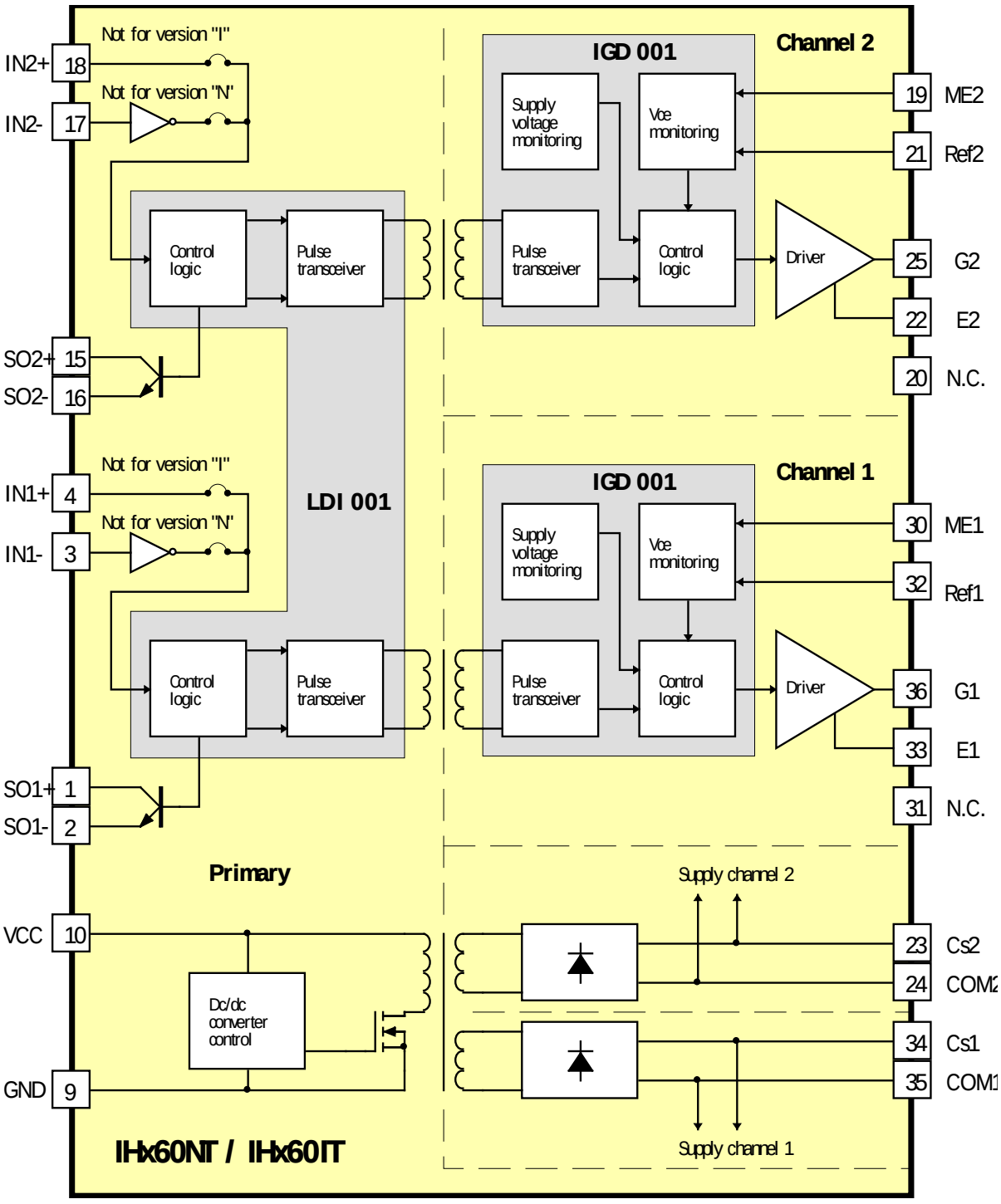

Fig. 1 Block diagram of the IHDx60 (option T, i.e. fault signal via signal transformer interface). Non-inverting inputs (option N) or inverting inputs (option I). Not connected pins are designated as N.C.

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Block Diagram of IHDx60 Option C

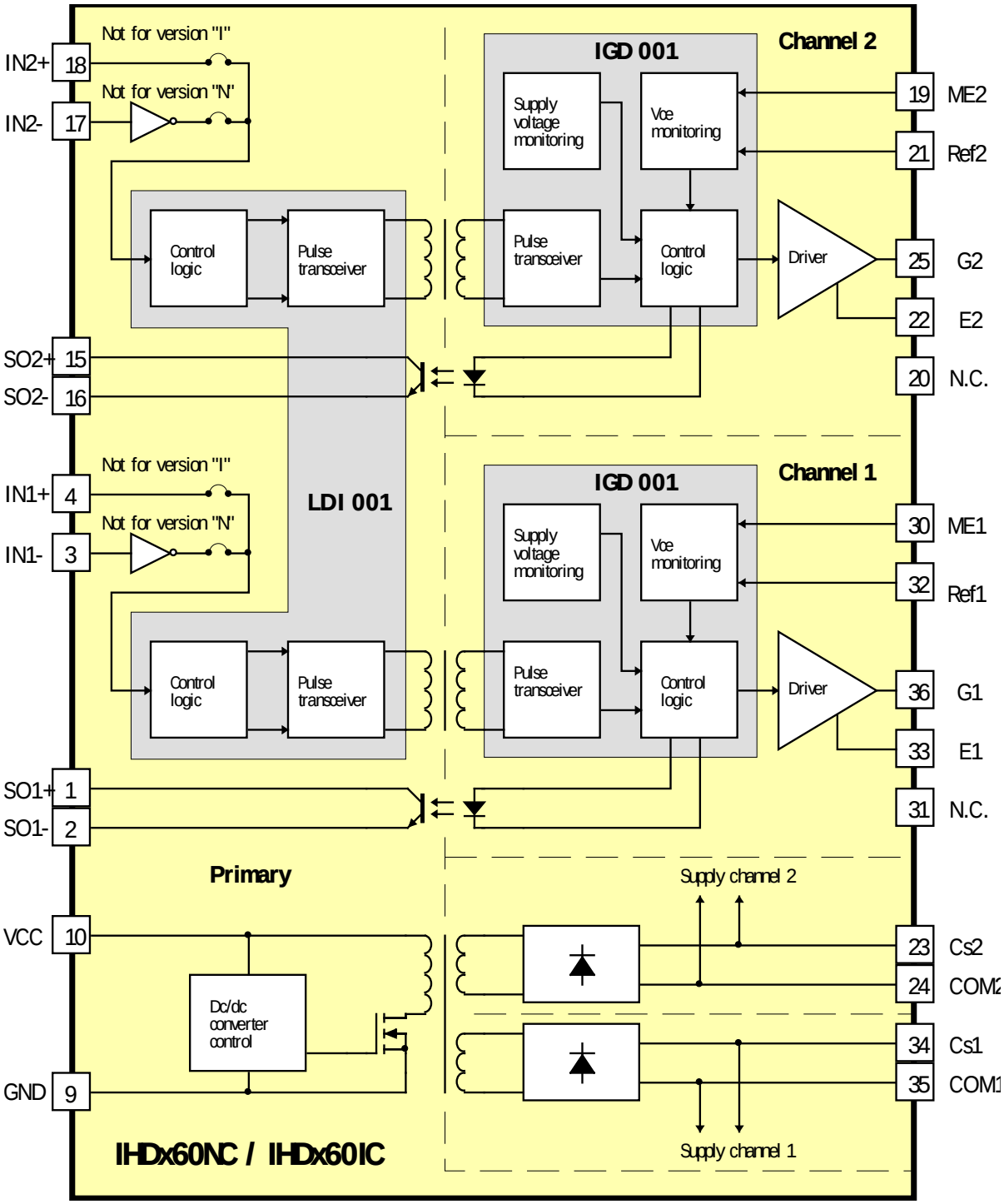

Fig. 2 Block diagram of the IHDx60 (option C, i.e. fault signal via optocoupler). Non-inverting inputs (option N) or inverting inputs (option I). Not connected pins are designated as N.C.

Pin Description

No.	Pin Name	Function
1-18		**Primary-side terminal**
1	SO1+	Status output positive voltage referenced to pin SO1- for channel 1
2	SO1-	Status output negative voltage referenced to pin SO1+ for channel 1
3	IN1-	For option I: Inverting input referenced to GND for channel 1
		For option N: Functionless CMOS input (must be terminated to logic high or logic low)
4	IN1+	For option N: Non-inverting input referenced to GND for channel 1
		For option I: Functionless CMOS input (must be terminated to logic high or logic low)
5-8	free	Not physically present
9	GND	Power supply and logic ground
10	VCC	Power supply positive voltage referenced to pin GND
11-14	free	Not physically present
15	SO2+	Status output positive voltage referenced to pin SO1- for channel 2
16	SO2-	Status output negative voltage referenced to pin SO1+ for channel 2
17	IN1-	For option I: Inverting input referenced to GND for channel 2
		For option N: Functionless CMOS input (must be terminated to logic high or logic low)
18	IN1+	For option N: Non-inverting input referenced to GND for channel 2
		For option I: Functionless CMOS input (must be terminated to logic high or logic low)
36-19		**Secondary-side terminal**
36	G1	Gate driver output for channel 1
35	COM1	Common terminal for channel 1
34	Cs1	16.4V nominal voltage power supply referenced to pin COM1
33	E1	IGBT emitter channel 1 terminal
32	REF1	Reference voltage for short-circuit monitoring referenced to pin E1 for channel 1
31	N.C.	The command blocking time at fault is set at the factory; options upon request
30	ME1	IGBT collector voltage monitoring input referenced to pin E1 for channel 1
29-26	free	Not physically present
25	G2	Gate driver output for channel 2
24	COM2	Common terminal for channel 2
23	Cs2	16.4V nominal voltage power supply referenced to pin COM2
22	E2	IGBT emitter channel 2 terminal
21	REF2	Reference voltage for short-circuit monitoring referenced to pin E2 for channel 2
20	N.C.	The command blocking time at fault is set at the factory; options upon request
19	ME2	IGBT collector voltage monitoring input referenced to pin E2 for channel 2

Not connected pins are designated as N.C.

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Mechanical Data

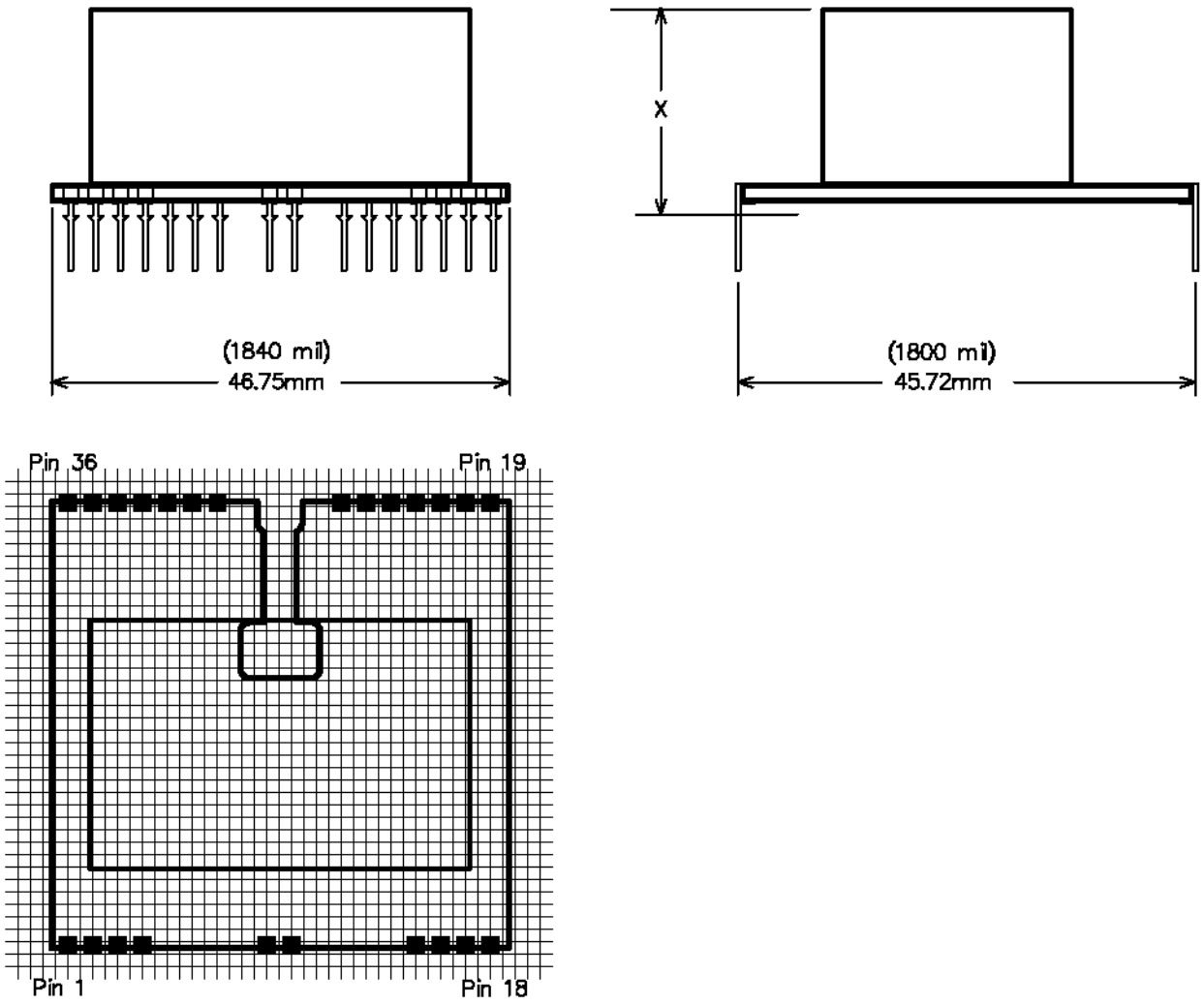

Fig. 3 *Footprint of IHDX60. Grid is 1.27mm (50mil). Recommended diameter of solder pad is 1.6mm. Recommended diameter of drill holes is 1.0mm.*
Height X = 18.5mm +/- 0.5mm for option T.
Height X = 20.5mm +/- 0.5mm for option C.

Absolute Maximum Ratings

Parameter	Condition/remark	Min.	Max.	Units
Primary supply voltage VCC	To GND	0	16	V
Pin G* IGBT gate pulse current		-6.0	+6.0	A
IGBT average gate power IHD260	(Note 2)		1.0	W
IGBT average gate power IHD660	(Note 2, fig. 4)		3.0	W
Primary supply current IHD260	Continuous, after startup sequence		200	mA
Primary supply current IHD660	Continuous, after startup sequence		500	mA
Pin IN* voltage		0	VCC	V
Pin SO* voltage		0	VCC	V
Pins REF*, ME* voltages	To respective COM*	0	VCC	V
Operating ambient temperature	Continuous	-40	85	°C
Storage ambient temperature		-45	90	°C
Lead temperature	Soldering, 5 seconds		260	°C

Unless otherwise specified, all data refer to a primary supply voltage of 15V and an ambient temperature of +25°C.

Recommended Operating Conditions

Parameter	Condition/remark	Min.	Max.	Units
Primary supply voltage VCC	To GND	14	16	V
Duty cycle		0	1	
Total external gate resistance	(Note 3)	4.7		Ω

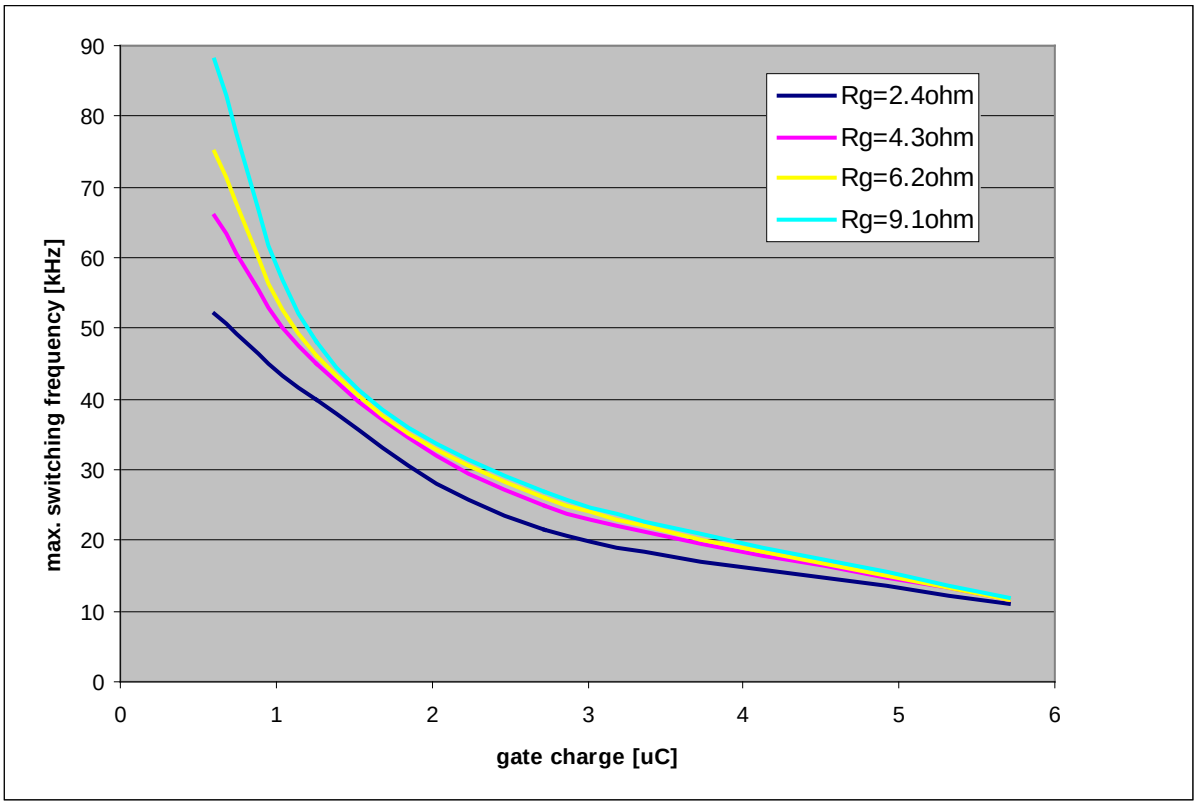

Fig. 4 Derating curves valid for IHD660 at an ambient temperature of 85°C (no derating for IHD260)

Electrical Characteristics

Unless otherwise specified, all data refer to a primary supply voltage of 15V and an ambient temperature of +25°C. Minimum and maximum values refer to the specified maximum rated operating range at ambient temperature.

Power supply	**Condition/remark**	**Min.**	**Typ.**	**Max.**	**Units**
Primary supply current	Without gate load		70		mA
Secondary supply voltage V(Cs, COM)		15.6	16.4	16.8	V
Turn-on gate-to-emitter voltage		14.0	15.1	15.95	V
Turn-off gate-to-emitter voltage		-14.0	-15.1	-15.95	V

Power supply monitoring	**Condition/remark**	**Min.**	**Typ.**	**Max.**	**Units**
Secondary supply |V(G, E)|	Clear fault state (note 1)		11.5		V
	Set fault state		10.8		V
	Hysteresis		0.7		V

Short-circuit monitoring	Condition/remark	Min.	Typ.	Max.	Units
Pin REF pull-up resistor to pin Cs		1425	1500	1575	Ω
Pin REF source current	From Cs (note 5)		150		µA
Pin ME pull-up resistor to pin Cs	(Note 5)	2090	2200	2310	Ω
Pin ME on-state source current	From Cs (note 5)		1.4		mA
Pin ME off-state sink current	Towards COM	80			mA
Pin ME off-state resistance	Towards COM			125	Ω
Pin REF on-state reference voltage	Functional limits (note 5)	2.5		12.5	V

Command blocking

When a fault state has been cleared, the next turn-on commands are ignored by the ASIC during the command blocking time to avoid thermal overload of the power MOSFET or IGBT driven by the gate driver.

	Condition/Remark	Min.	Typ.	Max.	Units
Command blocking time	Factory-set (other values upon request)	17	22	27	ms

Pins IN* Command Inputs	Condition/Remark	Min.	Typ.	Max.	Units
Logic level	Positive-going threshold		10		V
	Negative-going threshold		5		V
Bias sink current				1	mA
Pin capacitance				3	pF

Pin SO* Status Outputs

Secondary-side faults cause the relevant channel to turn off immediately. Fault states are transmitted to the primary side via the signal transformer interface (option T) or via an optocoupler (option C), in the latter case with an additional delay. They are then reported at Pin SOA for channel A and at pin SOB for channel B.

	Condition/Remark	Min.	Typ.	Max.	Units
Available current at pins SO	[V(VCC) – 1.2V] > V(SO+) > V(SO-)				
	Fault state			1	µA
	Otherwise	1000			µA
Delay to report a fault state	Option T:				
	during command blocking time	Until next change in relevant IN*			
	Option C		20		µs

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Gate Driving Characteristics	Condition/Remark	Min.	Typ.	Max.	Units
Equiv. delay time (note 4)	IGBT turn-on, option N		300		ns
	IGBT turn-off, option N		350		ns
	IGBT turn-on, option I		315		ns
	IGBT turn-off, option I		365		ns
Equiv. rise time (note 4)	IGBT turn-on		100		ns
Equiv. fall time (note 4)	IGBT turn-off		80		ns
Supported gate charge	(Note 9)			5.4	µC

Data refer to a gate charge of 1.2µC and a total external gate resistance of 5.6Ω.

Electrical Insulation	Condition/Remark	Min.	Typ.	Max.	Units
Operating voltage	For option T; continuous (note 6)			1500	V_{DC}
For option C; continuous (note 6)			600	1000	V_{DC}
Permitted d/dt V_{C*E*}	Ensured by design	100			V/ns
Test voltage	50 Hz/1 min (note 7)			4000	$V_{AC, eff}$
Partial discharge extinction volt.	To IEC270 (note 8)	1700			$V_{AC, pk}$
Creep path primary-secondary	Option T	19			mm
	Option C	8			mm
Creep path secondary-secondary		19			mm

Footnotes

1) The unipolar primary supply voltage with a nominal value of V(VCC, GND) = 15.0V is multiplied by a magnetic transformer, resulting in a unipolar secondary power supply voltage with a nominal value of V(Cs, COM) = 16.4V. To provide a bipolar gate-driving voltage with the nominal values of V(G, E) = +15.1V for turn-on and V(G, E) = - 15.1V for turn-off, both gate and emitter are switched in full-bridge configuration via biploar junction transistors (providing a total nominal level shift of 1.3V). The primary side is equipped with an automatic power-on reset which clears the fault memories when the supply voltage approaches a specified limit with a maximum value of 13.5V.
2) In typical applications (hard-switching topology using recommended gate resistors and gate charge) the switching frequency is primarily limited by the switching losses of the IGBT module or by the gate power due to the gate charge required by the module. The switching losses of the gate driver depend strongly on the particular operating conditions and increase with reducing the gate resistance and increasing switching frequency. For switching frequencies beyond 10kHz or gate charges beyond 55µC, the thermal limits of the gate driver may be exceeded. A derating of the IGBT average gate power is required under these estimated exemplary conditions. Conditions other than those specified may affect the reliability or lead to thermal breakdown of the gate drivers. Please ask our support team for a specific estimation. As a rule, the case temperature of any component of the gate driver should stay below 65°C for an ambient temperature of 25°C.
3) The total external gate resistance is the sum of the IGBT-internal chip resistances and the externally used gate resistors. Note that the driver-internal minimum resistance is below 0.2Ω. Due to the finite slew rate of the driver output voltage and to parasitic inductances in the gate control loop, however, the resulting gate current may not approach the nominal maximum value of 6.0A.
4) Equivalent delay, rise or fall times are derived from comparisons with the results obtained when modeling the driver as an ideal pulse-shaped voltage source with no delay and an infinite slew rate.
5) At the REF pin, a 1.5 kΩ resistor is connected to the positive voltage terminal Cs of the secondary-side power supply in parallel with a nominal 150µA current source. The reference voltage may be set via an external Zener diode or an external resistor connected to pin E. Furthermore, at pin ME a 2.2 kΩ resistor is connected to Cs in parallel with a nominal 1.4mA current source. This solution should be fully compatible with IHD series gate drivers in terms of function and parameters.
6) Maximum continuous or repeatedly applied DC voltage or peak value of the repeatedly applied AC voltage between any primary-side pin and any secondary-side pin. **Caution for option C:** operating voltages exceeding 600V may degrade the long-term characteristics of the optocouplers, resulting in an increased delay or a reduced current capability at pins SO*.
7) The test voltage of 4000 Vac(rms)/50 Hz may be applied only once during one minute. It should be noted that with this (strictly speaking obsolete) test method, some (minor) damage occurs to the insulation layers due to the partial discharge. Consequently, this test is not performed at CONCEPT as a series test. Where repeated insulation tests (e.g. module test, equipment test, system test) are run, the subsequent tests should be performed at a lower test voltage: the test voltage is reduced by 400 V for each additional test. The more modern if more elaborate partial-discharge measurement is preferable to such test methods as it is almost entirely non-destructive.
8) The partial discharge test is performed for each driver within the scope of series production.
9) The supported gate charge refers to the stability of the power supply voltages and to a dynamic voltage drop of 0.3V. Exceeding the maximum supported gate charge may lead to malfunction or thermal overload of the gate drivers. The customer may increase the specified maximum value of the supported gate charge by connecting additional supply capacitors between terminals Cs and COM up to a total of 47µF. Absolute gate charge must not exceed 55µC.

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Important Notice

The data contained in this product data sheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory!

Any handling of electronic devices is subject to the general specifications for protecting electrostatic-sensitive devices according to international standard IEC 747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

Disclaimer

This data sheet specifies devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given – either expressly or implicitly – regarding delivery, performance or suitability.

CT-Concept Technologie AG reserves the right to make modifications to its technical data and product specifications at any time without prior notice. The general terms and conditions of delivery of CT-Concept Technologie AG apply.

Technical Support

CONCEPT provides expert help for your questions and problems:

Internet: www.IGBT-Driver.com/go/support

Quality

The obligation to high quality is one of the central features laid down in the mission statement of CT-Concept Technologie AG. The quality management system covers all stages of product development and production up to delivery. The drivers of the SCALE series are manufactured to the ISO 9001 standard.