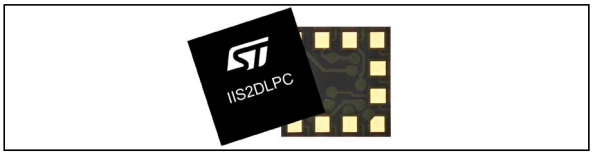
IIS2DLPC

MEMS digital output motion sensor: high-performance ultra-low-power 3-axis accelerometer for industrial applications

Datasheet - production data



Features

- ±2*g*/±4*g*/±8*g*/±16*g* full scale
- Multiple operating modes reconfigurable on the fly: from ultra-low-power to high-performance high-resolution mode
- Ultra-low power consumption: 50 nA in power-down mode, below 1 µA in active low-power mode, 120 µA in high-performance mode
- Output data rates from 1.6 Hz to 1600 Hz; bandwidth up to 800 Hz
- Single data conversion on demand
- Very low noise: down to 90 µ*g*/√Hz
- 32-level FIFO and 2 independent programmable interrupts
- High-speed I²C/SPI digital output interface
- Supply voltage, 1.62 V to 3.6 V
- Embedded temperature sensor
- Self-test
- 10000 *g* high shock survivability
- ECOPACK, RoHS and “Green” compliant

Applications

- Industrial IoT and connected devices
- Anti-tampering devices
- Appliances and robotics
- Industrial tools and factory equipment
- Portable healthcare devices and hearing aids
- Vibration monitoring
- Tilt/inclination measurements
- Smart power saving & motion-activated functions
- Impact recognition and logging

Description

The IIS2DLPC is an ultra-low-power high-performance three-axis linear accelerometer with digital I²C/SPI output interface which leverages on the robust and mature manufacturing processes already used for the production of micromachined accelerometers.

The IIS2DLPC has user-selectable full scales of ±2g/±4g/±8g/±16*g* and is capable of measuring accelerations with output data rates from 1.6 Hz to 1600 Hz.

The IIS2DLPC has one high-performance mode and 4 low-power modes which can be changed on the fly, providing outstanding versatility and adaptability to the requirements of the application.

The IIS2DLPC has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The IIS2DLPC has a dedicated internal engine to process motion and acceleration detection including free-fall, wakeup, highly configurable single/double-tap recognition, activity/inactivity, stationary/motion detection, portrait/landscape detection and 6D/4D orientation.

The IIS2DLPC is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order code	Temp. range [°C]	Package	Packaging
IIS2DLPCTR	-40 to +85	LGA-12	Tape and reel

Product label
LONGEVITY 10 YEARS COMMITMENT

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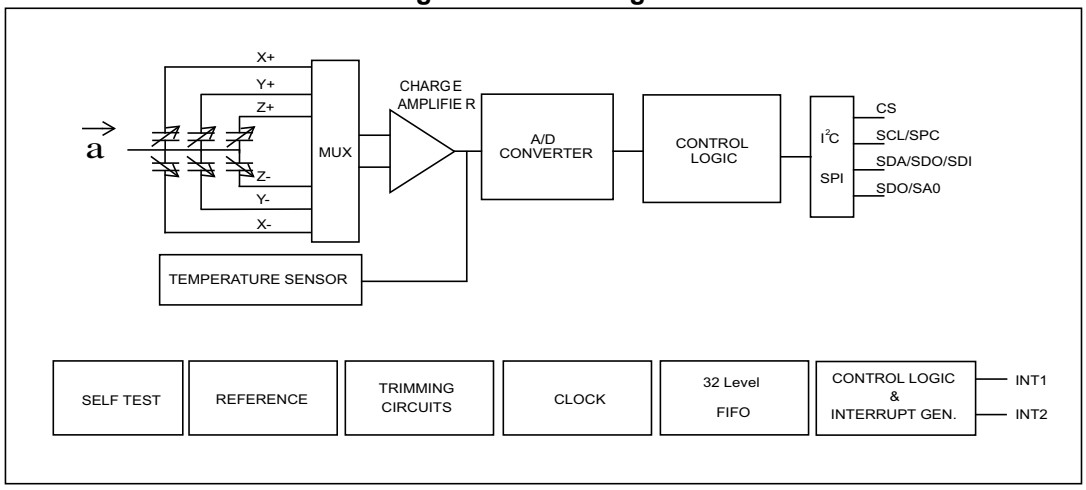
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

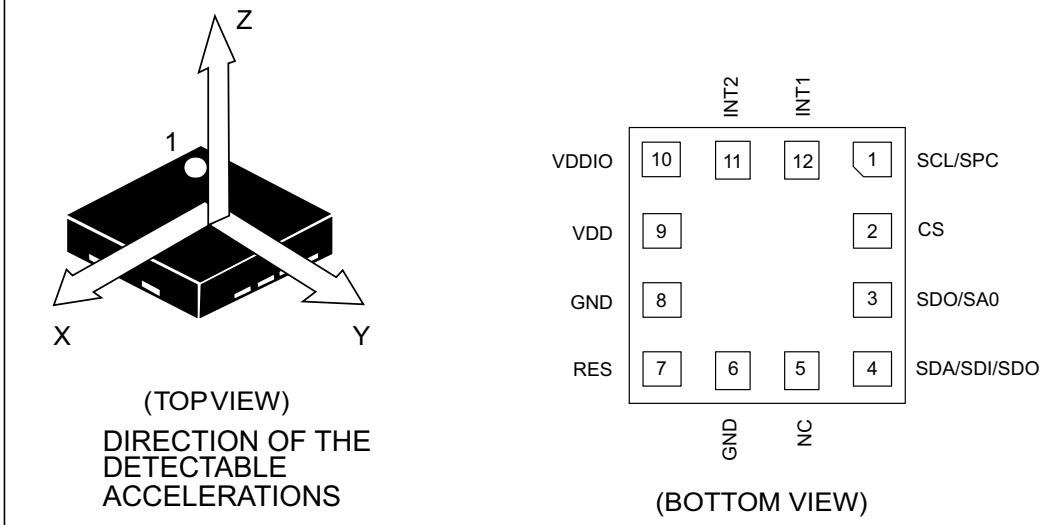


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2(1)	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3(1)	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	VDD	Power supply
10	VDD_IO	Power supply for I/O pins
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.
12	INT1	Interrupt pin 1

1. SDO/SA0 and CS pins are internally pulled up. Refer to *Table 3* for the internal pull-up values (typ).

Table 3. Internal pull-up values (typ.) for SDO/SA0 and CS pins

Vdd_IO	Resistor value for SDO/SA0 and CS pins
	Typ. (kΩ)
1.7 V	54.4
1.8 V	49.2
2.5 V	30.4
3.6 V	20.4

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Table 4. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.(2)	Typ.(3)	Max.(2)	Unit
FS	Measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Sensitivity(4)	@ FS ±2 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1	-3%	0.244	+3%	mg/digit
		@ FS ±4 *g* in High-Performance Mode and all Low-Power Modes except Low-Power Mode 1	-3%	0.488	+3%	
		@ FS ±8 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1	-3%	0.976	+3%	
		@ FS ±16 *g* in High-Performance Mode and all Low-Power modes except Low-Power Mode 1	-3%	1.952	+3%	
		@ FS ±2 *g* in Low-Power Mode 1	-3%	0.976	+3%	
		@ FS ±4 *g* in Low-Power Mode 1	-3%	1.952	+3%	
		@ FS ±8 *g* in Low-Power Mode 1	-3%	3.904	+3%	
		@ FS ±16 *g* in Low-Power Mode 1	-3%	7.808	+3%	
An	Noise density - High-performance Mode(5)	@ FS ±2 *g*		90	160	µg/√Hz
RMS	RMS noise - Low-Power Modes(6) @ FS ±2 *g*	Low-Power Mode 4		1.3	2.6	mg(RMS)
		Low-Power Mode 3		1.8	3.6	
		Low-Power Mode 2		2.4	4.8	
		Low-Power Mode 1		4.5	9	
TyOff	Zero-*g* level offset accuracy(7)		-30	±20	+30	mg
TCO	Zero-*g* offset change vs. temperature		-1	±0.2	+1	mg/°C

Table 4. Mechanical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.(2)	Typ.(3)	Max.(2)	Unit
f_0	Sensor resonant frequency	X		3.4		kHz
		Y		3.4		
		Z		2.8		
TCS	Sensitivity change vs. temperature			0.01		%/°C
ST	Self-test positive difference		70		1500	mg

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.
2. Minimum and maximum values are based on characterization data at 3σ and are not guaranteed.
3. Typical specifications are not guaranteed.
4. Sensitivity values after factory calibration test and trimming.
5. Noise density is the same for all ODRs. Low-noise setting enabled.
6. RMS noise is the same for all ODRs. Low-noise setting enabled.
7. Values after factory calibration test and trimming.

2.2 Electrical characteristics

Table 5. Electrical characteristics @ Vdd = 1.8 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.(2)	Typ.(3)	Max.(2)	Unit
Vdd	Supply voltage		1.62	1.8	3.6	V
Vdd_IO	I/O pins supply voltage(4)		1.62		Vdd+0.1	V
IddHR	Current consumption in High-Performance Mode(5)	@ ODR range 12.5 Hz - 1600 Hz, 14-bit		120	130	µA
IddLP	Current consumption in Low-Power Mode(6)	ODR 100 Hz		5	5.65	µA
		ODR 50 Hz		3	3.1	
		ODR 12.5 Hz		1	1.05	
		ODR 1.6 Hz		0.38	0.45	
Idd_PD	Current consumption in power-down			50	100	nA
V_{IH}	Digital high-level input voltage		0.8*Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.2*Vdd_IO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(7)	VDD_IO - 0.2 V			
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(7)			0.2 V	

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.
2. Minimum and maximum values are based on characterization data at 3σ and are not guaranteed.
3. Typical specifications are not guaranteed.
4. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
5. Low-noise setting enabled.
6. Low-Power Mode 1. Low-noise setting disabled.
7. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

2.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted

Table 6. Temperature sensor characteristics

Symbol	Parameter	Min.(1)	Typ.(2)	Max.(1)	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset(3)	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		1(4)		LSB/°C
			16(5)		
TODR	Temperature refresh rate in High-Performance Mode for all ODRs or in Low-Power Modes for ODRs equal to 200/100/50 Hz		50		Hz
	Temperature refresh rate in Low-Power Modes for ODR equal to 25 Hz		25		
	Temperature refresh rate in Low-Power Modes for ODR equal to 12.5 Hz		12.5		
	Temperature refresh rate in Low-Power Modes for ODR equal to 1.6 Hz		1.6		

1. Minimum and maximum values are based on characterization data at 3σ and are not guaranteed.
2. Typical specifications are not guaranteed.
3. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
4. 8-bit resolution.
5. 12-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

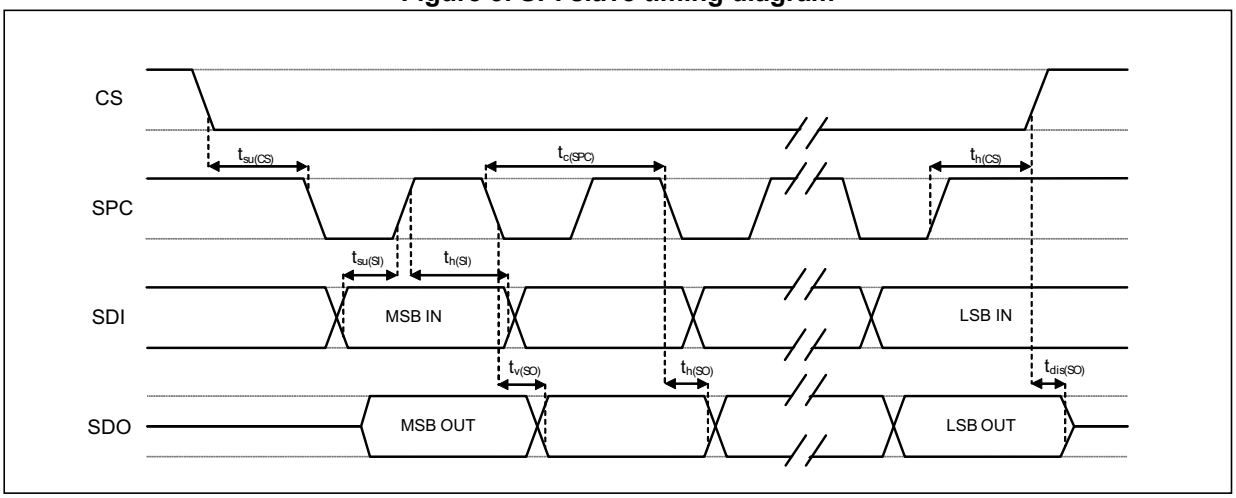
Subject to general operating conditions for Vdd and Top.

Table 7. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	12		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

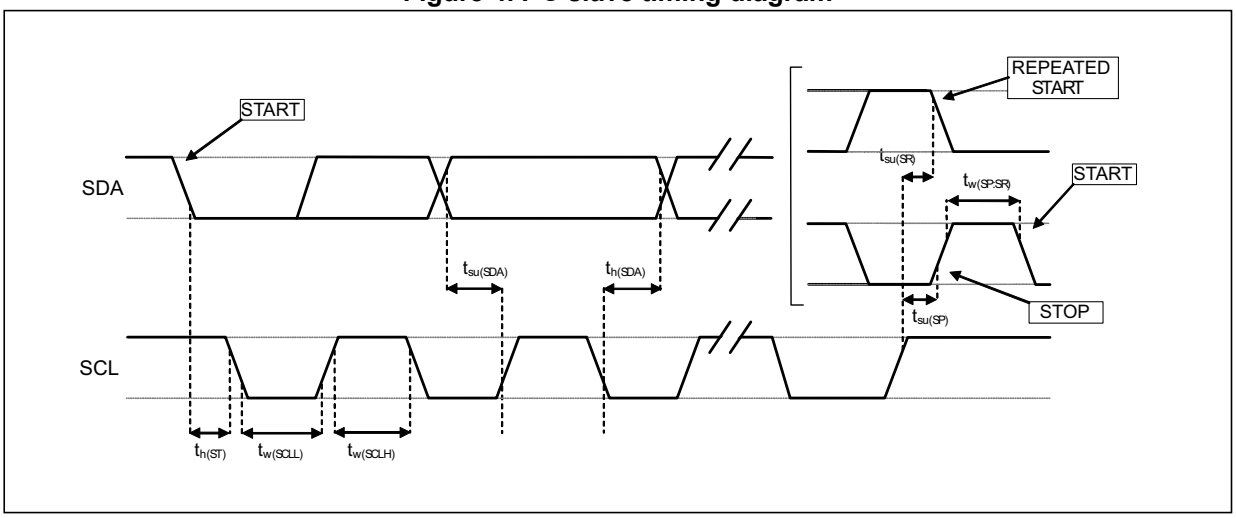
Subject to general operating conditions for Vdd and Top.

Table 8. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

Table 9. I^2C high-speed mode specifications at 1 MHz and 3.4 MHz

	Symbol	Parameter	Min	Max	Unit
Fast mode plus(1)	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*Vdd/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*Vdd/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1Vdd	-	V
	V_{nH}	Noise margin at high level	0.2Vdd	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns
High-speed mode(1)	f_{SCLH}	SCLH clock frequency	0	3.4	MHz
	$t_{SU;STA}$	Setup time for a repeated START condition	160	-	ns
	$t_{HD;STA}$	Hold time (repeated) START condition	160	-	
	t_{LOW}	Low period of the SCLH clock	160	-	
	t_{HIGH}	High period of the SCLH clock	60	-	
	$t_{SU;DAT}$	Data setup time	10	-	
	$t_{HD;DAT}$	Data hold time	0	70	
	t_{rCL}	Rise time of SCLH signal	10	40	
	t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	
	t_{fCL}	Fall time of SCLH signal	10	40	
	t_{rDA}	Rise time of SDAH signal	10	80	
	t_{fDA}	Fall time of SDAH signal	10	80	
	$t_{SU;STO}$	Setup time for STOP condition	160	-	
	C_b	Capacitive load for each bus line	-	100	pF
	V_{nH}	Noise margin at high level	0.2Vdd	-	V
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	10	ns

1. Data based on characterization, not tested in production

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 1.8 V)	3000 *g* for 0.5 ms	*g*
		10000 *g* for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	*g*
		10000 *g* for 0.2 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology and functionality

3.1 Terminology

3.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Zero-*g* level offset

Zero-*g* level offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from ideal value in this case is called Zero-*g* level offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level offset change vs. temperature".

3.2 Functionality

3.2.1 Operating modes

Two sets of operating modes have been designed to offer the customer a broad choice of noise/power consumption combinations:

- Low-noise disabled (see *Table 11*)
- Low-noise enabled (see *Table 12*)

Writing the LOW_NOISE bit in *CTRL6 (25h)* selects the operating mode (low-noise).

From each of these two sets, five operating modes have been designed:

- 1 High-Performance Mode: focus on low noise
- 4 Low-Power Modes: trade-off between noise and power consumption

These operating modes are selected by writing the MODE[1:0] and LP_MODE[1:0] bits in *CTRL1 (20h)*.

Table 11. Operating modes - low-noise setting disabled

Parameter		High Performance Mode	Low-Power Mode 4	Low-Power Mode 3	Low-Power Mode 2	Low-Power Mode 1
Resolution [bit]		14-bit	14-bit	14-bit	14-bit	12-bit
ODR [Hz]		12.5 - 1600	1.6 - 200	1.6 - 200	1.6 - 200	1.6 - 200
BW [Hz]		ODR/2 (N/A for 1600 Hz), ODR/4, ODR/10, ODR/20	180 ODR/4, ODR/10, ODR/20	360 ODR/4, ODR/10, ODR/20	720 ODR/4, ODR/10, ODR/20	3200 ODR/4, ODR/10, ODR/20
Typ. noise density [µg/√Hz](1) @ FS = ±2 *g*, ODR=200 Hz		110	-	-	-	-
Typ. RMS noise [mg(RMS)](1) @ FS = ±2 *g*		-	1.6	2.1	3	5.5
Typ. current consumption [µA] @ Vdd=1.8 V(1)	ODR=1.6 Hz	-	0.65	0.55	0.45	0.38
	ODR=12.5 Hz	90	4	2.5	1.6	1
	ODR=25 Hz	90	8.5	4.5	3	1.5
	ODR=50 Hz	90	16	9	5.5	3
	ODR=100 Hz	90	32	17.5	10.5	5
	ODR=200 Hz	90	63	34.5	20.5	10
	ODR=400,800, 1600 Hz	90	-	-	-	-

Table 11. Operating modes - low-noise setting disabled (continued)

Parameter		High Performance Mode	Low-Power Mode 4	Low-Power Mode 3	Low-Power Mode 2	Low-Power Mode 1
Typ. current consumption [µA] @ Vdd=3 V(1)	ODR=1.6 Hz	-	1.3	0.95	0.75	0.67
	ODR=12.5 Hz	110	5.3	3	2	1.3
	ODR=25 Hz	110	10.5	6	3.8	2.1
	ODR=50 Hz	110	20.5	11.5	7	3.7
	ODR=100 Hz	110	40	22	13.5	6.5
	ODR=200 Hz	110	80	44	26	12.5
	ODR=400,800, 1600 Hz	110	-	-	-	-

1. Verified at characterization level.

Table 12. Operating modes - low-noise setting enabled

Parameter		High Performance Mode	Low-Power Mode 4	Low-Power Mode 3	Low-Power Mode 2	Low-Power Mode 1
Resolution [bit]		14-bit	14-bit	14-bit	14-bit	12-bit
ODR [Hz]		12.5 - 1600	1.6 - 200	1.6 - 200	1.6 - 200	1.6 - 200
BW [Hz]		ODR/2 (N/A for 1600 Hz), ODR/4, ODR/10, ODR/20	180 ODR/4, ODR/10, ODR/20	360 ODR/4, ODR/10, ODR/20	720 ODR/4, ODR/10, ODR/20	3200 ODR/4, ODR/10, ODR/20
Typ. noise density [µg/√Hz](1) @ FS = ±2 *g*, ODR=200 Hz		90	-	-	-	-
Typ. RMS noise [mg(RMS)](1) @ FS = ±2 *g*		-	1.3	1.8	2.4	4.5
Typ. current consumption [µA] @ Vdd=1.8 V(1)	ODR=1.6 Hz	-	0.7	0.6	0.5	0.4
	ODR=12.5 Hz	120	5	3	2	1.1
	ODR=25 Hz	120	10	6	3.5	2
	ODR=50 Hz	120	20	11	7	3.5
	ODR=100 Hz	120	39	21.5	13	6
	ODR=200 Hz	120	77	42	25	12
	ODR=400,800, 1600 Hz	120	-	-	-	-
Typ. current consumption [µA] @ Vdd=3 V(1)	ODR=1.6 Hz	-	1.35	1	0.8	0.7
	ODR=12.5 Hz	140	7	4	2.5	1.5
	ODR=25 Hz	140	12.5	7	4.5	2.5
	ODR=50 Hz	140	24.5	14	8.5	4.5
	ODR=100 Hz	140	48.5	26.5	16	8
	ODR=200 Hz	140	95.5	52.5	31	14.5
	ODR=400,800, 1600 Hz	140	-	-	-	-

1. Verified at characterization level.

3.2.2 Single data conversion on demand mode

The device features a single data conversion on demand mode which is valid for both sets of operating modes (low-noise disabled or enabled) in the 4 low-power modes. This mode is enabled by writing the MODE[1:0] bits to '10' in *CTRL1 (20h)*. Low power modes are selected by writing the LP_MODE[1:0] bits in *CTRL1 (20h)*.

The trigger for output data generation can be managed through the I^2C/SPI or by applying a clock signal on the INT2 pin acting here as an input by writing the SLP_MODE_ SEL bit in *CTRL3 (22h)*:

- When SLP_MODE_SEL = '0', output data generation is triggered by the clock signal on the INT2 pin (see *Figure 5*).
- When SLP_MODE_SEL = '1', output data generation starts when the SLP_MODE_1 bit is set to '1' logic through the I^2C/SPI. When XL data are available in the registers, this bit is automatically set to '0' and the device is ready for another triggered session.

Output data are generated according to the selected low-power mode.

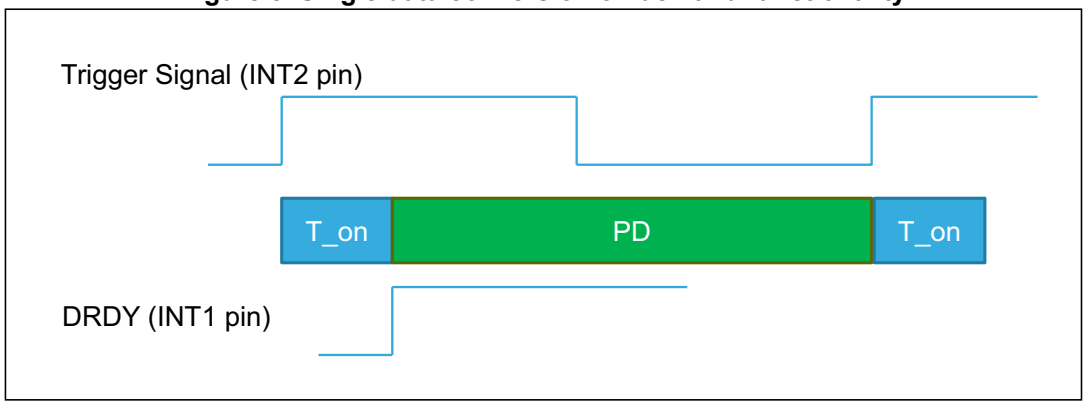
When output data is saved in an output register or FIFO, the device goes to power-down mode and waits for a new trigger.

All ODRs in the range from 0 to up to 200 Hz are supported due to the INT2 clock input.

A DRDY signal or FIFO flags are available on the INT1 pin.

Power consumption is the same as that of standard low-power modes for the same ODR.

Figure 5. Single data conversion on demand functionality



At the end of turn-on time T_on, the DRDY interrupt is activated, output data are available to be read and the device goes into power-down. T_on values depend on the low-power mode as follows:

T_on (typ.) =

- 1.20 ms for Low-Power Mode 1
- 1.70 ms for Low-Power Mode 2
- 2.30 ms for Low-Power Mode 3
- 3.55 ms for Low-Power Mode 4

3.2.3 Self-test

The self-test allows checking the sensor functionality without moving it. The self-test function is off when the self-test bits (ST) are programmed to ‘00’. When the self-test bits are changed, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 4*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

3.2.4 Activity/Inactivity, stationary/motion-detection functions

The activity/inactivity function recognizes the device’s sleep state and allows reducing system power consumption.

When the activity/inactivity function is activated by setting the INTERRUPTS_ENABLE bit in *CTRL7 (3Fh)* and the SLEEP_ON bit in *WAKE_UP_THS (34h)*, the IIS2DLPC automatically goes to 12.5 Hz ODR in the low-power mode previously selected by the LP_MODE[1:0] bits in *CTRL1 (20h)* if the sleep state condition is detected and wakes up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The stationary/motion-detection function only recognizes the device’s sleep state.

When the stationary/motion-detection function is activated by setting the STATIONARY bit in *WAKE_UP_DUR (35h)*, the IIS2DLPC detects acceleration below a fixed threshold but does not change either ODR or operating mode (High-Performance mode or Low-Power mode) after sleep state detection.

The Activity/Inactivity recognition function can use the high-pass filter or the offset outputs, this choice can be made through the USR_OFF_ON_OUT bit in *CTRL7 (3Fh)*.

If the device is in sleep (inactivity/stationary) mode, when at least one of the axes exceeds the threshold in *WAKE_UP_THS (34h)*, the device goes into a sleep-to-wake state (as wake-up).

For the activity/inactivity function, the device, in a wake-up state, will return to the operating mode (HP or LP) and ODR before sleep state detection.

Activity/Inactivity, stationary/motion-detection threshold and duration can be configured in the following control registers:

WAKE_UP_THS (34h)

WAKE_UP_DUR (35h)

3.2.5 High tap/double-tap user configurability

The device embeds the possibility to select the following parameters:

- single axis or multiple axes in *TAP_THS_Z (32h)*
- axis priority in *TAP_THS_Y (31h)*
- threshold value of each axis in *TAP_THS_X (30h)*, *TAP_THS_Y (31h)*, and *TAP_THS_Z (32h)*
- max time threshold between 2 consecutive taps for double-tap recognition, min time threshold between 2 consecutive taps to detect a new tap event in *INT_DUR (33h)*

3.2.6 Offset management

The user can manage offset in the output or for wakeup detection using dedicated embedded hardware (see *Section 5.1: Block diagram of filters*).

3.3 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. In order to be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

3.4 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The IIS2DLPC features a data-ready signal which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

3.5 Factory calibration

The IC interface is factory-calibrated for sensitivity (So) and Zero-*g* level offset.

The trim values are stored inside the device in nonvolatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration. If an accidental write occurs in the registers where trimming parameters are stored, the BOOT bit in *CTRL2 (21h)* can help to retrieve the correct trimming parameters from nonvolatile memory without the need to switch on/off the device. This bit is automatically reset at the end of the download operation. Setting this bit has no impact on the control registers.

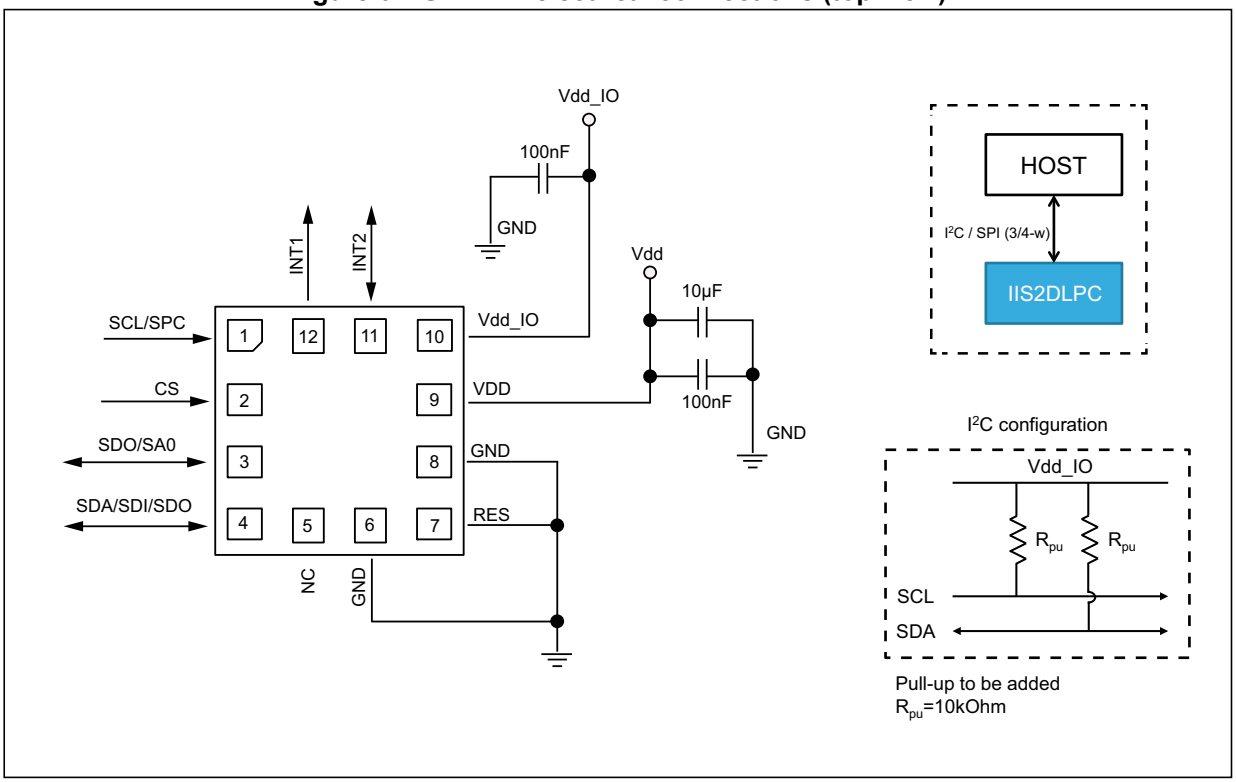
3.6 Temperature sensor

The temperature is available in *OUT_T_L (0Dh)*, *OUT_T_H (0Eh)* stored as two's complement data, left-justified in 12-bit mode and in *OUT_T (26h)* stored as two's complement data, left-justified in 8-bit mode.

Refer to *Table 6: Temperature sensor characteristics* for the conversion factor.

4 Application hints

Figure 6. IIS2DLPC electrical connections (top view)



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 6*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

Table 13. Internal pin status

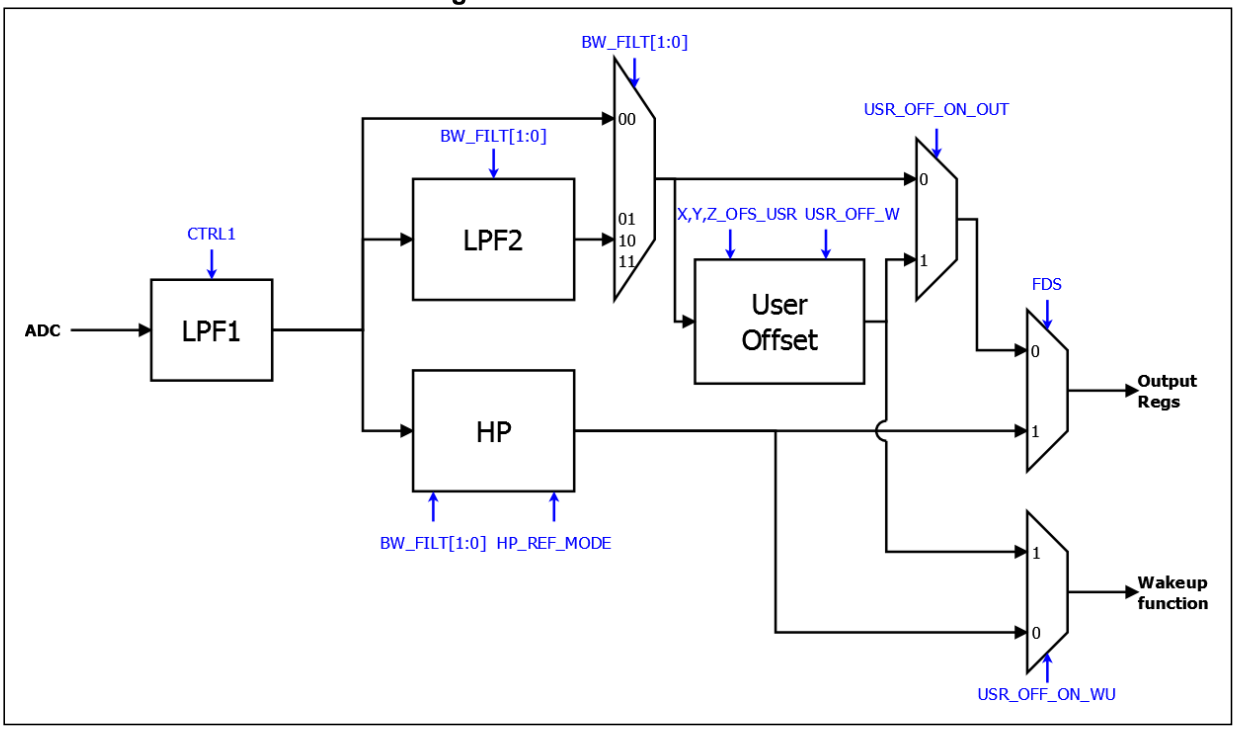
Pin #	Name	Function	Pin status
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)	Default: open drain
2	CS	SPI enable I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled	Default: input with internal pull-up(1)
3	SDO SA0	Serial data output (SDO) I^2C less significant bit of the device address (SA0)	Default: input with internal pull-up
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input open drain
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.	
6	GND	0 V supply	
7	RES	Connect to GND	
8	GND	0 V supply	
9	VDD	Power supply	
10	VDD_IO	Power supply for I/O pins	
11	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.	Default: push-pull output forced to Gnd
12	INT1	Interrupt pin 1	Default: push-pull output forced to Gnd

1. In order to disable the internal pull-up on the CS pin, write '1' to the CS_PU_DISC bit in *CTRL2 (21h)*.

5 Digital main blocks

5.1 Block diagram of filters

Figure 7. Accelerometer chain



Referring to *Figure 7*, the first block is the Low-Pass Filter 1 (LPF1) whose behavior is a function of the actual ODR and mode selected in *CTRL1 (20h)*. The signal is then downsampled and can be either directly sent to the output registers or to the Low-Pass Filter 2 (LPF2) or High-Pass-Filter (HP) using the BW_FILT[1:0] bits and FDS bit in *CTRL6 (25h)*.

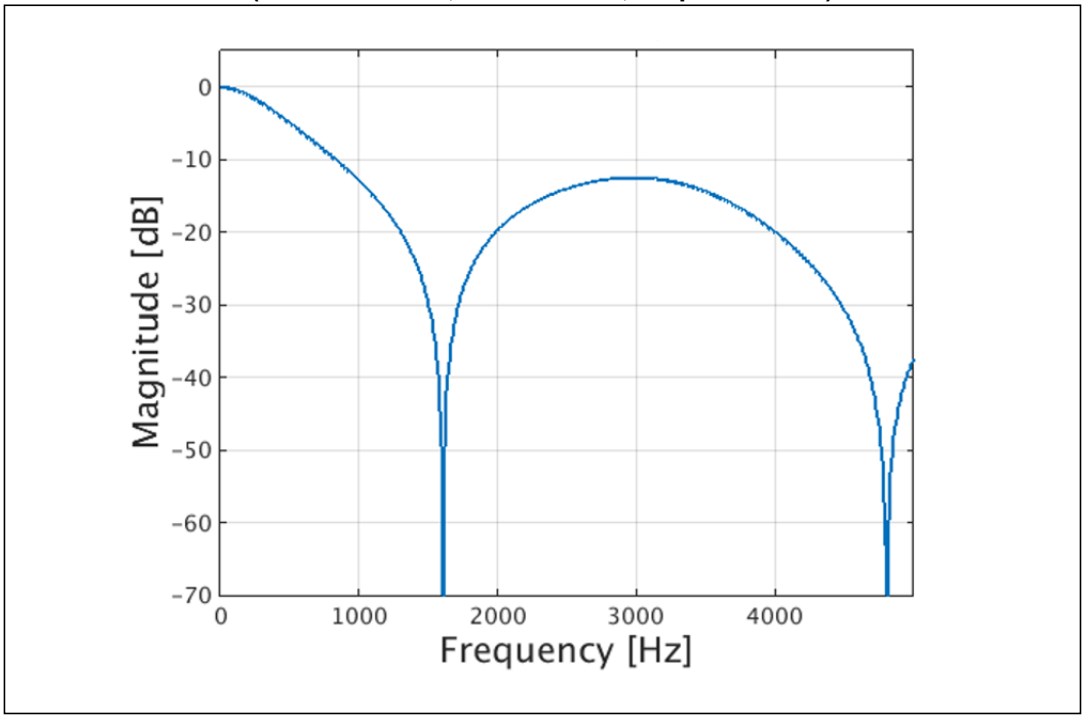
In the low-pass path, it is possible to apply a user offset determined by the *X_OFS_USR (3Ch)*, *Y_OFS_USR (3Dh)*, *Z_OFS_USR (3Eh)* register values and the USR_OFF_W bit in *CTRL7 (3Fh)* and send the result to the output using the USR_OFF_ON_OUT bit in *CTRL7 (3Fh)*.

In the high-pass path, it is possible to use the high-pass filter reference mode (HP) using the HP_REF_MODE bit in *CTRL7 (3Fh)*.

5.2 Frequency response

The following figures indicate the frequency response[a] of the sensor in various configurations.

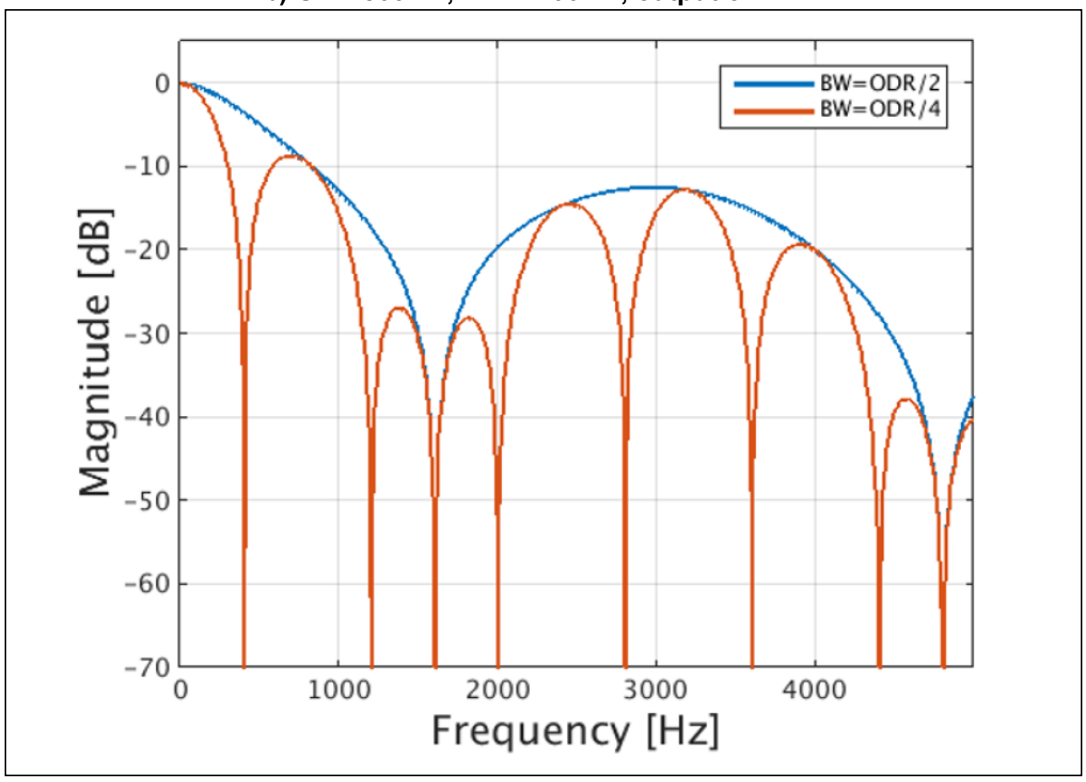
Figure 8. Frequency response - high-performance mode (ODR = 1600 Hz, BW = 400 Hz, output of LPF1)



1. ODR 1600 Hz, BW = 400 Hz,
Output of LPF1 (CTRL1.ODR = 1001; CTRL1.MODE = 01; CTRL6.BW_FILT = 00)

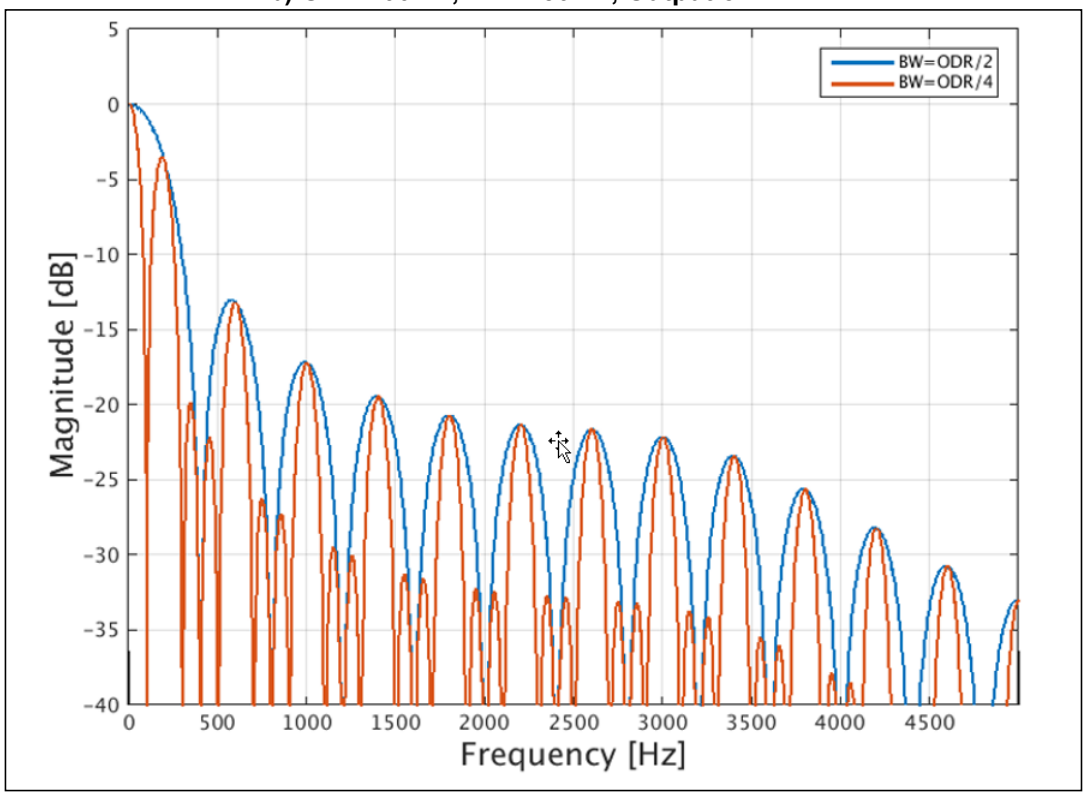
a. The frequency response is determined by CAD simulation.

Figure 9. Frequency response - high-performance mode
a) ODR 800 Hz, BW = 400 Hz, output of LPF1
b) ODR 800 Hz, BW = 200 Hz, output of LPF2



1. ODR 800 Hz, BW = 400 Hz,
   Output of LPF1 (CTRL1.ODR = 1000; CTRL1.MODE = 01; CTRL6.BW_FILT = 00)
2. ODR 800 Hz, BW = 200 Hz,
   Output of LPF2 (CTRL1.ODR = 1000; CTRL1.MODE = 01; CTRL6.BW_FILT = 01)

Figure 10. Frequency response - low-power mode 4 (LPM4)
a) ODR 200 Hz, BW = 180 Hz, Output of LPF1
b) ODR 200 Hz, BW = 50 Hz, Output of LPF2



1. ODR 200 Hz, BW = 180 Hz,
   Output of LPF1 (CTRL1.ODR = 0110; CTRL1.MODE = 00; CTRL1.MODE = 11; CTRL6.BW_FILT = 00)
2. ODR 200Hz, BW = 50 Hz,
   Output of LPF2 (CTRL1.ODR = 0110 ; CTRL1.MODE = 00; CTRL1.MODE = 11; CTRL6.BW_FILT = 01)

5.3 Data stabilization time vs. ODR/device setting

Some data samples need to be discarded when changing the ODR in HP mode with ODR/2 bandwidth selection.

The table below provides the number of samples to be discarded in order to obtain valid usable data.

Table 14. Number of samples to be discarded

MODE[1:0] in *CTRL1 (20h)*	ODR [Hz]	BW_FILT[1:0] in *CTRL6 (25h)*	Samples to be discarded
00	-	00	0
01	12.5		0
	25		0
	50		0
	100		1
	200		1
	400		1
	800		1
	1600		2

5.4 FIFO

The IIS2DLPC embeds 32 slots of 14-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration data. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The internal FIFO allows collecting 32 samples (14-bit size data) for each axis.

When the FIFO mode is other than Bypass, reading the output registers (28h to 2Dh) returns the oldest FIFO sample set. In order to minimize communication between the master and slave, the address read may be automatically incremented by the device by setting the IF_ADD_INC bit of *CTRL2 (21h)* to '1'; the device rolls back to 0x28 when register 0x2D is reached.

This buffer can work according to the following 5 different modes:

- Bypass mode
- FIFO mode
- Continuous-to-FIFO
- Bypass-to-Continuous
- Continuous

Each mode is selected by the FMode[2:0] bits in the *FIFO_CTRL (2Eh)* register.

Programmable FIFO threshold is selected in *FIFO_CTRL (2Eh)*. Status and FIFO overrun events are available in the *FIFO_SAMPLES (2Fh)* register and can be used to generate dedicated interrupts on the INT1 and INT2 pins using the *CTRL4_INT1_PAD_CTRL (23h)* and *CTRL5_INT2_PAD_CTRL (24h)* registers.

FIFO_SAMPLES (2Fh) (FIFO_FTH) goes to '1' when the number of unread samples *FIFO_SAMPLES (2Fh)* (Diff[5:0]) is greater than or equal to FTH[4:0] in *FIFO_CTRL (2Eh)*.

If FTH[4:0] is equal to '0', *FIFO_SAMPLES (2Fh)* (FIFO_FTH) goes to '0'.

FIFO_SAMPLES (2Fh) (FIFO_OVR) is equal to '1' if a FIFO slot is overwritten.

FIFO_SAMPLES (2Fh) (Diff[5:0]) contains stored data levels of unread samples. When Diff[5:0] is equal to ‘000000’, FIFO is empty. When Diff[5:0] is equal to ‘100000’, FIFO is full and the unread samples are 32.

To guarantee the correct acquisition of data during the switching into and out of FIFO, the first sample acquired must be discarded.

When the FIFO threshold status flag is '0'-logic, FIFO filling is lower than the threshold level and when '1'-logic, FIFO filling is equal to or higher than the threshold level.

5.4.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)* (FMode [2:0])= 000), the FIFO is not operational, no data is collected in FIFO memory, and it remains empty with the only actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

For each channel only the first address is used. When new data is available, the old data is overwritten.

5.4.2 FIFO mode

In FIFO mode (*FIFO_CTRL (2Eh)*(FMode [2:0])= 001) data from the X, Y and Z channels are stored in the FIFO until it is full, when 32 unread samples are stored in memory, data collecting is stopped.

To reset the FIFO content, Bypass mode should be written in the *FIFO_CTRL (2Eh)* register, setting the FMODE [2:0] bits to '000'. After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL (2Eh)*(FMODE [2:0]).

The FIFO buffer can memorize 32 slots of X, Y and Z data.

5.4.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)* (FMode[2:0] = 110) provides a continuous FIFO update: when 32 unread samples are stored in memory, as new data arrives the oldest data is discarded and overwritten by the newer.

A FIFO threshold flag *FIFO_SAMPLES (2Fh)* (FIFO_FTH) is asserted when the number of unread samples in FIFO is greater than or equal to (*FIFO_CTRL (2Eh)*FTH[4:0]).

It is possible to route *FIFO_SAMPLES (2Fh)*(FTH) to the INT1 pin by writing the INT1_FTH bit to '1' in register *CTRL4_INT1_PAD_CTRL (23h)* or to the INT2 pin by writing the INT2_FTH bit to '1' in register *CTRL5_INT2_PAD_CTRL (24h)*.

If an overrun occurs, the oldest sample in FIFO is overwritten and the FIFO_OVR flag in *FIFO_SAMPLES (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SAMPLES (2Fh)* (Diff[5:0]).

5.4.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode *FIFO_CTRL (2Eh)*(FMode[2:0] = 011), FIFO operates in Continuous mode and FIFO mode starts upon an internal trigger event. When the FIFO is full, data collecting is stopped. The trigger could be a single or double tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed on the corresponding pad to be used as a trigger.

Figure 11. Continuous-to-FIFO mode

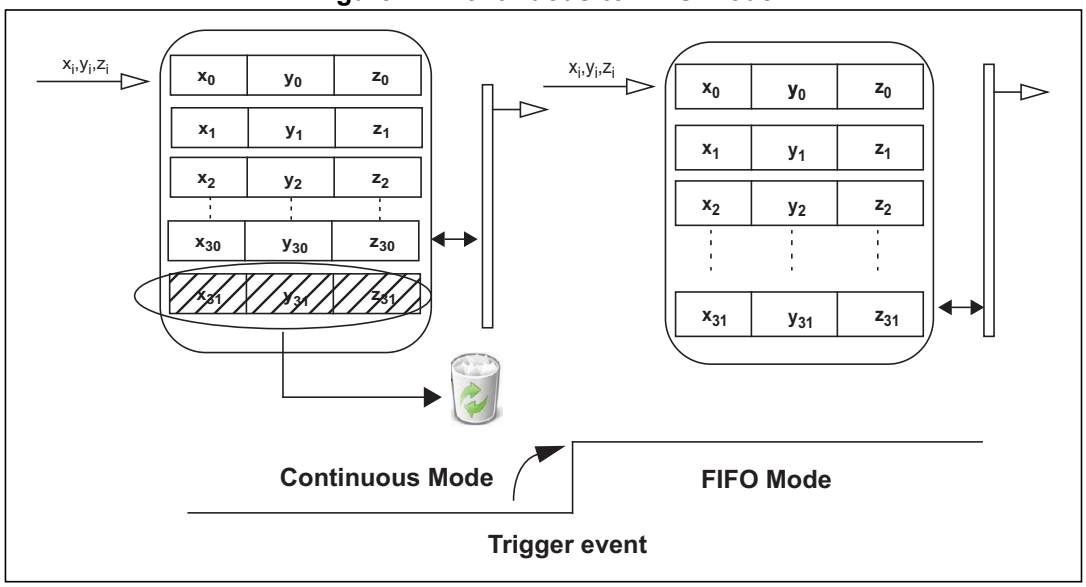
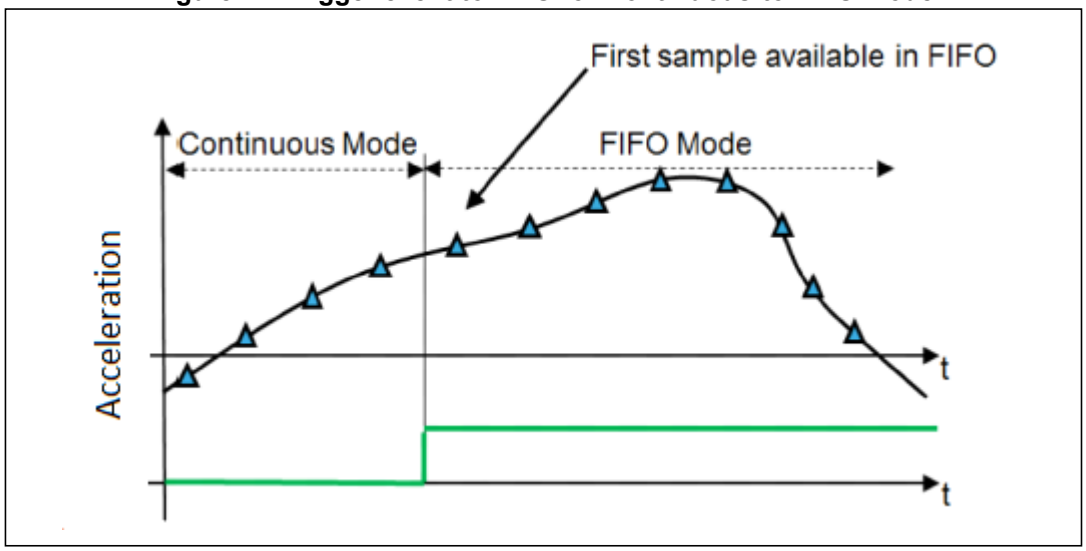


Figure 12. Trigger event to FIFO for Continuous-to-FIFO mode



5.4.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMode[2:0] = '100'), data measurement storage inside FIFO starts in Continuous mode upon an internal trigger event, then the sample that follows the trigger is available in FIFO. The trigger could be a single or double tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed on the corresponding pad to be used as a trigger.

Figure 13. Bypass-to-Continuous mode

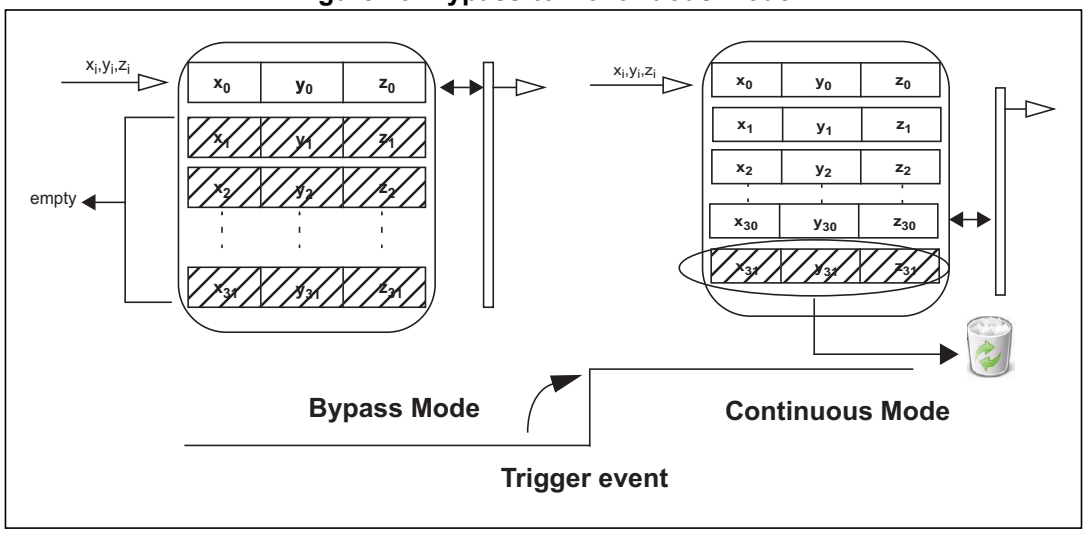
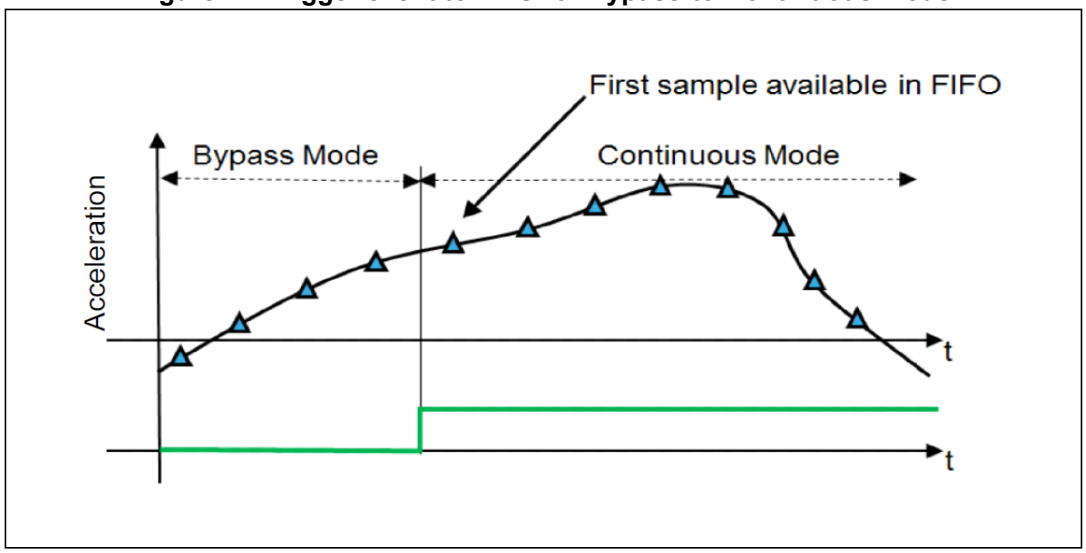


Figure 14. Trigger event to FIFO for Bypass-to-Continuous mode



6 Digital interfaces

The registers embedded inside the IIS2DLPC may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 15. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C address selection (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The IIS2DLPC I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 16. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

In order to disable the I^2C block, *CTRL2 (21h)* (I2C_DISABLE) = 1 must be set.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the IIS2DLPC is 001100xb where the x bit is modified by the SA0/SDO pin in order to modify the device address. If the SA0/SDO pin is connected to the supply voltage, the address is 0011001b, otherwise if the SA0/SDO pin is connected to ground, the address is 0011000b. This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the IIS2DLPC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represents the actual register address while the *CTRL2 (21h)* (IF_ADD_INC) bit defines the address increment.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 17* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 17. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Table 18. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 19. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 20. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 21. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

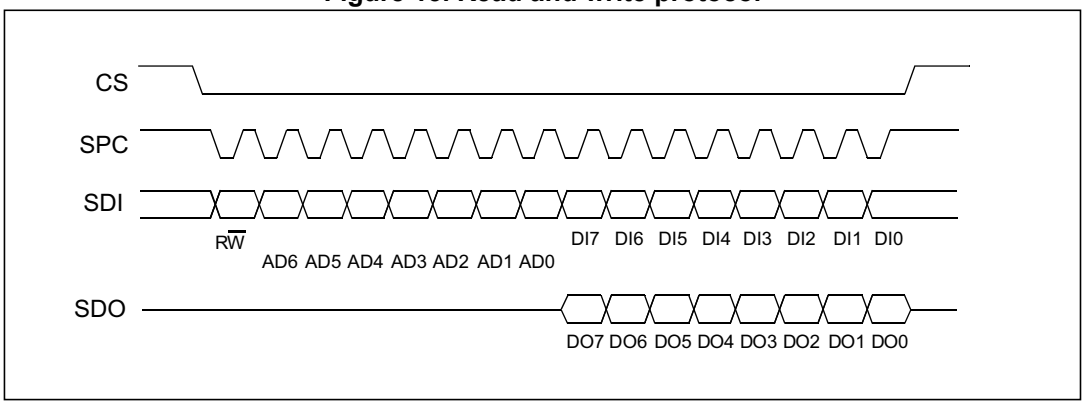
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

6.2 SPI bus interface

The IIS2DLPC SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 15. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

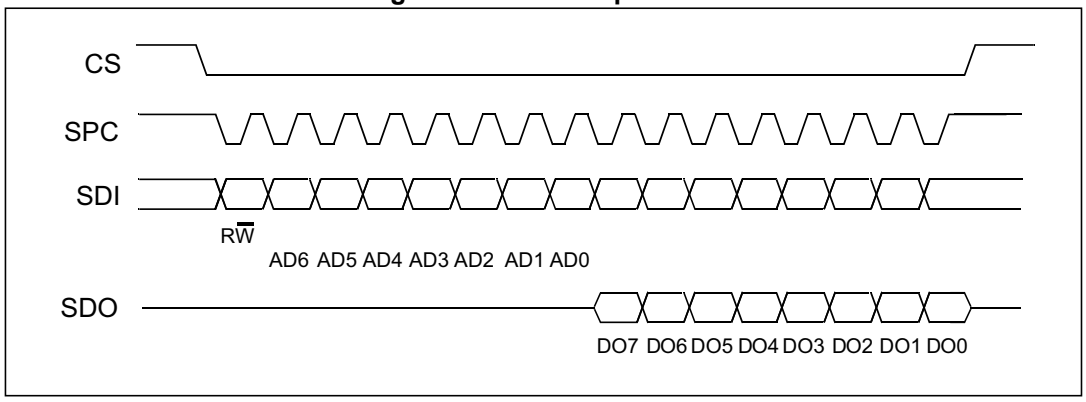
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods will be added. When the *CTRL2 (21h)* (IF_ADD_INC) bit is ‘0’, the address used to read/write data remains the same for every block. When the *CTRL2 (21h)* (IF_ADD_INC) bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 16. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

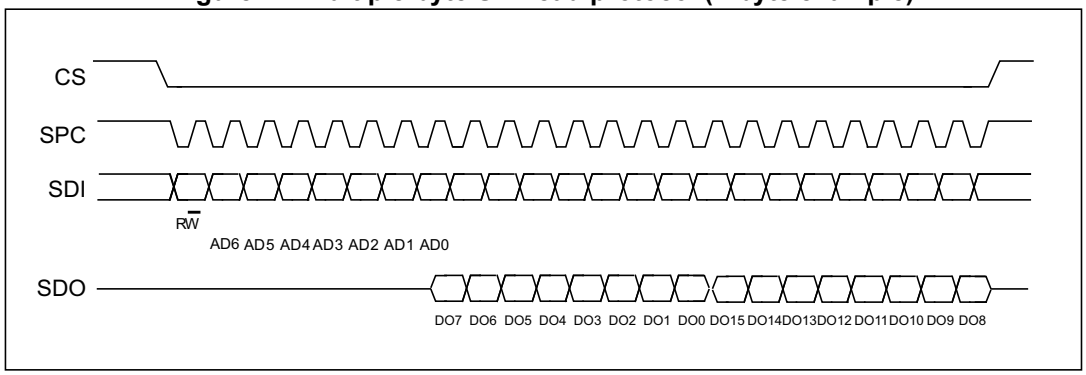
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

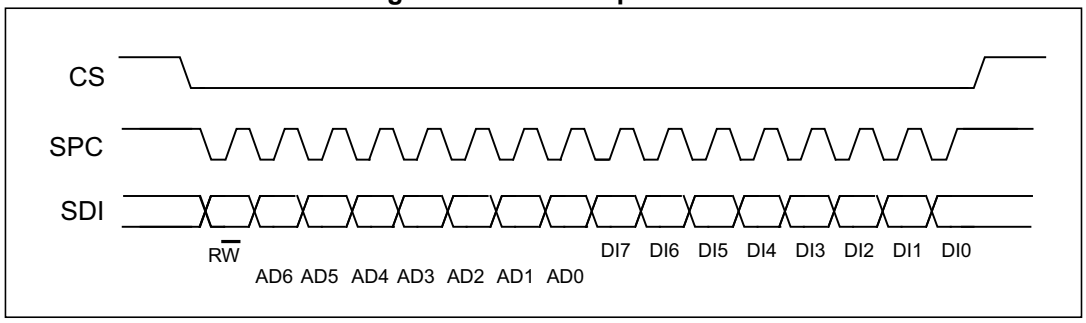
bit 16-... : data DO(...-8). Additional data in multiple byte reads.

Figure 17. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 18. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

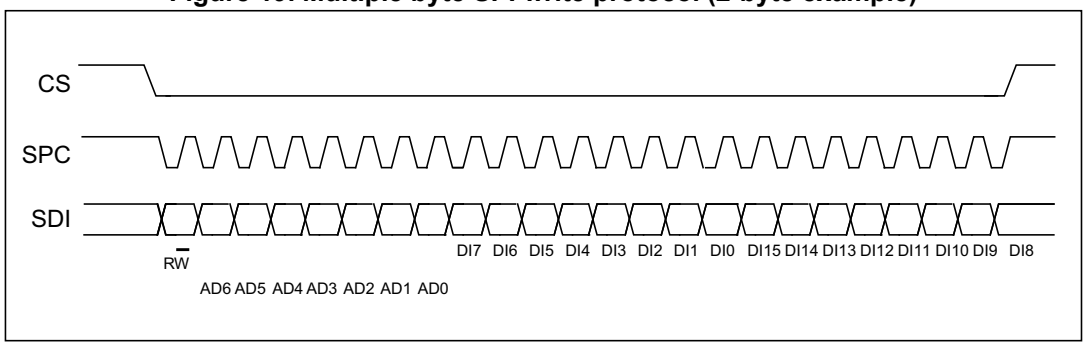
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Additional data in multiple byte writes.

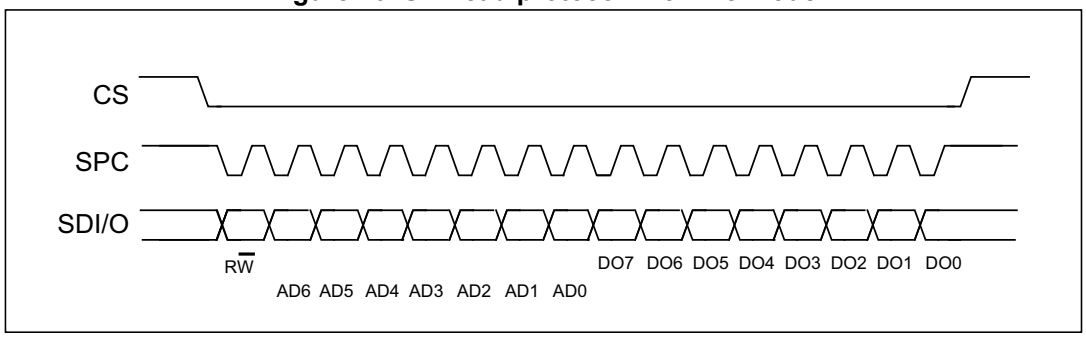
Figure 19. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL2 (21h)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 20. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

Table 22. Register map

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
OUT_T_L	R	0D	00001101	00000000	Temp sensor output
OUT_T_H	R	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01000100	Who am I ID
RESERVED	-	10-1F		-	RESERVED
CTRL1	R/W	20	00100000	00000000	Control registers
CTRL2	R/W	21	00100001	00000100	
CTRL3	R/W	22	00100010	00000000	
CTRL4_INT1_PAD_CTRL	R/W	23	00100011	00000000	
CTRL5_INT2_PAD_CTRL	R/W	24	00100100	00000000	
CTRL6	R/W	25	00100101	00000000	
OUT_T	R	26	00100110	00000000	Temp sensor output
STATUS	R	27	00100111	00000000	Status data register
OUT_X_L	R	28	00101000	00000000	Output registers
OUT_X_H	R	29	00101001	00000000	
OUT_Y_L	R	2A	00101010	00000000	
OUT_Y_H	R	2B	00101011	00000000	
OUT_Z_L	R	2C	00101100	00000000	
OUT_Z_H	R	2D	00101101	00000000	
FIFO_CTRL	R/W	2E	00101110	00000000	FIFO control register
FIFO_SAMPLES	R	2F	00101111	00000000	Unread samples stored in FIFO
TAP_THS_X	R/W	30	00110000	00000000	Tap thresholds
TAP_THS_Y	R/W	31	00110001	00000000	
TAP_THS_Z	R/W	32	00110010	00000000	
INT_DUR	R/W	33	00110011	00000000	Interrupt duration
WAKE_UP_THS	R/W	34	00110100	00000000	Tap/double-tap selection, inactivity enable, wakeup threshold
WAKE_UP_DUR	R/W	35	00110101	00000000	Wakeup duration

Table 22. Register map (continued)

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
FREE_FALL	R/W	36	00110110	00000000	Free-fall configuration
STATUS_DUP	R	37	00110111	00000000	Status register
WAKE_UP_SRC	R	38	00111000	00000000	Wakeup source
TAP_SRC	R	39	00111001	00000000	Tap source
SIXD_SRC	R	3A	00111010	00000000	6D source
ALL_INT_SRC	R	3B	00111011	00000000	
X_OFS_USR	R/W	3C	00111100	00000000	
Y_OFS_USR	R/W	3D	00111110	00000000	
Z_OFS_USR	R/W	3E	00000100	00000000	
CTRL7	R/W	3F	00000100	00000000	

1. R = read-only register, R/W = readable/writable register

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 OUT_T_L (0Dh)

Temperature output register in 12-bit resolution (r).

Table 23. OUT_T_L register

TEMP3	TEMP2	TEMP1	TEMP0	0	0	0	0

Table 24. OUT_T_L register description

TEMP[3:0]	The 8 least significant bits of the temperature sensor output. Sensitivity = 16 LSB/°C. Together with *OUT_T_H (0Eh)*, it forms the output value expressed as a 16-bit word in 2's complement.

8.2 OUT_T_H (0Eh)

Temperature output register in 12-bit resolution (r).

Table 25. OUT_T_H register

TEMP11	TEMP10	TEMP9	TEMP8	TEMP7	TEMP6	TEMP5	TEMP4

Table 26. OUT_T_H register description

TEMP[11:4]	The 8 most significant bits of the temperature sensor output. Sensitivity = 16 LSB/°C. Together with *OUT_T_L (0Dh)*, it forms the output value expressed as a 16-bit word in 2's complement

8.3 WHO_AM_I (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 44h.

Table 27. WHO_AM_I register default values

0	1	0	0	0	1	0	0

8.4 CTRL1 (20h)

Control register 1 (r/w)

Table 28. Control register 1

ODR3	ODR2	ODR1	ODR0	MODE1	MODE0	LP_MODE1	LP_MODE0

Table 29. Control register 1 description

ODR[3:0]	Output data rate and mode selection (see *Table 30*)
MODE[1:0]	Mode selection (see *Table 31*)
LP_MODE[1:0]	Low-power mode selection (see *Table 32*)

ODR[3:0] is used to set the power mode and ODR selection. The following table lists the bit settings for power-down mode and each available frequency.

Table 30. Data rate configuration

ODR[3:0]	Power mode / data rate configuration
0000	Power-down
0001	High-Performance / Low-Power mode 12.5/1.6 Hz
0010	High-Performance / Low-Power mode 12.5 Hz
0011	High-Performance / Low-Power mode 25 Hz
0100	High-Performance / Low-Power mode 50 Hz
0101	High-Performance / Low-Power mode 100 Hz
0110	High-Performance / Low-Power mode 200 Hz
0111	High-Performance / Low-Power mode 400/200 Hz
1000	High-Performance / Low-Power mode 800/200 Hz
1001	High-Performance / Low-Power mode 1600/200 Hz

Table 31. Mode selection

MODE[1:0]	Mode and resolution
00	Low-Power Mode (12/14-bit resolution)
01	High-Performance Mode (14-bit resolution)
10	Single data conversion on demand mode (12/14-bit resolution)
11	-

Table 32. Low-power mode selection

LP_MODE[1:0]	Power mode and resolution
00	Low-Power Mode 1 (12-bit resolution)
01	Low-Power Mode 2 (14-bit resolution)
10	Low-Power Mode 3 (14-bit resolution)
11	Low-Power Mode 4 (14-bit resolution)

8.5 CTRL2 (21h)

Control register 2 (r/w)

Table 33. Control register 2

BOOT	SOFT_ RESET	0(1)	CS_PU_ DISC	BDU	IF_ADD_ INC	I2C_ DISABLE	SIM

1. This bit must be set to '0' for the correct operation of the device.

Table 34. Control register 2 description

BOOT	Boot enables retrieving the correct trimming parameters from nonvolatile memory into registers where trimming parameters are stored. Once the operation is over, this bit automatically returns to 0. Default value: 0 (0: disabled; 1: enabled)
SOFT_RESET	Soft reset acts as reset for all control registers, then goes to 0. Default value: 0 (0: disabled; 1: enabled)
CS_PU_DISC	Disconnect CS pull-up. Default value: 0 (0: pull-up connected to CS pin; 1: pull-up disconnected to CS pin)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)
IF_ADD_INC	Register address automatically incremented during multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
I2C_DISABLE	Disable I^2C communication protocol. Default value: 0 (0: SPI and I^2C interfaces enabled; 1: I^2C mode disabled)
SIM	SPI serial interface mode selection. Default value: 0 0: 4-wire interface; 1: 3-wire interface

The BDU bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = '0') the output register values are updated continuously. When the BDU is activated (BDU = '1'), the content of the output registers is not updated until both MSB and LSB are read which avoids reading values related to different sample times.

8.6 CTRL3 (22h)

Control register 3 (r/w)

Table 35. Control register 3

ST2	ST1	PP_OD	LIR	H_LACTIVE	0	SLP_ MODE_SEL	SLP_ MODE_1

Table 36. Control register 3 description

ST[2:1]	Self-test enable. Default value: 00 (00: Self-test disabled; Other: see *Table 37*)
PP_OD	Push-pull/open-drain selection on interrupt pad. Default value: 0 (0: push-pull; 1: open-drain)
LIR	Latched Interrupt. Switches between latched ('1'-logic) and pulsed ('0'-logic) mode for function source signals and interrupts routed to pins (wakeup, single/double-tap). Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
H_LACTIVE	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
SLP_ MODE_SEL	Single data conversion on demand mode selection: 0: enabled with external trigger on INT2; 1: enabled by I^2C/SPI writing SLP_MODE_1 to 1.
SLP_ MODE_1	Single data conversion on demand mode enable. When SLP_MODE_SEL = '1' and this bit is set to '1' logic, single data conversion on demand mode starts. When XL data are available in the registers, this bit is set to '0' automatically and the device is ready for another triggered session.

Table 37. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	-

8.7 CTRL4_INT1_PAD_CTRL (23h)

Control register 4 (r/w)

Table 38. Control register 4

INT1_6D	INT1_ SINGLE _TAP	INT1_WU	INT1_FF	INT1_TAP	INT1_ DIFF5	INT1_ FTH	INT1_ DRDY

Table 39. Control register 4description

INT1_6D	6D recognition is routed to INT1 pad. Default: 0 (0: disabled; 1: enabled)
INT1_SINGLE_TAP	Single-tap recognition is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_WU	Wakeup recognition is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FF	Free-fall recognition is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_TAP	Double-tap recognition is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DIFF5	FIFO full recognition is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY	Data-Ready is routed to INT1 pad. Default value: 0 (0: disabled; 1: enabled)

8.8 CTRL5_INT2_PAD_CTRL (24h)

Control register 5 (r/w)

Table 40. Control register 5

INT2_ SLEEP_ STATE	INT2_ SLEEP_ CHG	INT2_ BOOT	INT2_ DRDY_T	INT2_ OVR	INT2_ DIFF5	INT2_ FTH	INT2_ DRDY

Table 41. Control register 5 description

INT2_SLEEP_STATE	Enable routing of SLEEP_STATE on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_SLEEP_CHG	Sleep change status routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _BOOT	Boot state routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_T	Temperature data-ready is routed to INT2. Default value: 0 (0: disabled; 1: enabled)
INT2 _OVR	FIFO overrun interrupt is routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DIFF5	FIFO full recognition is routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _FTH	FIFO threshold interrupt is routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _DRDY	Data-ready is routed to INT2 pad. Default value: 0 (0: disabled; 1: enabled)

8.9 CTRL6 (25h)

Control register 6 (r/w)

Table 42. Control register 6

BW_FILT1	BW_FILT0	FS1	FS0	FDS	LOW_ NOISE	0	0

Table 43. Control register 6 description

BW_FILT[1:0]	Bandwidth selection (see *Table 44*)
FS[1:0]	Full-scale selection (see *Table 45*)
FDS	Filtered data type selection. Default value: 0 (0: low-pass filter path selected; 1: high-pass filter path selected)
LOW_NOISE	Low-noise configuration. (0: disabled; 1: enabled)

Table 44. Digital filtering cutoff selection

BW_FILT[1:0]	Bandwidth selection
00	ODR/2 (up to ODR = 800 Hz, 400 Hz when ODR = 1600 Hz)
01	ODR/4 (HP/LP)
10	ODR/10 (HP/LP)
11	ODR/20 (HP/LP)

Table 45. Full-scale selection

FS[1:0]	Full-scale selection
00	±2 *g*
01	±4 *g*
10	±8 *g*
11	±16 *g*

8.10 OUT_T (26h)

Temperature output register in 8-bit resolution (r)

Table 46. OUT_T register

TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 47. OUT_T register description

TEMP[7:0]	Temperature sensor output data. The value is expressed as two's complement sign. Sensitivity = 1°C/LSB 0 LSB represents T=25 °C ambient.

8.11 STATUS (27h)

Status register (r).

Table 48. STATUS register

FIFO_THS	WU_IA	SLEEP_ STATE	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 49. STATUS register description

FIFO_THS	FIFO threshold status flag. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than the threshold level.)
WU_IA	Wakeup event detection status. (0: Wakeup event not detected; 1: Wakeup event detected)
SLEEP_ STATE	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.12 OUT_X_L (28h)

X-axis LSB output register (r).

Table 50. OUT_X_L register

X_L7	X_L6	X_L5	X_L4	X_L3(1)	X_L2(1)	0	0

1. If Low-Power Mode 1 is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_H (29h)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.13 OUT_X_H (29h)

X-axis MSB output register (r).

Table 51. OUT_X_H register

X_H7	X_H6	X_H5	X_H4	X_H3	X_H2	X_H1	X_H0

The 8 most significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_L (28h)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.14 OUT_Y_L (2Ah)

Y-axis LSB output register (r).

Table 52. OUT_Y_L register

Y_L7	Y_L6	Y_L5	Y_L4	Y_L3(1)	Y_L2(1)	0	0

1. If Low-Power Mode 1 is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_H (2Bh)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.15 OUT_Y_H (2Bh)

Y-axis MSB output register (r).

Table 53. OUT_Y_H register

Y_H7	Y_H6	Y_H5	Y_H4	Y_H3	Y_H2	Y_H1	Y_H0

The 8 most significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_L (2Ah)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.16 OUT_Z_L (2Ch)

Z-axis LSB output register (r).

Table 54. OUT_Z_L register

Z_L7	Z_L6	Z_L5	Z_L4	Z_L3(1)	Z_L2(1)	0	0

1. If Low-power Mode 1 is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_H (2Dh)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.17 OUT_Z_H (2Dh)

Z-axis MSB output register (r).

Table 55. OUT_Z_H register

Z_H7	Z_H6	Z_H5	Z_H4	Z_H3	Z_H2	Z_H1	Z_H0

The 8 most significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_L (2Ch)* register, it forms the output value expressed as a 16-bit word in 2's complement.

8.18 FIFO_CTRL (2Eh)

FIFO control register (r/w).

Table 56. FIFO_CTRL register

FMode2	FMode1	FMode0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 57. FIFO_CTRL register description

FMode[2:0]	FIFO mode selection bits. Default: 000. For further details refer to *Table 58*
FTH[4:0]	FIFO threshold level setting.

Table 58. FIFO mode selection

FMode[2:0]	Mode description
000	Bypass mode: FIFO turned off
001	FIFO mode: Stops collecting data when FIFO is full.
010	Reserved
011	Continuous-to-FIFO: Stream mode until trigger is deasserted, then FIFO mode
100	Bypass-to-Continuous: Bypass mode until trigger is deasserted, then FIFO mode
101	Reserved
110	Continuous mode: If the FIFO is full, the new sample overwrites the older sample.
111	Reserved

8.19 FIFO_SAMPLES (2Fh)

FIFO_SAMPLES control register (r).

Table 59. FIFO_SAMPLES register

FIFO_ FTH	FIFO_ OVR	Diff5	Diff4	Diff3	Diff2	Diff1	Diff0

Table 60. FIFO_SAMPLES register description

FIFO_FTH	FIFO threshold status flag. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than the threshold level.)
FIFO_OVR	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
Diff[5:0]	Represents the number of unread samples stored in FIFO. (000000 = FIFO empty; 100000 = FIFO full, 32 unread samples).

8.20 TAP_THS_X (30h)

4D configuration enable and TAP threshold configuration (r/w).

Table 61. TAP_THS_X register

4D_EN	6D_THS1	6D_THS0	TAP_ THSX_4	TAP_ THSX_3	TAP_ THSX_2	TAP_ THSX_1	TAP_ THSX_0

Table 62. TAP_THS_X register description

4D_EN	4D detection portrait/landscape position enable. (0: no position detected; 1: portrait/landscape detection and face-up/face-down position enabled).
6D_THS[1:0]	Thresholds for 4D/6D function @ FS = ±2 *g* (refer to *Table 63*)
TAP_THSX_[4:0]	Threshold for TAP recognition @ FS = ±2 *g* on X direction

Table 63. 4D/6D threshold setting FS @ ±2 *g*

6D_THS[1:0]	Threshold decoding (degrees)
00	6 (80 degrees)
01	11 (70 degrees)
10	16 (60 degrees)
11	21 (50 degrees)

8.21 TAP_THS_Y (31h)

Table 64. TAP_THS_Y register

TAP_ PRIOR_2	TAP_ PRIOR_1	TAP_ PRIOR_0	TAP_ THSY_4	TAP_ THSY_3	TAP_ THSY_2	TAP_ THSY_1	TAP_ THSY_0

Table 65. TAP_THS_Y register description

TAP_PRIOR_[2:0]	Selection of priority axis for tap detection (see *Table 66*).
TAP_THSY_[4:0]	Threshold for tap recognition @ FS = ±2 *g* on Y direction.

Table 66. Selection of axis priority for tap detection

TAP_PRIOR_[2:0]	Max priority	Mid priority	Min priority
000	X	Y	Z
001	Y	X	Z
010	X	Z	Y
011	Z	Y	X
100	X	Y	Z
101	Y	Z	X
110	Z	X	Y
111	Z	Y	X

8.22 TAP_THS_Z (32h)

Table 67. TAP_THS_Z register

TAP_X_ EN	TAP_Y_ EN	TAP_Z_ EN	TAP_ THSZ_4	TAP_ THSZ_3	TAP_ THSZ_2	TAP_ THSZ_1	TAP_ THSZ_0

Table 68. TAP_THS_Z register description

TAP_X_EN	Enables X direction in tap recognition. (0: disabled; 1: enabled)
TAP_Y_EN	Enables Y direction in tap recognition. (0: disabled; 1: enabled)
TAP_Z_EN	Enables Z direction in tap recognition. (0: disabled; 1: enabled)
TAP_ THSZ_[4:0]	Threshold for tap recognition @ FS = ±2 *g* on Z direction.

8.23 INT_DUR (33h)

Interrupt duration register (r/w).

Table 69. INT_DUR register

LATENCY3	LATENCY2	LATENCY1	LATENCY0	QUIET1	QUIET0	SHOCK1	SHOCK0

Table 70. INT_DUR register description

LATENCY[3:0]	Duration of maximum time gap for double-tap recognition. When double-tap recognition is enabled, this register expresses the maximum time between two successive detected taps to determine a double-tap event. Default value is LATENCY[3:0] = 0000 (which is 16 * 1/ODR 1 LSB = 32 * 1/ODR
QUIET[1:0]	Expected quiet time after a tap detection: this register represents the time after the first detected tap in which there must not be any overthreshold event. Default value is QUIET[1:0] = 00 (which is 2 * 1/ODR) 1 LSB = 4 * 1/ODR
SHOCK[1:0]	Maximum duration of over-threshold event: this register represents the maximum time of an over-threshold signal detection to be recognized as a tap event. Default value is SHOCK[1:0] = 00 (which is 4 * 1/ODR) 1 LSB = 8 *1/ODR

8.24 WAKE_UP_THS (34h)

Wakeup threshold register (r/w).

Table 71. WAKE_UP_THS register

SINGLE_ DOUBLE_ TAP	SLEEP_ ON	WK_THS5	WK_THS4	WK_THS3	WK_THS 2	WK_THS 1	WK_THS 0

Table 72. WAKE_UP_THS register description

SINGLE_ DOUBLE_ TAP	Enable single/double-tap event. Default value: 0 (0: only single-tap event is enabled; 1: single and double-tap events are enabled)
SLEEP_ON	Sleep (inactivity) enable. Default value: 0 (0: sleep disabled; 1: sleep enabled)
WK_THS[5:0]	Wakeup threshold, 6-bit unsigned 1 LSB = 1/64 of FS. Default value: 000000

8.25 WAKE_UP_DUR (35h)

Wakeup and sleep duration configuration register (r/w).

Table 73. WAKE_UP_DUR register

FF_DUR5	WAKE_ DUR1	WAKE_ DUR0	STATIONARY	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0

Table 74. WAKE_UP_DUR register description

FF_DUR5	Free-fall duration. In conjunction with FF_DUR [4:0] bit in *FREE_FALL (36h)* register. 1 LSB = 1 * 1/ODR
WAKE_DUR[1:0]	Wakeup duration. 1 LSB = 1 *1/ODR
STATIONARY	Enable stationary detection / motion detection with no automatic ODR change when detecting stationary state. Default value: 0 (0: disabled; 1: enabled)
SLEEP_ DUR[3:0]	Duration to go in sleep mode. Default value is SLEEP_ DUR[3:0] = 0000 (which is 16 * 1/ODR) 1 LSB = 512 * 1/ODR

8.26 FREE_FALL (36h)

Free-fall duration and threshold configuration register (r/w).

Table 75. FREE_FALL register

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0

Table 76. FREE_FALL register description

FF_DUR [4:0]	Free-fall duration. In conjunction with FF_DUR5 bit in *WAKE_UP_DUR (35h)* register. 1 LSB = 1 * 1/ODR
FF_THS [2:0]	Free-fall threshold @ FS = ±2 *g* (refer to *Table 77*)

Table 77. FREE_FALL threshold decoding @ ±2 *g* FS

FF_THS[2:0]	Threshold decoding (LSB)
000	5
001	7
010	8
011	10
100	11
101	13
110	15
111	16

8.27 STATUS_DUP (37h)

Event detection status register (r).

Table 78. STATUS_DUP register

OVR	DRDY_T	SLEEP_ STATE_IA	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 79. STATUS_DUP register description

OVR	FIFO overrun status flag. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
DRDY_T	Temperature status. (0: data not available; 1: a new set of data is available)
SLEEP_ STATE_IA	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status: (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status: (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.28 WAKE_UP_SRC (38h)

Wakeup source register (r).

Table 80. WAKE_UP_SRC register

0	0	FF_IA	SLEEP_ STATE IA	WU_IA	X_WU	Y_WU	Z_WU

Table 81. WAKE_UP_SRC register description

FF_IA	Free-fall event detection status. (0: FF event not detected; 1: FF event detected)
SLEEP_ STATE IA	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
WU_IA	Wakeup event detection status. (0: Wakeup event not detected; 1: Wakeup event is detected)
X_WU	Wakeup event detection status on X-axis. (0: Wakeup event on X not detected; 1: Wakeup event on X-axis is detected)
Y_WU	Wakeup event detection status on Y-axis. (0: Wakeup event on Y not detected; 1: Wakeup event on Y-axis is detected)
Z_WU	Wakeup event detection status on Z-axis. (0: Wakeup event on Z not detected; 1: Wakeup event on Z-axis is detected)

8.29 TAP_SRC (39h)

Tap source register (r).

Table 82. TAP_SRC register

0	TAP_IA	SINGLE_ TAP	DOUBLE_ TAP	TAP_SIGN	X_TAP	Y_TAP	Z_TAP

Table 83. TAP_SRC register description

TAP_IA	Tap event status. (0: tap event not detected; 1: tap event detected)
SINGLE_TAP	Single-tap event status. (0: single-tap event not detected; 1: single-tap event detected)
DOUBLE_TAP	Double-tap event status. (0: double-tap event not detected; 1: double-tap event detected)
TAP_SIGN	Sign of acceleration detected by tap event. (0: positive sign of acceleration detected; 1: negative sign of acceleration detected)
X_TAP	Tap event detection status on X-axis. (0: Tap event on X not detected; 1: Tap event on X-axis is detected)
Y_TAP	Tap event detection status on Y-axis. (0: Tap event on Y not detected; 1: Tap event on Y-axis is detected)
Z_TAP	Tap event detection status on Z-axis. (0: Tap event on Z not detected; 1: Tap event on Z-axis is detected)

8.30 SIXD_SRC (3Ah)

6D source register (r).

Table 84. SIXD_SRC register

0	6D_IA	ZH	ZL	YH	YL	XH	XL

Table 85. SIXD_SRC register description

6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
ZH	ZH over threshold. (0: ZH does not exceed the threshold; 1: ZH is over the threshold)
ZL	ZL over threshold. (0: ZL does not exceed the threshold; 1: ZL is over the threshold)
YH	YH over threshold. (0: YH does not exceed the threshold; 1: YH is over the threshold)
YL	YL over threshold. (0: YL does not exceed the threshold; 1: YL is over the threshold)
XH	XH over threshold. (0: XH does not exceed the threshold; 1: XH is over the threshold)
XL	XL over threshold. (0: XL does not exceed the threshold; 1: XL is over the threshold)

8.31 ALL_INT_SRC (3Bh)

Reading this register, all related interrupt function flags routed to the INT pads are reset simultaneously.

Table 86. ALL_INT_SRC register

0	0	SLEEP_ CHANGE_IA	6D_IA	DOUBLE_ TAP	SINGLE_ TAP	WU_IA	FF_IA

Table 87. ALL_INT_SRC register description

SLEEP_ CHANGE_IA	Sleep change status. (0: Sleep change not detected; 1: Sleep change detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position detected)
DOUBLE_TAP	Double-tap event status. (0: double-tap event not detected; 1: double-tap event detected)
SINGLE_ TAP	Single-tap event status. (0: single-tap event not detected; 1: single-tap event detected)
WU_IA	Wakeup event detection status. (0: wakeup event not detected; 1: wakeup event detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)

8.32 X_OFS_USR (3Ch)

Table 88. X_OFS_USR register

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0

Table 89. X_OFS_USR register description

X_OFS_USR_[7:0]	Two's complement user offset value on X-axis data, used for wakeup function.

8.33 Y_OFS_USR (3Dh)

Table 90. Y_OFS_USR register

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0

Table 91. Y_OFS_USR register description

Y_OFS_USR_[7:0]	Two's complement user offset value on Y-axis data, used for wakeup function.

8.34 Z_OFS_USR (3Eh)

Table 92. Z_OFS_USR register

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0

Table 93. Z_OFS_USR register description

Z_OFS_USR_[7:0]	Two's complement user offset value on Z-axis data, used for wakeup function.

8.35 CTRL7 (3Fh)

Table 94. CTRL7 register

DRDY_ PULSED	INT2_ON _INT1	INTERRUPTS _ENABLE	USR_OFF _ON_OUT	USR_OFF _ON_WU	USR_OFF _W	HP_REF _MODE	LPASS_ ON6D

Table 95. CTRL7 register description

DRDY_ PULSED	Switches between latched and pulsed mode for data ready interrupt. (0: latched mode is used; 1: pulsed mode enabled for data-ready)
INT2_ON_INT1	Signal routing. (1: all signals available only on INT2 are routed on INT1)
INTERRUPTS_ ENABLE	Enable interrupts.
USR_OFF _ON_OUT	Enable application of user offset value on XL output data registers. FDS bit in *CTRL6 (25h)* must be set to '0'-logic (low-pass path selected).
USR_OFF _ON_WU	Enable application of user offset value on XL data for wakeup function only.
USR_OFF_W	Selects the weight of the user offset words specified by X_OFS_USR_[7:0], Y_OFS_USR_[7:0] and Z_OFS_USR_[7:0] bits. (0: 977 µg/LSB; 1: 15.6 mg/LSB)
HP_REF_MODE	High-pass filter reference mode enable. (0: high-pass filter reference mode disabled (default); 1: high-pass filter reference mode enabled)
LPASS_ON6D	(0: ODR/2 low pass filtered data sent to 6D interrupt function (default); 1: LPF2 output data sent to 6D interrupt function)

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Soldering information

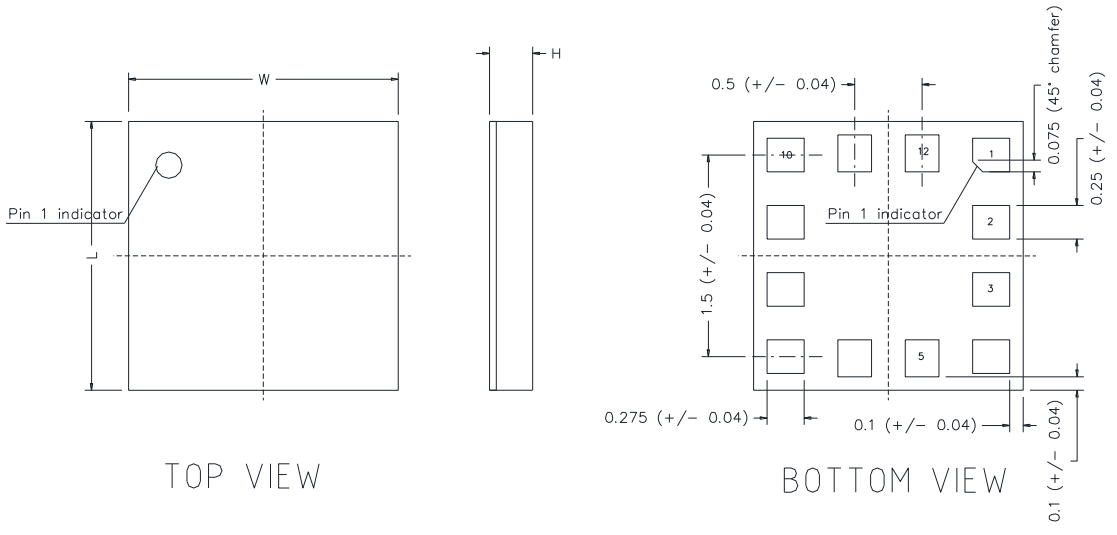
The LGA package is compliant with the ECOPACK, RoHS and “Green” standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Land pattern and soldering recommendations are available at www.st.com.

9.2 LGA-12 package information

Figure 21. LGA-12 2.0 x 2.0 x 0.7 mm package outline and mechanical data



Note : coplanarity of package terminals : 0.1mm

Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.15mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.1
Width [W]	2	±0.1
Height [H]	0.7 MAX	/

DM00170568_2

9.3 LGA-12 packing information

Figure 22. Carrier tape information for LGA-12 package

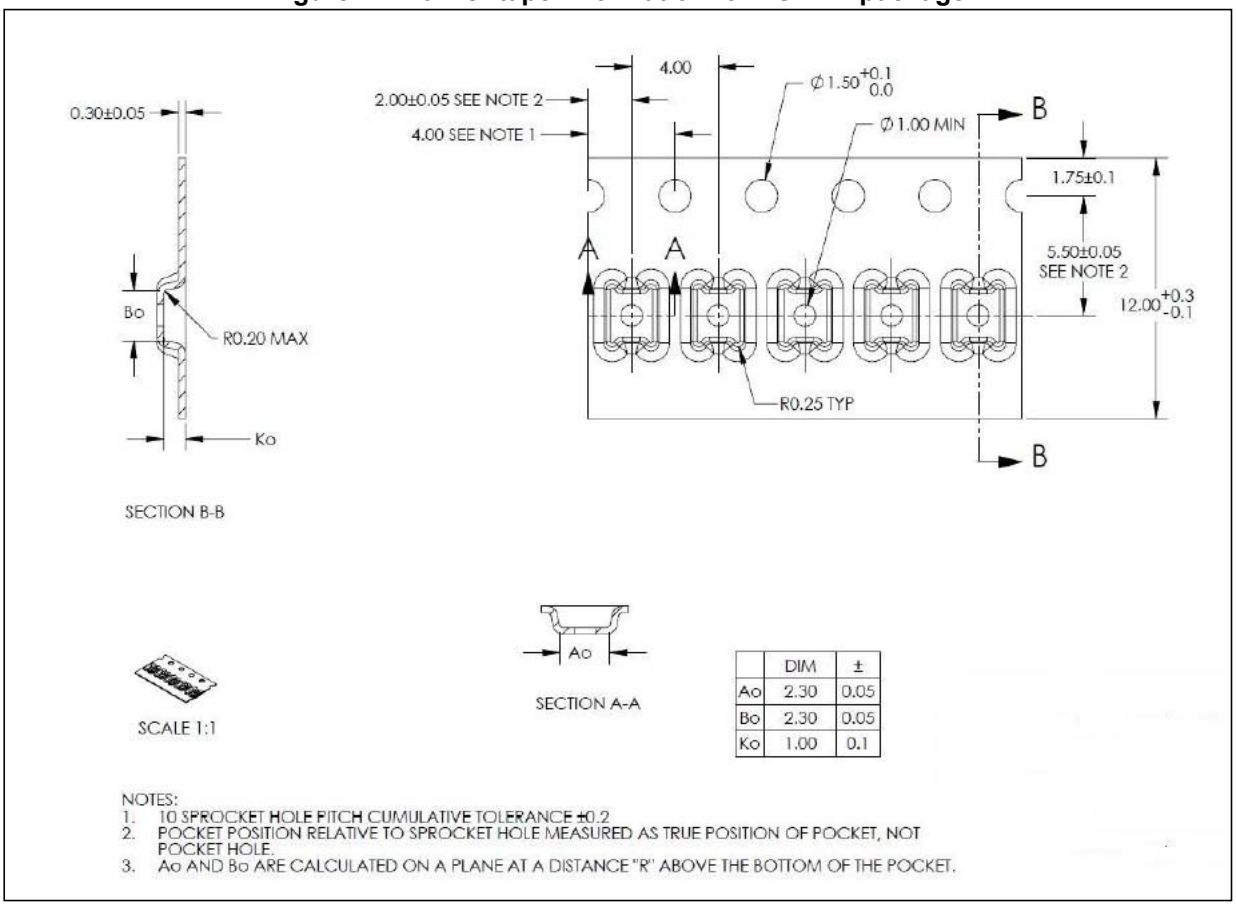
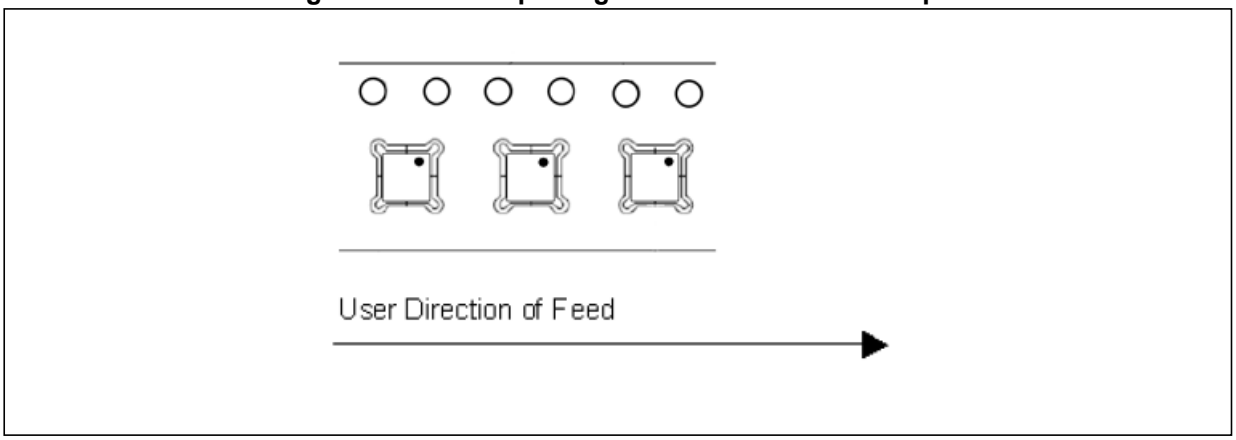


Figure 23. LGA-12 package orientation in carrier tape



10 Revision history

Table 96. Document revision history

Date	Revision	Changes
04-May-2018	1	Initial release
12-Jul-2018	2	First public release
23-Oct-2018	3	Updated *Section 3.2.4: Activity/Inactivity, stationary/motion-detection functions* Updated *Figure 6: IIS2DLPC electrical connections (top view)* Added *Section 9.3: LGA-12 packing information*
03-May-2019	4	Updated *Figure 22: Carrier tape information for LGA-12 package*