

G1 Ruby

Industrial microSD Card 6.10 datasheet
16GB - 128GB



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1. Product Summary

| | |
|------------------------------|--|
| <u>Capacity Range</u> | 16GB – 128GB |
| <u>Form Factor</u> | microSD Card |
| <u>Host Interface</u> | SD6.1 |
| <u>Speed Class</u> | CLASS10, UHS-I grade 3,V30, A2 |
| <u>Performance</u> | Sequential read: up to 100 MB/s Sequential write: up to 88 MB/s |
| <u>Reliability</u> | MTBF: 2 million hours UBER: <1 sector / 10¹⁶ bits read |
| <u>Operating Temperature</u> | |
| Or | Mobile: -25°C ~ 85°C Industrial: -40°C ~ 85°C |
| <u>Storage Temperature</u> | -40°C ~ 85°C |
| <u>Special Features</u> | CPRM (Content Protection for Recordable Media) * Password Protection of cards (optional) |
| <u>Compliances</u> | RoHS*, CE*, FCC*, WEEE* *Note: Please contact with Intelligent Memory represent for the detail of compliance conformity. |

2. Order Information

Table 1 – Part Numbers

| Part Number | Capacity | Speed Class | Operating Temperature range |
|-------------------------|----------|---------------------------------|-----------------------------|
| IMSDUDA8D2A2A1E2A5A0000 | 16GB | CLASS10, UHS-I Grade 3, V30, A2 | -25°C ~ 85°C |
| IMSDUDB1D2A2A1E2A6A0000 | 32GB | CLASS10, UHS-I Grade 3, V30, A2 | |
| IMSDUDB2D2A2A1E2A8A0000 | 64GB | CLASS10, UHS-I Grade 3, V30, A2 | |
| IMSDUDB4D2A2A1E2B1A0000 | 128GB | CLASS10, UHS-I Grade 3, V30, A2 | |
| IMSDUDA8D2A2A1I2A5A0000 | 16GB | CLASS10, UHS-I Grade 3, V30, A2 | -40°C ~ 85°C |
| IMSDUDB1D2A2A1I2A6A0000 | 32GB | CLASS10, UHS-I Grade 3, V30, A2 | |
| IMSDUDB2D2A2A1I2A8A0000 | 64GB | CLASS10, UHS-I Grade 3, V30, A2 | |
| IMSDUDB4D2A2A1I2B1A0000 | 128GB | CLASS10, UHS-I Grade 3, V30, A2 | |

3. Product Information

3.1 Compliant Specifications – SD Memory Card Specifications:

Compliant with Part 1 Physical Layer Specification Ver. 6.10

Compliant with Part 2 File System Specification Ver. 3.00

Compliant with Part 3 Security Specification Ver. 7.00

microSD Card Addendum Ver. 4.20

3.2 Bus Speed Mode (use 4 parallel data lines)

Non-UHS mode

- Default Speed Mode: 3.3V signaling, frequency up to 25MHz, data transfer up to 12.5MB/sec
- High Speed Mode: 3.3V signaling, frequency up to 50MHz, data transfer up to 25MB/sec

UHS-I mode

- SDR12: SDR up to 25MHz, 1.8V signaling
- SDR25: SDR up to 50MHz, 1.8V signaling
- SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
- SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec.
- DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/sec

Note: Timing in 1.8V signaling is different from that of 3.3V signaling.

3.3 Product Features

Electrical/Physical Interface: SD

- Support SD SPI mode
- Designed for read-only and read/write cards
- The command list supports [Part 1 Physical Layer Specification Ver 6.01] definitions
- Support CPRM (Content Protection for Recordable Media) of SD Card (optional)
- Support Hot Plug
 - Card removal during read operation will never harm the content
- Password Protection of cards (optional)
- Built-in write protection features (mechanical switch, permanent and temporary)
- +4KV/-4KV ESD protection in contact pads
- Operation voltage range: 2.7 ~ 3.6V

Copyrights Protection Mechanism

- Compliant with Part 1 Physical Layer Specification ver. 6.10, CPRM is Optional in SDHC/SDXC.

Advanced Flash Management

LDPC ECC (Low Density Parity Check Error Correction Code)

The deterioration of the flash memory cell over time and the disruptions from neighboring flash memory pages can lead to random bit errors in the stored data. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. Error detection and correction codes are used in flash memory storage systems to protect the data from corruption.

Static and Dynamic Wear Leveling

Wear leveling is a process that helps reduce premature wearing out of NAND Flash devices. The Flash controller manages access to the NAND Flash memory devices and determines how the NAND Flash blocks are used. In most cases, the NAND Flash controller maintains a lookup table to translate the memory array's physical block address (PBA) to the logical block address (LBA) used by the host system known as Physical to Logical Address Translation Table.

Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks"

pSLC (pseudo SLC)

The pSLC configuration on 3D TLC NAND only takes 1 bit for data storage from original 3 bits TLC NAND. It can dramatically increase the reliability, endurance of NAND Flash. It makes the SD Card meet high P/E cycle, high TBW demand in industrial and embedded applications and also increases data access performance.

3.4 SD Card Comparison

Table 2 – SDSC, SDHC, and SDXC Comparison table

| Comparison Table | | | |
|------------------------|-----------------------|--------------------------|--------------------------|
| | microSDSC | microSDHC | microSDXC |
| File System | FAT 12/16 | FAT32 | exFAT |
| Addressing Mode | Byte (1 byte unit) | Block (512 byte unit) | Block (512 byte unit) |
| HCS/CCS bits of ACMD41 | Support | Support | Support |
| CMD8 (SEND_IF_COND) | Support | Support | Support |
| CMD16 (SET_BLOCKLEN) | Support | Support (Only CMD42) | Support (Only CMD42) |
| Partial Read | Support | Not Support | Not Support |
| Lock/Unlock Function | Mandatory | Mandatory | Mandatory |

| | | | |
|---|-----------|-------------------------------------|-------------------------------------|
| Write Protect Groups | Optional | Not Support | Not Support |
| Supply Voltage 2.0V – 2.7V (for operation) | Support | Support | Support |
| Total Bus Capacitance for each signal line | 40pF | 40pF | 40pF |
| CSD Version (CSD_STRUCTURE Value) | 1.0 (0x0) | 2.0 (0x1) | 2.0 (0x1) |
| Speed Class | Optional | Mandatory (Class 2 / 4 / 6 / 10) | Mandatory (Class 2 / 4 / 6 / 10) |

4. Product Specification

4.1 Performance

We specify the performance of our NAND products in 2 ways:

- **“Peak”** describes the measured performance when the product is new and unused. It is commonly used by vendors in their datasheets. However, SSDs by design reduce performance after a relatively short usage period, so peak values cannot be used to predict an application’s longer-term performance.

Table 3 – Burst Performance

| Capacity | Speed Class | Sequential performance | |
|----------|------------------------------|------------------------|--------------|
| | | Read (MB/s) | Write (MB/s) |
| 16GB | A2, V30, CL10, UHS-I Grade 3 | 100 | 85 |
| 32GB | | 100 | 88 |
| 64GB | | 100 | 88 |
| 128GB | | 100 | 88 |

Notes:

1. Peak performance measured in **Fresh Out of the Box (FOB)** condition
2. Sequential performance is measured with 128KB transfer size; QD32 and 4KB align with IO Meter.
3. Random performance tested with IO Meter: 4KB random write with QD32.
4. Performance may differ depending on application and platform.

4.2 Endurance and Reliability

Endurance

The lifetime of our NAND products is specified in TBW (Tera Bytes Written), i.e. the total amount of data that the host can write to the NAND media in a defined pattern. In our case this pattern is based on the workload definitions set by JEDEC in JESD219A.

Same as for performance, endurance specification varies greatly depending on the underlying assumptions (especially also if the formula set by JEDEC, including the guard band is used) and I'M recommend assuring these assumptions are the same when comparing TBW values of different products.

Our endurance whitepaper is available here and also offers a simple calculator to validate and analyze different endurance values

Table 4 – Tera Bytes Written

| Capacity | TBW |
|----------|------|
| 16GB | 457 |
| 32GB | 914 |
| 64GB | 1828 |
| 128GB | 3657 |

Notes:
 1. TBW values are specified based on JEDEC 219A client and enterprise workload
 2. Actual lifetime may vary depending on platform and application

Reliability

Table 5 – Reliability

| Parameter | Value |
|-----------|-----------------|
| MTBF | 2,000,000 Hours |

5. Electrical Specifications

5.1 Power Consumption

Table 6 – Power Consumption

| Power Consumption | | | | | |
|--------------------|--------------|-----------------------|------------------|-----------------|--------------|
| Mode | | Max Power Consumption | | | |
| | | Power Up Current (uA) | Read (mA)@ @3.6V | Write (mA)@3.6V | Standby (mA) |
| Default Speed Mode | | 250 | 150 | 150 | 1 |
| High Speed Mode | | 250 | 200 | 200 | 1 |
| UHS-1 Mode | UHS50/DDR50 | 250 | 400 | 400 | 1 |
| | UHS104/DDR50 | 250 | 400 | 400 | 1 |

Notes:
 1.Power consumption are measured at room temperature.
 2.Power consumption of Max. Standby Current is for microSD cards uwith the max. capacity
 3.For SDXC, up to 100mA from VDD1 when XPC=0; up to 150mA from VDD1 when XPC=1.

5.2 DC Characteristic

Table 7 – Bus Operating Conditions – Threshold Level

| Bus Operating Conditions – Threshold Level | | | | | |
|--|--------|-----------|-----------|------|--------------------|
| Parameter | Symbol | Min | Max | Unit | Condition |
| Supply Voltage | VDD | 2.7 | 3.6 | V | |
| Output High Voltage | VOH | 0.75*VDD | | V | IOH=-2mA VDD Min |
| Output Low Voltage | VOL | | 0.125*VDD | V | IOL=2mA VDD Min |
| Input High Voltage | VIH | 0.625*VDD | VDD+0.3 | V | |
| Input Low Voltage | VIL | VSS-0.3 | 0.25*VDD | V | |
| Power Up Time | | | 250 | ms | From 0V to VDD min |

Table 8 – Peak Voltage and Leakage Current

| Peak Voltage and Leakage Current | | | |
|----------------------------------|------|---------|------|
| Parameter | Min | Max | Unit |
| Peak voltage on all lines | -0.3 | VDD+0.3 | V |
| All inputs | | | |
| Input Leakage Current | -10 | 10 | uA |
| All outputs | | | |
| Output Leakage Current | -10 | 10 | uA |

5.3 Bus Signal Line Levels

Table 9 – Bus Operation Conditions – Signal Line's Load

| Bus Operation Conditions – Signal Line's Load | | | | | |
|---|-----------------------------------|-----|-----|------|---|
| Parameter | Symbol | Min | Max | Unit | Remark |
| Pull-up resistance | R _{CMD} R _{DAT} | 10 | 100 | kΩ | To prevent bus floating |
| Total bus capacitance for each signal line | C _L | | 40 | pF | 1 card C _{HOST} +C _{BUS} shall not exceed 30 pF |
| Card Capacitance for each signal pin | C _{CARD} | | 10 | pF | |
| Maximum signal line inductance | | | 16 | nH | |
| Pull-up resistance inside card (pin1) | R _{DAT3} | 10 | 90 | kΩ | May be used for card detection |
| Capacity Connected to Power Line | C _C | | 5 | uF | To prevent inrush current |
| Notes: 1.The total capacitance CL the CLK line of the SD Memory Card bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line: $CL = CHOST + CBUS + N * CCARD$, Where N is the number of connected cards. | | | | | |

5.4 Power up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

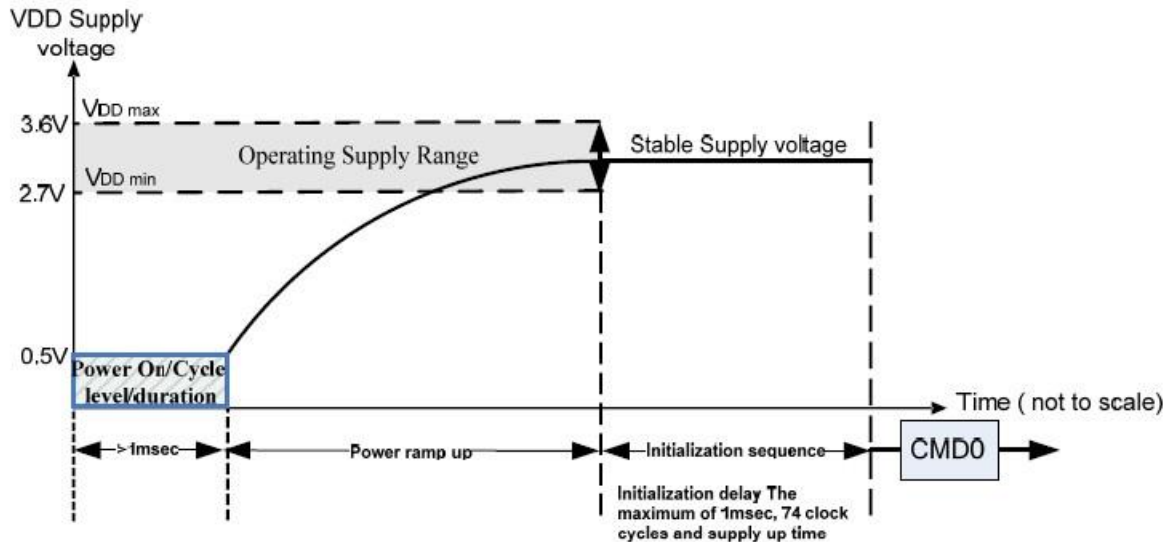


Figure 1 – Power up Time of Host

Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

- (1) Voltage level shall be below 0.5V
- (2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

- (1) Voltage of power ramp up should be monotonic as much as possible.
- (2) The minimum ramp up time should be 0.1ms.
- (3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
- (4) Host shall wait until VDD is stable.
- (5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

Power Down and Power Cycle

When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To

create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

5.5 Power Up Time of Card

A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.

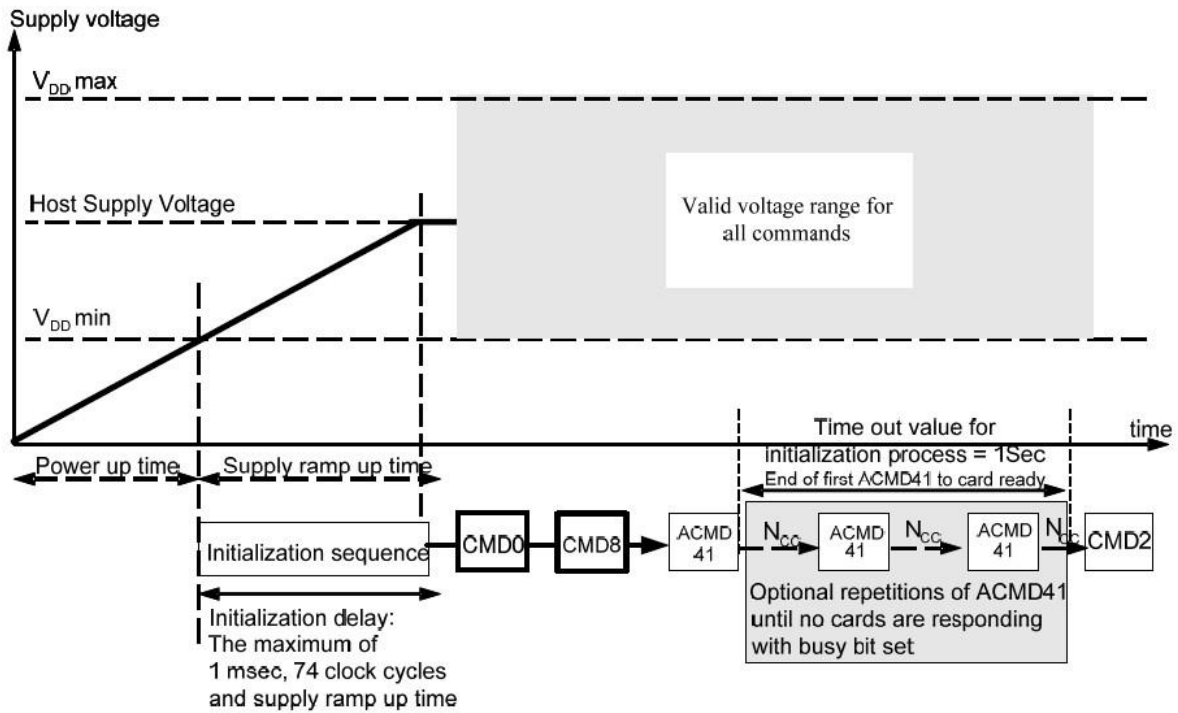


Figure 2 – Power up Time of Card

5.6 SD Interface Timing (Default)

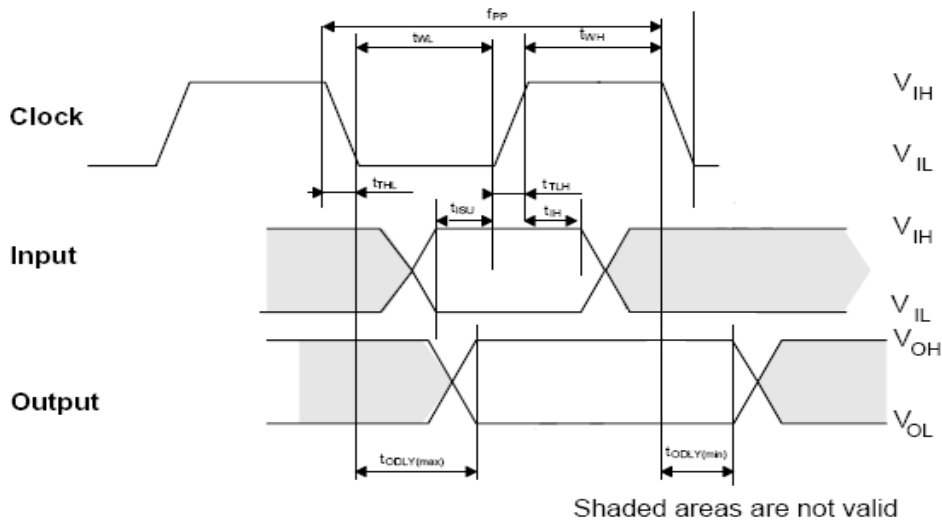


Figure 3 – Input/Output Timing (Default Speed Mode)

Table 10 – Bus Operation Conditions – Signal Line’s Load

| Interface timing (Default) | | | | | |
|---|-------------------|---------------------|-----|------|-----------------------------------|
| Parameter | Symbol | Min | Max | Unit | Remark |
| Clock CLK (All values are referred to min(V _{IH}) and max(V _{IL})) | | | | | |
| Clock frequency Data Transfer Mode | f _{PP} | 0 | 25 | MHz | C _{card} ≤ 10pF (1 card) |
| Clock frequency Identification Mode | f _{OD} | 0 ₁ /100 | 400 | kHz | C _{card} ≤ 10pF (1 card) |
| Clock low time | t _{WL} | 10 | | n | C _{card} ≤ 10pF (1 card) |
| Clock high time | t _{WH} | 10 | | ns | C _{card} ≤ 10pF (1 card) |
| Clock rise time | t _{TLH} | | 10 | ns | C _{card} ≤ 10pF (1 card) |
| Clock fall time | t _{THL} | | 10 | ns | C _{card} ≤ 10pF (1 card) |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| Input set-up time | t _{ISU} | 5 | | ns | C _{card} ≤ 10pF (1 card) |
| Input hold time | t _{IH} | 5 | | ns | C _{card} ≤ 10pF (1 card) |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| Output Delay time during Data Transfer Mode | t _{ODLY} | 0 | 14 | ns | C _L ≤ 40pF (1 card) |
| Output Delay time during Identification Mode | t _{ODLY} | 0 | 50 | ns | C _L ≤ 40pF (1 card) |
| Notes: | | | | | |
| *1: 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required. | | | | | |

5.7 SD Interface Timing (High-Speed Mode)

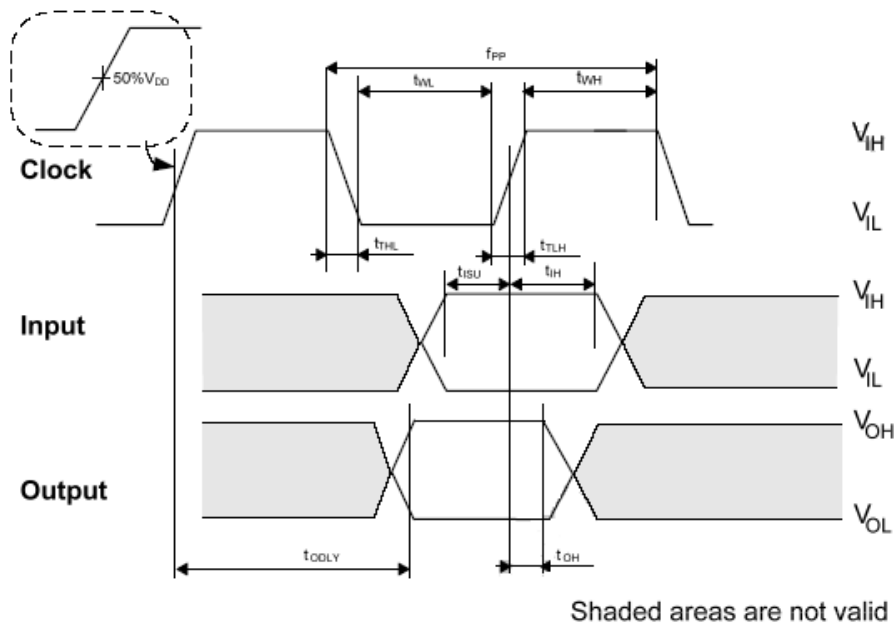


Figure 4 – Input/Output Timing (High-Speed Mode)

Table 11 – Interface timing (High-Speed Mode)

| Interface timing (High-Speed Mode) | | | | | |
|--|-------------------|-----|-----|------|-----------------------------------|
| Parameter | Symbol | Min | Max | Unit | Remark |
| Clock CLK (All values are referred to min(V _{IH}) and max(V _{IL})) | | | | | |
| Clock frequency Data Transfer Mode | f _{PP} | 0 | 50 | MHz | C _{card} ≤ 10pF (1 card) |
| Clock low time | t _{WL} | 7 | | ns | C _{card} ≤ 10pF (1 card) |
| Clock high time | t _{WH} | 7 | | ns | C _{card} ≤ 10pF (1 card) |
| Clock rise time | t _{TLH} | | 3 | ns | C _{card} ≤ 10pF (1 card) |
| Clock fall time | t _{THL} | | 3 | ns | C _{card} ≤ 10pF (1 card) |
| Inputs CMD, DAT (referenced to CLK) | | | | | |
| Input set-up time | t _{ISU} | 6 | | ns | C _{card} ≤ 10pF (1 card) |
| Input hold time | t _{IH} | 2 | | ns | C _{card} ≤ 10pF (1 card) |
| Outputs CMD, DAT (referenced to CLK) | | | | | |
| Output Delay time during Data Transfer Mode | t _{ODLY} | | 14 | ns | C _L ≤ 40pF (1 card) |
| Output Hold time | T _{OH} | 2.5 | | ns | C _L ≤ 15pF (1 card) |
| Total System capacitance of each line*1 | C _L | | 40 | nF | C _L ≤ 15pF (1 card) |
| Notes: | | | | | |
| *1: In order to satisfy severe timing, the host shall drive only one card. AC Characteristic (SDR12, SDR25, SDR50 and SDR10) | | | | | |

5.8 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

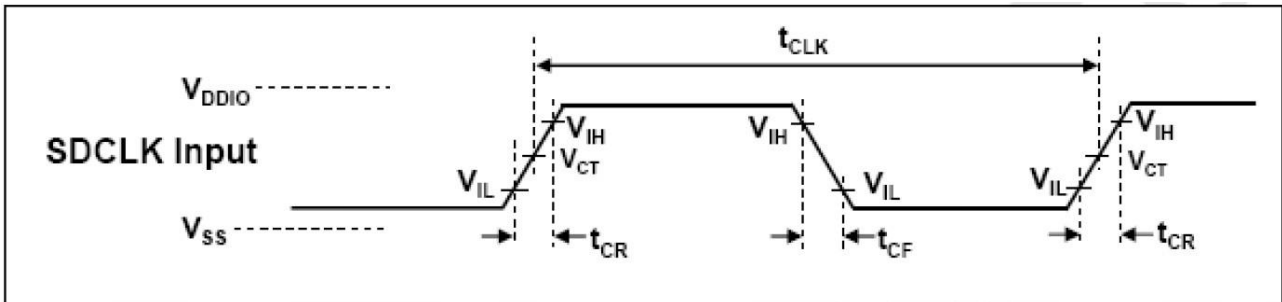


Figure 5 – Clock Signal Timing

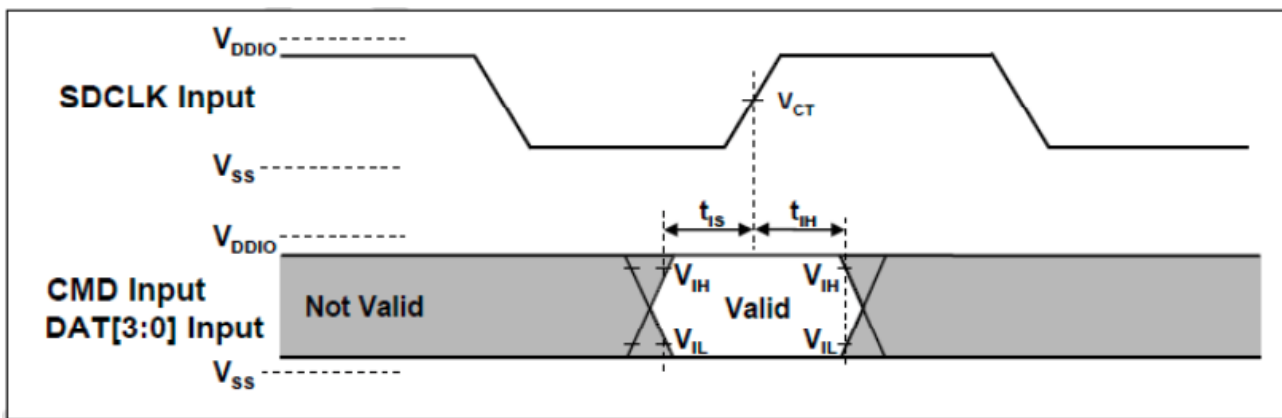


Figure 6 – Card Input Timing

Table 12 – Interface timing (High-Speed Mode)

| Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes Input) | | | | |
|---|------|-----------------------|------|---|
| Symbol | Min | Max | Unit | Remark |
| t _{CLK} | 4.8 | - | ns | 208MHz (Max.), Between rising edge, V _{CT} = 0.975V |
| t _{CR} , t _{CF} | - | 0.2* t _{CLK} | ns | t _{CR} , t _{CF} < 0.96ns (max.) at 208MHz, CCARD =10pF t _{CR} , t _{CF} < 2.00ns (max.) at 100MHz, CCARD =10pF The absolute maximum value 17ft he, t _{CF} is 10ns regardless of clock frequency |
| Clock Duty | 30 | 70 | % | |
| Symbol | Min | Max | Unit | SDR 104 Mode |
| t _{IS} | 1.40 | - | ns | CCARD =10pF, V _{CT} = 0.975V |
| t _{IH} | 0.81 | - | ns | CCARD = 5pF, V _{CT} = 0.975V |
| Symbol | Min | Max | Unit | SDR50 Mode |
| t _{IS} | 3.00 | - | ns | CCARD =10pF, V _{CT} = 0.975V |
| t _{IH} | 0.81 | - | ns | CCARD = 5pF, V _{CT} = 0.975V |

6. Environmental Specifications

Table 13 – Environmental Specifications

| Environmental Specifications | | |
|------------------------------|---|--|
| Test | Test Condition | |
| Temperature | Operation | Mobile temperature: -25°C ~ 85°C, 0% RH, 96 hours Industrial temperature: -40°C ~ 85°C, 0% RH, 300 hours |
| | Storage | Mobile temperature: -40°C, 0% RH, 168 hours ; 85°C, 0% RH, 500 hours Industrial temperature: -40°C, 0% RH, 500 hours ; 85°C, 0% RH, 500 hours |
| Humidity | Operation | Mobile temperature: 25°C, 95% RH 1 hours Industrial temperature: 55°C, 95% RH 4 hours |
| | Storage | Mobile temperature: 40°C, 95% RH 500 hours Industrial temperature: 55°C, 95% RH 500 hours |
| Shock | Mobile temperature: 500G, 0.5ms Industrial temperature: 1500G, 0.5ms | |
| Vibration | 20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/30mins each | |
| Drop | 150cm free fall, 6 face of each | |
| Bending | ≥10N, hold 1Min / 5 Times | |
| Torque | 0.1N-m or +/-2.5deg, hold 30 seconds / 5 Times | |
| Durability | 10,000 times mating cycle | |
| ESD | Non-operation | Contact: +/- 4KV each item; 5 times/Pin Air: +/- 15KV ; 5 times/Position |
| | Operation | Air: +/- 8KV ; 10 times/Position (B-Grade) |

7. Interface

7.1 Pin Assignment and Descriptions

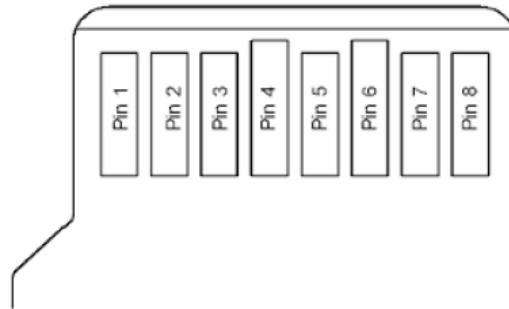


Figure 7 – Pin Locations

Table 14 – Signal Segment Pin Assignment and Descriptions

| Pin Assignment and Descriptions | | | | | | |
|---------------------------------|----------------------|---------------------|------------------------------|----------|----------------|-----------------------|
| Pin # | SD Mode | | | SPI Mode | | |
| | Name | Type1 | Description | Name | Type | Description |
| 1 | DAT2 | I/O/PP | Data Line[bit2] | RSV | | |
| 2 | CD/DAT3 ² | I/O/PP ³ | Card Detect/ Data Line[bit3] | CS | I ³ | Chip Select (negtrue) |
| 3 | CMD | PP | Command/Response | DI | I | Data In |
| 4 | VDD | S | Supply voltage | VDD | S | Supply voltage |
| 5 | CLK | I | Clock | SCLK | I | Clock |
| 6 | VSS | S | Supply voltage ground | VSS | S | Supply voltage ground |
| 7 | DAT0 | I/O/PP | Data Line[bit0] | DO | O/PP | Data Out |
| 8 | DAT1 | I/O/PP | Data Line[bit1] | RSV | | |

Note:
 S: power supply
 I: input
 O: output using push-pull drivers
 PP: I/O using push-pull drivers
 The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.
 At power up this line has a 50Kohm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. The user should disconnect this pull-up during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

8. Physical Dimension

15.0 mm(L) x 11.0 mm(W) x 1.00 mm(T)

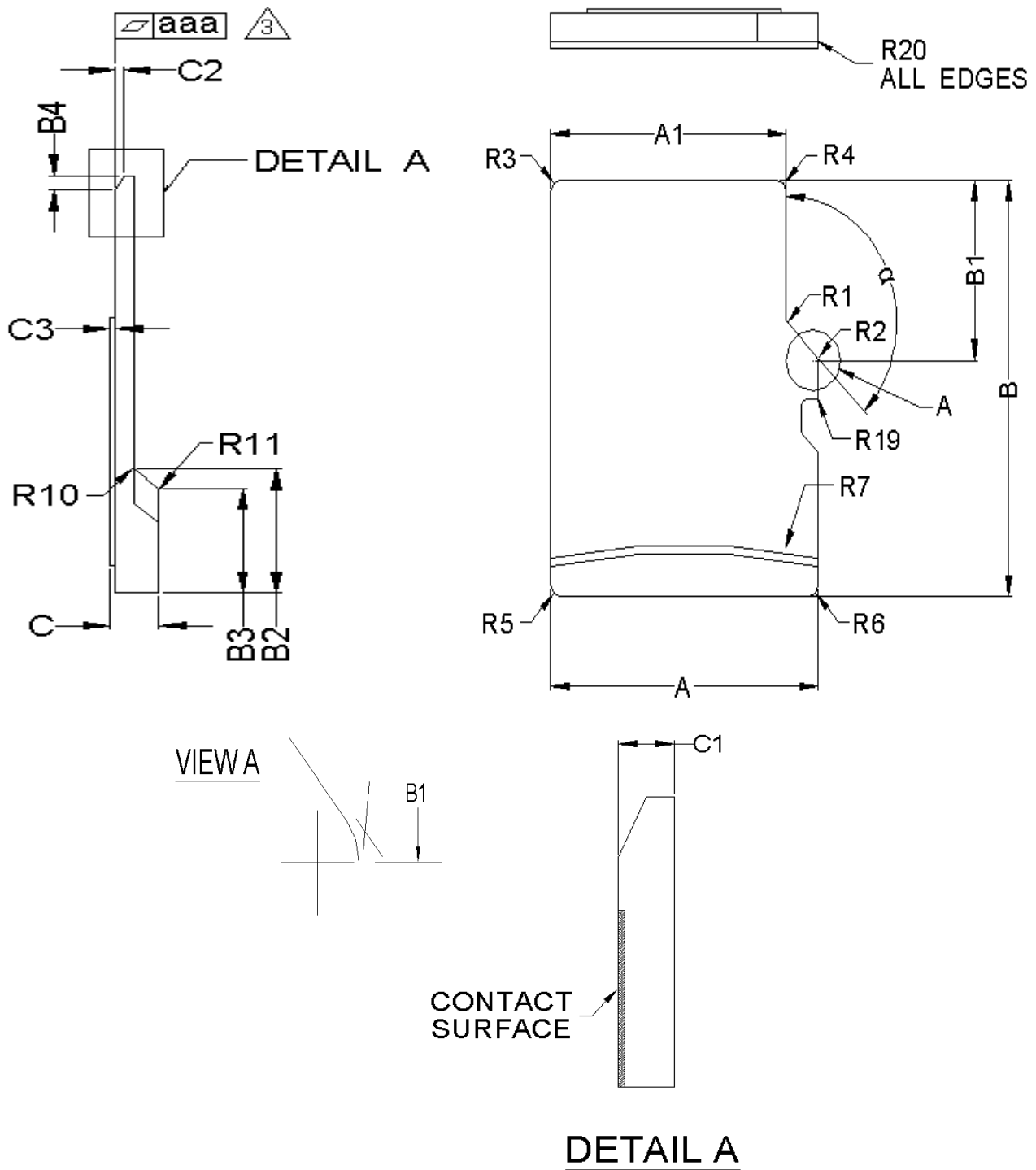


Figure 8 – Device Physical Dimension