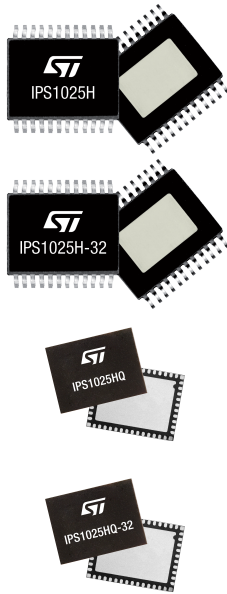


## High efficiency, high-side switch with extended diagnostics and smart driving for capacitive loads



### Features

- 8 V to 60 V operating supply voltage range
- Operating output current: 2.4 A (IPS1025H/HQ) or 5.6 A (IPS1025H-32/HQ-32)
- Smart driving of capacitive load
- Fast demagnetization of inductive loads
- Under-voltage lock-out
- $V_{CC}$  over-voltage protection
- Output overload and over-temperature protections
- Case over-temperature protection
- Ground disconnection protection
- Overload event diagnostic pin
- Over-temperature event diagnostic pin
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- Packages: PowerSSO-24 and QFN48L 8x6x0.9 mm

### Applications

- Programmable logic control
- Vending machines
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

### Description

The IPS1025H/HQ and IPS1025H-32/HQ-32 are single high-side switch ICs able to drive capacitive, resistive or inductive loads with one side connected to ground.

The very low  $R_{DS-ON}$  ( $\leq 25 \text{ m}\Omega$  up to  $T_J = 125 \text{ }^\circ\text{C}$ ) makes the IC suitable for the applications with up to 2.4 A (IPS1025H/HQ) or 5.6 A (IPS1025H-32/HQ-32) steady state operating current.

The output channel is protected against junction over-temperature events by a junction temperature sensor, and a further temperature sensor is included to monitor case temperature, so the overheated output channel can only be turned back ON when the case temperature returns below the reset temperature.

The embedded overload protection circuit monitors the output current and, on triggering of the activation threshold ( $I_{PK}$ ), starts modulating the impedance of the output switch to limit the output current to  $I_{LIM}$ , for both IC and load protection.

The IC offers two different sets of activation threshold and limitation levels ( $I_{PKH}$ ,  $I_{LIMH}$  and  $I_{PKL}$ ,  $I_{LIML}$ ) for smart driving of capacitive loads (such as bulb lamps) and loads with initial peak current requirements.

The IC diagnostics is based on  $FLT_1$  and  $FLT_2$  pins (both current source); activated by respective overload or overtemperature events on the output channel.

#### Product status link

[IPS1025H](#)

[IPS1025H-32](#)

[IPS1025HQ](#)

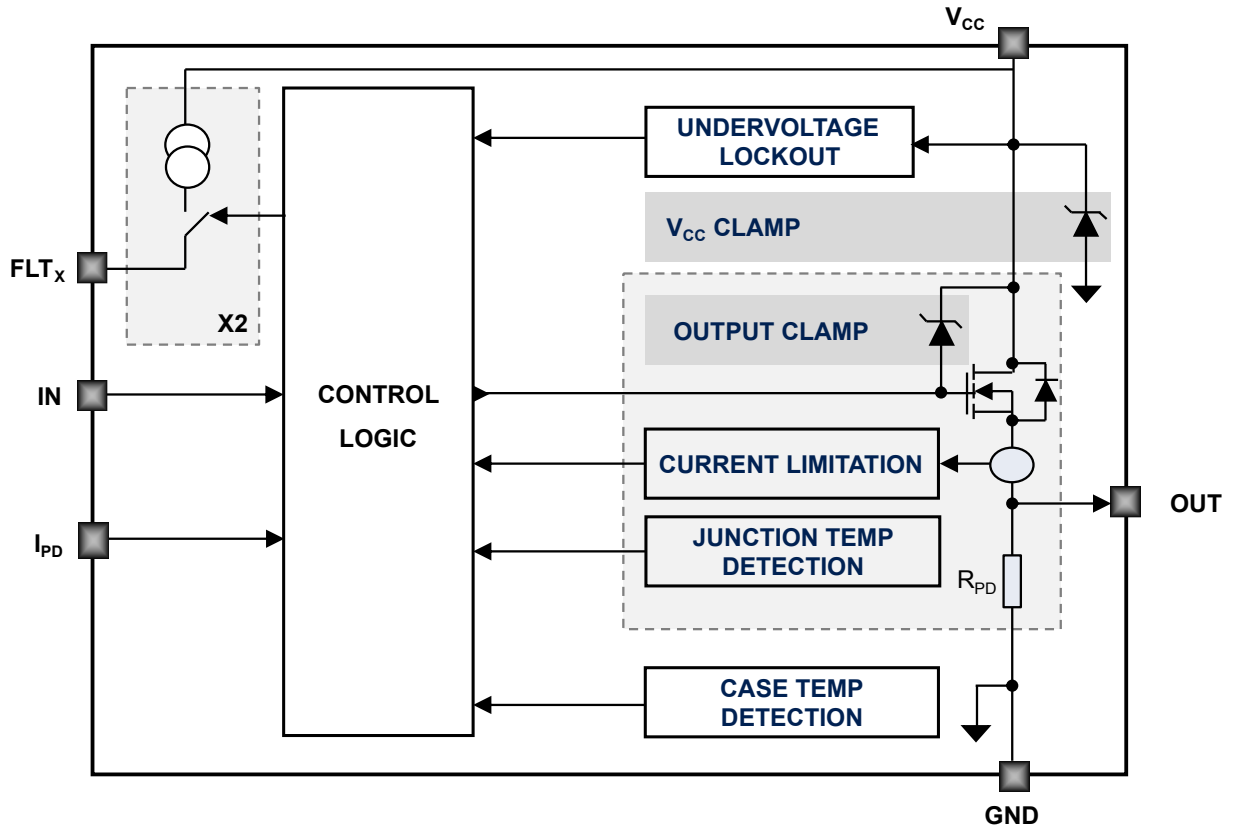
[IPS1025HQ-32](#)

#### Product label



# 1 Block diagram

Figure 1. IPS1025H/HQ, IPS1025H-32/HQ-32 block diagram



## 2 Pin connection

Figure 2. Pin connections (top through view)

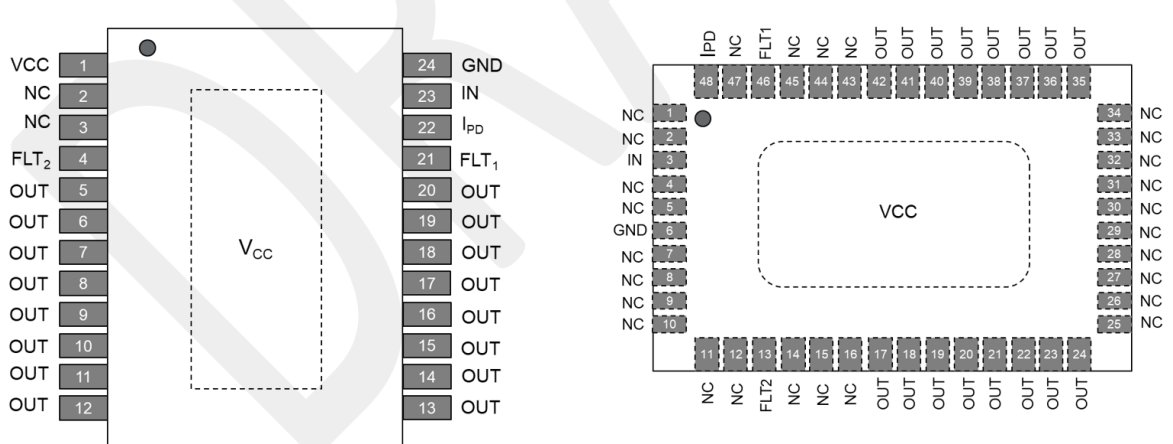


Table 1. Pin descriptions

Pin no.		Name	Description
PSSO24	QFN48L		
1, exposed pad	exposed pad	VCC	Supply voltage
2,3	1,2,4,5,7,8,9,10,11,12,14,16,25,26,27,28,29,30,31,32,33,34,43,45,47	N.C.	Not connected
4	13	FLT2	Overload event diagnostic pin
5 to 20	17 to 24, 35 to 42	OUT	Power stage output channel
21	46	FLT1	Over-temperature event diagnostic pin
22	48	IPD	Initial current duration / level selector. Connect to GND by a capacitor to set duration of $I_{PKH}$ (see Section 7.3 and Table 9 / Table 10). Connect to IN pin by a 220 kΩ resistor to disable initial $I_{PKH}$ threshold (the over-current limit is only $I_{PKL}$ ). Connect to GND by a 10 kΩ resistor to disable $I_{PKL}$ (the over-current threshold is only $I_{PKH}$ ). <i>Note: Leaving <math>I_{PD}</math> floating is equivalent to a 1 μs duration for <math>I_{PKH}</math>.</i>
23	3	IN	Input
24	6	GND	Device ground

### 3 Absolute maximum ratings

Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.3 to 65	V
$I_{CC}$	Maximum DC reverse current (from GND to $V_{CC}$ )	-250	mA
$I_{OUT}$	Output stage current	Internally limited	A
$-I_{OUT}$	Reverse current (from OUT to $V_{CC}$ )	5	A
$V_{IN}$	IN pin voltage	-0.3 to $V_{CC}$	V
$I_{IN}$	IN pin current	-10/+10	mA
$V_{PD}$	$I_{PD}$ pin voltage	-0.3 to 5.5	V
$I_{PD}$	$I_{PD}$ pin current	-1/+10	mA
$V_{FAULT}$	FLT pins voltage	-0.3 to 5.5	V
$I_{FAULT}$	FLT pins current	-1 <sup>(1)</sup> /+10	mA
$E_{AS}$	Single pulse avalanche energy ( $T_{AMB} = 125\text{ °C}$ , $V_{CC} = 24\text{ V}$ , $I_{OUT} = 2\text{ A}$ )	14 <sup>(2)</sup>	J
		5.8 <sup>(3)</sup>	J
$P_{TOT}$	Power Dissipation at $T_C = 25\text{ °C}$	Internally limited	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Junction Operating Temperature	Internally limited	°C
$T_C$	Case Operating Temperature	-40 to 150	°C

1. intended as worst case when IC is in normal operation (no fault)

2. IPS1025H / IPS1025H-32

3. IPS1025HQ / IPS1025HQ-32

## 4 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	PSSO24	QFN48L	Unit
$R_{th(JC)}$ <sup>(1)</sup>	Thermal resistance junction-case	0.7	1	°C/W
$R_{th(JA)}$ <sup>(2)</sup>	Thermal resistance junction-ambient	22	26	°C/W

1.  $R_{th}$  between the die and the bottom case surface measured by cold plate as per JESD51.
2. JESD51-7.

## 5 Electrical characteristics

(8 V < V<sub>CC</sub> < 60 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified)

**Table 4. Supply**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>UVON</sub>	Under-voltage ON threshold	-	6.9	-	8	V
V <sub>UVOFF</sub>	Under-voltage OFF threshold	-	6.5	-	7.8	V
V <sub>UVH</sub>	Under-voltage hysteresis	-	0.15	0.5	-	V
I <sub>SOFF</sub>	Supply current in OFF state	V <sub>CC</sub> = 24 V, I <sub>IN</sub> = GND, O <sub>UT</sub> = open load;	0.28	-	0.64	mA
		V <sub>CC</sub> = 36 V, I <sub>IN</sub> = GND, O <sub>UT</sub> = open load;	0.28	-	0.64	mA
		V <sub>CC</sub> = 60 V, I <sub>IN</sub> = GND, O <sub>UT</sub> = open load;	0.29	-	0.685	mA
I <sub>SON</sub>	Supply current in ON state	V <sub>CC</sub> = 24 V, I <sub>IN</sub> = 5 V, O <sub>UT</sub> = open load;	1.05	-	2.25	mA
		V <sub>CC</sub> = 36 V, I <sub>IN</sub> = 5 V, O <sub>UT</sub> = open load;	1.15	-	2.35	mA
		V <sub>CC</sub> = 60 V, I <sub>IN</sub> = 5 V, O <sub>UT</sub> = open load;	1.35	-	2.55	mA

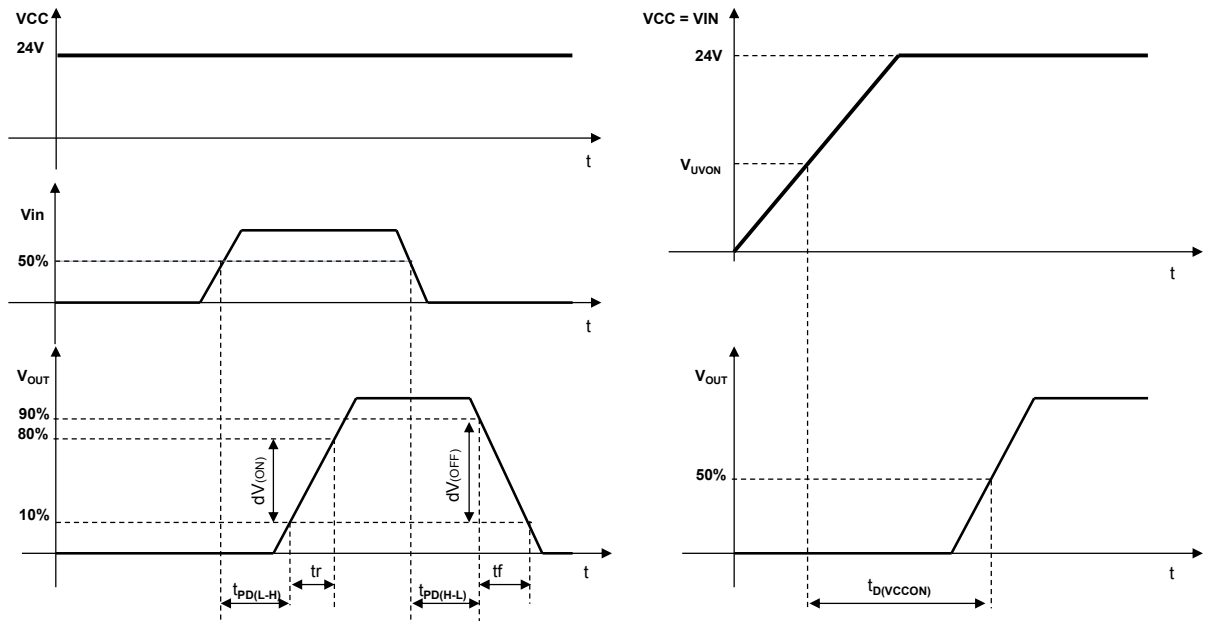
**Table 5. Output stage**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R <sub>DS(ON)</sub>	On-state resistance	V <sub>CC</sub> = 24 V, R <sub>LOAD</sub> = 12 Ω, @ T <sub>J</sub> = 25 °C	-	12	15	mΩ
		V <sub>CC</sub> = 24 V, R <sub>LOAD</sub> = 12 Ω, @ T <sub>J</sub> = 125 °C	-	-	25	mΩ
V <sub>OUT(OFF)</sub>	OFF state output voltage	V <sub>IN</sub> = 0 V and I <sub>O<sub>UT</sub></sub> = 0 A	-	-	2	V
I <sub>O<sub>UT</sub>(OFF)</sub>	OFF state output current	V <sub>IN</sub> = 0 V, V <sub>O<sub>UT</sub></sub> = 0 V	-	-	10	μA

**Table 6. Switching**

(V<sub>CC</sub> = 24 V; -40 °C < T<sub>J</sub> < 125 °C, R<sub>LOAD</sub> = 12 Ω, input rise time < 0.1 μs)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t <sub>r</sub>	Rise time		-	30	60	μs
t <sub>f</sub>	Fall time		-	25	60	μs
t <sub>PD(L-H)</sub>	Propagation delay time IN to OUT, low to high		-	13	25	μs
t <sub>PD(H-L)</sub>	Propagation delay time IN to OUT, high to low		-	60	100	μs
td(V <sub>con</sub> )	Propagation delay time IN to OUT at power-on	V <sub>IN</sub> = V <sub>CC</sub> and rising from 0 to 24 V	150	500	1600	μs

**Figure 3. Timing**

**Table 7. Input pin (IN)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{IL}$	Input pin low level voltage	-	-	-	0.8	V
$V_{IH}$	Input pin high level voltage	-	2.2	-	-	V
$V_{I(HYST)}$	Input pin hysteresis voltage	-	-	0.4	-	V
$I_{IN}$	Input pin current	$V_{IN} = V_{CC} = 36\text{ V}$	-	-	200	$\mu\text{A}$
		$V_{IN} = V_{CC} = 60\text{ V}$	-	-	600	

**Table 8. Diagnostic pins (FLT<sub>1</sub>, FLT<sub>2</sub>)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{HFLT}$	Diagnostic pins source current in fault condition.	$V_{FLT} = 1\text{ V}$ (fault condition active)	-2.0	-	-4.0	mA
		$V_{FLT} = 5\text{ V}$ (fault condition active)	-0.4	-0.7	-1.0	
$I_{LFLT}$	Diagnostic pins leakage current	Normal operation $V_{CC} = 60\text{ V}$	0	-	-25	$\mu\text{A}$
$BT_{FLT}$	Diagnostic pins blanking time	-	60	-	400	$\mu\text{s}$
$V_{CLFLT}$	Diagnostic pins clamp voltage	$I_{FLT} = +1\text{ mA}$	6	6.8	8	V
		$I_{FLT} = -1\text{ mA}$	-	-	0.7	

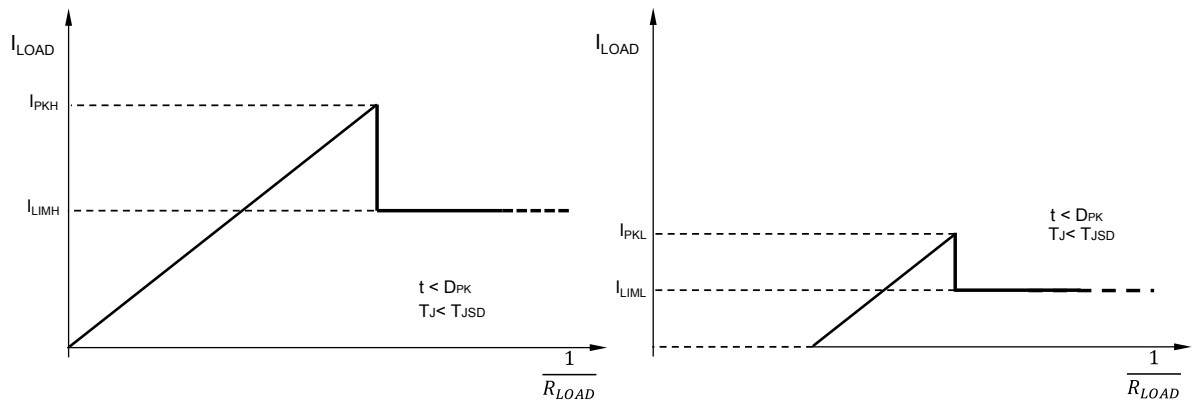
**Table 9. IPS1025H/HQ Overload protections**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Overload with Dual Threshold Protection: I<sub>PD</sub> pin to GND by C<sub>PD</sub> (470 pF ≤ C<sub>PD</sub> ≤ 470 nF); see Section 7.3.1</b>						
I <sub>PKH</sub>	Initial over-current activation threshold	V <sub>CC</sub> = 24 V	-	15.4	-	A
I <sub>LIMH</sub>	Initial over-current limitation level		6.25	9.0	11.75	A
D <sub>PK</sub>	Time limit of Initial over-current		-	215*C <sub>PD</sub> [nF]	-	μs
I <sub>PKL</sub>	Steady state over-current activation threshold		-	8.0	-	A
I <sub>LIML</sub>	Steady state over-current limitation level		2.5	3.5	4.5	A
I <sub>HYS</sub>	Steady state output Current limitation hysteresis		-	0.3	-	A
I <sub>LIML-OFF</sub>	Steady state over-current limitation deactivation threshold		-	I <sub>LIML</sub> - I <sub>HYS</sub>	-	A
<b>Overload with Single Level (Lowest) Protection: I<sub>PD</sub> pin connected to IN by 10 kΩ resistor; see Section 7.3.2</b>						
I <sub>PKL</sub>	Steady state over-current activation threshold	V <sub>CC</sub> = 24 V	-	8.0	-	A
I <sub>LIML</sub>	Steady state over-current limitation level		2.5	3.5	4.5	A
I <sub>HYS</sub>	Steady state output Current limitation hysteresis		-	0.3	-	A
I <sub>LIML-OFF</sub>	Steady state over-current limitation deactivation threshold		-	I <sub>LIML</sub> -I <sub>HYS</sub>	-	A
<b>Overload with Single Level (Highest) Protection: I<sub>PD</sub> pin connected to GND by 10 kΩ resistor; see Section 7.3.3</b>						
I <sub>PKH</sub>	Initial over-current activation threshold	V <sub>CC</sub> = 24 V	-	15.4	-	A
I <sub>LIMH</sub>	Initial over-current limitation level		6.25	9.0	11.75	A

**Table 10. IPS1025H-32/HQ-32 Overload protections**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Overload with Dual Threshold Protection: I<sub>PD</sub> pin to GND by C<sub>PD</sub> (470 pF ≤ C<sub>PD</sub> ≤ 470 nF); see Section 7.3.1</b>						
I <sub>PKH</sub>	Initial over-current activation threshold	V <sub>CC</sub> = 24 V	-	25.1	-	A
I <sub>LIMH</sub>	Initial over-current limitation level		12.5	17.9	23.2	A
D <sub>PK</sub>	Time limit of Initial over-current		-	215*C <sub>PD</sub> [nF]	-	μs
I <sub>PKL</sub>	Steady state over-current activation threshold		-	13.1	-	A
I <sub>LIML</sub>	Steady state over-current limitation level		5.7	8.0	10.4	A
I <sub>HYS</sub>	Steady state output Current limitation hysteresis		-	0.3	-	A
I <sub>LIML-OFF</sub>	Steady state over-current limitation deactivation threshold		-	I <sub>LIML</sub> - I <sub>HYS</sub>	-	A
<b>Overload with Single Level (Lowest) Protection: I<sub>PD</sub> pin connected to IN by 10 kΩ resistor; see Section 7.3.2</b>						
I <sub>PKL</sub>	Steady state over-current activation threshold	V <sub>CC</sub> = 24 V	-	13.1	-	A
I <sub>LIML</sub>	Steady state over-current limitation level		5.7	8.0	10.4	A
I <sub>HYS</sub>	Steady state output Current limitation hysteresis		-	0.3	-	A
I <sub>LIML-OFF</sub>	Steady state over-current limitation deactivation threshold		-	I <sub>LIML</sub> -I <sub>HYS</sub>	-	A
<b>Overload with Single Level (Highest) Protection: I<sub>PD</sub> pin connected to GND by 10 kΩ resistor; see Section 7.3.3</b>						
I <sub>PKH</sub>	Initial over-current activation threshold	V <sub>CC</sub> = 24 V	-	25.1	-	A
I <sub>LIMH</sub>	Initial over-current limitation level		12.5	17.9	23.2	A



**Figure 4. High (left) and Low (right)  $I_{LOAD}$  control activation thresholds ( $I_{PK}$ ) and limitation levels ( $I_{LIM}$ )**

**Table 11. Other protections**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Over-temperature protections</b>						
$T_{JSD}$	Junction temperature shutdown	-	150	170	190	°C
$T_{JR}$	Junction temperature reset	-	-	150	-	°C
$T_{JHYS}$	Junction temperature hysteresis	-	-	20	-	°C
$T_{CSD}$	Case temperature shutdown	-	-	130	-	°C
$T_{CR}$	Case temperature reset	-	-	110	-	°C
$T_{CHYS}$	Case temperature hysteresis	-	-	20	-	°C
<b>Ground disconnection/Wire break</b>						
$I_{LGND}$	GND disconnection output current	$V_{INX} = V_{CC} = 24\text{ V}$ , $V_{OUT} = 0\text{ V}$	-	-	0.5	mA
<b>V<sub>CC</sub> over-voltage</b>						
$V_{CLAMP}$	V <sub>CC</sub> Clamp Voltage	$I_{CC} \leq 10\text{ mA}$	65.5	70.0	73.5	V
<b>Demagnetization of inductive load</b>						
$V_{DEMAG}$	Demagnetization Voltage	$I_{OUT} = 0.5\text{ A}$ , Load $\geq 10\text{ mH}$	$V_{CC}-76$	$V_{CC}-72.5$	$V_{CC}-68$	V

## 6 Output Logic

**Table 12. Output stage truth table**

(L = pin voltage Low, H = pin voltage High, X = not determined)

Condition	IN	OUT	FLT1	FLT2
Normal Operation	L H	L H	L L	L L
Overload protection	L H	L X <sup>(1)</sup>	L L	L H
Junction over-temperature protection (see <a href="#">Over-temperature</a> )	L H	L L	L H	L L
Case over-temperature protection (see <a href="#">Over-temperature</a> )	L H	L L	L H	L L
UVLO	L H	L L	X X	X X

1. Pin voltage =  $I_{OUT} * R_{LOAD}$

**Figure 5. Typical application diagram with opto-couplers**

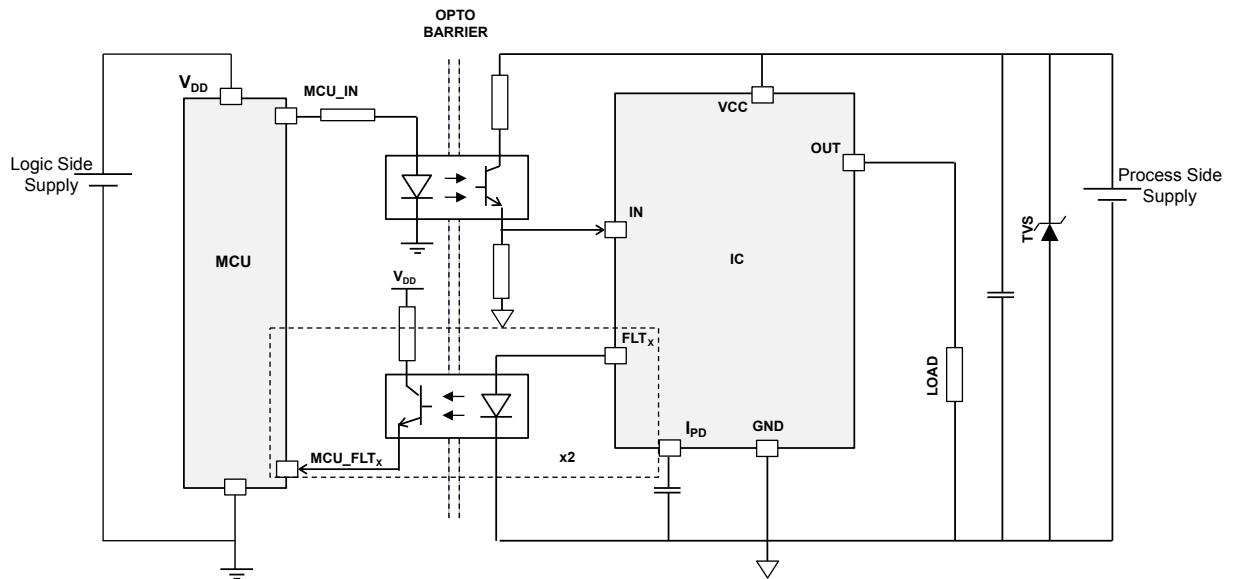
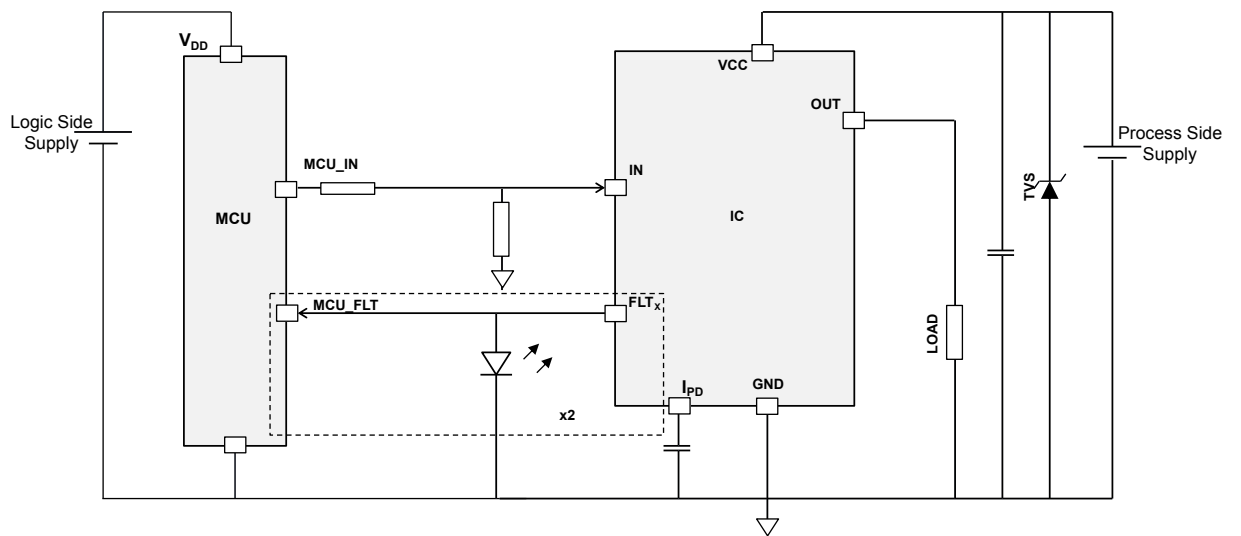


Figure 6. Typical application diagram without opto-couplers



## 7 Protections and diagnostic

The IC integrates several protections to help the design of robust applications.

### 7.1 Under-voltage lock-out

The IC is turned off if the voltage on  $V_{CC}$  pin falls below the turn-off threshold ( $V_{UVOFF}$ ). Normal operation restarts after  $V_{CC}$  exceeds the turn-on threshold ( $V_{UVON}$ ). Turn-on and turn-off thresholds are defined in [Table 4](#).

### 7.2 Over-temperature

The device is protected against overheating in case of overload conditions. During the driving period (when the MCU is forcing the IN pin high), if the output is overloaded, the device suffers two different thermal stresses: one related to the junction temperature of each output channel, and the other related to the whole case temperature. The two thermal faults (Thermal Junction and Thermal Case) have different trigger thresholds:  $T_{JSD}$  and  $T_{CSD}$ , respectively.

Usually, in thermal stress conditions due to overload, the junction thermal shutdown is the first protection that is activated: the output channel (OUT) is turned off when its junction temperature ( $T_J$ ) is higher than the activation threshold ( $T_{JSD}$ ) and turned back on when it falls below the reset threshold ( $T_{JR}$ ). This behavior continues while overload on the output persists. When the thermal protection is active, the  $FLT_1$  (current source) becomes active accordingly.

If the thermal protection is active and the temperature of the case ( $T_C$ ) increases over the case protection threshold ( $T_{CSD}$ ), then the thermal case protection is activated and the output is switched off until the junction temperature and case temperature fall below their respective reset thresholds ( $T_{CR}$  and  $T_{JR}$ ). The  $FLT_1$  pin is active even when thermal case events occur.

[Figure 7](#) shows the thermal protection behavior, while [Figure 8](#) shows typical temperature trends and output vs. input state.

Figure 7. Thermal protection flowchart

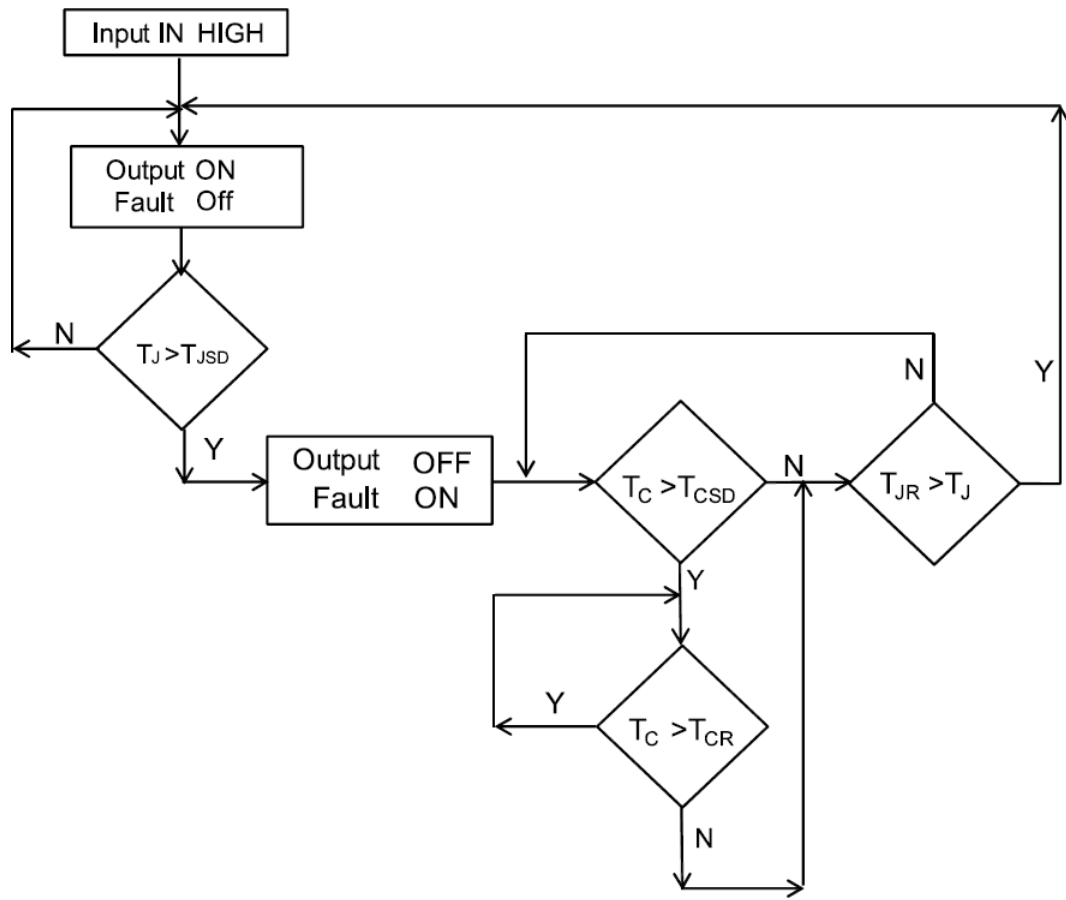
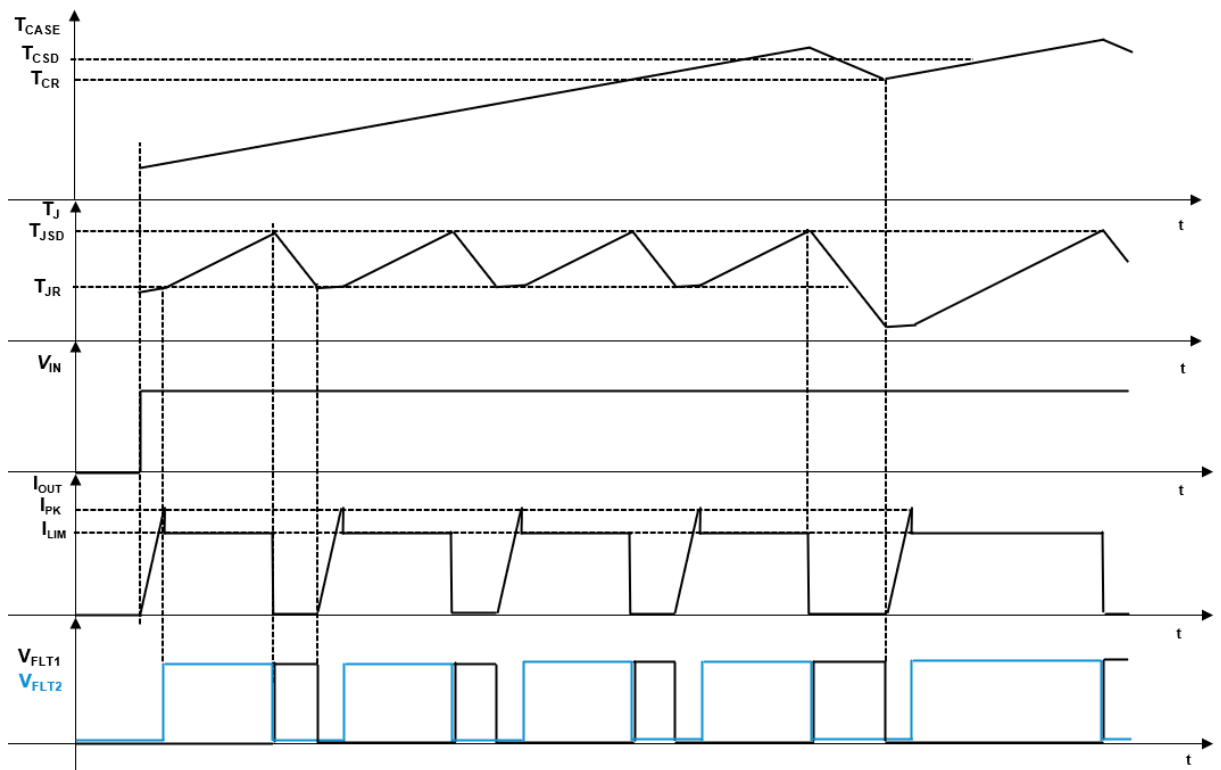


Figure 8. Thermal protection plot



## 7.3 Overload

The IC integrates an overload protection circuit consisting of an output current sensing section and an output current limitation section.

When the output channel is ON, the sensing circuitry monitors the current supplied to the load: if the activation threshold ( $I_{PK}$ ) is triggered, then the current limitation control circuitry is activated to limit output current to the current limitation level ( $I_{LIM}$ ) and  $FLT_2$  pin is activated until the overload condition is removed.

See the following sections for details and [Table 9](#) / [Table 10](#) for specific activation thresholds and limitation levels.

Note that while the output channel operates below its activation threshold, the power dissipation can be calculated by  $R_{ON} * I_{OUT}^2$ , but when the current limitation circuit is activated, power dissipation increases and can be calculated by  $V_{DS} * I_{OUT}$ , where  $V_{DS}$  is the voltage drop between the OUT and  $V_{CC}$  pins of the IC. In order to protect the IC against thermal stress, the over-temperature protection is always active and retains the highest priority.

### 7.3.1 Overload protection with dual threshold

This case is activated when the pin  $I_{PD}$  is connected to GND by a capacitor ( $C_{PD}$ ) and the IC works with two activation thresholds  $I_{PKH}$  and  $I_{PKL}$ .

The  $I_{PKH}$  is active only in the limited time frame between the L-H transition of the IN signal and the  $D_{PK}$  delay defined by the following design rule:

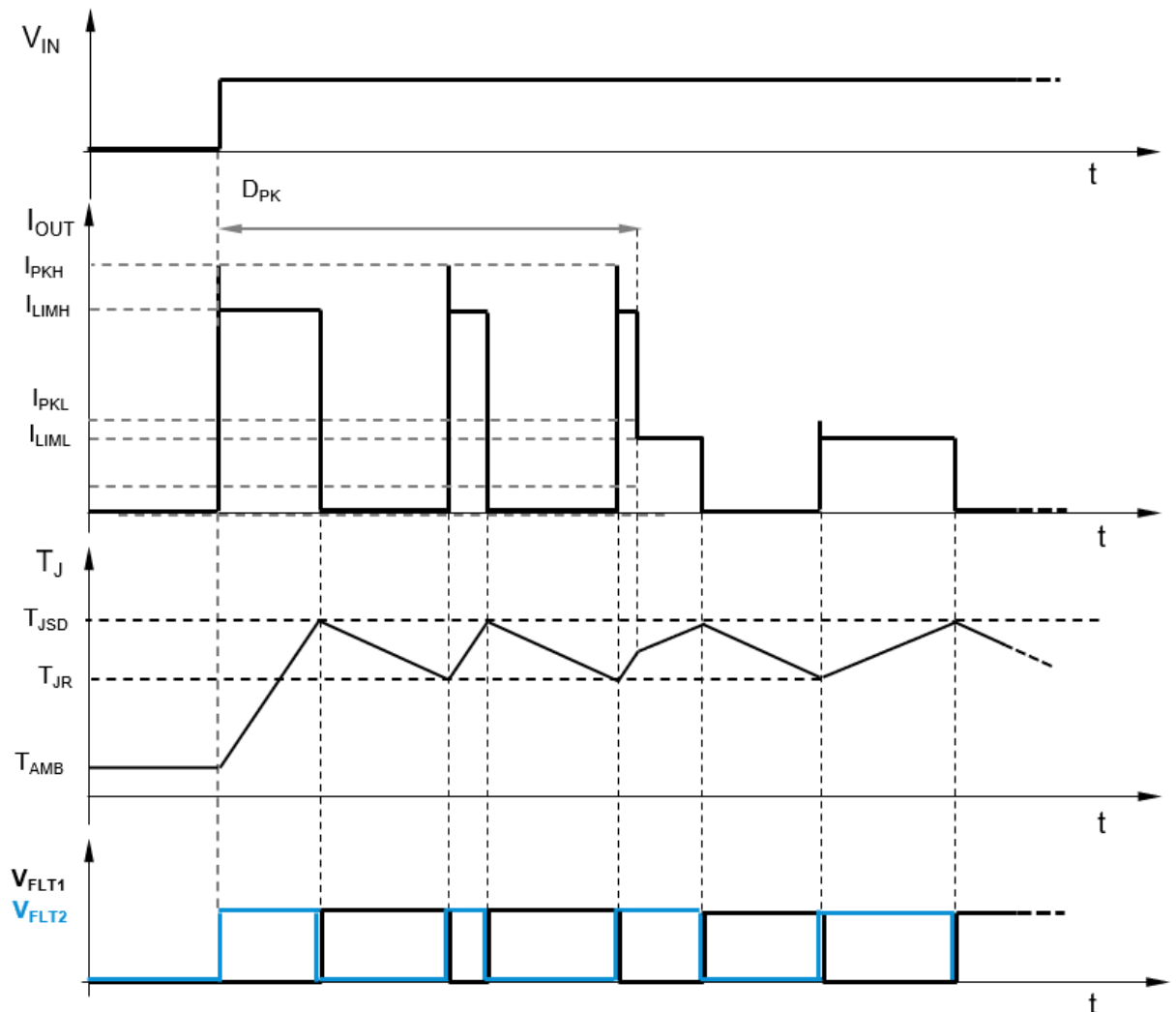
$$D_{PK} [\mu s] = 215 \times C_{PD} [nF]$$

The above design rule is valid in the range  $470 \text{ pF} \leq C_{PD} \leq 470 \text{ nF}$  (see [Table 9](#) / [Table 10](#)).

If the  $I_{PKH}$  is triggered within the  $D_{PK}$  time frame, then the output current is limited to  $I_{LIMH}$ .

After  $D_{PK}$  has elapsed, the IC operates with  $I_{PKL}$  activation threshold and  $I_{LIML}$  limitation level, respectively.

Figure 9. Short-circuit behavior with dual threshold ( $T_{CASE} < T_{CSD}$ )



### 7.3.2 Overload protection with single (low) threshold

The user can set the activation threshold to  $I_{PKL}$  and the limitation level to  $I_{LIML}$  by connecting the  $I_{PD}$  pin to the IN pin with a 220 K $\Omega$  resistor.

This condition is equivalent to setting  $D_{PK} = 0 \mu s$ .

*Note:* Leaving  $I_{PD}$  floating is equivalent to having an initial peak duration of 1  $\mu s$ .

### 7.3.3 Overload protection with single (high) threshold

The user can set the activation threshold to  $I_{PKH}$  and the limitation level to  $I_{LIMH}$  by connecting the  $I_{PD}$  pin to GND with a 10 K $\Omega$  resistor.

## 7.4 V<sub>CC</sub> disconnection protection

V<sub>CC</sub> disconnection involves the disconnection of the module from the supply line. When this condition is detected, the output channel can be driven normally until the voltage on V<sub>CC</sub> pin remains higher than the UVLO threshold.

In case of inductive load, if the V<sub>CC</sub> is disconnected while the channel is active, the energy stored in the inductance is discharged through the power switch thanks to the integrated demagnetization circuit.

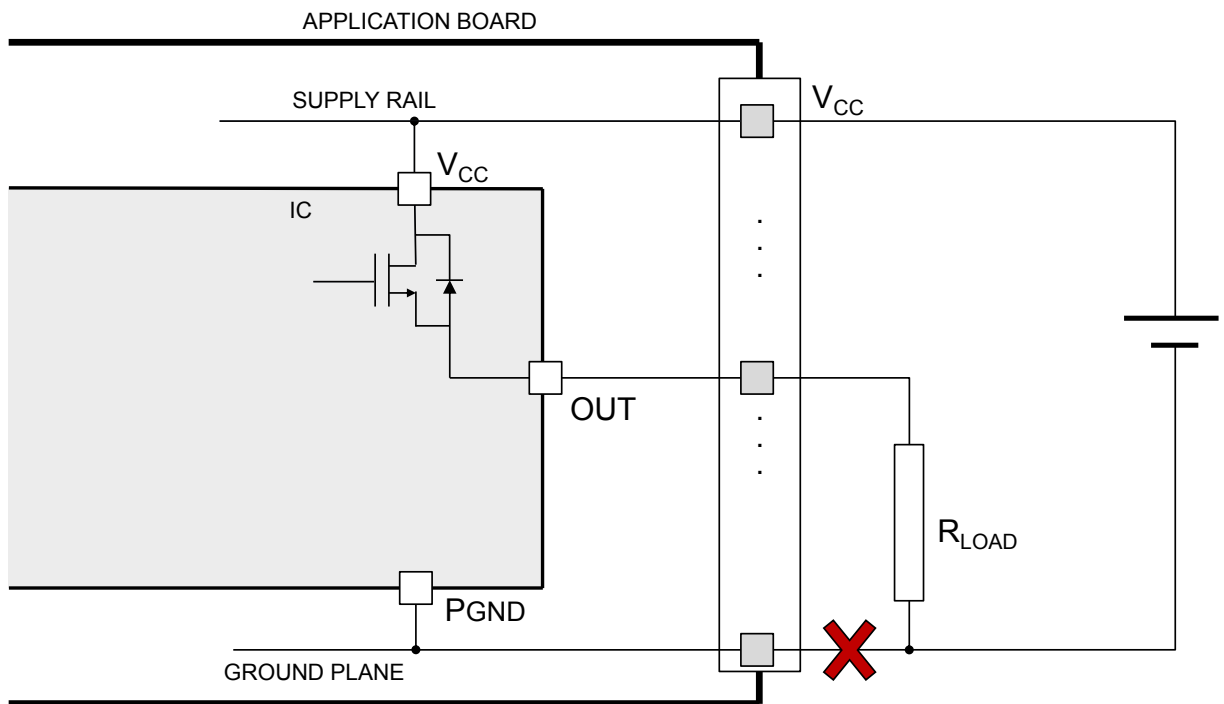
### 7.5 GND disconnection protection

GND disconnection is the disconnection of the module from the reference line. When this condition occurs, the output channel is turned off regardless of the input status.

When this event occurs, the IC continues working normally until the voltage between  $V_{CC}$  and GND pins of the IC results  $\geq V_{UVOFF}$ . The voltage on the GND pin of the IC rises up to the supply rail voltage level. In case of a GND disconnection event, a current ( $I_{LGND}$ ) flows through OUT pin.

For an inductive load, if the GND is disconnected while the output channel is active, the current flows through the power, which is activated by an active clamp as if the input had been deactivated.

Figure 10. Ground disconnection



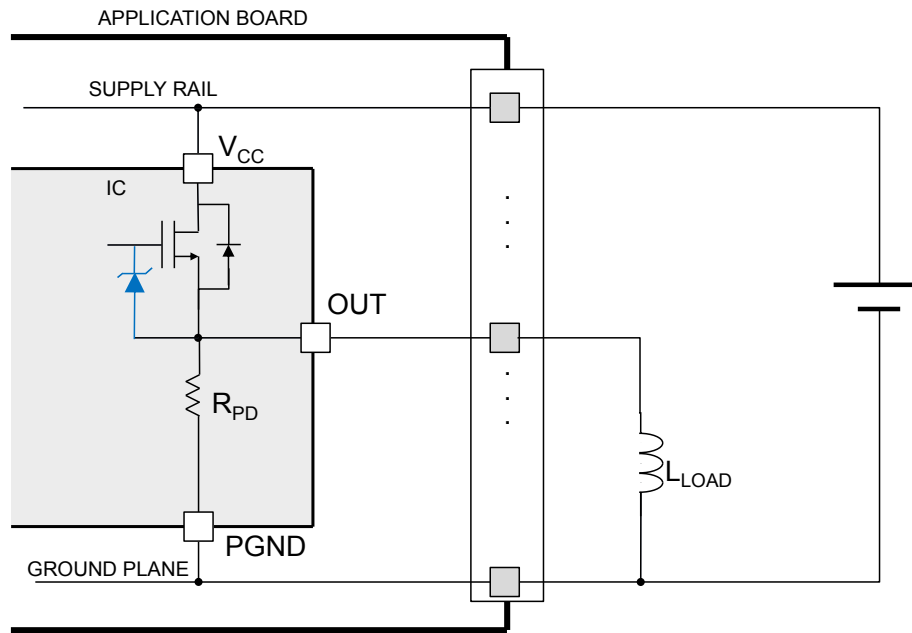


## 8 Active clamp

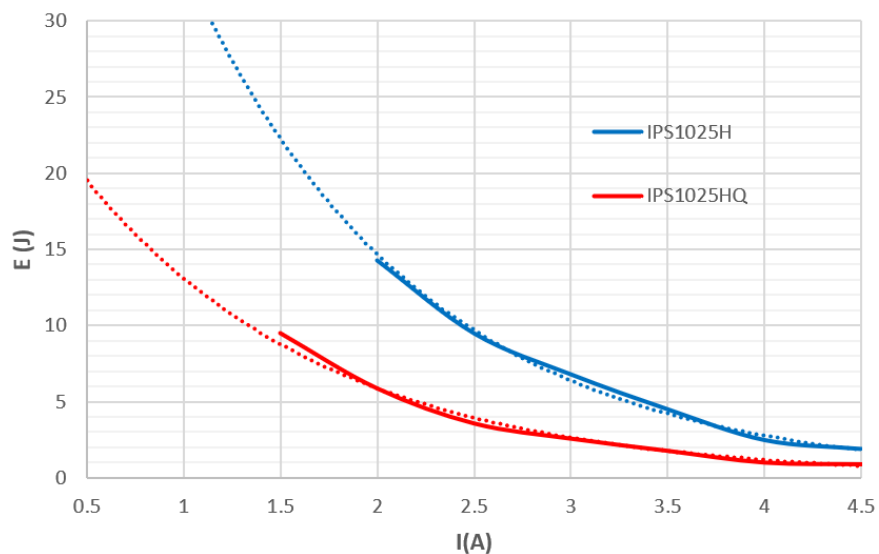
Active clamp is also known as Fast Demagnetization of inductive loads or Fast Current Decay. When a high-side driver turns off an inductance, an under-voltage on output is detected.

The OUT pin is pulled-down to  $V_{CC} - V_{DEMAG}$ . The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at  $\sim V_{DEMAG}$  until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

**Figure 11. Active clamp equivalent principle schematic**



**Figure 12. Typical demagnetization energy (single pulse) at  $V_{CC} = 24\text{ V}$  and  $T_{AMB} = 125\text{ }^{\circ}\text{C}$**



## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 Package mechanical data

Figure 13. PowerSSO-24 package dimensions [mm]

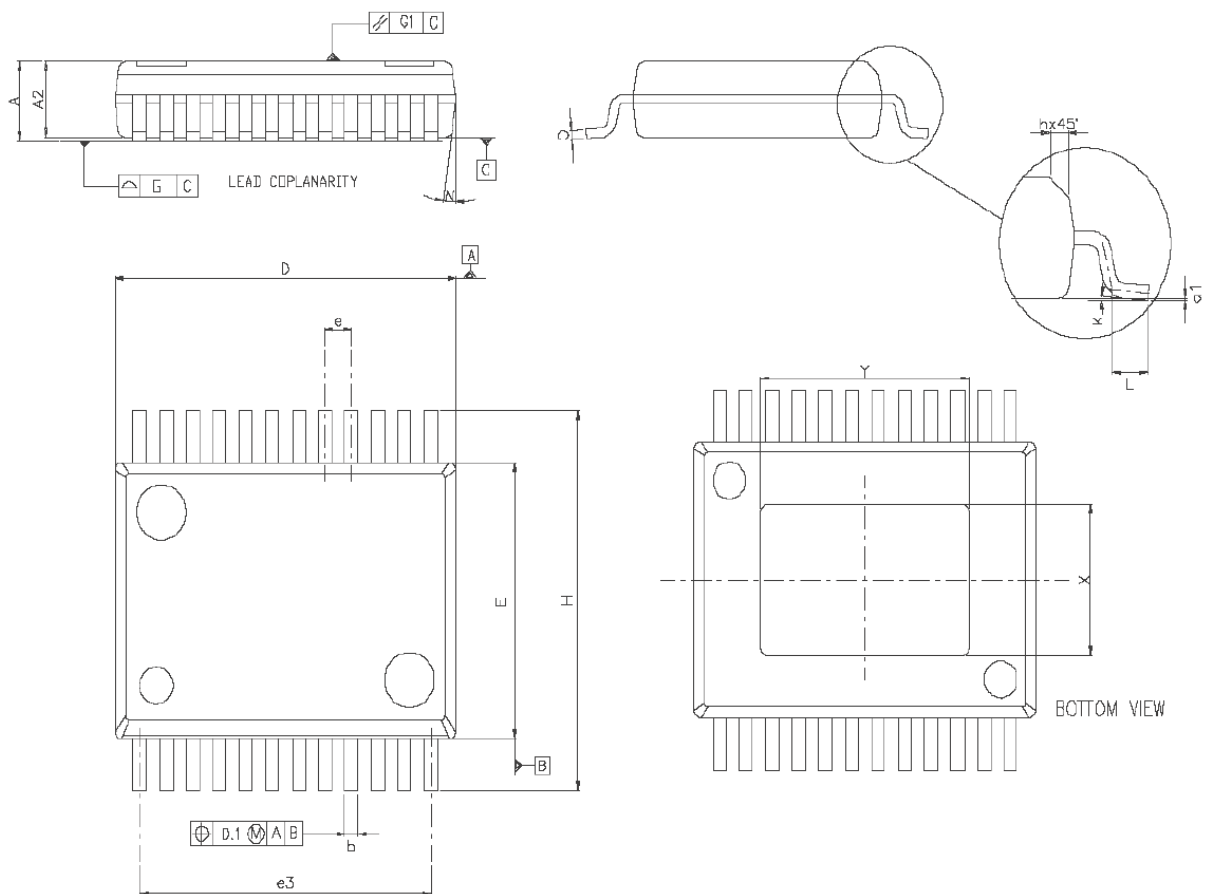


Table 13. PowerSSO-24 mechanical data

Dim.	[mm]		
	Min.	Nom.	Max.
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.33	-	0.51
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6



Figure 15. QFN48L package dimensions [mm]

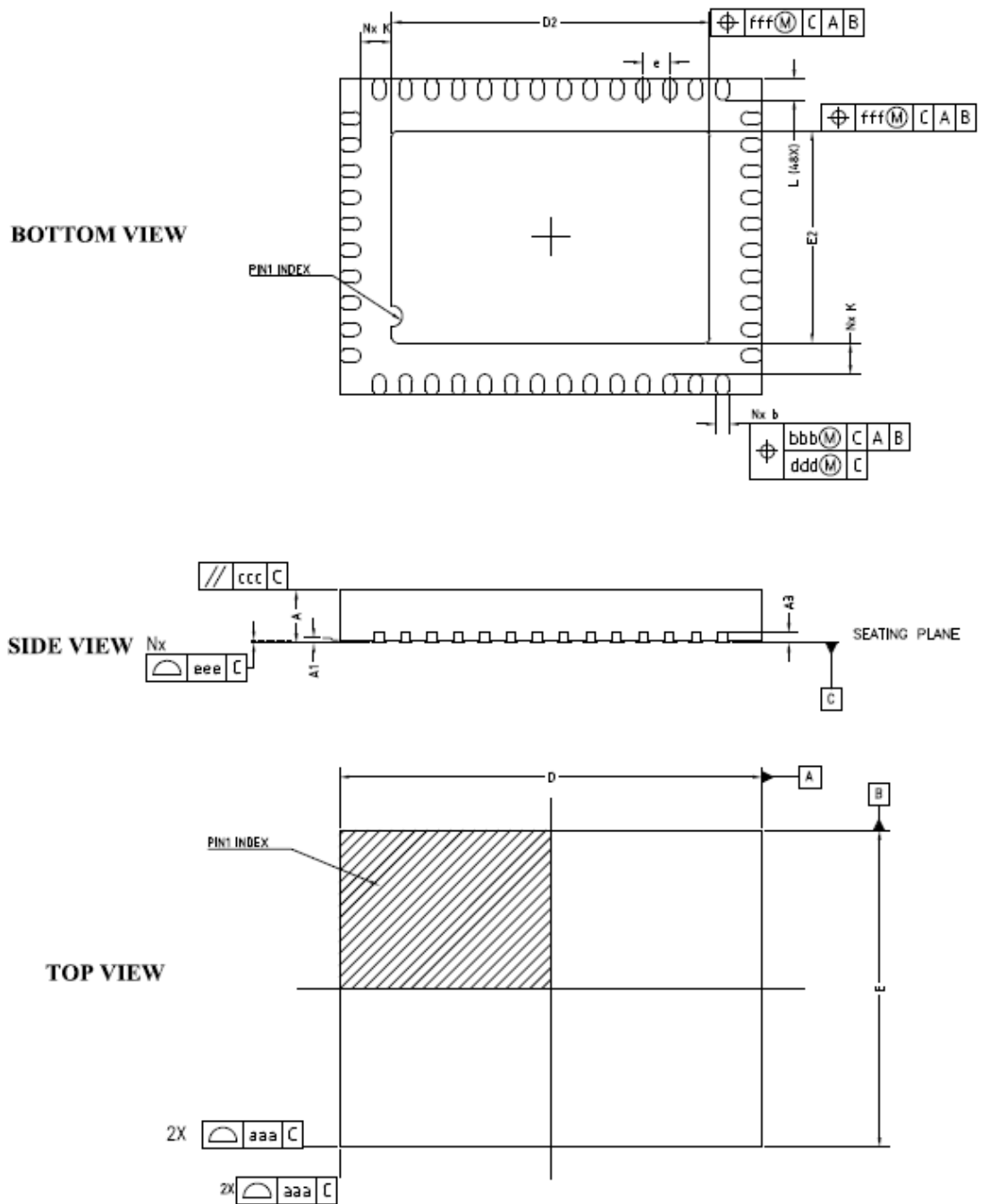


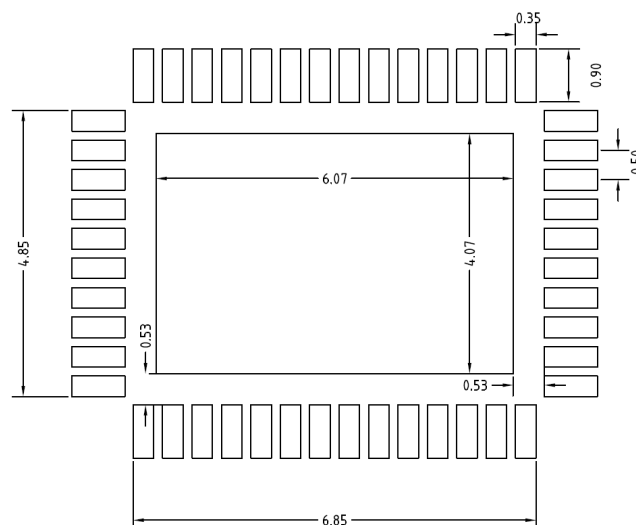
Table 14. QFN48L mechanical data

Dim.	[mm]		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.20	0.25	0.30
D	8.00 BSC		
e	0.50 BSC		
E	6.00 BSC		
D2	5.97	6.02	6.07
E2	3.97	4.02	4.07
L	0.365	0.40	0.435
k	0.53	-	-
N	48		

Table 15. Tolerance of forms and positions

Dim.	Tolerance of forms and positions
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Figure 16. QFN48L suggested footprint [mm]



## 10 Packing information

### 10.1 Packing mechanical data

Figure 17. PowerSSO-24 tube shipment (no suffix)

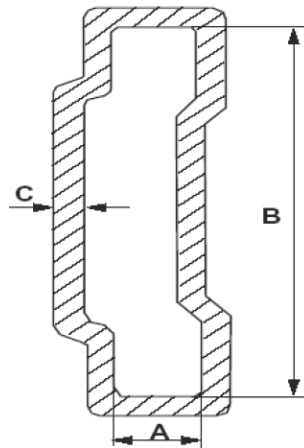


Table 16. PowerSSO-24 tube shipment information

All dimensions are in mm

Description	Value
Base quantity	49
Bulk quantity	1225
Tube length ( $\pm 0.5$ )	532
A	3.5
B	13.8
C ( $\pm 0.1$ )	0.6

Figure 18. PowerSSO-24 reel shipment

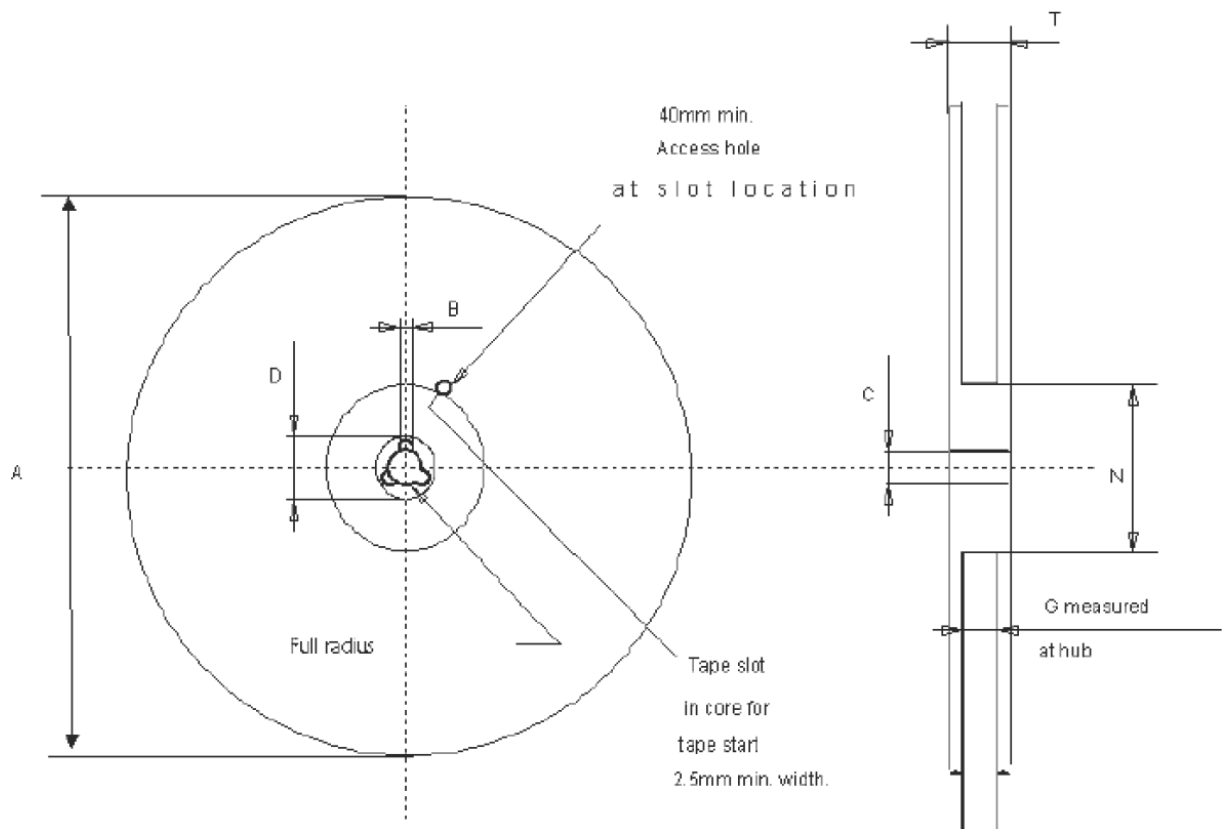


Table 17. PowerSSO-24 reel information

All dimensions are in mm

Description	Value
Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C (±0.2)	13
F	20.2
G (2 ±0)	24.4
N (min.)	100
T (max.)	30.4

Figure 19. PowerSSO-24 tape drawings

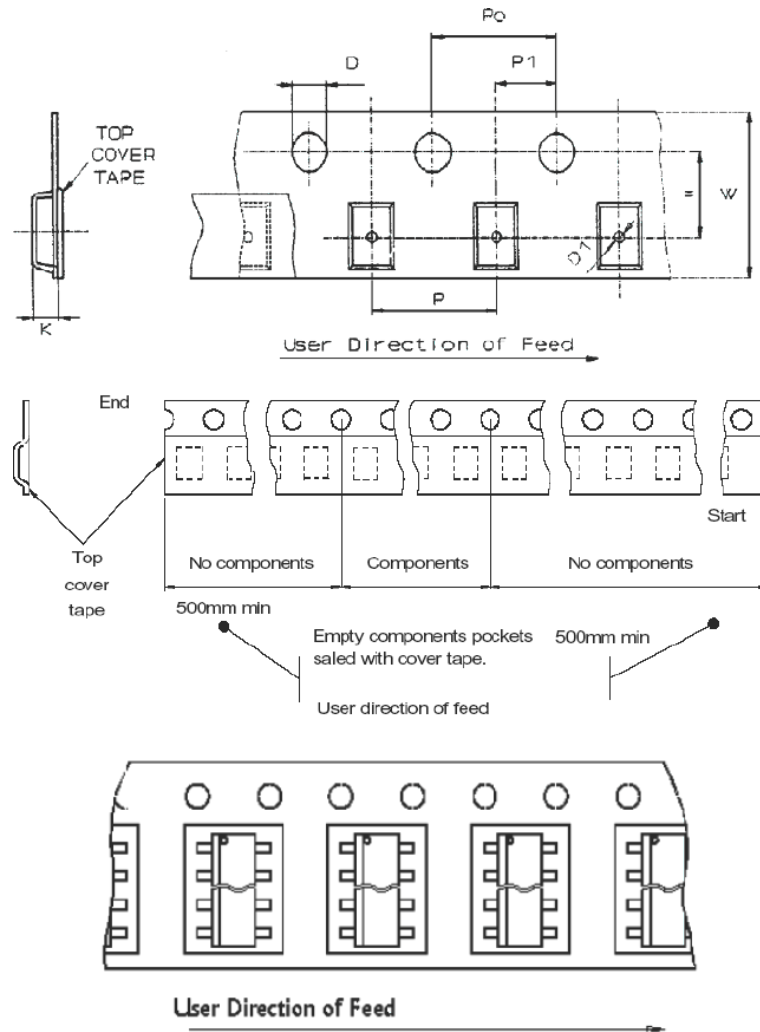


Table 18. PowerSSO-24 tape dimension

All dimensions are in mm

Description	Symbol	Value
Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to the Electronic Industries Association (EIA) standard 481 rev. A, Feb 1986.



Figure 20. QFN48L reel shipment reference

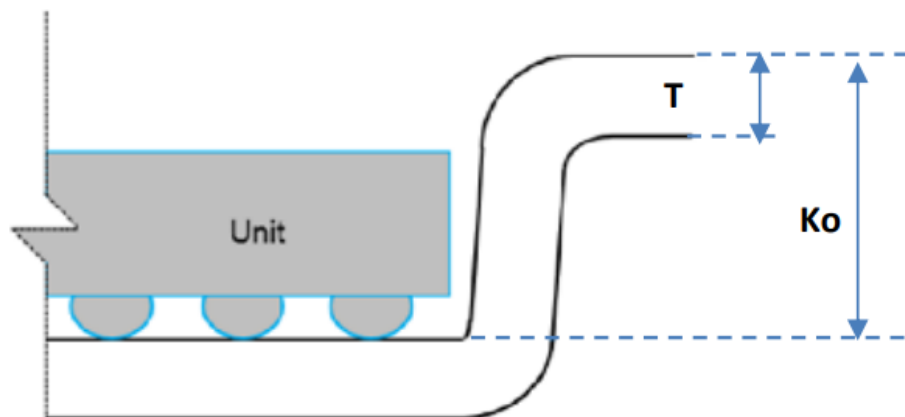
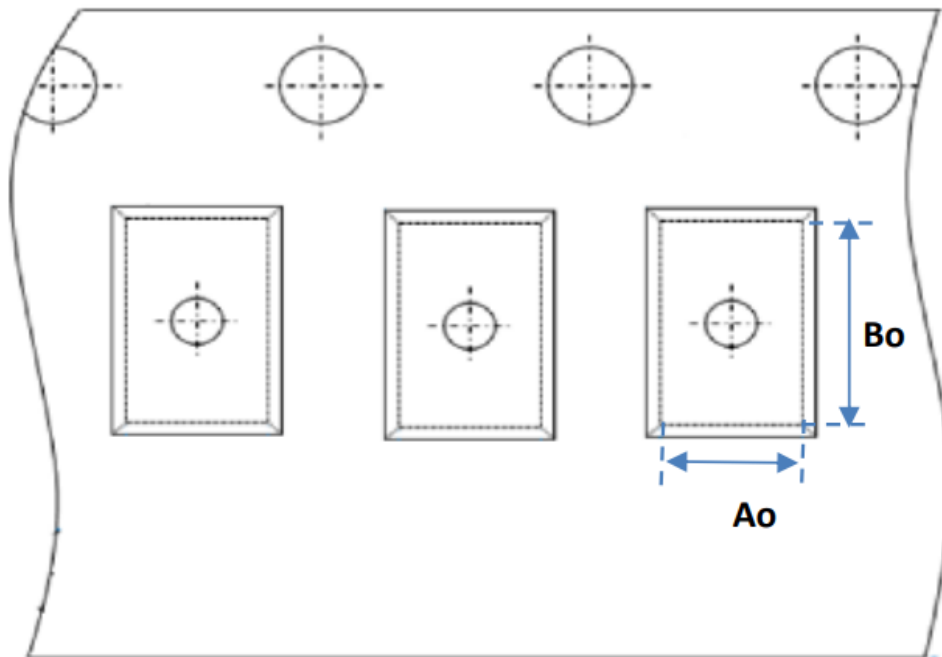


Table 19. Standard SPC parameters

Item	Description
Ao	Pocket Length
Bo	Pocket Width
Ko	Pocket Depth
T	Tape Thickness

Figure 21. QFN48L carrier tape dimensions

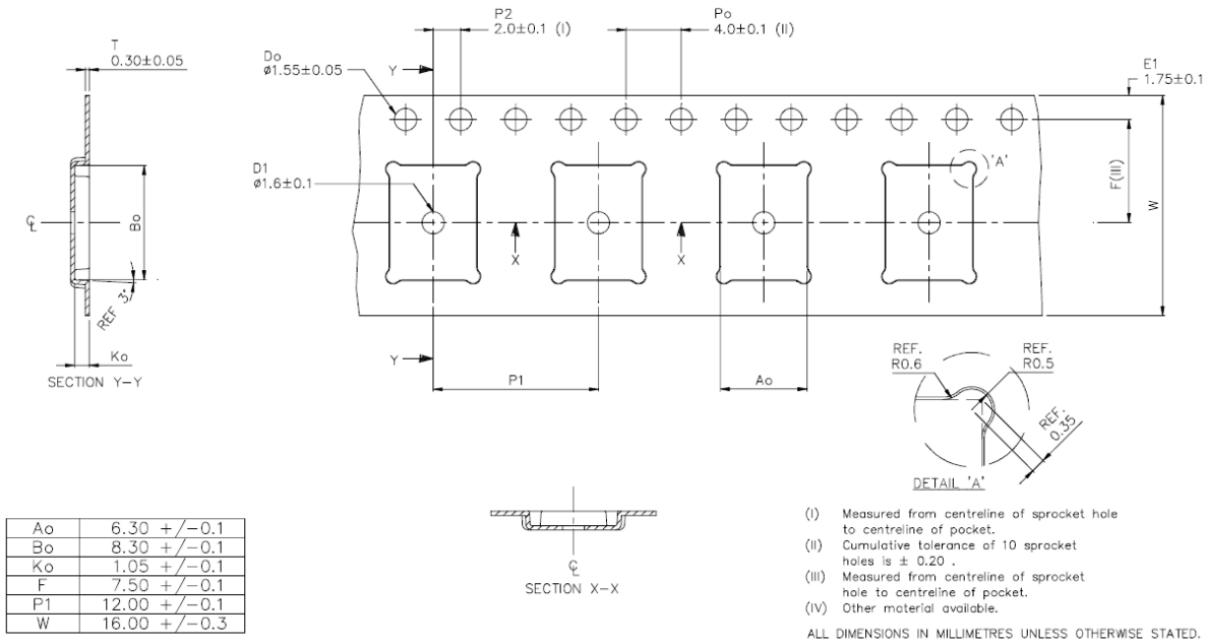
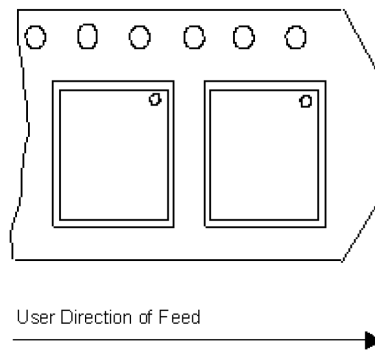


Figure 22. QFN48L carrier tape, Pin 1 indication



## 11 Ordering information

**Table 20. Ordering information**

Part number	Package	Packaging
IPS1025H	PowerSSO-24	Tube
IPS1025HTR		Tape and reel
IPS1025H-32		Tube
IPS1025HTR-32		Tape and reel
IPS1025HQ	QFN48L 8x6x0.9 mm	Tape and reel
IPS1025HQ-32		

## Revision history

**Table 21. Document revision history**

Date	Version	Changes
15-Nov-2021	1	Initial release.
28-Mar-2022	2	Table 9: specified only typical values for IPKH and IPKL; table 10: added column for FLT <sub>2</sub> behavior ; changed fig.12; some minor changes.
01-Aug-2022	3	Add QFN data: fig.2, 12, 15, 16, 20, 21, 22; tables 1, 2, 3, 14, 15, 19, 20. Divided table 9 in tables 9, 10, 11. Some minor changes.

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