

IR2308(S) & (PbF)

HALF-BRIDGE DRIVER

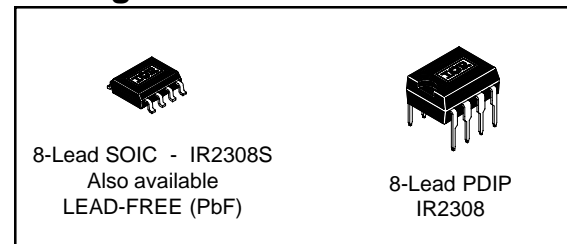
Features

- Floating channel designed for bootstrap operation
 Fully operational to +600V
 Tolerant to negative transient voltage
 dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time
- Lower di/dt gate driver for better noise immunity
- Also available LEAD_FREE

Description

The IR2308(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

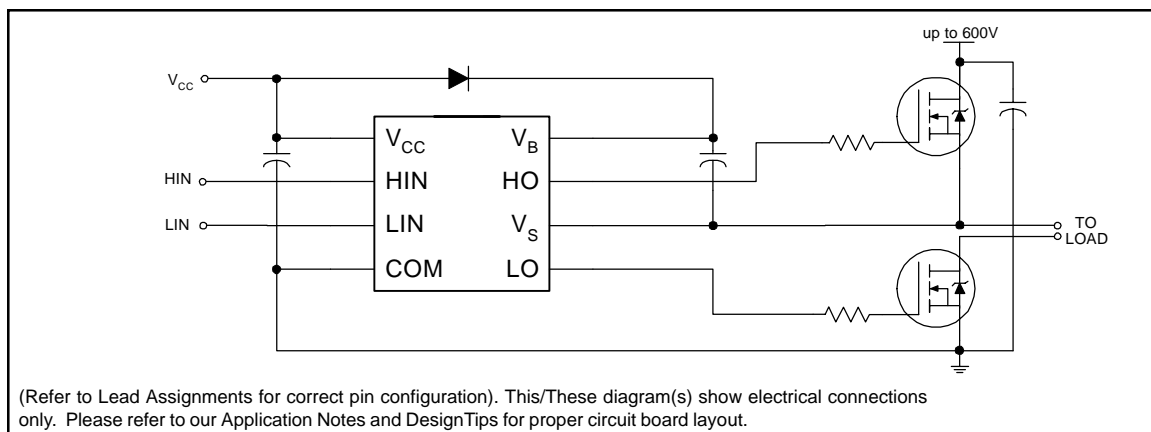
Packages



2106//2108//2109/2304/2308 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/LIN	yes	Internal 540ns Programmable 0.54-5 μs	COM
21084				VSS/COM
2109	IN/SD	yes	Internal 540ns Programmable 0.54-5 μs	COM
21094				VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM
2308	HIN/LIN	yes	Internal 540ns	COM

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V _B	High side floating absolute voltage	-0.3	625	V	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN)	V _{SS} - 0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	—	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R _{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T _J	Junction temperature	—	150	°C	
T _S	Storage temperature	-50	150		
T _L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply absolute voltage	V _S + 10	V _S + 20	V
V _S	High side floating supply offset voltage	Note 1	600	
V _{HO}	High side floating output voltage	V _S	V _B	
V _{CC}	Low side and logic fixed supply voltage	10	20	
V _{LO}	Low side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage	COM	V _{CC}	
T _A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to -V_{BS}. (Please refer to the Design Tin DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or $600V$
MT	Delay matching $ t_{on} - t_{off} $	—	0	46		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DT _{LO-HO}) & HO turn-off to LO turn-on (DT _{HO-LO})	400	540	680		
MDT	Deadtime matching = $ DT_{LO-HO} - DT_{HO-LO} $	—	0	60		

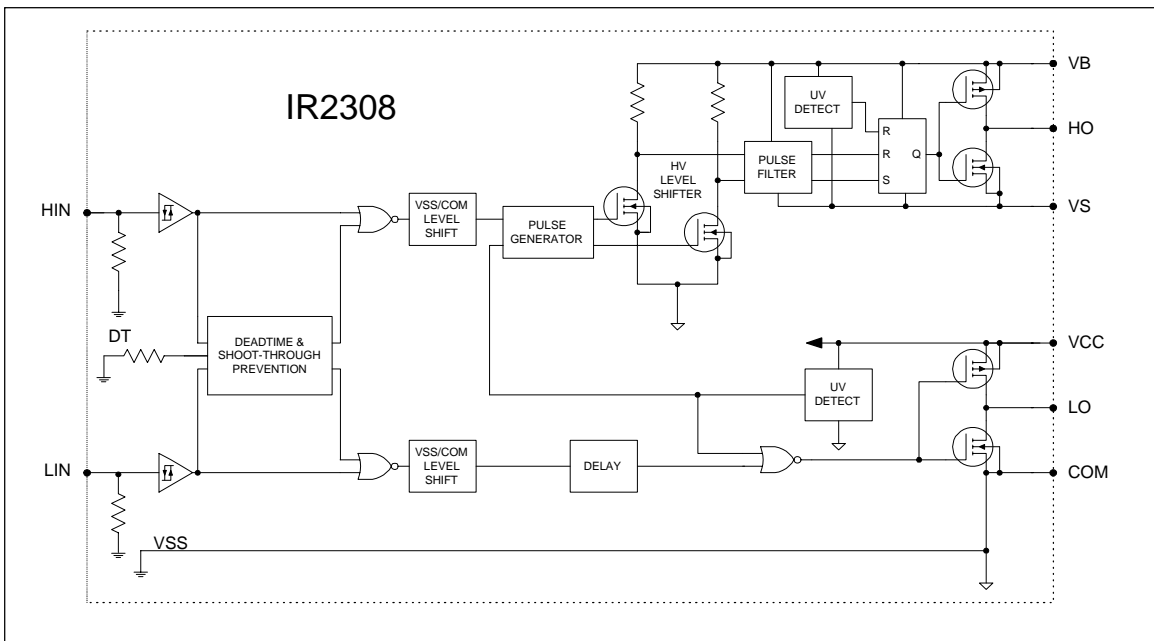
Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, DT = V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL} , V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and LIN. The V_O , I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HIN & LIN	2.9	—	—	V	$V_{CC} = 10V$ to $20V$
V_{IL}	Logic "0" input voltage for HIN & LIN	—	—	0.8		$V_{CC} = 10V$ to $20V$
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
V_{OL}	Low level output voltage, V_O	—	0.3	0.6		$I_O = 20$ mA
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	20	60	150	μA	$V_{IN} = 0V$ or $5V$
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V$ or $5V$
I_{IN+}	Logic "1" input bias current	—	5	20	μA	HIN = 5V, LIN = 5V
I_{IN-}	Logic "0" input bias current	—	1	2		HIN = 0V, LIN = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	10	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	97	200	—	mA	$V_O = 0V$, PW ≤ 10 μs
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, PW ≤ 10 μs

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Functional Block Diagram



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V _B	High side floating supply
HO	High side gate driver output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate driver output
COM	Low side return

Lead Assignments

<p>8 Lead PDIP</p>	<p>8 Lead SOIC Also available LEAD-FREE(PbF)</p>
IR2308	IR2308S

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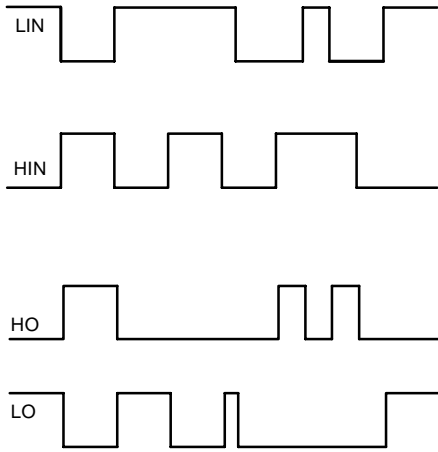


Figure 1. Input/Output Timing Diagram

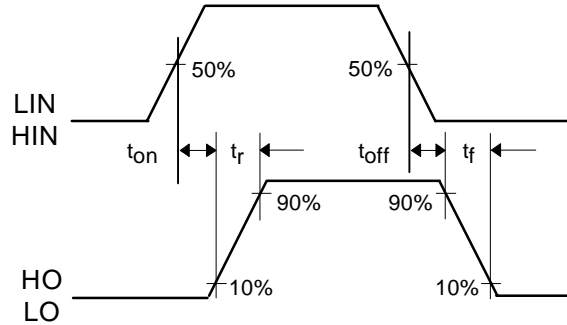


Figure 2. Switching Time Waveform Definitions

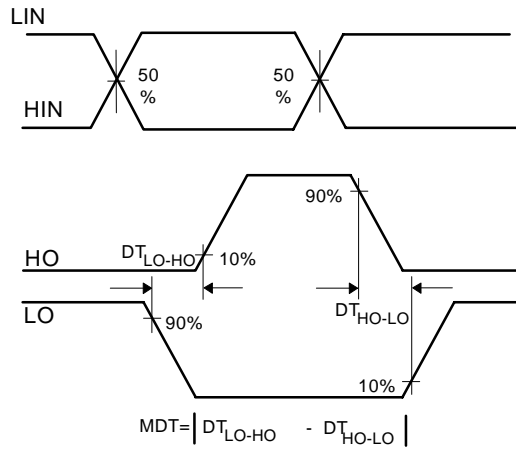


Figure 3. Deadtime Waveform Definitions

Case outlines

