2 Mb / 4 Mb Single Operating Voltage Serial Flash Memory With 104 MHz Dual or 100MHz Quad-Output SPI Bus Interface

PRELIMINARY DATASHET

FEATURES

• Single Power Supply Operation
- Low voltage range: 2.3 V - 3.6 V

• Memory Organization
- IS25LQ020: 256K x 8 (2 Mbit)
- IS25LQ040: 512K x 8 (4 Mbit)

• Cost Effective Sector/Block Architecture
- 2Mb / 4Mb : Uniform 4KByte sectors / sixteen uniform 64KByte blocks

• Serial Peripheral Interface (SPI) Compatible
- Supports single-, dual- or quad-output
- Supports SPI Modes 0 and 3
- Maximum 33 MHz clock rate for normal read
- Maximum 104 MHz clock rate for fast read
- Maximum 208MHz clock rate equivalent Dual SPI
- Maximum 400MHz clock rate equivalent Quad SPI

• Byte Program Operation
- Typical 10 us/Byte

• Page Program (up to 256 Bytes) Operation
- Maximum 0.7ms per page program

• Sector, Block or Chip Erase Operation
- Sector Erase (4KB)→150ms (Typ)
- Block Erase (64KB)→500ms (Typ)
- Chip Erase →0.5s (2Mb)
- Chip Erase → 1s (4Mb)

• Low Power Consumption
- Max 12 mA active read current
- Max 20 mA program/erase current
- Max 50 uA standby current

• Hardware Write Protection
- Protect and unprotect the device from write operation by Write Protect (WP#) Pin

• Software Write Protection
- The Block Protect (BP3, BP2, BP1, BP0) bits allow partial or entire memory to be configured as read-only

• High Product Endurance
- Guaranteed 100,000 program/erase cycles per single sector
- Minimum 20 years data retention

• Industrial Standard Pin-out and Package
- 8-pin SOIC 208mil
- 8-pin SOIC 150mil
- 8-pin VVSOP 150mil
- 8-pin WSON (5x6mm)
- 8-pin USON (2x3mm)
- KGD (Call Factory)
- Lead-free (Pb-free) package
- Automotive Temperature Ranges Available

•Additional 256-byte Security information one-time programmable (OTP) area
•Special protect function
- **Safe guard function (Appendix 1)**
- **Sector unlock function (Appendix**

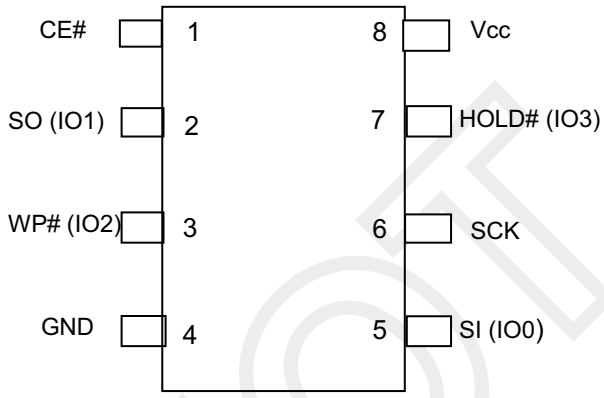
GENERAL DESCRIPTION

The IS25LQ020/040 is 2 Mbit / 4 Mbit Serial Peripheral Interface (SPI) Flash memories, providing single-, dual or quad-output. The devices are designed to support a 33 MHz fclock rate in normal read mode, and 104 MHz in fast read (Quad output is 100MHz), the fastest in the industry. The devices use a single low voltage power supply, ranging from 2.3 Volt to 3.6 Volt, to perform read, erase and program operations. The devices can be programmed in standard EPROM programmers.

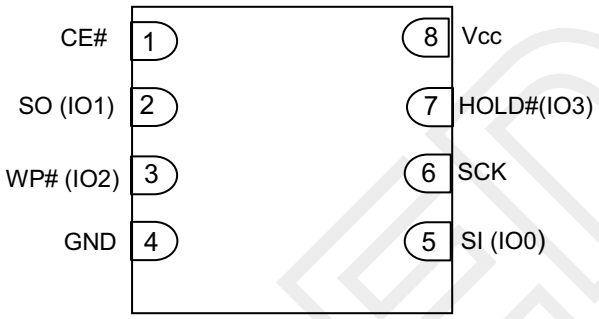
The IS25LQ020/040 are accessed through a 4-wire SPI Interface consisting of Serial Data Input/Output (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. The devices support page program mode, where 1 to 256 bytes data can be programmed into the memory in one program operation. These devices are divided into uniform 4 KByte sectors or uniform 64 KByte blocks.

The IS25LQ020/040 are offered in 8-pin SOIC 208mil, 8-pin VVSOP, 8-pin WSON and 8-pin USON.

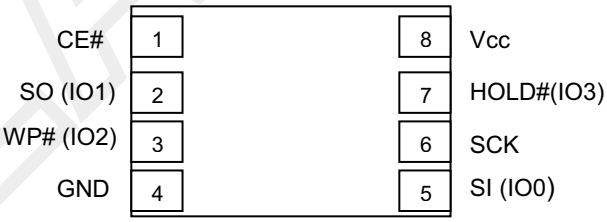
CONNECTION DIAGRAMS



8-Pin SOIC/VVSOP



8-Pin WSON



8-Pin USON

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Chip Enable: CE# low activates the devices internal circuitries for device operation. CE# high deselects the devices and switches into standby mode to reduce the power consumption. When a device is not selected, data will not be accepted via the serial input pin (SI), and the serial output pin (SO) will remain in a high impedance state.
SCK	INPUT	Serial Data Clock
SI (IO0)	INPUT/OUTPUT	Serial Data Input/Output
SO (IO1)	INPUT/OUTPUT	Serial Data Input/Output
GND		Ground
Vcc		Device Power Supply
WP# (IO2)	INPUT/OUTPUT	Write Protect/Serial Data Output: A hardware program/erase protection for all or part of a memory array. When the WP# pin is low, memory array write-protection depends on the setting of BP3, BP2, BP1 and BP0 bits in the Status Register. When the WP# is high, the status register are not write-protected. When the QE bit of is set "1", the /WP pin (Hardware Write Protect) function is not available since this pin is used for IO2
HOLD# (IO3)	INPUT/OUTPUT	Hold: Pause serial communication by the master device without resetting the serial sequence. When the QE bit of Status Register is set for "1", the function is Serial Data Input & Output (for 4xI/O read mode)