IS32LT3129A

TRIPLE CHANNEL LINEAR LED DRIVER WITH I2C INTERFACE AND FADE ON/OFF

February 2020

GENERAL DESCRIPTION

The IS32LT3129A is a programmable triple channel linear current regulator; two channels of up to 150mA each for LED lighting and a single channel of up to 30mA for illuminating switches. The device operates as a fully configurable theatrical dimming LED driver; External resistors will program the current levels as well as the LED fade ON/OFF ramp rate.

In additional, the I2C interface supports writing/reading function for MCU to select switch type (momentary contact or latched), individually configure the output current levels and fade on/off ramp rate, or get the state of device and the fault flag of open/short circuit and thermal shutdown.

An integrated debounce and latch circuit on the channel enable pin (EN1/2) is enabled when the device is configured for a momentary contact switch interface. The other option is to configure the EN pins to accept a static level signal for operation with latched switches. If configured for Internal-PWM-Dimming mode, the integrated PWM source will be triggered by an I2C command. This enables LED dimming without the need for an external PWM input. The I2C command input has a higher priority and will override EN inputs. See Figure 63~69 for the details.

The device integrates a 63 step fade ON/OFF algorithm (Gamma correction) which causes the output LED brightness to gradually ramp up to the full source value after the EN1/2 pins are triggered or send I2C commands (when configured for Internal-PWM-Dimming mode). The same controller causes the LED brightness to gradually ramp down to zero if the EN1/2 pins are triggered or send I2C commands (when configured for Internal-PWM-Dimming mode) while the output channel is ON. The fade ramp can be interrupted mid-cycle before completion of the ramp cycle.

The IS32LT3129A is targeted at the automotive market with end applications to include map and dome lighting as well as exterior accent lighting. For 12V automotive applications the low dropout driver can support 1 to 3 LEDs per channel. It is offered in a small thermally enhanced eTSSOP-20 package.

FEATURES

- Operating voltage range, 5V to 42V
- 1MHz I2C-compatible interface
- Dual channel current sources
  - Individual programmable current via a single external resistor and I2C
  - Configurable from 20mA to 150mA
- Single channel 30mA (Max.) current source for switch illumination
- EN input supports either momentary contact or latched switch
  - Input is debounced and latched
  - Lower priority than I2C input
  - Gamma corrected Fade ON/OFF algorithm
  - Pull down resistors or I2C set independent fade ON and OFF ramp time
- Selectable internal PWM source
  - Internal 220Hz PWM source with Gamma corrected algorithm for automatic dimming the current source
- Fault Protection:
  - Fault Reporting
    - ✓ LED strings short
    - ✓ LED strings open
    - ✓ Over temperature thermal shutdown
  - ISET pin shorted to GND
  - Over temperature current roll off
- Operating temperature range from -40°C ~ +125°C
- AEC-Q100 Qualified

APPLICATIONS

- Automotive Interior:
  - Map/Dome light
  - Puddle lamp in doors
  - Glove box light
  - Vanity mirror light

TYPICAL APPLICATION CIRCUIT

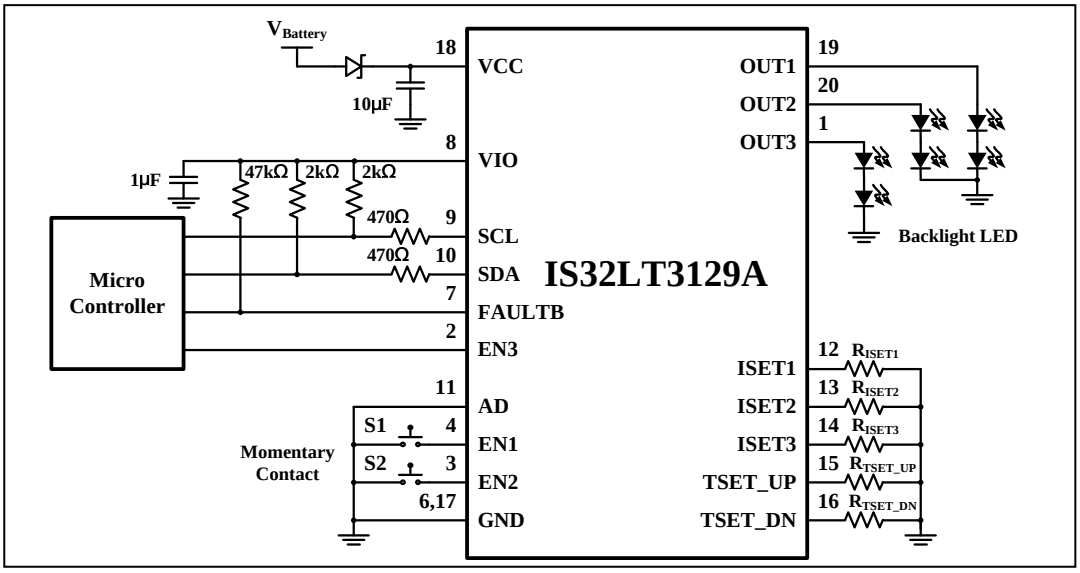


Figure 1 Typical Application Circuit with Momentary Contact Switch

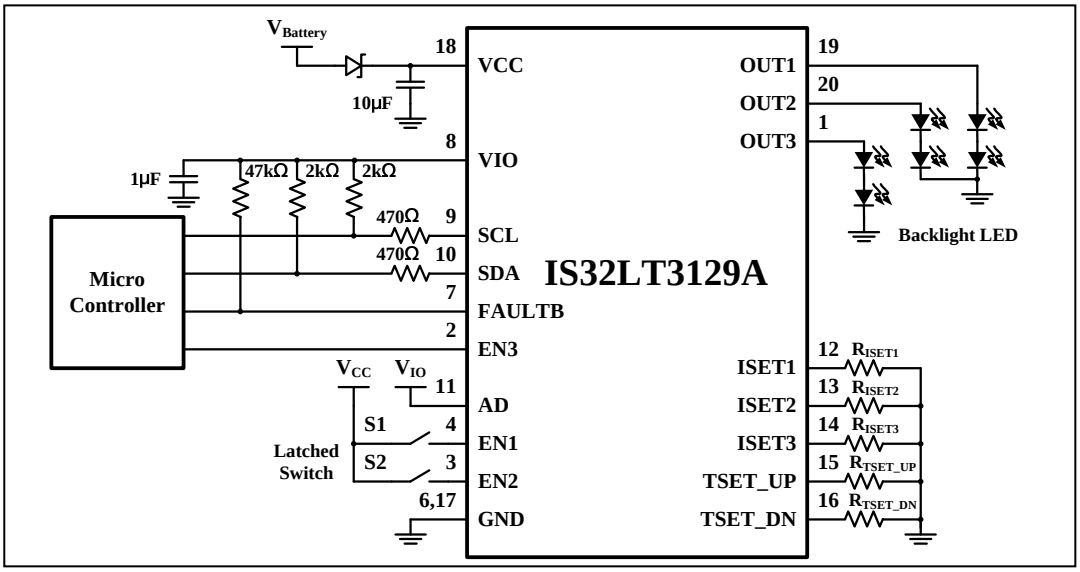
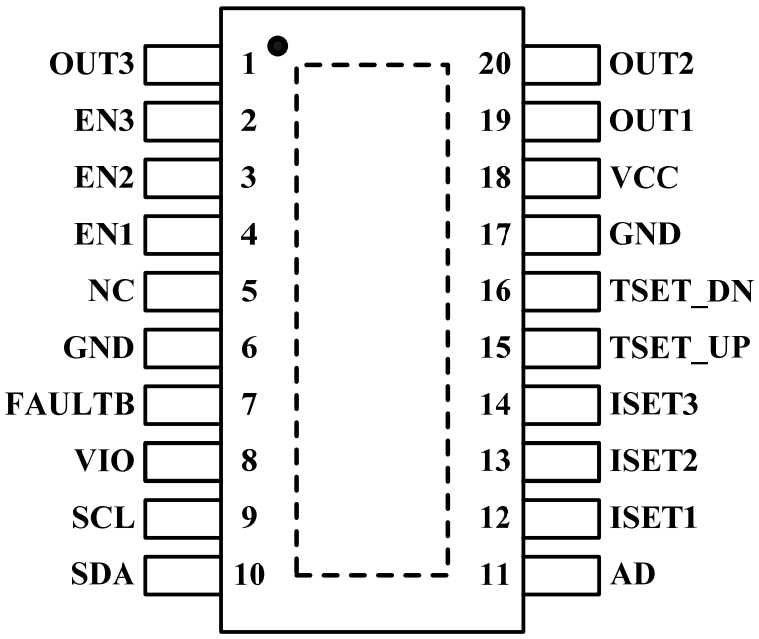


Figure 2 Typical Application Circuit with Latched Switch

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-20	

PIN DESCRIPTION

No.	Pin	Description
1	OUT3	Maximum 30mA output current source for switch backlight LEDs.
2	EN3	Internally deglitch input pin for control of OUT3 current. Pull high (>V_{IH}) to enable OUT3 current. Pull low (<V_{IL}) to disable OUT3 current.
3,4	EN2, EN1	Internally debounced input pin for control of OUT1/2 current. When configured for Low Pulse Mode: EN1/2 pins are internally pulled up to internal 4V LDO by 50kΩ resistors. A low going pulse on either of these two pins will toggle the state of the corresponding OUT1 or OUT2 current. When configured for Level Control Mode: EN1/2 pins are internally pulled down by a 50kΩ resistor to ground. A high level voltage applied to EN1 or EN2 will enable the corresponding OUT1 or OUT2 current while a ground signal will disable the OUT1 or OUT2 current.
5	NC	Not connect.
6,17	GND	Ground pins for the device.
7	FAULTB	Open drain fault reporting pin. Pull low to report LED strings short/open and thermal shutdown fault condition.
8	VIO	Internal LDO output pin for pulling up configuration.
9	SCL	I2C compatible serial clock.
10	SDA	I2C compatible serial data.
11	AD	I2C address setting.
12~14	ISET1~ISET3	Output current setting for OUT1/2/3. Connect a resistor between this pin and GND to set the maximum output current.
15	TSET_UP	Timing control for the Fade ON feature. Connect a resistor between this pin and GND to set the Fade ON time. Connect this pin directly to ground to disable the fade function for instant ON.
16	TSET_DN	Timing control for the Fade OFF feature. Connect a resistor between this pin and GND to set the Fade OFF time. Connect this pin directly to ground to disable the fade function for instant OFF.
18	VCC	Power supply input pin.
19,20	OUT1,OUT2	Maximum 150mA output current source channels.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3129A-ZLA3-TR	eTSSOP-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC, OUT1/2/3, EN1/2/3	-0.3V ~ +45V
VIO, SCL, SDA, AD, FAULTB, ISET1/2/3, TSET_UP, TSET_DN	-0.3V ~ +7.0V
Ambient operating temperature, T_A=T_J	-40°C ~ +150°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	34°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JESD 51-8), θ_{JP}	14.46°C/W
Maximum power dissipation, P_{DMAX}	2.94W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J= -40°C ~ +125°C, V_{CC}= 12V, refer to each condition description. Typical values are at T_J= 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range		5		42	V
V_{HR}	Minimum headroom voltage	V_{CC} -$V_{OUT1/2}$, $I_{OUT1/2}$= -150mA (Note 2)			900	mV
		V_{CC} -$V_{OUT1/2}$, $I_{OUT1/2}$= -100mA (Note 2)			700	
		V_{CC} -V_{OUT3}, I_{OUT3}= -30mA (Note 2)			900	
I_{CC}	Quiescent supply current	OUT1/2/3 output current are all disabled	0.1	0.31	1	mA
		R_{ISET1}= R_{ISET2} =R_{ISET3}= 15kΩ, OUT1/2/3 output current are all enabled by ENx, but OUT1/2/3 are all floating		5.5	6.6	mA
		V_{CC}= 4.2V, OUT1/2 output current are all are enabled by EN1/2 (only for EN Low Pulse Mode), EN3 floating		0.25		mA
t_{ON}	Startup time	V_{CC}> 6V to I_{OUT}< -5mA (Note 3)			400	μs
I_{OUT_LIM}	OUT1/2 limit current (Note 4)	V_{HR}= 2V, OUT1/2 sourcing current, $V_{ISET1/2}$= GND	-240	-205	-160	mA
	OUT3 limit current (Note 4)	V_{HR}= 2V, OUT3 sourcing current, V_{ISET3}= GND	-48	-40	-32	
I_{OUT}	OUT1/2 output current (Note 4)	$R_{ISET1/2}$= 15kΩ, V_{HR}= 1V, -40°C< T_J< +125°C	-105	-100	-95	mA
	OUT3 output current (Note 4)	R_{ISET3}= 15kΩ, V_{HR}= 1V, -40°C< T_J< +125°C	-22	-20	-18	
E_{OUT}	OUT1/2 absolute current accuracy (Note 4)	-50mA≤ $I_{OUT1/2}$≤ -20mA, V_{HR}= 1V, -40°C< T_J< +125°C	-8		8	%
		-150mA≤ $I_{OUT1/2}$< -50mA, V_{HR}= 1V, -40°C< T_J< +125°C	-6		6	%
E_{IOUTM}	OUT1/2 current matching in case of the same $R_{ISET1/2}$ value (Note 4,5)	$I_{OUT1/2}$= -100mA, V_{HR}= 1V, T_J= 25°C			4	%
		$I_{OUT1/2}$= -100mA, V_{HR}= 1V, -40°C< T_J< +125°C			6	%
t_{SL}	Current slew time	Current rise/fall between 0%~100%, V_{TSET}= GND	45	75	100	μs

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J= -40°C ~ +125°C, V_{CC}= 12V, the detail refer to each condition description. Typical values are at T_J= 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{INTPWM}	Internal PWM frequency			220		Hz
t_{SW}	Input pin debounce time (EN1/2 pins and I2C command latency in internal PWM mode)		25	37	50	ms
UVLO	Release from under voltage lock out V_{CC} voltage	V_{CC} rising release from UVLO	4.4	4.6	4.8	V
	Into under voltage lock out V_{CC} voltage	V_{CC} falling into UVLO	4.2	4.5	4.7	V
TSET_UP, TSET_DN and VIO						
V_{TSET}	Voltage reference of TSET_UP and TSET_DN			1		V
T_{ACC}	Fade timing accuracy	*Neglecting the R_{TSET} Tolerance* R_{TSET_UP}= 100kΩ, T_J= 25°C	-5		5	%
V_{IO}	VIO pin output voltage			4.3		V
Logic Input EN1/2/3						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
V_{IN_HY}	Input hysteresis	(Note 3)	150	350		mV
I_{PU}	EN1/2 internal pull-up current	EN_M bit= 1, $V_{EN1/2}$= GND		67		µA
I_{PD}	EN1/2 internal pull-down current	EN_M bit= 0, $V_{EN1/2}$= 12V		50		µA
	EN3 internal pull-down current	V_{EN3}= 12V		28		µA
Protection						
V_{SCD}	OUTx pins short detect voltage	Measured at OUTx, voltage falling	1.2		1.8	V
V_{SCD_HY}	OUTx pins short detect voltage hysteresis	(Note 3)		220		mV
V_{OCD}	OUTx pins open threshold	Measured at (V_{CC}-V_{OUTx}), voltage rising		200		mV
V_{OCD_HY}	OUTx pins open hysteresis	Measured at (V_{CC}-V_{OUTx}) (Note 3)		130		mV
t_{FD_OC}	Open fault detect persistence time	DELAY bits= 0001 (Default)		110		µs
t_{FD_SC}	Short fault detect persistence time			5		ms
V_{FAULTB}	FAULTB pin voltage	Sink current= 5mA		22	80	mV
T_{RO}	Thermal roll off threshold	(Note 3)		145		°C
T_{SD}	Thermal shutdown threshold	Temperature increasing (Note 3)		175		°C
T_{HY}	Thermal shutdown hysteresis	Recovery = T_{SD} - T_{HY} (Note 3)		30		°C

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J= -40°C ~ +125°C, V_{CC}= 12V, the detail refer to each condition description. Typical values are at T_J= 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I2C Logic Electrical Characteristics (SDA, SCL, AD)						
V_{IL}	Logic “0” input voltage	(Note 3)			0.8	V
V_{IH}	Logic “1” input voltage	(Note 3)	2			V
V_{HYS}	Input schmitt trigger hysteresis	(Note 3)	150	350		mV
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 3)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{IO} (Note 3)		5		nA

DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 3)

Symbol	Parameter	Fast Mode			Fast Mode Plus			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Serial-clock frequency	-		400	-		1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3		-	0.5		-	µs
$t_{HD, STA}$	Hold time (repeated) START condition	0.6		-	0.26		-	µs
$t_{SU, STA}$	Repeated START condition setup time	0.6		-	0.26		-	µs
$t_{SU, STO}$	STOP condition setup time	0.6		-	0.26		-	µs
$t_{HD, DAT}$	Data hold time	-		-	-		-	µs
$t_{SU, DAT}$	Data setup time	100		-	50		-	ns
t_{LOW}	SCL clock low period	1.3		-	0.5		-	µs
t_{HIGH}	SCL clock high period	0.7		-	0.26		-	µs
t_R	Rise time of both SDA and SCL signals, receiving	-		300	-		120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-		300	-		120	ns

Note 2: I_{OUT} output current in case of V_{CC}-V_{OUT}=V_{HR} called I_{OUT_VHR}. I_{OUT} output current in case of V_{CC}-V_{OUT}=2V called I_{OUT_VHR2V}, V_{HR} accuracy is computed as $|I_{OUT\_VHR}-I_{OUT\_VHR2V}|/I_{OUT\_VHR2V}<5\%$.

Note 3: Guaranteed by design.

Note 4: Output current accuracy is not intended to be guaranteed at output voltages less than 1.8V.

Note 5: OUT1/2 current matching is computed as $100\times[1 - 2\times I_{OUTx}/(I_{OUT1}+I_{OUT2})]$. Output current channel to channel match is computed as $100 \times [Max (|I_{OUTx}– I_{OUT(AV)}|) / I_{OUT(AV)}]$, where $I_{OUT(AV)}$ is the average current of all active outputs.

TYPICAL PERFORMANCE CHARACTERISTICS

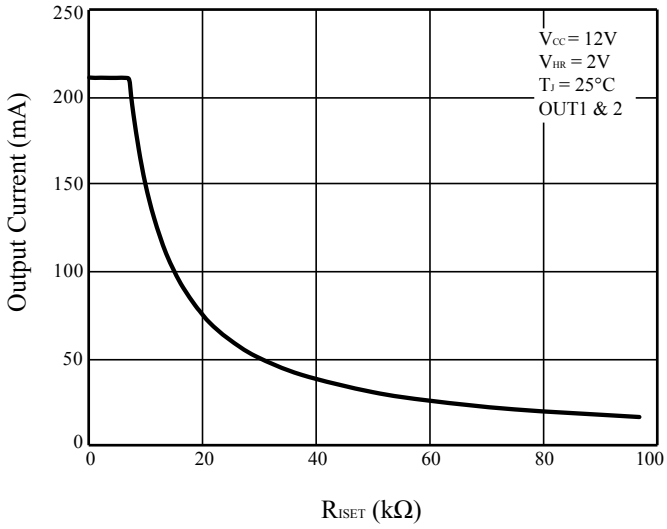


Figure 3 Output Current 1&2 vs. $R_{ISET1/2}$

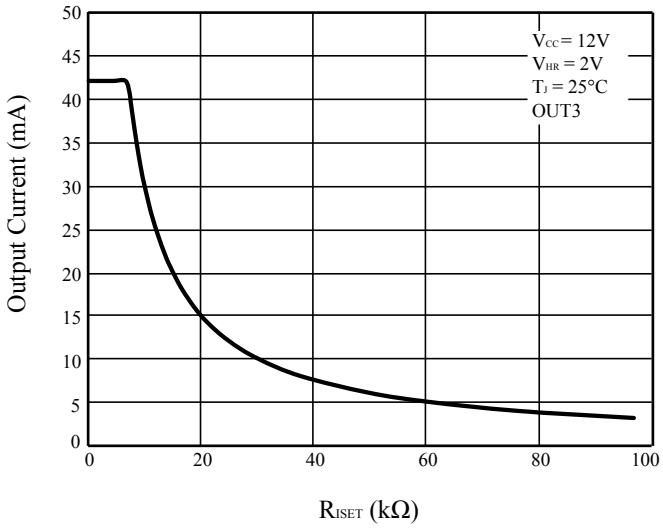


Figure 4 Output Current 3 vs. R_{ISET3}

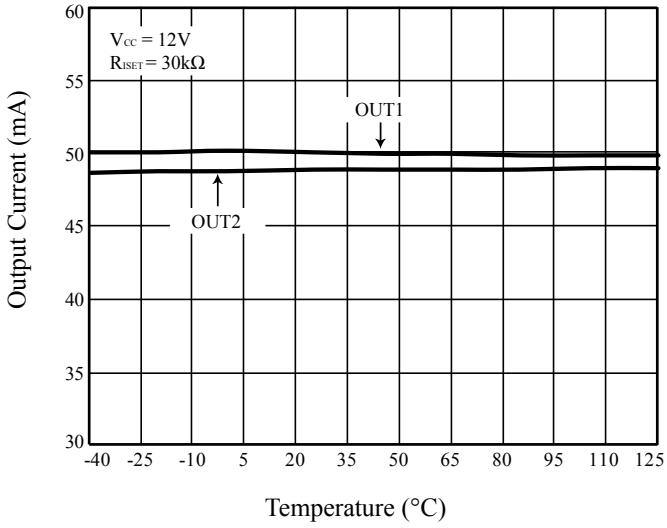


Figure 5 Output Current 1&2 vs. Temperature

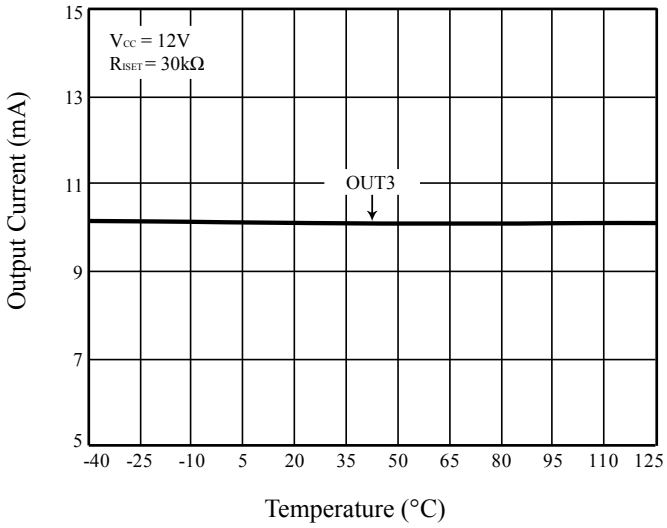


Figure 6 Output Current 3 vs. Temperature

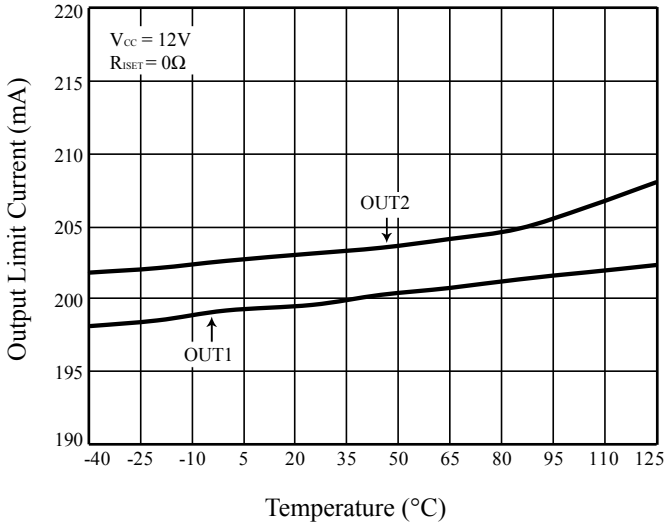


Figure 7 Output 1&2 Limit Current vs. Temperature

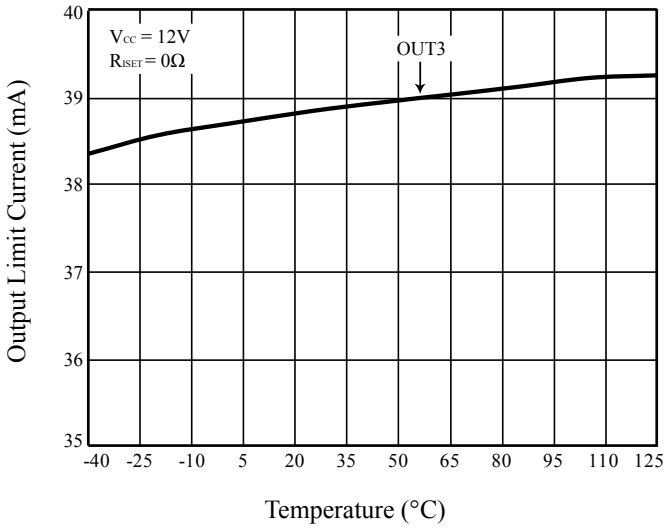


Figure 8 Output 3 Limit Current vs. Temperature

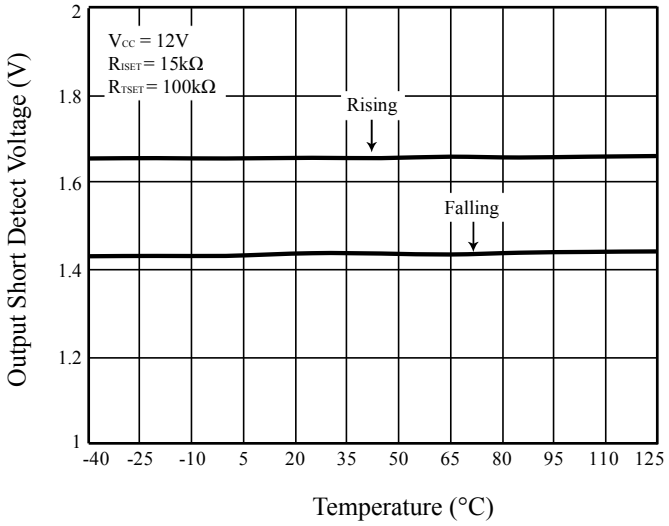


Figure 9 Output Short Detect Voltage vs. Temperature

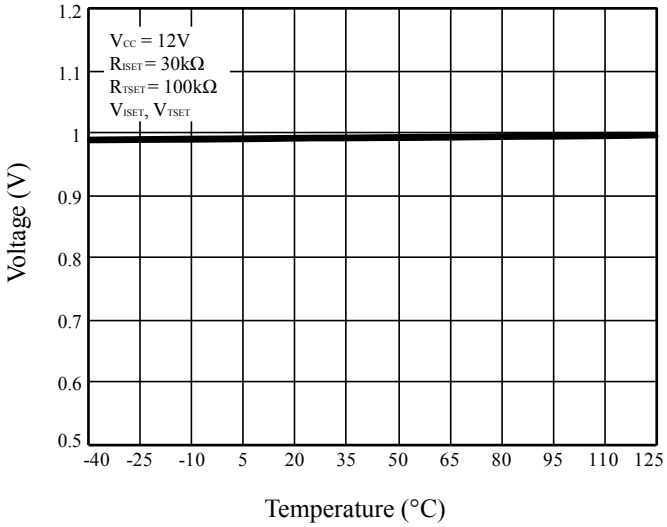


Figure 10 V_{ISET} & V_{TSET} vs. Temperature

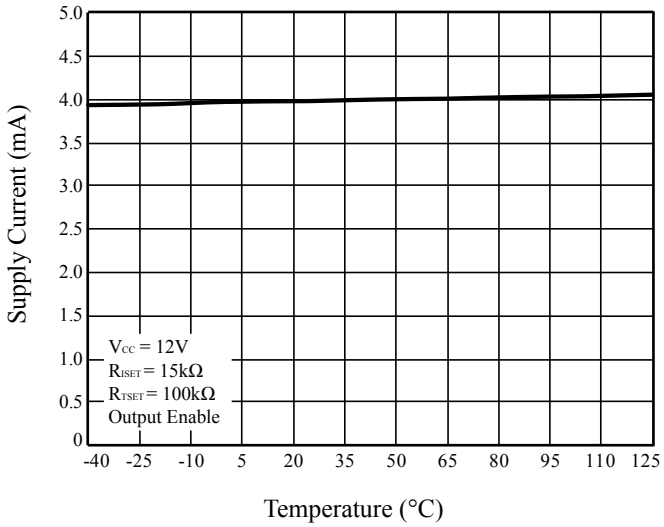


Figure 11 Supply Current vs. Temperature

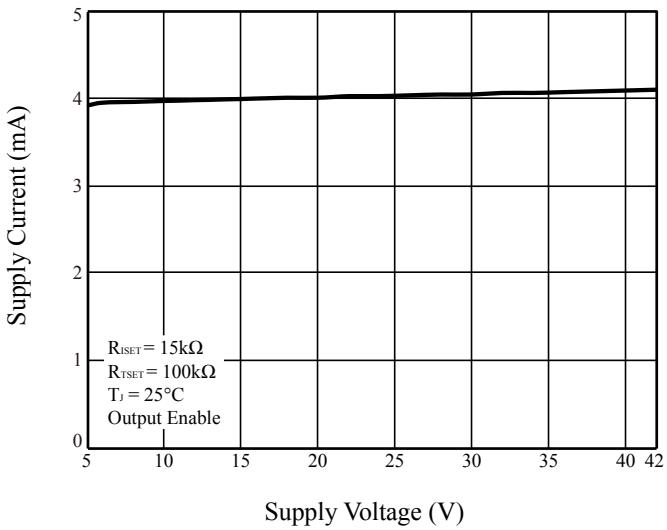


Figure 12 Supply Current vs. Supply Voltage

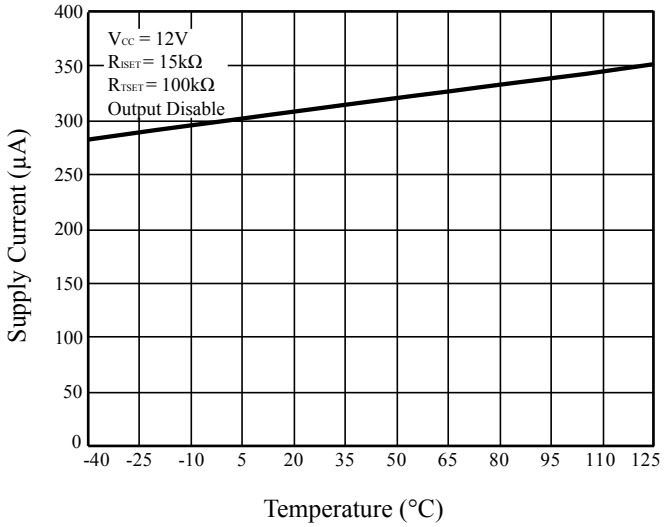


Figure 13 Supply Current vs. Temperature

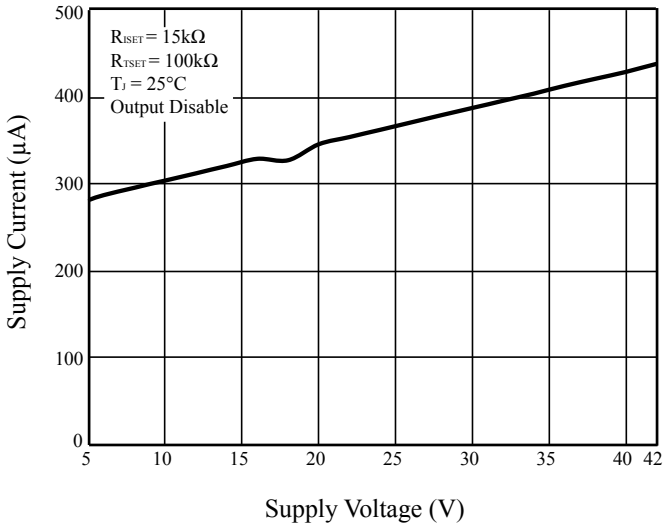


Figure 14 Supply Current vs. Supply Voltage

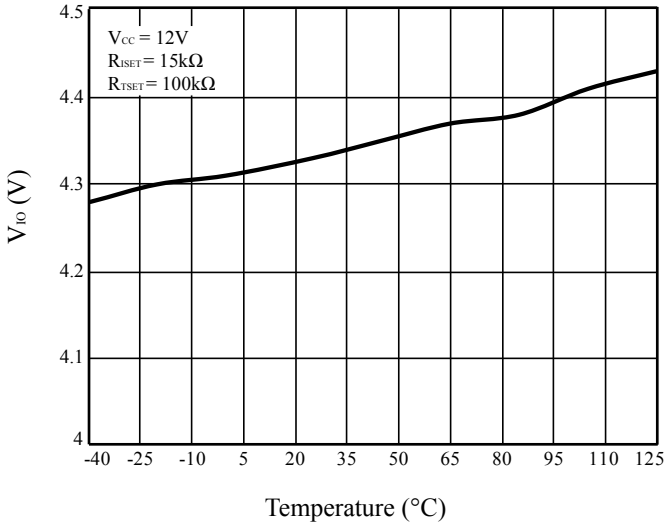


Figure 15 V_{IO} vs. Temperature

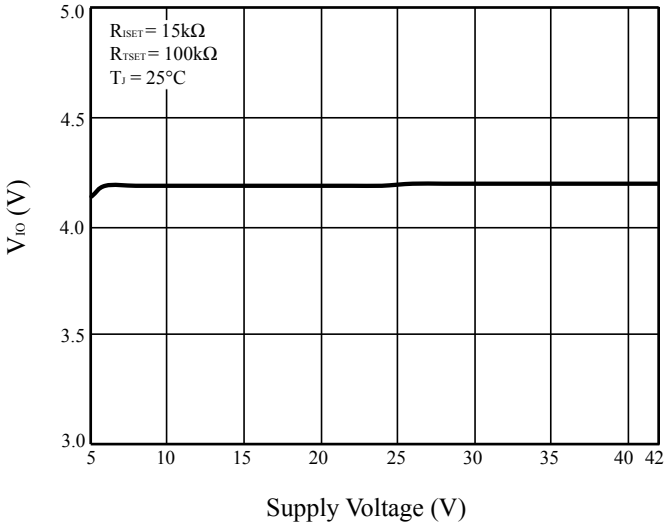


Figure 16 V_{IO} vs. Supply Voltage

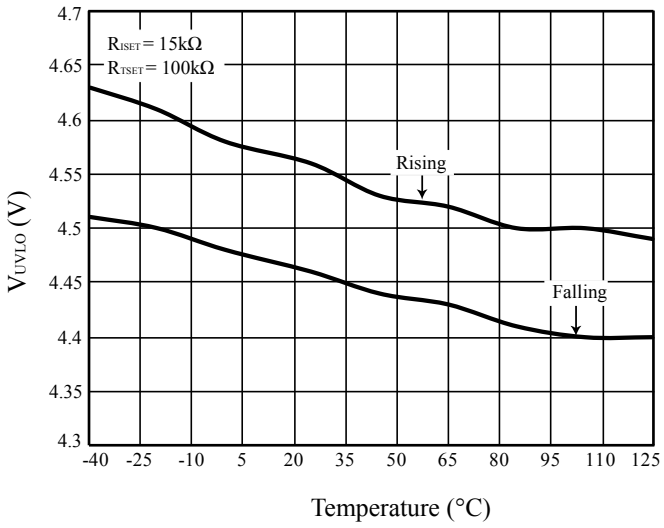


Figure 17 V_{UVLO} vs. Temperature

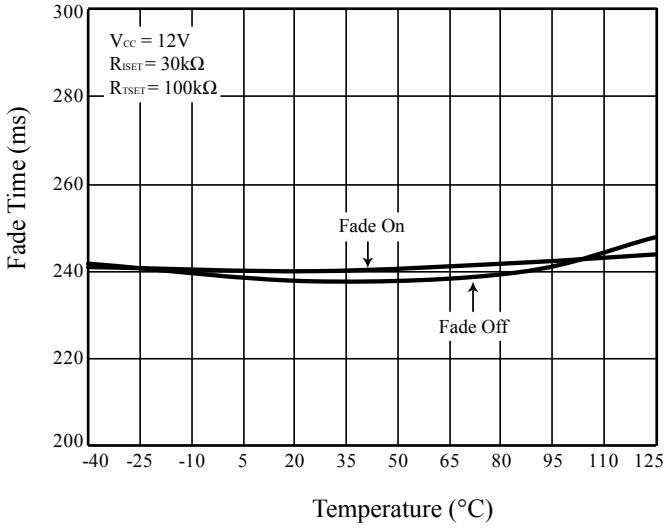


Figure 18 Fade Time vs. Temperature

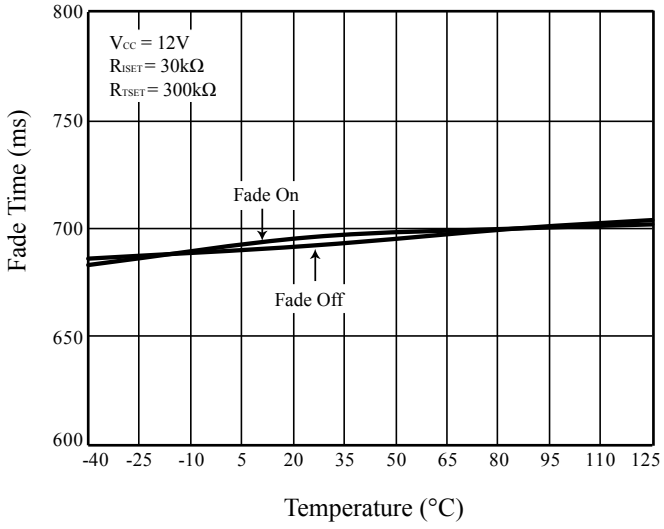


Figure 19 Fade Time vs. Temperature

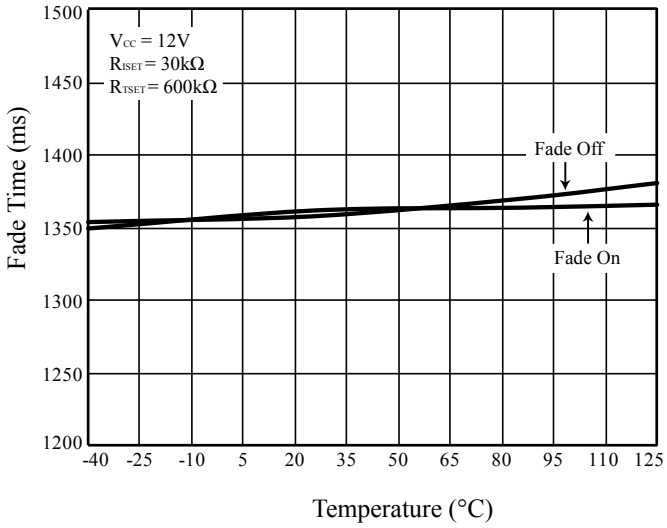


Figure 20 Fade Time vs. Temperature

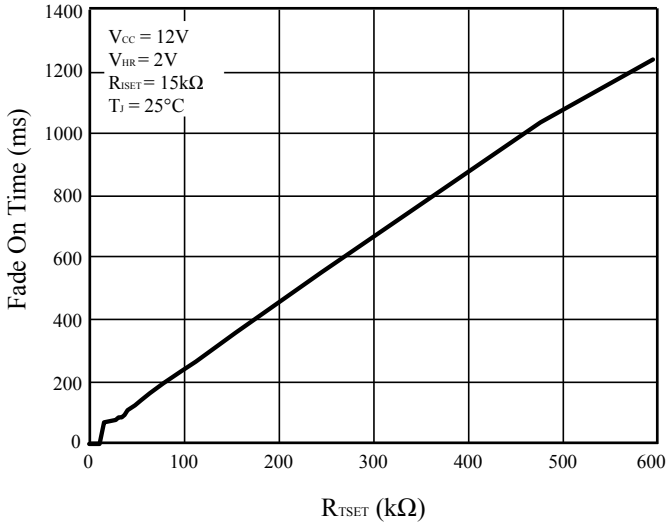


Figure 21 Fade ON Time vs. R_{TSET}

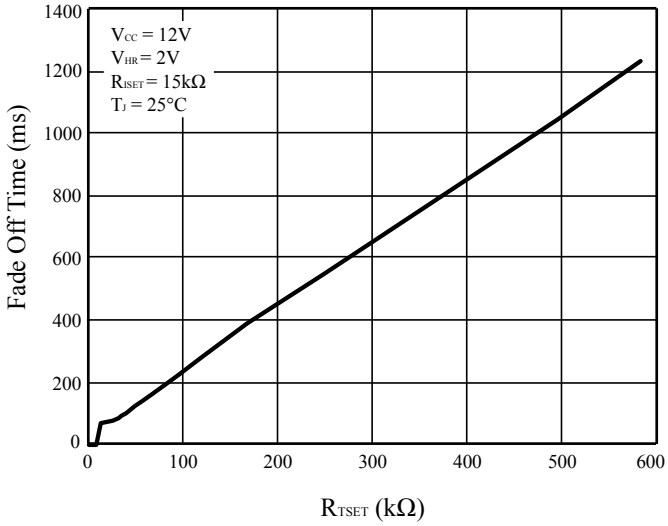


Figure 22 Fade OFF Time vs. R_{TSET}

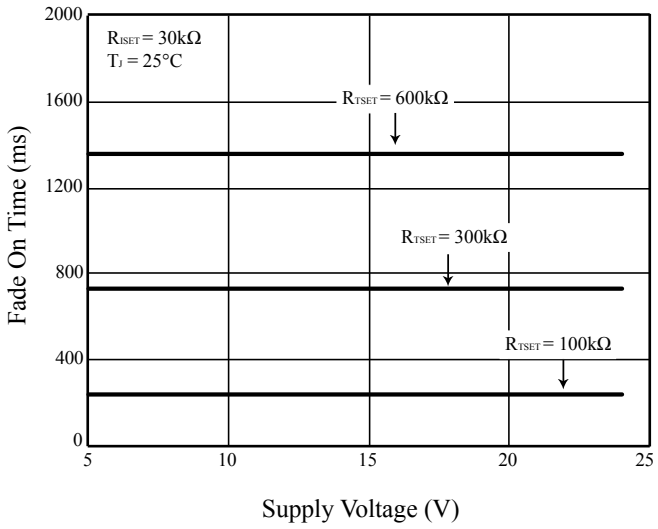


Figure 23 Fade ON Time vs. Supply Voltage

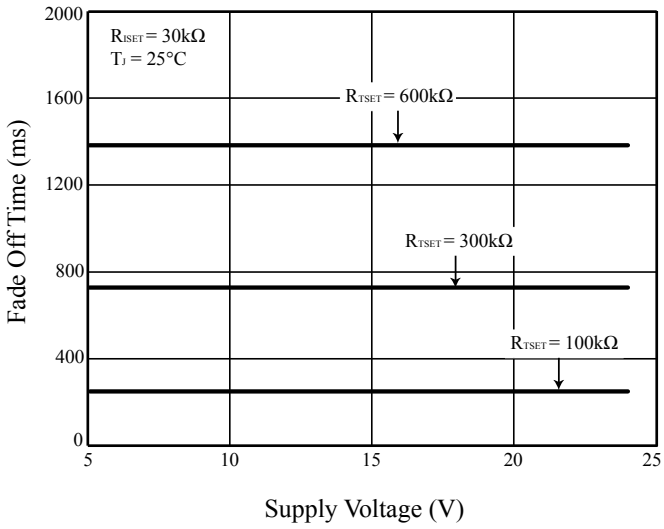


Figure 24 Fade OFF Time vs. Supply Voltage

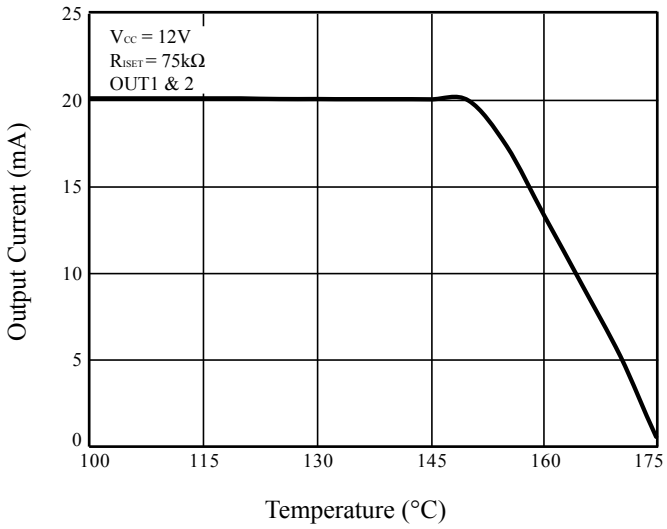


Figure 25 Thermal Roll Off

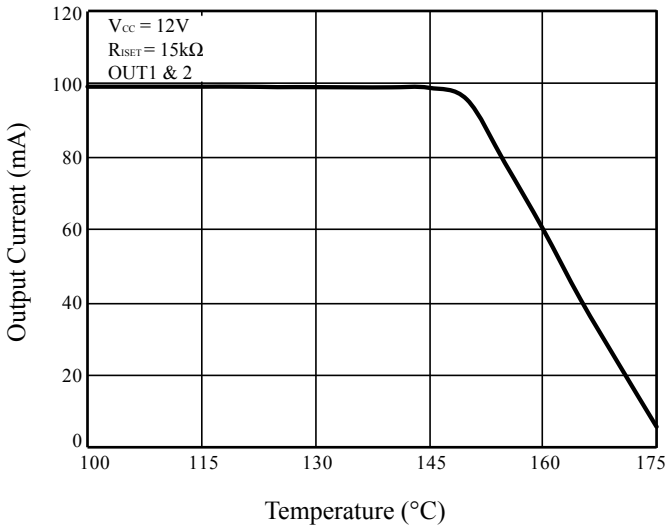


Figure 26 Thermal Roll Off

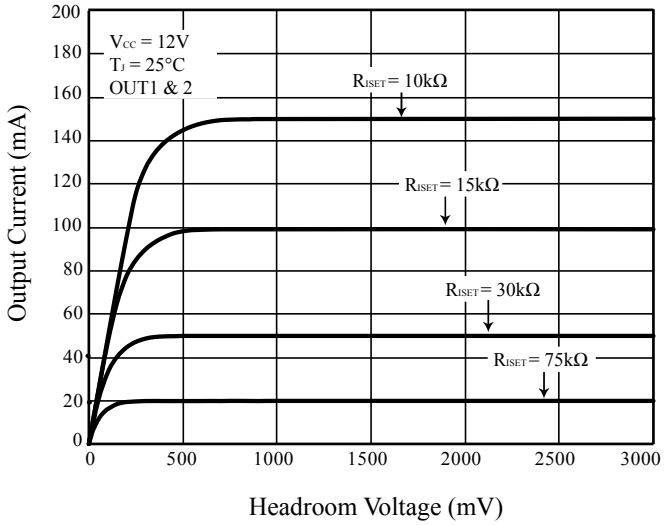


Figure 27 Output Current 1&2 vs. Headroom Voltage

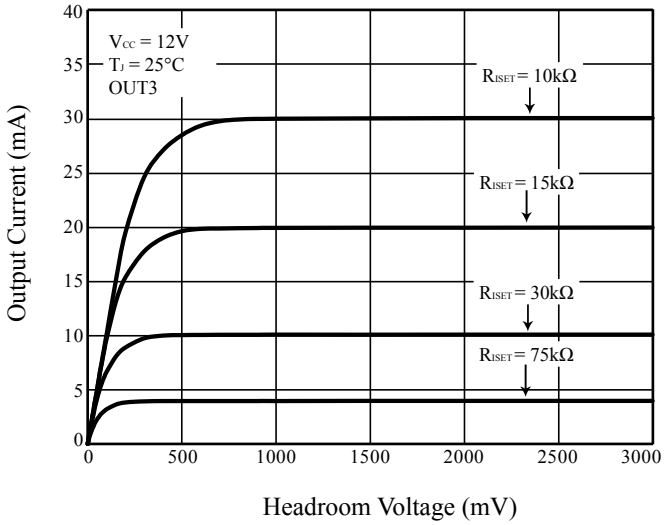


Figure 28 Output Current 3 vs. Headroom Voltage

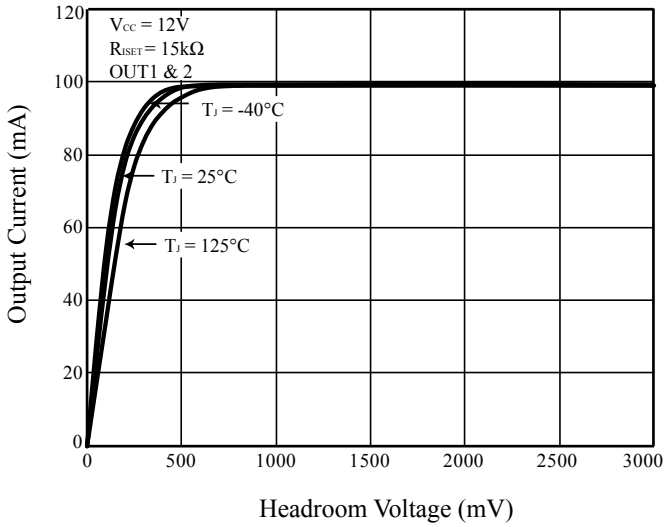


Figure 29 Output Current 1&2 vs. Headroom Voltage

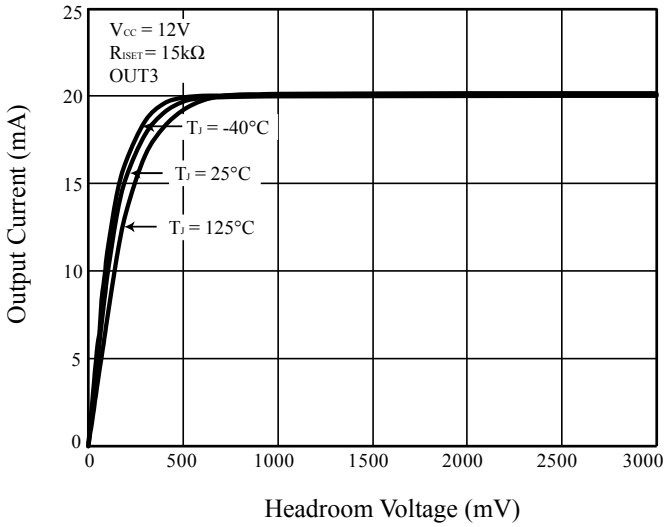


Figure 30 Output Current 3 vs. Headroom Voltage

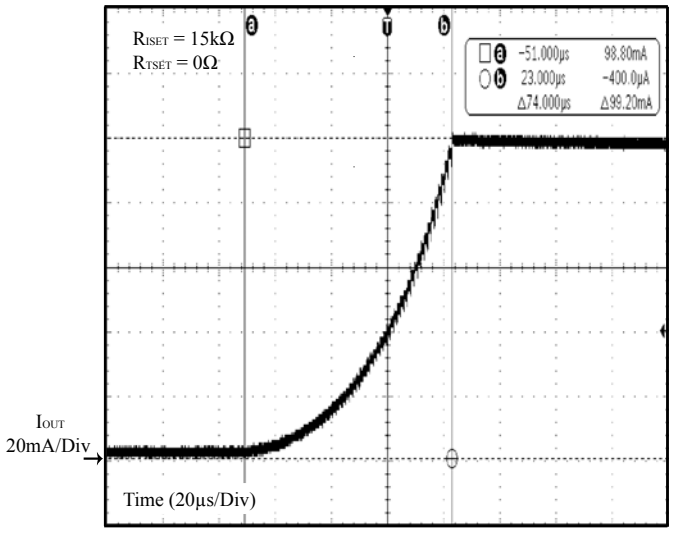


Figure 31 Instant On

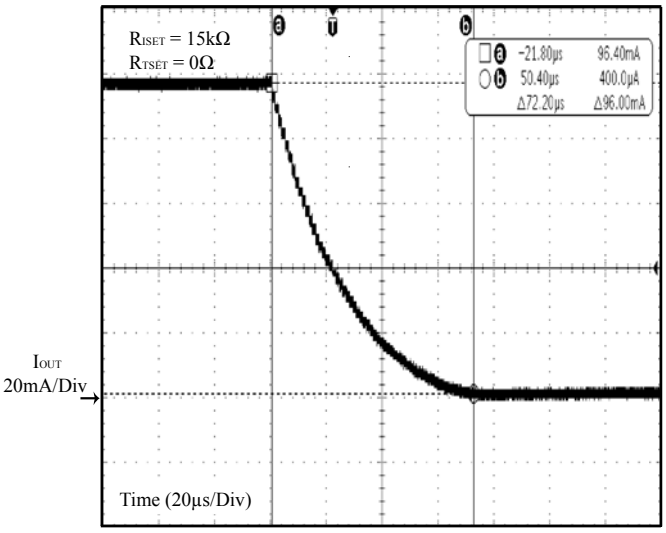


Figure 32 Instant Off

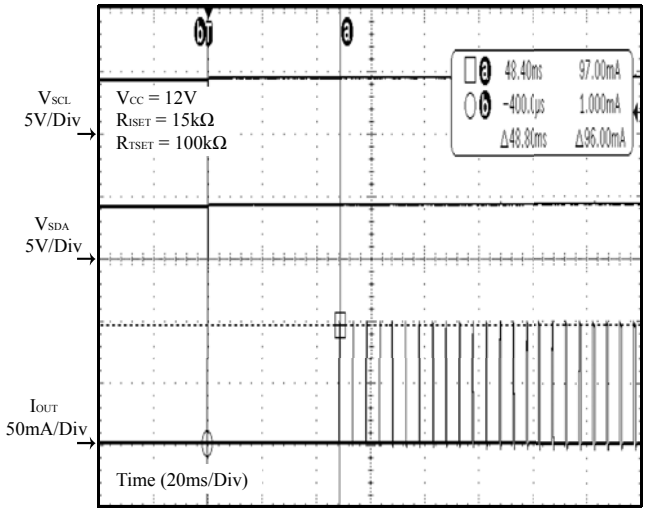


Figure 33 Auto Internal PWM Rising

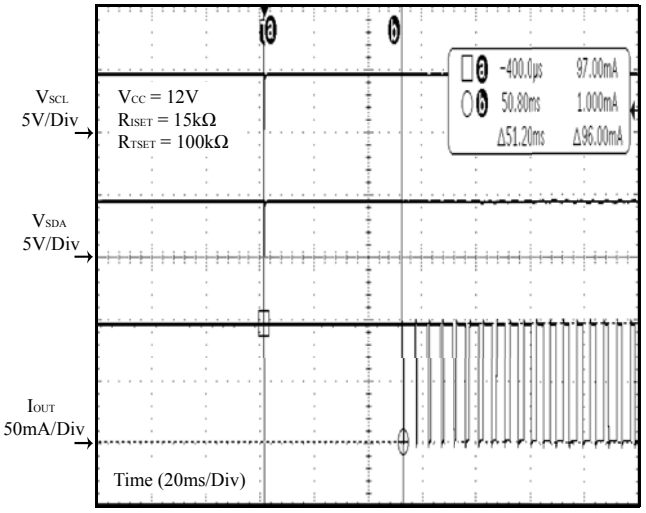


Figure 34 Auto Internal PWM Falling

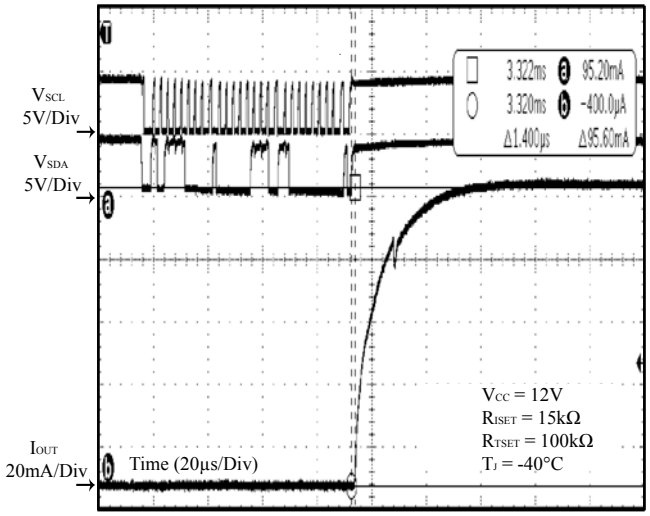


Figure 35 I2C Dimming Rising (T_J= -40°C)

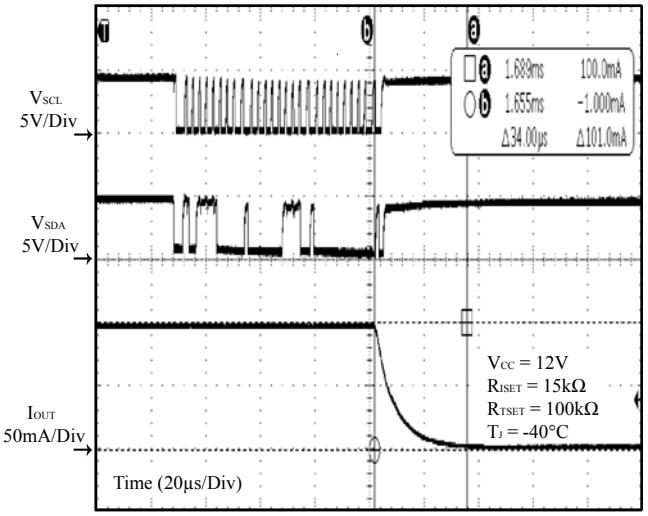


Figure 36 I2C Dimming Falling (T_J= -40°C)

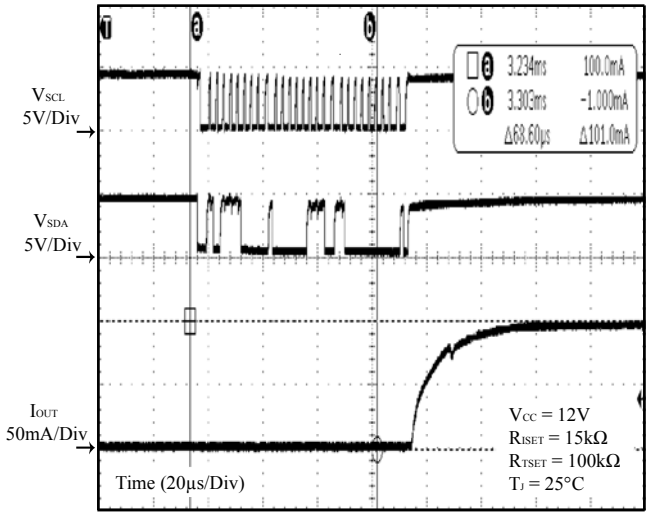


Figure 37 I2C Dimming Rising (T_J= 25°C)

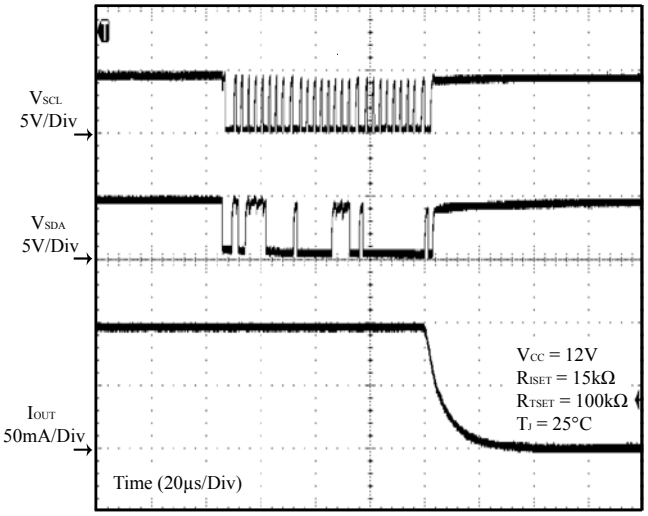


Figure 38 I2C Dimming Falling (T_J= 25°C)

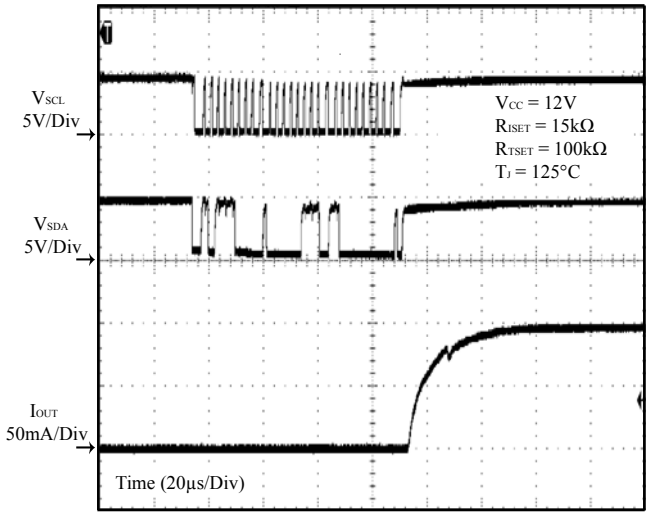


Figure 39 I2C Dimming Rising (T_J= 125°C)

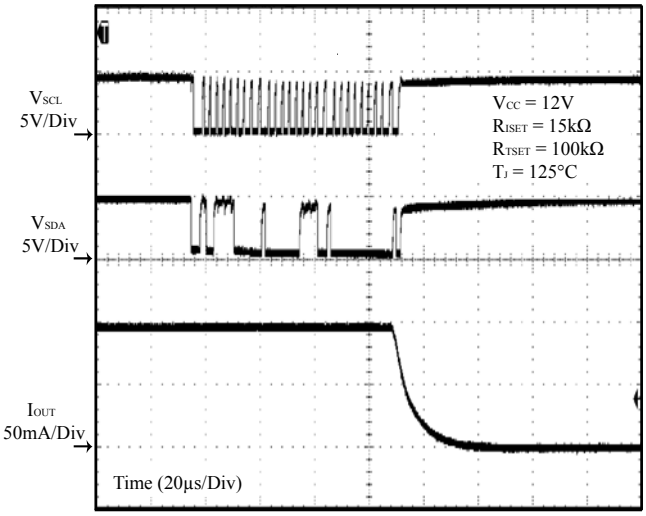


Figure 40 I2C Dimming Falling (T_J= 125°C)

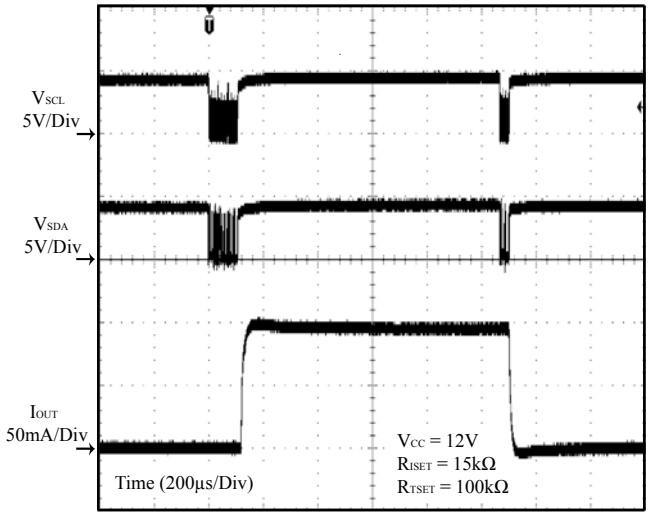


Figure 41 I2C Dimming

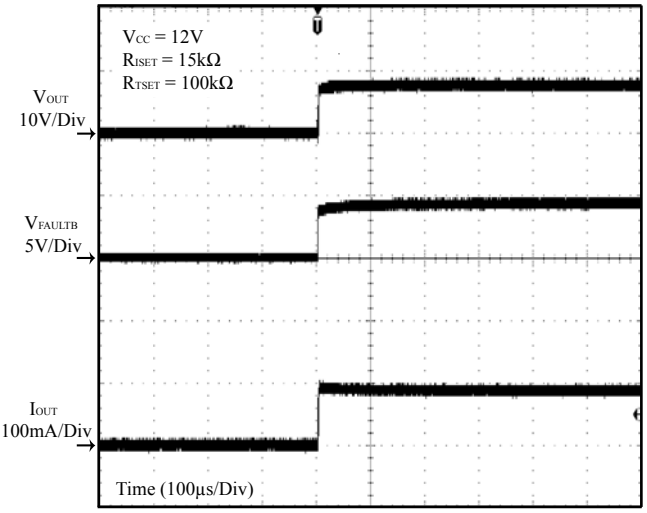


Figure 42 Output Short Recovery

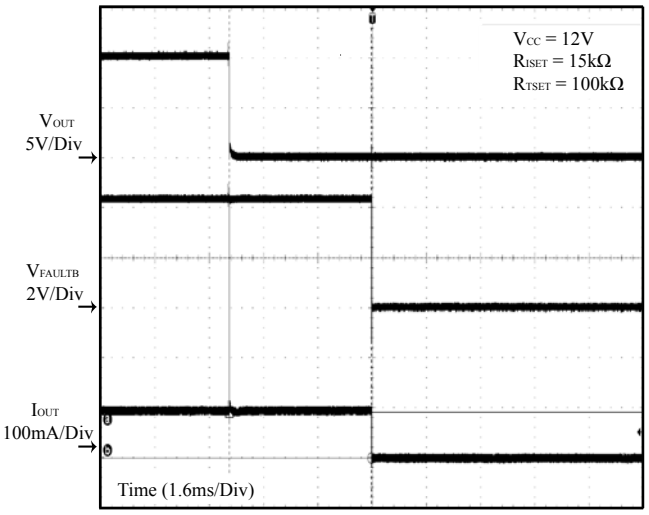


Figure 43 Output Short Detection

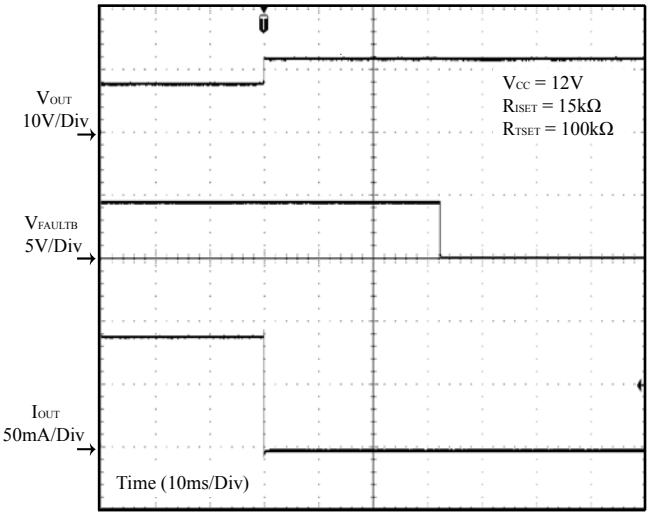


Figure 44 Output Open Detection

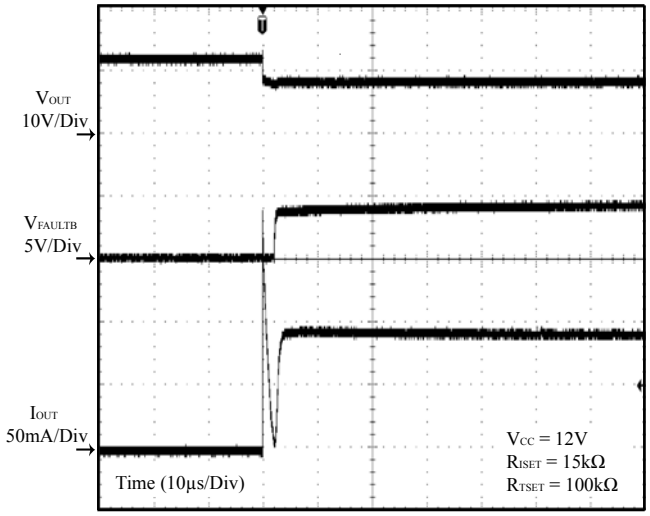


Figure 45 Output Open Recovery

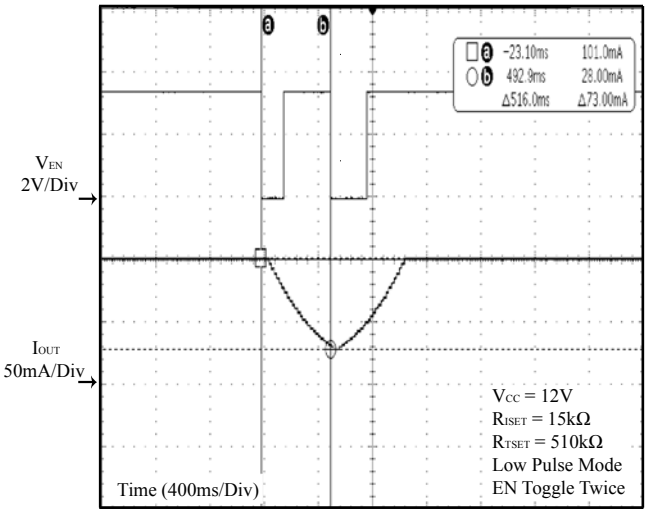


Figure 46 V_{EN} vs. I_{OUT}

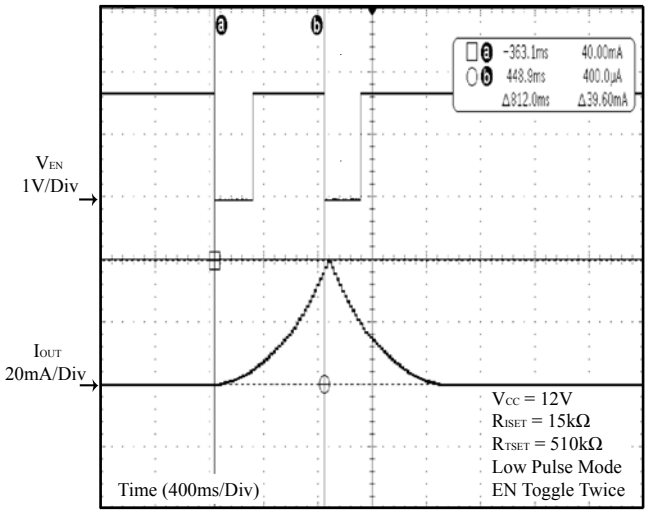


Figure 47 V_{EN} vs. I_{OUT}

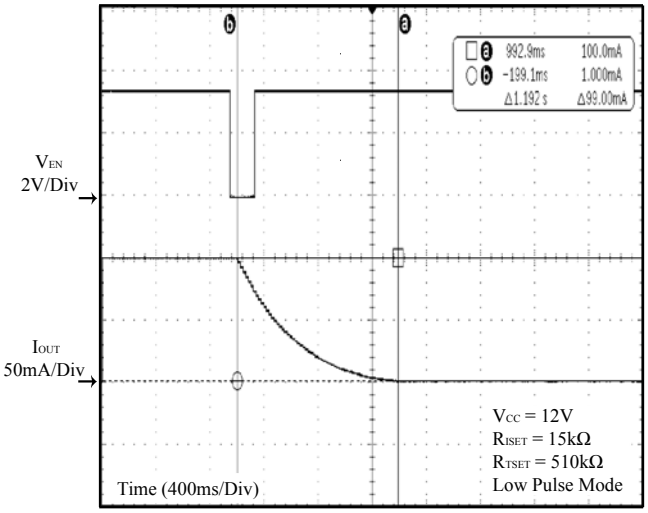


Figure 48 V_{EN} vs. I_{OUT}

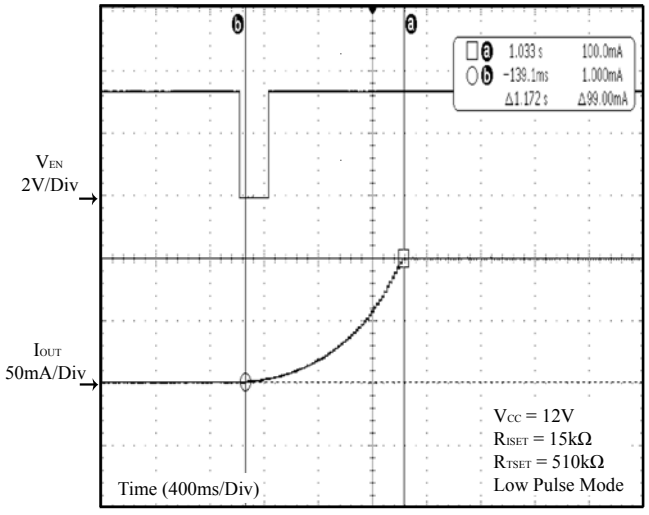


Figure 49 V_{EN} vs. I_{OUT}

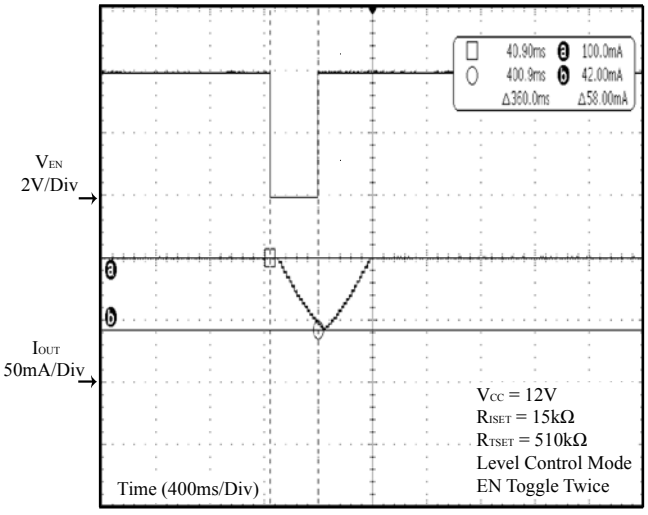


Figure 50 V_{EN} vs. I_{OUT}

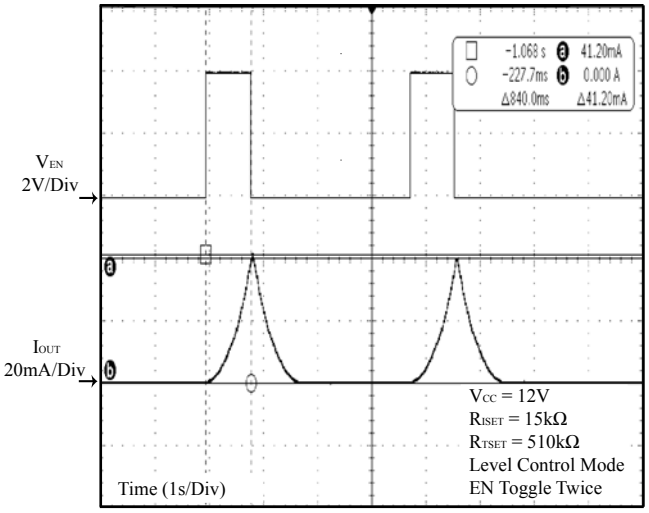


Figure 51 V_{EN} vs. I_{OUT}

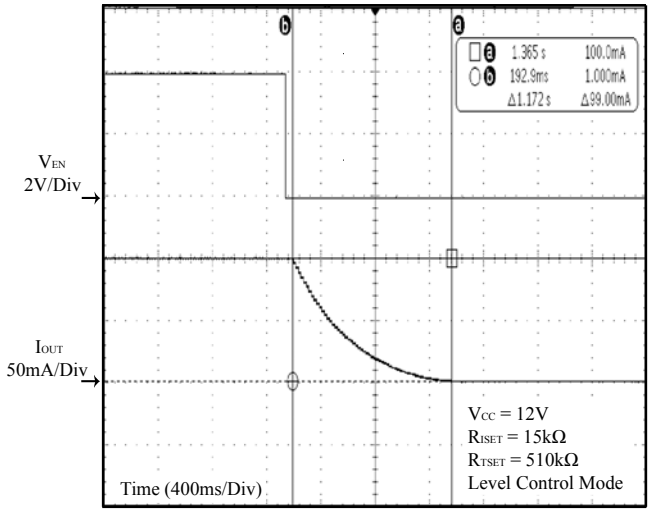


Figure 52 V_{EN} vs. I_{OUT}

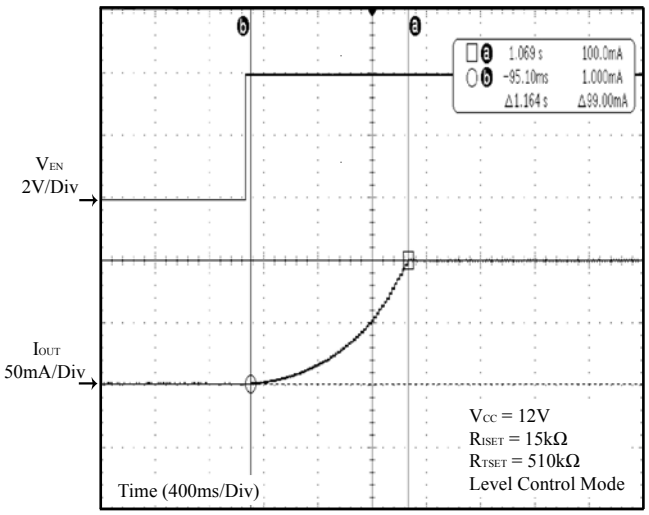
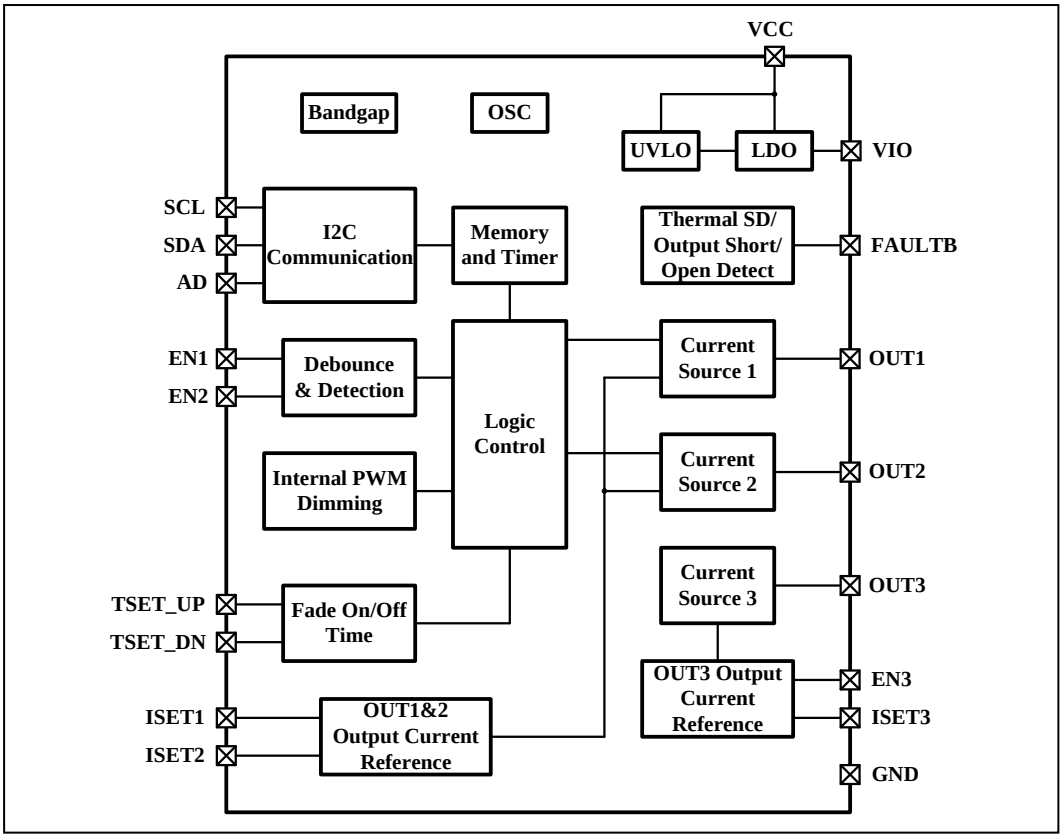


Figure 53 V_{EN} vs. I_{OUT}

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS32LT3129A uses a serial bus, which conforms to the I2C protocol, to control the chip's functions and diagnostic with two wires: SCL and SDA. The IS32LT3129A has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address (Write Only)

Bit	A7:A3	A2:A1	A0
Value	10111	AD	0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (Typ. 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS32LT3129A.

The timing diagram for the I2C is shown in Figure 54. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32LT3129A's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS32LT3129A has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32LT3129A, the register address byte is sent, most significant bit first. IS32LT3129A must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32LT3129A must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32LT3129A, load the address of the data register that the first data byte is intended for. During the IS32LT3129A acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32LT3129A will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32LT3129A (Figure 57).

READING OPERATION

All of registers in IS32LT3129A can be read. To read the device data, the bus master must first send the IS32LT3129A address with the R/$\overline{W}$ bit set to "0", then send command data which determines which response register is accessed. Then restart I2C, the bus master should send the IS32LT3129A address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS32LT3129A to the master (Figure 58).

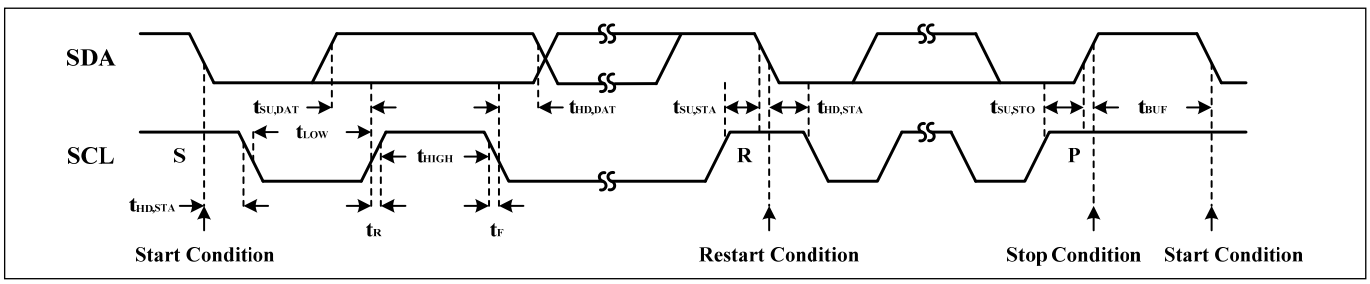


Figure 54 Interface Timing

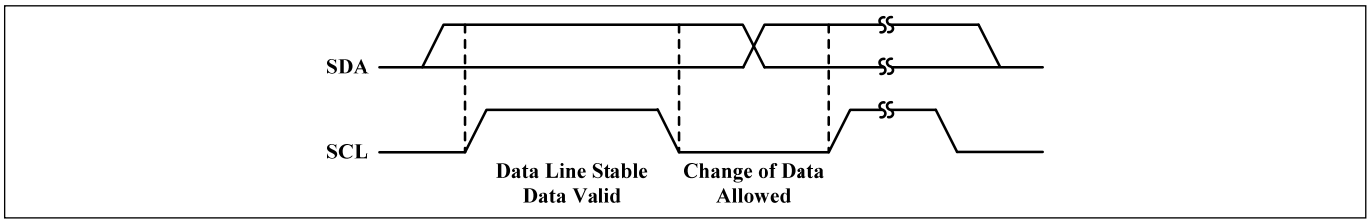


Figure 55 Bit Transfer

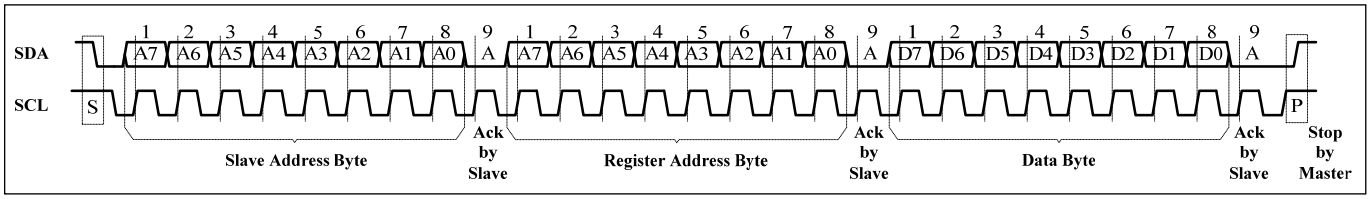


Figure 56 Writing to IS32LT3129A (Typical)

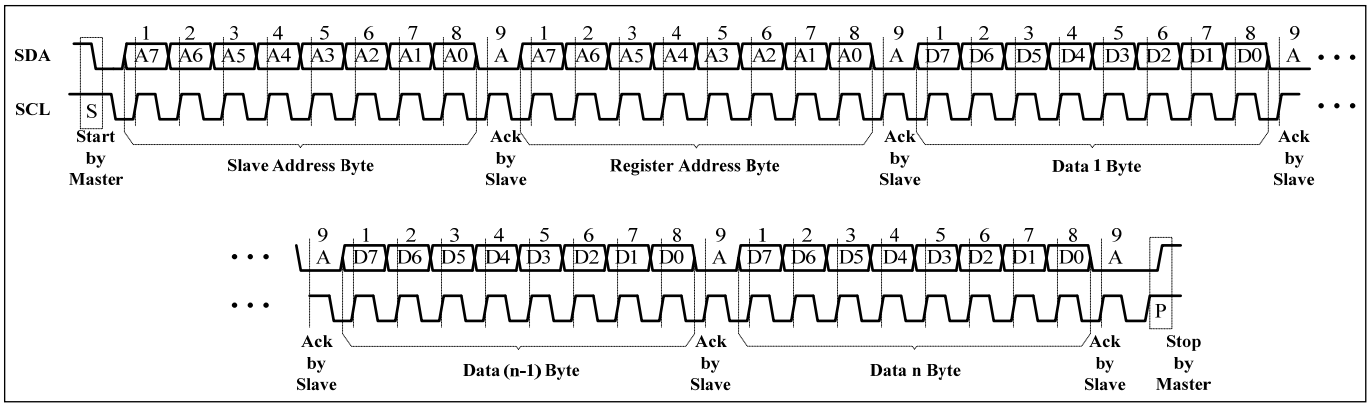


Figure 57 Writing to IS32LT3129A (Automatic Address Increment)

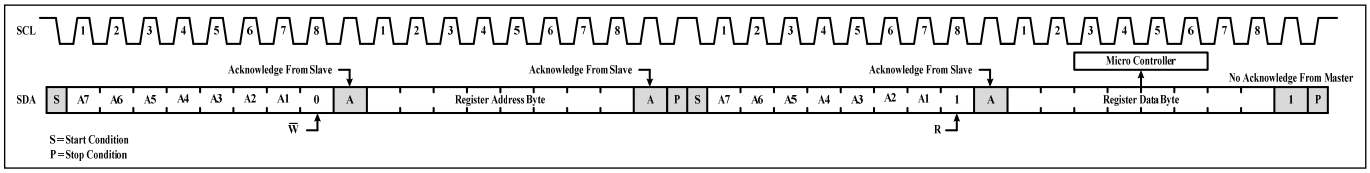


Figure 58 Reading from IS32LT3129A

REGISTERS DEFINITIONS

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
01h	Configuration Register	Thermal roll off, Fade ON/OFF, EN3 mode, PWM dimming, EN1/2 mode and fault UVLO configuration	R/W	3	1000 0100
02h	OUT3 Control Register	Enable and set the OUT3 output current	R/W	4	0000 0000
03h	FITS Configuration Register	Fade ON time configuration	R/W	5	0110 0100
04h	FOTS Configuration Register	Fade OFF time configuration	R/W	6	0110 0100
05h	OUT1 Current Configuration Register	Set the OUT1 maximum output current level	R/W	7	0000 0000
06h	OUT2 Current Configuration Register	Set the OUT2 maximum output current level	R/W	8	0000 0000
07h	Fault Reporting and PWM Enable Register	Fault flag bits and PWM enable bit	R/W	9	0000 0000
08h	Open Fault Configuration Register	Open Fault UVLO and delay time configuration	R/W	10	0001 1010
09h	I2C Writing Lock Register	Writing data protection	R/W	11	0000 0000
0Ah	Protection Configuration Register	Fault protection and FAULTB reporting function configuration	R/W	12	0111 1000

Table 3 01h Configuration Register

Bit	D7	D6	D5	D4
Name	TEN	UV_V	EN3_M	FIT
Default	1	0	0	0
Bit	D3	D2	D1	D0
Name	FOT	PWM_M	-	EN_M
Default	0	1	0	0

TEN Thermal Roll Off Enable Bit
0 Disable thermal roll off
1 Enable thermal roll off

UV_V Fault UVLO Voltage Level Select Bit
0 For 12V battery system
1 For 24V battery system

EN3_M OUT3 Enable Mode Select Bit
0 External EN3 pin high/low voltage level to turn on/off OUT3
1 EN3 bit in 02h register to turn on/off OUT3

FIT Fade ON Time Select Bit
0 Fade ON time depends on the external resistor R_{TSET_UP}
1 Fade ON time depends on the internal memory (Table 5)

FOT Fade OFF Time Select Bit
0 Fade OFF time depends on the external resistor R_{TSET_DN}
1 Fade OFF time depends on the internal memory (Table 6)

PWM_M Internal PWM Dimming Mode Select Bit
0 Internal PWM dimming mode
1 External PWM dimming mode

EN_M EN1/2 Pin Control Mode Select Bit
1 Low Pulse Mode. EN1/2 pin internally pull up by a 50kΩ resistor to 4V. A low going pulse on this pin will toggle the state of the OUT1/2 current
0 Level Control Mode. EN1/2 pin internally pull down by a 50kΩ resister to ground. EN1/2 high voltage to enable OUT1/2 current and low voltage to disable OUT1/2 current

In both control mode, the EN1/2 pin condition is continuously monitored after the de-bounce time typical 37ms.

Table 4 02h OUT3 Control Register

Bit	D7:D5	D4	D3	D2:D0
Name	-	EN3	-	OUT3_C
Default	000	0	0	000

EN3 OUT3 Enable Bit
When EN3_M is set to "1":
0 Turn off OUT3
1 Turn on OUT3

OUT3_C OUT3 Output Current Set Bits
The OUT3 maximum current (I_{MAX3}) is set by external resistor R_{ISET3}. OUT3_C sets the OUT3 current to:
000 I_{MAX3} (Default Value)
001 1/8 I_{MAX3}
010 2/8 I_{MAX3}
011 3/8 I_{MAX3}
100 4/8 I_{MAX3}
101 5/8 I_{MAX3}
110 6/8 I_{MAX3}
111 7/8 I_{MAX3}

Table 5 03h FITS Configuration Register

Bit	D7:D0
Name	FITS
Default	0110 0100

When FIT=1, the fade ON time:
0x00 T_{FADE_ON} = 75μs
0x01~0xFF T_{FADE_ON} = FITS × 7ms
The default value is 700ms.

Table 6 04h FOTS Configuration Register

Bit	D7:D0
Name	FOTS
Default	0110 0100

When FOT=1, the fade OFF time:
0x00 T_{FADE_OFF} = 75μs
0x01~0xFF T_{FADE_OFF} = FOTS × 7ms
The default value is 700ms.

Table 7 05h OUT1 Current Configuration Register

Bit	D7:D0
Name	OUT1_C
Default	0000 0000

The OUT1 maximum current (I_{MAX1}) is set by external resistor R_{ISET1}. OUT1_C sets the OUT1 current to:
0x00 I_{OUT1} = I_{MAX1} (Default Value)
0x01~0xFF I_{OUT1} = (OUT1_C/256) × I_{MAX1}

Table 8 06h OUT2 Current Configuration Register

Bit	D7:D0
Name	OUT2_C
Default	0000 0000

The OUT2 maximum current (I_{MAX2}) is set by external resistor R_{ISET2}. OUT2_C sets the OUT2 current to:
0x00 I_{OUT2} = I_{MAX2} (Default Value)
0x01~0xFF I_{OUT2} = (OUT2_C/256) × I_{MAX2}

Table 9 07h Fault Reporting and PWM Enable Register (D6:D0 are read only)

Bit	D7	D6	D5:D3	D2:D0
Name	PWM_E	TSD	O1O:O3O	O1S:O3S
Default	0	0	000	000

PWM_E PWM Dimming Control Bit
0 If PWM_M=1, simultaneously turn off OUT1/2.
If PWM_M=0, internal PWM generator simultaneously controls OUT1/2 output current PWM duty cycle auto ramp down following Gamma curve, LED light intensity dimming down.
1 If PWM_M=1, simultaneously turn on OUT1/2.
If PWM_M=0, internal PWM generator simultaneously controls OUT1/2 output current PWM duty cycle auto ramp up following Gamma curve, LED light intensity dimming up.

TSD Thermal Shutdown Flag
0 No thermal shutdown
1 Thermal shutdown

OxO OUT1~OUT3 Open Circuit Flag
0 No open circuit
1 Open circuit

OxS OUT1~OUT3 Short Circuit Flag
0 No short circuit
1 Short circuit

Table 10 08h Open Fault Configuration Register

Bit	D7:D4	D3:D0
Name	DELAY	F_UVLO
Default	0001	1010

DELAY Open Fault Reporting Output Delay Time

0000	55μs	1000	14.52ms
0001	110μs (Default value)	1001	29ms
0010	225μs	1010	58ms
0011	450μs	1011	0.116s
0100	910μs	1100	0.232s
0101	1.82ms	1101	0.46s
0110	3.64ms	1110	0.92s
0111	7.28ms	1111	1.84s

F_UVLO Open Fault Detection UVLO Set

When UV_V=0:	When UV_V=1:
0000	5V	10V
0001	5.5V	11V
0010	6V	12V
0011	6.5V	13V
0100	7V	14V
0101	7.5V	15V
0110	8V	16V
0111	8.5V	17V
1000	9V	18V
1001	9.5V	19V
1010	10V	20V (Default value)
1011	10.5V	NA
1100	11V	NA
1101	11.5V	NA
1110	12V	NA
1111	12.5V	NA

Table 11 09h I2C Writing Lock Register

Bit	D7:D0
Name	LOCK
Default	0000 0000

This is a protection register to prevent accidental change to the registers. To write data to any other register, please write 0xC5 to this register first, otherwise any writing data will be ignored. After writing action, recommend to write a data besides 0xC5 to this register to lock again.

Table 12 0Ah Protection Configuration Register

Bit	D7	D6	D5	D4
Name	-	TSDEN	STREN	STEN
Default	0	1	1	1
Bit	**D3**	**D2:D0**		
Name	OPRTEN	OEN3:OEN1		
Default	1	000		

TSDREN Thermal Shut Down Report Enable Bit

0 Thermal SD FAULTB do not pull low

1 Thermal SD FAULTB pull low

STREN Shorted Reporting Enable Bit

0 OUT1/2/3 shorted do not pull low FAULTB pin

1 If any one of OUT1/2/3 shorted to GND, pull low FAULTB pin

STEN Short Detect Enable Bit

0 OUT1/2/3 short detect function is inactive

1 OUT1/2/3 short detect function is active.

OPRTEN Open Reporting Enable Bit

0 OUT1/2/3 open do not pull low FAULTB pin

1 If any one of OUT1/2/3 is open, pull low FAULTB pin

OENx OUT3~OUT1 Open Detect Enable Bit

0 OUT3 open detect function is inactive

1 OUT3 open detect function is active

APPLICATION INFORMATION

The IS32LT3129A is triple channel linear current driver optimized to drive an automotive interior LED map light, or other interior lamp which is frequently toggled between the ON and OFF condition. The device integrates a debounce input circuit to enable use of a low cost momentary contact switch or latched switch for controlling ON/OFF of an external LED. In addition, a programmable fade ramp timing function provides flexibility in setting different Fade ON and Fade OFF ramp duration periods. The fade ramp cycle can be interrupted mid-cycle before the ramp has completed, Figure 59.

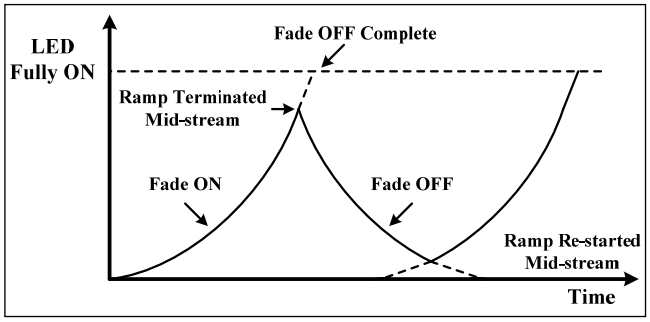


Figure 59 Fade Ramp Interrupted Mid-cycle

The regulated OUT1/2 LED current (up to 150mA) and OUT3 backlight LED current (up to 30mA) are independently set by their corresponding reference resistor $R_{ISET1/2}$ and R_{ISET3}.

OUTPUT CURRENT SETTING

An individual programming resistor (R_{ISETx}) is connected to the ISETx pin to set the maximum output current for each output channel.

The programming resistor of OUT1/2 can be computed using the following Equation (1):

$$R_{ISET1/2} = \frac{1500}{I_{OUT1/2}} \qquad (1)$$

($10k\Omega \le R_{ISET1/2} \le 75k\Omega$)

Where $I_{OUT1/2}$ is the desired output current value in Amps. In the meantime, the 05h/06h register can be used to adjust the OUT1/2 current in 256 steps based on above resistor setting.

The programming resistor of OUT3 can be computed using the following Equation (2):

$$R_{ISET3} = \frac{300}{I_{OUT3}} \qquad (2)$$

($10k\Omega \le R_{ISET3} \le 75k\Omega$)

Where I_{OUT3} is the desired output current value in Amps. In the meantime, the OUT3_C bits of 02h register can be used to adjust the OUT3 current in 8 steps based on above resistor setting.

It is highly recommend to use 1% accuracy R_{ISETx} resistors with good temperature characteristics to ensure accurate and stable output currents.

The device is protected from an output overcurrent condition caused by an accidental short circuit of the ISETx pin, by internally limiting the maximum current in the event of an ISETx short circuit to 205mA (Typ.) for OUT1/2 and 40mA (Typ.) for OUT3.

EN1/2 PIN OPERATION

The EN1/2 pins can individually control the state of the OUT1/2 channels. When driven, the output current will ramp up (or down) in 63 PWM steps, with integrated gamma correction for an extremely visual linear lumen output of the LED. The ramp time can be interrupted mid-cycle each time the EN1/2 pins are toggled.

There are two kinds of operation modes: Low Pulse Mode and Level Control Mode. The different modes are chosen by EN_M bit. EN_M=1 for Low Pulse Mode and EN_M=0 for Level Control Mode.

Table 1 EN1 And EN2 Mode

EN_M Bit	EN1/2 Pin	Output Current
1 (Low Pulse Mode)	Low going pulse	If LED off, fade on (ramp up) If LED on, fade off (ramp down)
0 (Level Control Mode)	Low to high	If LED off, fade on (ramp up) If LED on, keep on
	High to low	If LED on, fade off (ramp down) If LED off, keep off

Low Pulse Mode (EN_M=1):

In this mode, the ENx pin is internally pulled-up by a 50kΩ resistor to 4V LDO so that no external components are required to provide the input high level to the pin.

The output channels power up in the “OFF” condition. Toggling the ENx pin from high to low for a period of time that exceeds the debounce time (Typ. 37ms) will cause the corresponding output to be toggled and latched from the OFF condition to the current source condition. When this happens, the corresponding output current gradually ramps up from zero mA to the programmed value (set by $R_{ISET1/2}$ and 05h/06h register) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin or 03h register. Conversely, if it is already in the source condition, and the ENx pin is toggled low, then the corresponding output current will begin to ramp down towards zero mA in the time period as programmed by the resistor (R_{TSET_DN}) attached to the TSET_DN pin or 04h register. So a low cost momentary contact switch can be used in this mode.

Level Control Mode (EN_M=0):

In this mode, the ENx pin is internally pull-down by 50kΩ resistor to ground so that no external components are required to provide the input low level to the pin.

Externally pull ENx pin to high level (>V_{IH}) and keep it at high level, after a period of time that exceeds the debounce time (Typ. 37ms) that will cause the corresponding output to be toggled from the OFF condition to the current source condition. When this happens, the corresponding output current gradually ramps up from zero mA to the programmed value (set by $R_{ISET1/2}$ and 05h/06h register) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin or 03h register. Conversely, if ENx is already kept in high level and the output is in the source condition, the ENx pin is pulled to low level, then the corresponding output current will begin to ramp down towards zero mA in the time period as programmed by the resistor (R_{TSET_DN}) attached to the TSET_DN pin or 04h register. So a regular latched switch can be used in this mode.

Debounce – Output control is provided by a debounced switch input, providing an ON/OFF toggle action for various switch or button characteristics. An internal debounce circuit will condition the EN input signal so a single press of the mechanical switch doesn't appear like multiple presses. The EN input is debounced by typically 37ms.

Note: The debounce time applies to both falling and rising edges of the EN signal.

EN3 PIN OPERATION

The EN3 pin or EN3 bit of 02h register is the enable control of OUT3. There is no fade ON/OFF function as with the EN1/2 pins. EN3 pin is internally pulled down by a 100kΩ resistor to ground. The latency time from EN3 pin pull high over V_{IH} to OUT3 output current rise to 10% is 6μs (Typ.). Float or pull down EN3 to ground to disable OUT3. An external PWM signal driving EN3 pin can implement OUT3 dimming by modulating PWM duty cycle.

The recommended PWM signal frequency range is 50Hz-300Hz. The duty cycle can be 0~100%. The output current of the PWM dimming is given by Equation (3):

$$I_{OUT3\_PWM} = \frac{300}{R_{ISET3}} \times D_{PWM} \qquad (3)$$

Where, D_{PWM} is the duty cycle of the PWM.

In the meantime, the OUT3_C bits of 02h register can be used to adjust the OUT3 current in 8 steps based on above resistor setting.

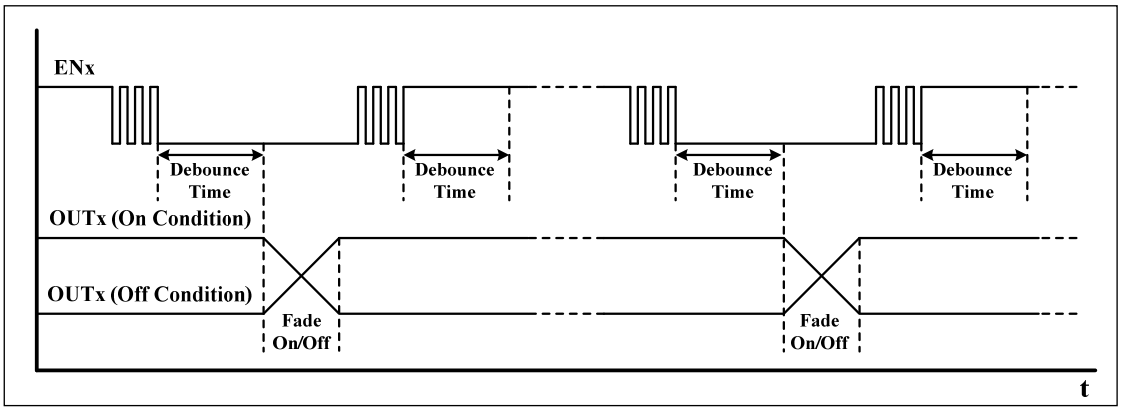


Figure 60 EN1/2 in Low Pulse Mode (Momentory Contact Switch)

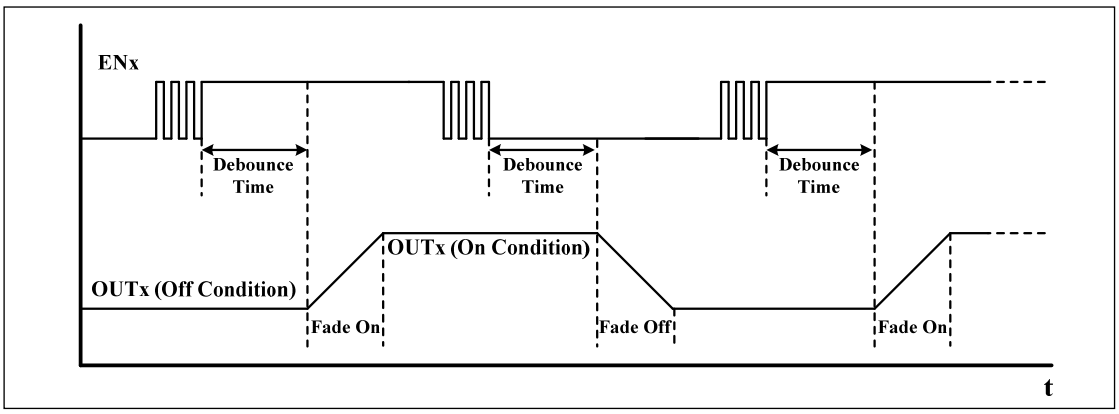


Figure 61 EN1/2 in Level Control Mode (Latched Switch)

FADE ON AND FADE OFF DIMMING

The OUT1/2 LED fade function can be accomplished in one of two methods; 1) by I2C refreshing the PWM_E bit, or 2) when the EN1/2 pin is toggled.

I2C Dimming

The PWM_E bit in 07h register will simultaneously control the both OUT1/2 channels. There are two kinds of dimming modes via I2C: External-PWM-dimming and Internal-PWM-Dimming. The different mode is chosen by PWM_M bit in 01h register. PWM_M=1 for External-PWM-dimming mode and PWM_M=0 for Internal-PWM-Dimming mode.

External-PWM-dimming (PWM_M=1):

In this mode, the OUT1/2 can be driven by an external I2C signal refreshing PWM_E bit to accomplish both channels simultaneously dimming. The integrated gamma correction and fade ON/OFF ramp functions are disabled when actively driving this bit.

To get better dimming ratio, the recommended refreshing PWM_E bit frequency range is 50Hz-300Hz. The duty cycle can be 0-100%. The output current of the PWM dimming is given by Equation (4):

$$I_{OUT1/2} = \frac{1500}{R_{ISET1/2}} \times D_{PWM} \qquad (4)$$

Where, D_{PWM} is the duty cycle of the external I2C signal refreshing PWM_E bit. Please refer to Figure 35~40 for the delay time of I2C command to current change edge.

Internal-PWM-Dimming (PWM_M=0):

In this mode, the integrated PWM source is operational. PWM_E=1 can trigger this PWM source. When PWM_E is changed the logic state and after a period of time that exceeds the debounce time (37ms), the both output current will either gradually ramp up from zero mA to the programmed value (set by $R_{ISET1/2}$ and 05h/06h register) over the time set by the resistor (R_{TSET_UP}) attached to the TSET_UP pin (or 03h register), or gradually ramp down from programmed value to zero mA over the time set by the resistor (R_{TSET_DN}) attached to the TSET_DN pin (or 04h register). The ramping up (or down) is accomplished by the internal 220Hz PWM source digitally modulating the both output current simultaneously with 63 steps gamma correction, that will perform an extremely visual linear light to human eye.

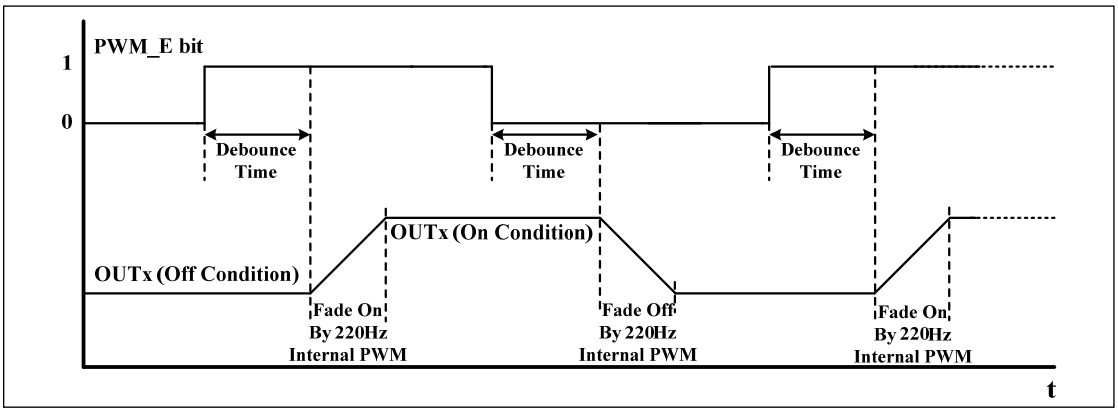


Figure 62 Ineternal-PWM-Dimming for OUT1/2

THE PRIORITY OF EN1/2 AND PWM DIMMING

EN1/2 pins can individually control the OUT1/2 while PWM_E bit can simultaneously control the both outputs. The Figure 63~69 lists some critical priority logic of them:

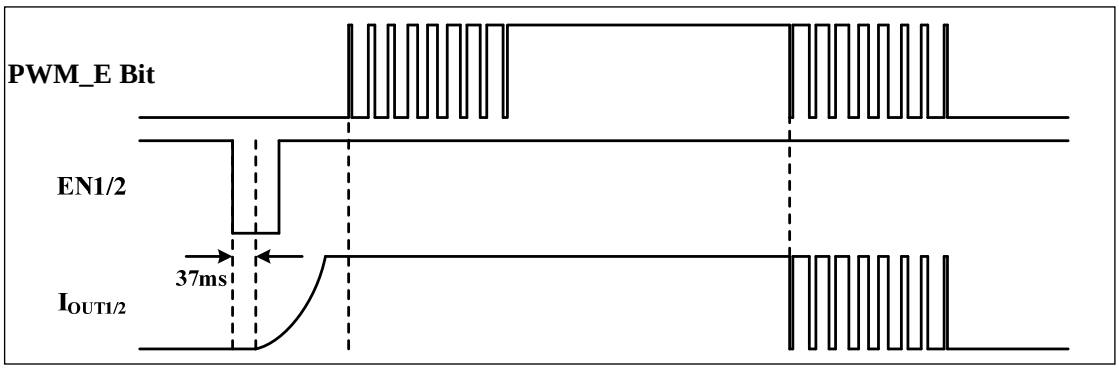


Figure 63 Priority Logic 1 of EN1/2 in Low Pulse Mode

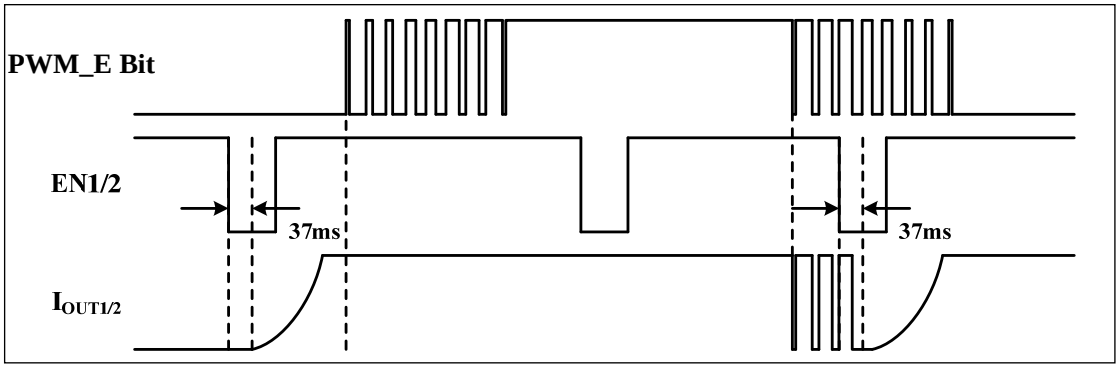


Figure 64 Priority Logic 2 of EN1/2 in Low Pulse Mode

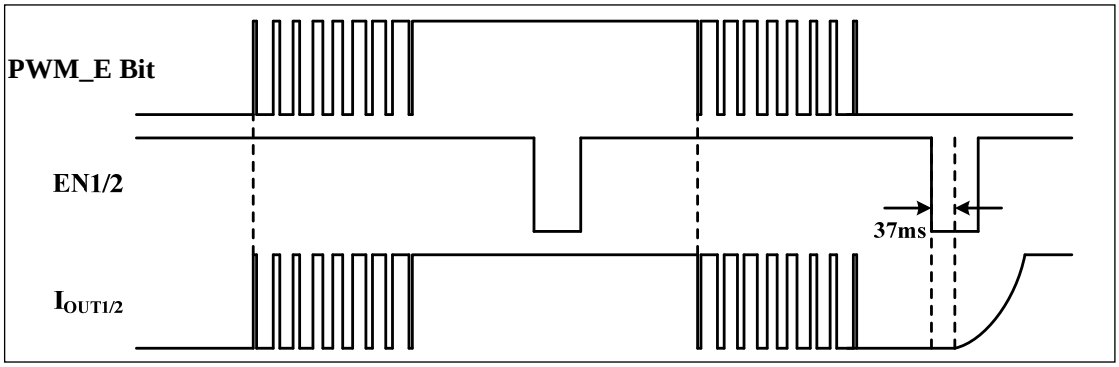


Figure 65 Priority Logic 3 of EN1/2 in Low Pulse Mode

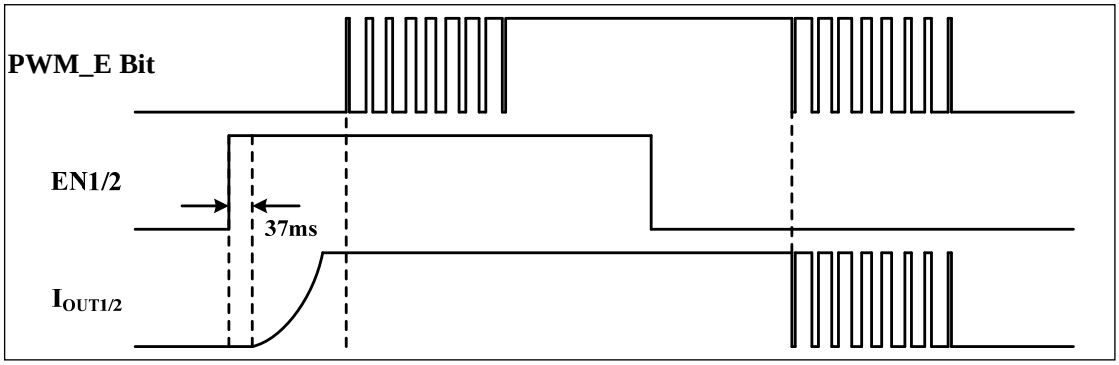


Figure 66 Priority Logic 1 of EN1/2 in Level Control Mode

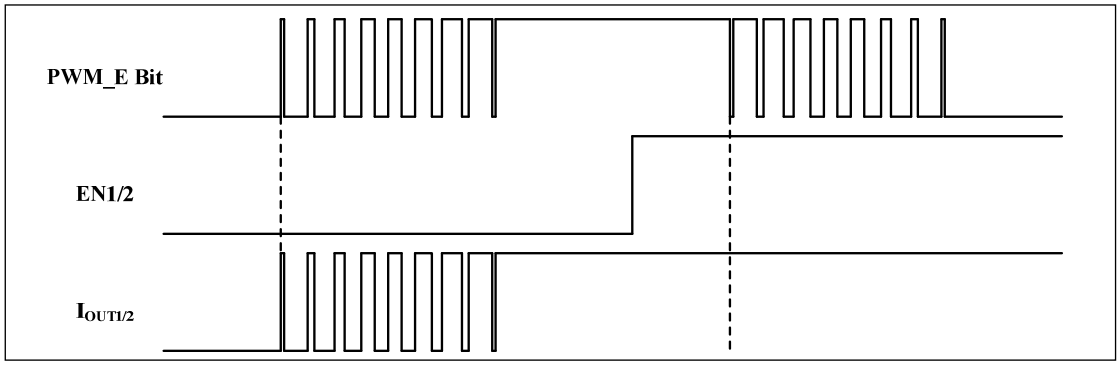


Figure 67 Priority Logic 2 of EN1/2 in Level Control Mode

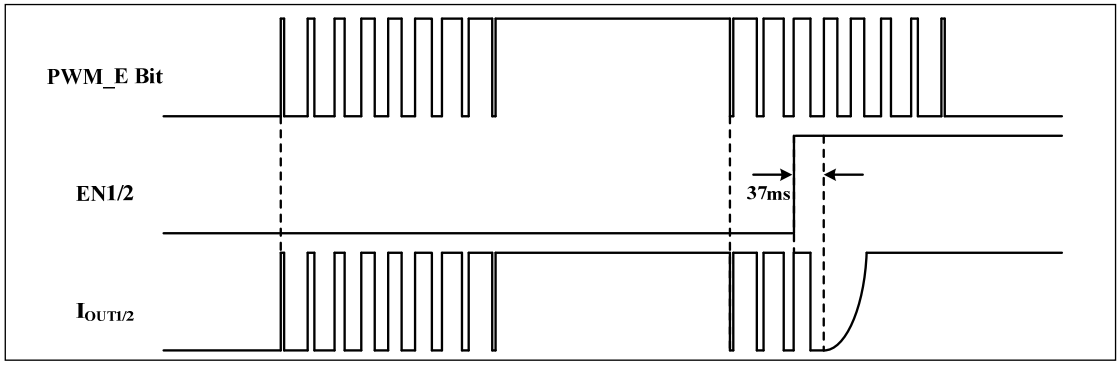


Figure 68 Priority Logic 3 of EN1/2 in Level Control Mode

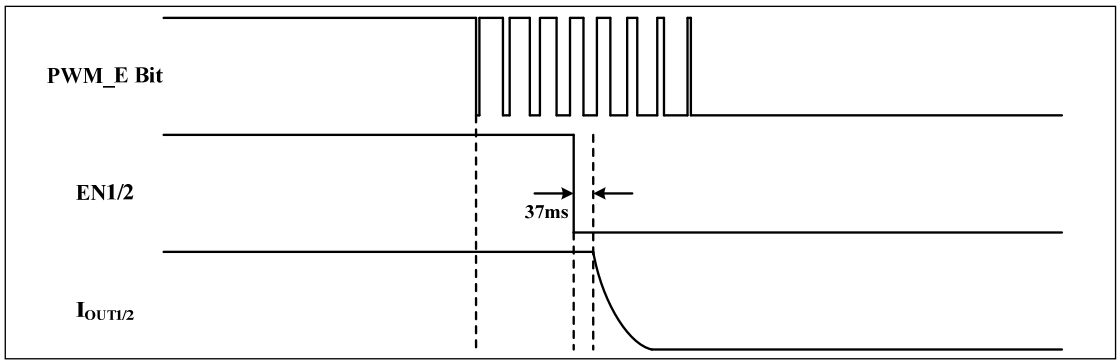


Figure 69 Priority Logic 4 of EN1/2 in Level Control Mode

UNDERVOLTAGE LOCKOUT

IS32LT3129A integrates an undervoltage lockout function to prevent mis-operation of the device during low input voltage conditions.

Should the VCC pin voltage fall below 4.5V (Typ.), the device will turn OFF the current source and maintain the EN latch status as long as the VCC pin voltage remains above 4.0V (Typ.). An external capacitor (Figure 70) is necessary to help maintain the VCC pin voltage >4.0V (Typ.) and to supply current to the device status latch circuitry. However, should the voltage drop below 4.0V (Typ.), the internal latch will be reset to the power on default status (LED initial off state).

The current source will be turned ON when the input voltage is re-applied and the VCC pin rises above 4.6V (Typ.).

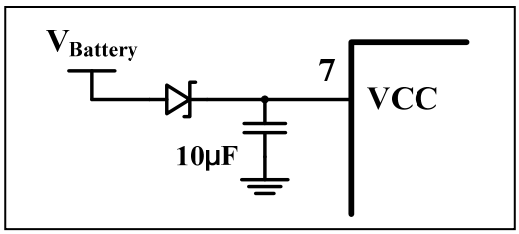


Figure 70 Capacitor For Latch Status

SETTING THE FADE TIME

The fade time can be configured by either the external resistors or I2C register, which is decided by the FIT and FOT bit of 01h register.

When FIT (or FOT) bit is set to “1”, the fade time is programmed by 03h (or 04h) 8 bits register with each 7ms per step over time range of 7ms~1785ms.

When FIT (or FOT) bit is set to “0”, the fade time is programmed by two external programming resistors; R_{TSET_UP} and R_{TSET_DN}. The R_{TSET_UP} connected to the TSET_UP pin configures the fade ramp ON time while the R_{TSET_DN} connected to the TSET_DN pin configures the fade ramp OFF time. The fade time (ON or OFF) is programmable by Equation (5):

$$t \approx R_{TSET} \times 2.5\mu s \qquad (5)$$

For example, R_{TSET}=100kΩ, Fade ON/OFF time is about 0.25s.

Note: In order to get the optimized effect, the recommended fading time is between 1.5s (R_{TSET}= 600kΩ) and 0.25s (R_{TSET}= 100kΩ).

If either the TSET_UP or TSET_DN pin is tied directly to GND or 03h/04h register set to “0000 0000”, the corresponding fade function is canceled and the ramp time is about 75μs, or “instant on”. However, the debounce feature of the EN pin is not disabled.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Gamma correction will vary the step size of the current such that the fading of the light appears linear to the human eye. Even though there may be 1000 linear steps for the fading algorithm, when gamma corrected, the actual number of steps could be as low as 63.

Table 2 63 Gamma Steps Correction

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	2	4	6	8	10	12	16
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
20	24	28	32	36	42	48	54
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
60	66	72	80	88	96	104	112
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
120	130	140	150	160	170	180	194
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
208	222	236	250	264	282	300	318
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
336	354	372	394	416	438	460	482
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
504	534	564	594	624	654	684	722
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	
760	798	836	874	914	956	1000	

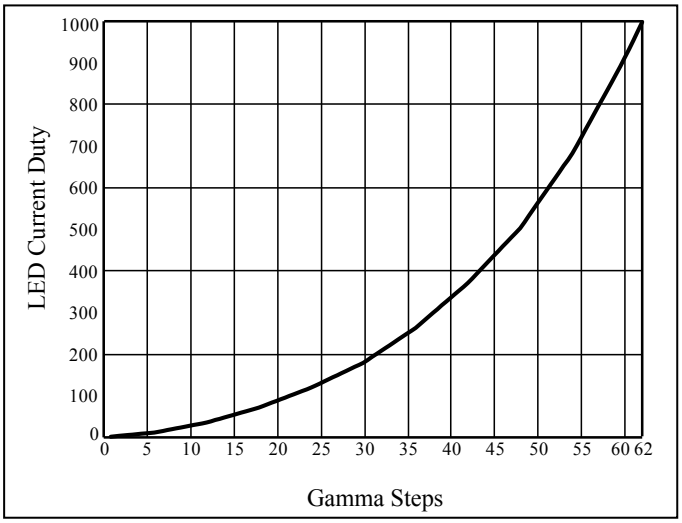


Figure 71 Gamma Correction (63 Steps)

FAULT DETECTION

When VCC voltage exceeds the voltage level which is set by F_UVLO bits in 08h register, the LED open fault detection is enabled. The intention is to prevent false fault reporting during abnormal VCC condition. Such as power up or EMS test condition. An output open circuit fault is detected if the voltage of V_{CC} to OUTx drops below open circuit detection threshold V_{OCD} (Typ. 200mV) and remains for t_{FD_OC} (programmed by DELAY bits in 08h register). The channel (OUT1/2/3) will keep normal sourcing but the corresponding output open circuit flag bit in 07h register will be set to “1” to report the fault and FAULTB pin will be pulled low. When the open condition is removed, the corresponding output open circuit flag bit in 07h register will be reset to “0” and FAULTB pin will recovery to high impedance.

An output shorted to GND fault is detected if the output voltage on a channel drops below the low voltage threshold V_{SCD} (Typ. 1.8V) and remains below the threshold for t_{FD_SC} (Typ. 5ms). The channel (OUT1/2/3) with the short condition will reduce its output current to 4mA and set the corresponding output short circuit flag bit in 07h register to "1" and FAULTB pin will be pulled low. When the short condition is removed, the output current will recover to original value and the corresponding output short circuit flag bit in 07h register will be reset to "0" and FAULTB pin will recovery to high impedance.

The FAULTB pin is an open drain structure. When a fault is asserted, the pin will change from high impedance to pull low state. If it is externally connected to a pull-up resistor, it will be at the pull-up voltage after fault is released.

The detect action and FAULTB pin reporting of the open/short circuit can be disabled by 0Ah register. A FAULTB pin assertion of open detection can be delayed that can be set by DELAY bits in 08h register.

When the ISET pin is shorted to GND and output current is larger than limit value, about 205mA for OUT1/2 and 40mA for OUT3, the output current will be clamped. Once the short fault condition is removed, the output current will recover to its original value.

OVERTEMPERATURE PROTECTION

The device features an integrated thermal rollback feature which will reduce the output current in a linear fashion if the silicon temperature exceeds 145°C (Typ.). In the event that the die temperature continues to increase, the device will enter thermal shutdown if the temperature exceeds 175°C.

THERMAL ROLLOFF

The output current will be equal to the set value as long as the die temperature of the IC remains below 145°C (Typ.). If the die temperature exceeds this threshold, the output current of the device will begin to reduce at a rate of 3.8%/°C until 5% of I_{OUT} and turn off after this current level.

The thermal rolloff function can be disabled by the TEN bit in 01h register.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 175°C, the output channel will go to the "OFF" state and TSD bit in 07h register will be set to "1" and FAULTB pin will be pulled low. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to < 145°C will be blocked and the IC will not be allowed to restart. Once restart, the TSD bit in 07h register will be reset to "0" and FAULTB pin will recovery to high impedance.

The FAULTB pin reporting of the thermal shutdown protection can be disabled by TSDREN bit in 0Ah register.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (6):

$$P_D = V_{CC} \times I_{CC} + \sum_{x=1}^{3} (V_{CC} - V_{LEDx}) \times I_{OUTx} \qquad (6)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (7)$$

Where I_{CC} is the IC quiescent current, V_{CC} is the supply voltage, V_{LED} is the voltage across VCC to OUT and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (8):

$$P_D < P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (8)$$

So,

$$P_D < \frac{125°C - 25°C}{34°C/W} \approx 2.94W$$

Figure 72, shows the power derating of the IS32LT3129A on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

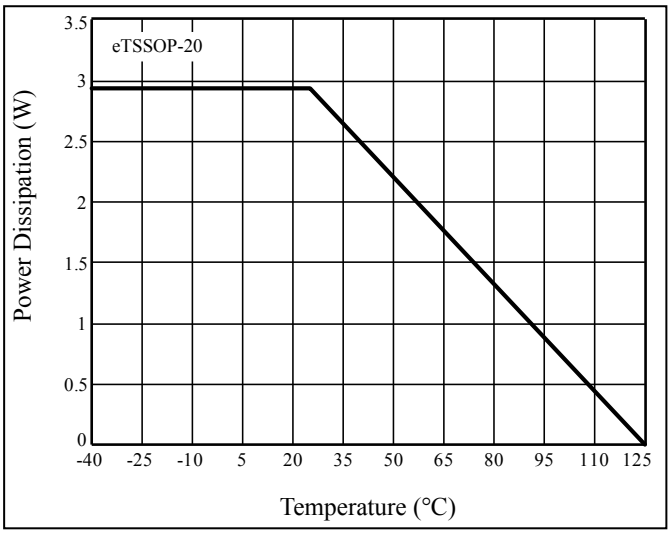


Figure 72 Dissipation Curve

The thermal resistance is achieved by mounting the IS32LT3129A on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3129A. Multiple thermal vias, as shown in Figure 73, help to conduct the heat from the exposed pad of the IS32LT3129A to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink or thicker copper plane.

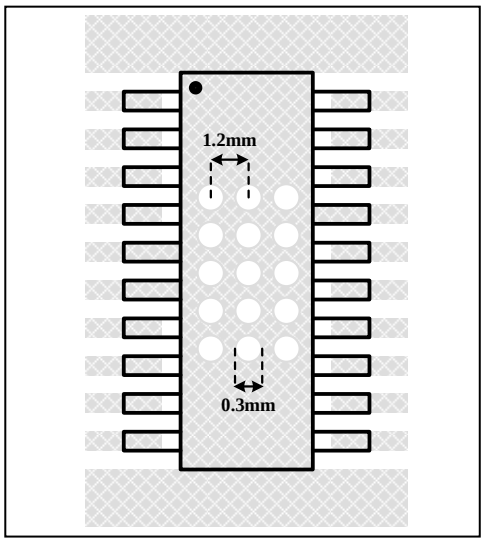


Figure 73 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

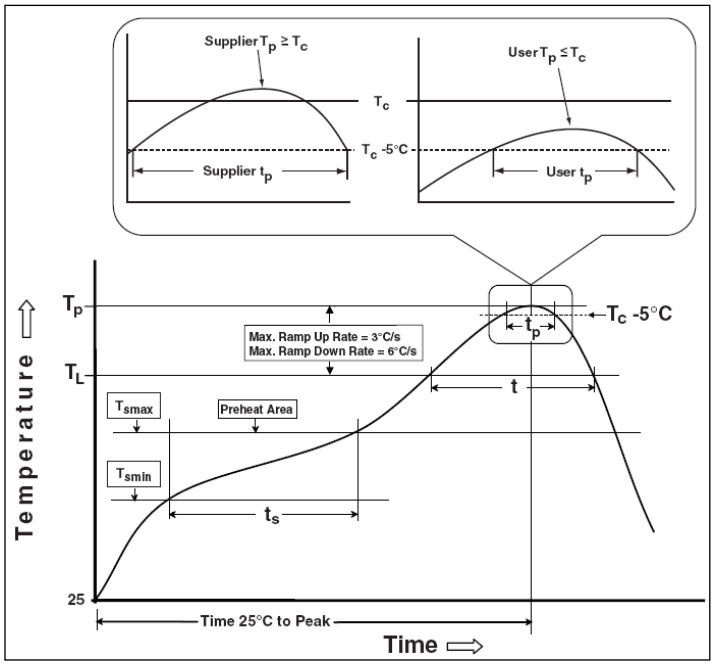
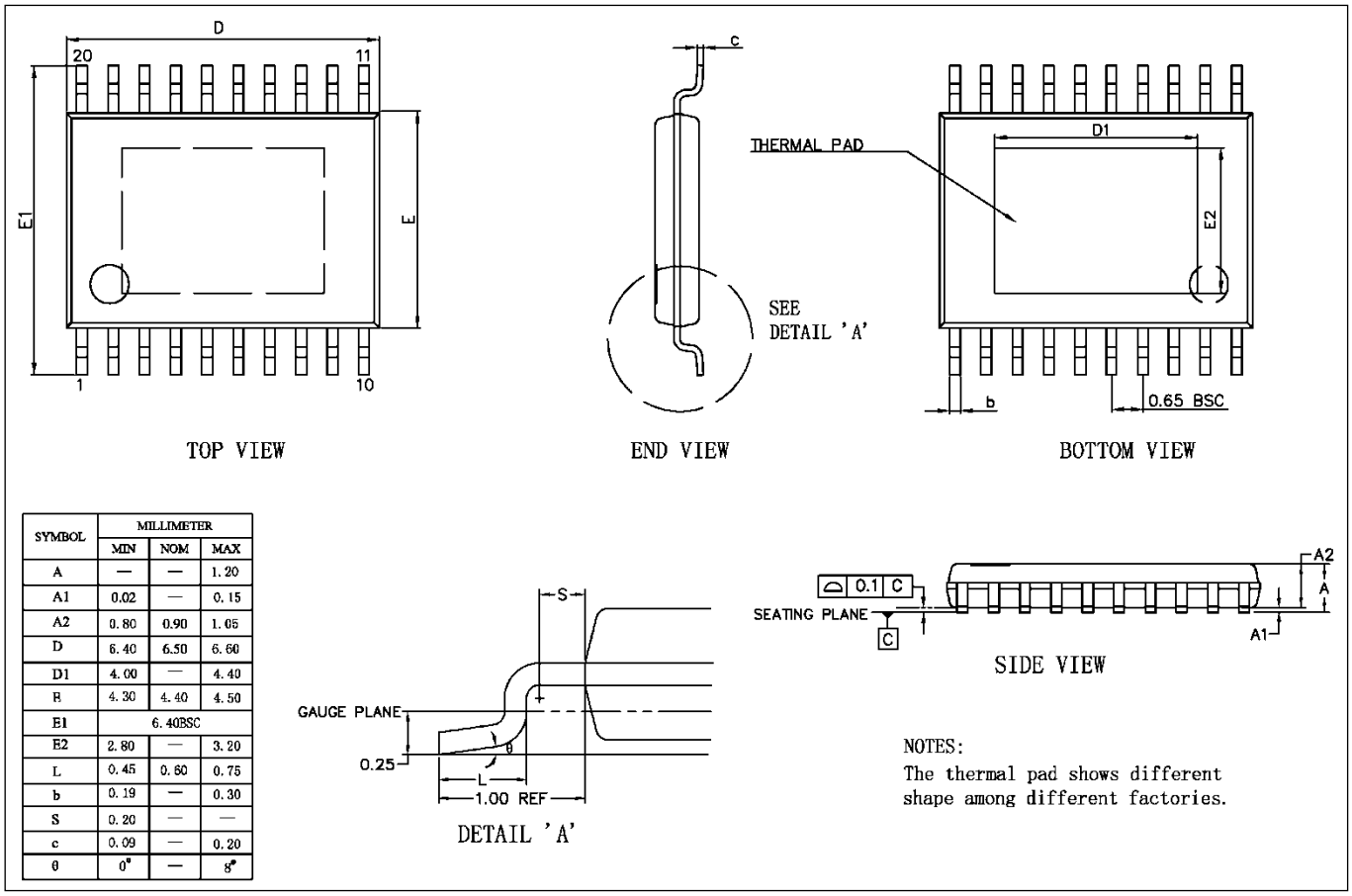


Figure 74 Classification Profile

PACKAGE INFORMATION

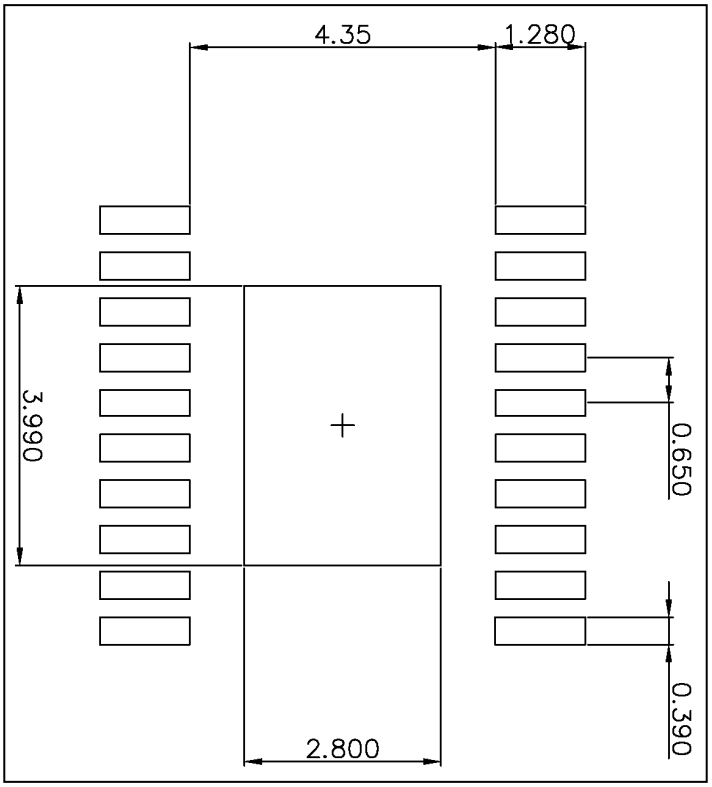
eTSSOP-20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.02	—	0.15
A2	0.80	0.90	1.05
D	6.40	6.50	6.60
D1	4.00	—	4.40
E	4.30	4.40	4.50
E1	6.40BSC		
E2	2.80	—	3.20
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

RECOMMENDED LAND PATTERN

eTSSOP-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.