# 12-CHANNEL LED ANIMATION CONTROLLER

## GENERAL DESCRIPTION

IS32LT3134 is a 12-channel LED driver with an embedded animation controller. Multiple IS32LT3134's can be cascaded in the same board design. Four animation patterns, pin-selectable, can be stored in the embedded Flash of each device. The patterns are played by a host controlling the input pins of the devices. For each pattern, two modes can be pre-defined: cascade mode, one device after the other; synchronous mode, all devices simultaneously.

IS32LT3134 is provided with a GUI on Windows PC for design and playback of the animation patterns when connected to a Lumissil evaluation board or a customer designed board with IS32LT3134. An In-System-Programming ("ISP") mode is provided for programming patterns into individual device when the ISP pin is asserted. GUI also provides a tool to automatically detect device position and assign device address when more than one IS32LT3134's is on the same board.

A watchdog timer is used to check if the animation reaches the end of the pattern in anticipated time, if not a fault is generated. In addition, short circuit condition of the LED output is also detected. If any of the above fails, the Fault pin will be asserted. There are two options under the fault condition: "one fails, all fail" or "one fails, others continue." The former would stop animation on all devices while the latter stop only the animation of the faulted IS32LT3431.

IS32LT3134 is available in WFQFN-24 package. It operates from 3.0V to 5.5V over the temperature range of -40°C to +125°C.

## FEATURES

- Supply voltage range: 3.0V to 5.5V
- UART interface operating at 19.2K supports dynamic addressing mode
- 12-channel push-pull outputs driver for common anode, common cathode, or multiplexed LED drive modes
- Duration of animation is from 0.1s up to 15s
- User programmable internal clock pre-scalar
- Four pattern banks each with 12KB Flash
- Watchdog timer to monitor valid clock signals and end of animation pattern; Fault is asserted when errors detected by the WDT
- Animation end pin signaling the end of a synchronous pattern for all devices, a start of animation of the next cascading device or the end of cascading pattern if it's asserted by the last device in the row.
- Support programmable duty cycle for dimming
- Programmable clock frequency by deriving from 16MHz internal oscillator with
- Clock input for external clock option
- WFQFN-24 package

## APPLICATIONS

- Taillight animation module with digital interface
- Interior light animation module with digital interface

## TYPICAL APPLICATION CIRCUIT

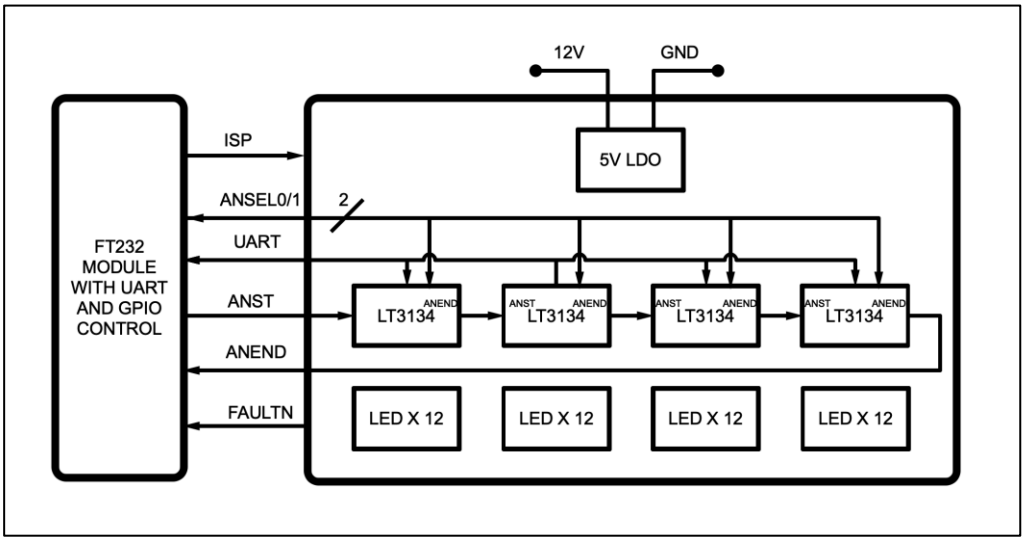
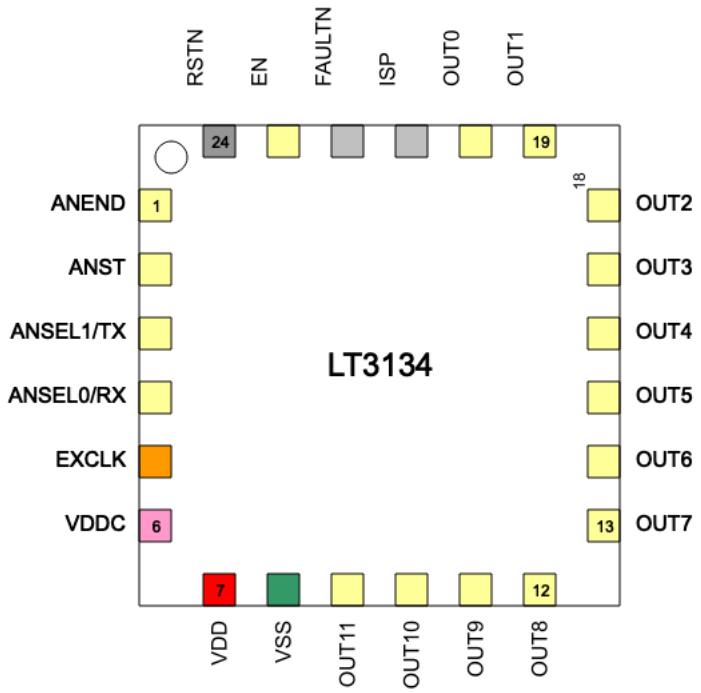



Figure 1 Typical Application Circuit: four LT3134 cascading for control of 48 LEDs

Note:

1. IC should be placed far away from the antenna in order to prevent the EMI.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| QFN-32 |  |

## PIN CONNECTION

| No. | Pin | Description |
|---|---|---|
| 1 | ANEND | ANEND = 1, when animation reaches the end |
| 2 | ANST | ANST = 1, start animation with selected pattern |
| 3 | ANSEL1/TX | Pattern selection pin; also serve as ISP UART TX. |
| 4 | ANSEL 0/RX | Pattern selection pin; also serve as ISP UART RX. |
| 5 | EXCLK | External input of pattern clock: 100 Hz – 400 Hz |
| 6 | VDDC | 1.5V internal regulator output; 0.1uF/1uF capacitors connected to VSS are required |
| 7 | VDD | Input voltage: 3.0V – 5.5V |
| 8 | VSS | Ground |
| 9-20 | OUT0 – OUT11 | Push-pull outputs for driving LEDs |
| 21 | ISP | ISP = 1, enter ISP mode; ANSEL0=RX, ANSEL1=TX |
| 22 | FAULTN | Open drain I/O; asserted when errors are detected |
| 23 | EN | EN = 0, enters low power mode |
| 24 | RSTN | Reset with on-chip pull-up resistor |

## ORDERING INFORMATION

### Industrial Range: -40°C to +125°C

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS32LT3134-QWLA3-TR | Wettable Flank QFN-24, Lead-free | 2500 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | -0.3V ~+6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}$+0.3V |
| Maximum junction temperature, $T_{JMAX}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~+150°C |
| Operating temperature range, $T_A$=$T_J$ | -40°C ~ +125°C |
| Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), $\theta_{JA}$ | 29°C/W |
| ESD (HBM)<br>ESD (CDM) | ±2kV<br>±750V |

Note 2:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

The following specifications apply for VCC= 5V, TA= 25°C, unless otherwise noted.

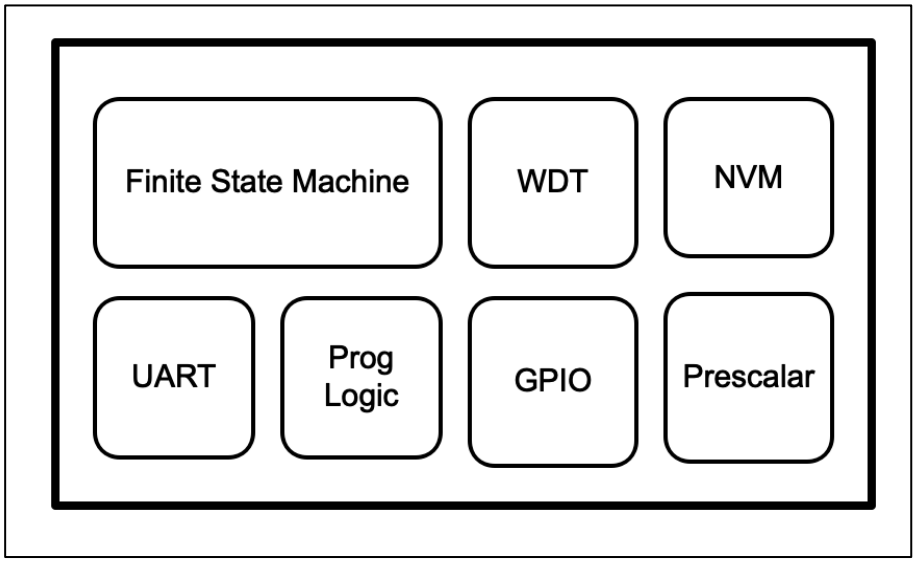
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3.0 | | 5.5 | V |
| $I_{SD}$ | Shutdown current | | | 1 | | uA |
| $I_{IL}$ | Logic “0” input current | (Note 3) | | 12 | | mA |
| $I_{OH}$ | Logic “1” output current | (Note 3) | | 4 | | mA |
| $V_{IL}$ | OUT0-OUT11 | (Note 3) | | 0.5 | | V |
| $V_{OH}$ | OUT0-OUT11 | (Note 3) | | $V_{DD}$-0.5 | | V |
| **Logic Electrical Characteristics (ANEND, ANST, ANSEL1/2, FAULTN)** | | | | | | |
| $V_{OL}$ | Logic “0” input voltage | | GND | | 0.2$V_{DD}$ | V |
| $V_{IH}$ | Logic “1” input voltage | | 0.75$V_{DD}$ | | $V_{DD}$ | V |
| $V_{HYS}$ | Input Schmitt trigger hysteresis | | | 0.2 | | V |
| $I_{IL}$ | Logic “0” input current | (Note 3) | | 5 | | nA |
| $I_{IH}$ | Logic “1” input current | (Note 3) | | 5 | | nA |

## DIGITAL INPUT UART SWITCHING CHARACTERISTICS (NOTE 5)

| Symbol | Parameter | Fast Mode | | | Units |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $f_{SCL}$ | Serial-clock frequency | - | | 400 | Hz |
| $t_R$ | Rise time of both SDA and SCL signals, receiving (Note 3) | - | 3 | | us |
| $t_F$ | Fall time of both SDA and SCL signals, receiving (Note 3) | - | 3 | | us |

Note 3: Guaranteed by design

## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

### UART INTERFACE

IS32LT3134 uses UART-based serial bus. Each frame contains a start byte, synchronous byte, command byte, address byte, data bytes, and checksum byte. Each byte has one start bit, eight data bit, and one stop bit without parity. The LSB follows the start bit as follows:

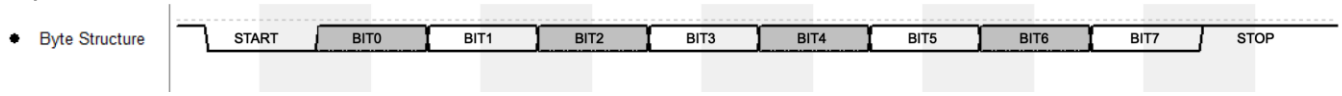



Figure 1. Byte structure

Slave address position detection (SAPD) can be achieved by bus command cascading method (BCCM).

Once a slave device receives a communication frame, it firstly verifies checksum. If the checksum is correct, the slave replies an acknowledge. If the communication frame is longer than timeout timer (1.5 times of a frame period), the slave will reset and wait for next synchronization on a new frame. If the communication fail, the master cannot receive a feedback from the slave. The master should wait for a timeout timer before retransmitting and the slave should clear his receiving buffer.

Both write or readback supports burst mode. Figure 1 and Figure 2 show Frame Structure.

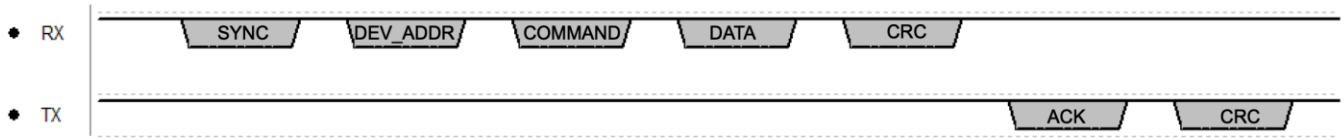



Figure 2, Write command with ACK feedback

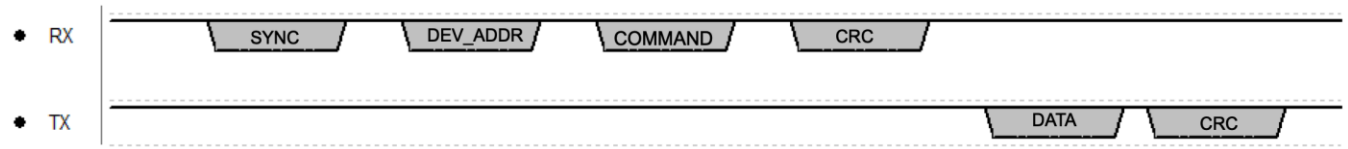



Figure 3, Read command with ACK feedback

Table 1 Frame Structure:

| Byte Name | Length | Description |
|---|---|---|
| SYNC | 1 | Synchronization byte sent from Master |
| DEV_ADDR | 1 | Device address, Read/Write Command, Burst mode |
| COMMAND | 1 | Device configuration, Pattern configuration |
| DATA | 0, 2, 8, 256 | Data byte |
| ACK | 1 | Acknowledge, reply ID number |
| CRC | 1 | CRC for Dev_Add and all Data |

**SYNC**

SYNC is 0x55. The first byte is a frame header. It can be a synchronization signal came from master. Based on the signal, slaves can adjust internal UART's clock automatically.

Table 2 Description of DEV_ADD byte

| Bit. | Field | Description |
|---|---|---|
| 3-0 | Device address | FL3134 protocol can define maximum 16 slave devices |
| 5-4 | Data Length | 00: single byte command with 0 byte of data<br>01: single byte command with 2 byte of data<br>10: burst mode with 8 bytes of data<br>11: burst mode with 256 bytes of data |
| 6 | Broadcast | Single device = 0; Broadcast = 1 |
| 7 | Read/Write | Read = 0; Write = 1 |

Table 3 UART Commands

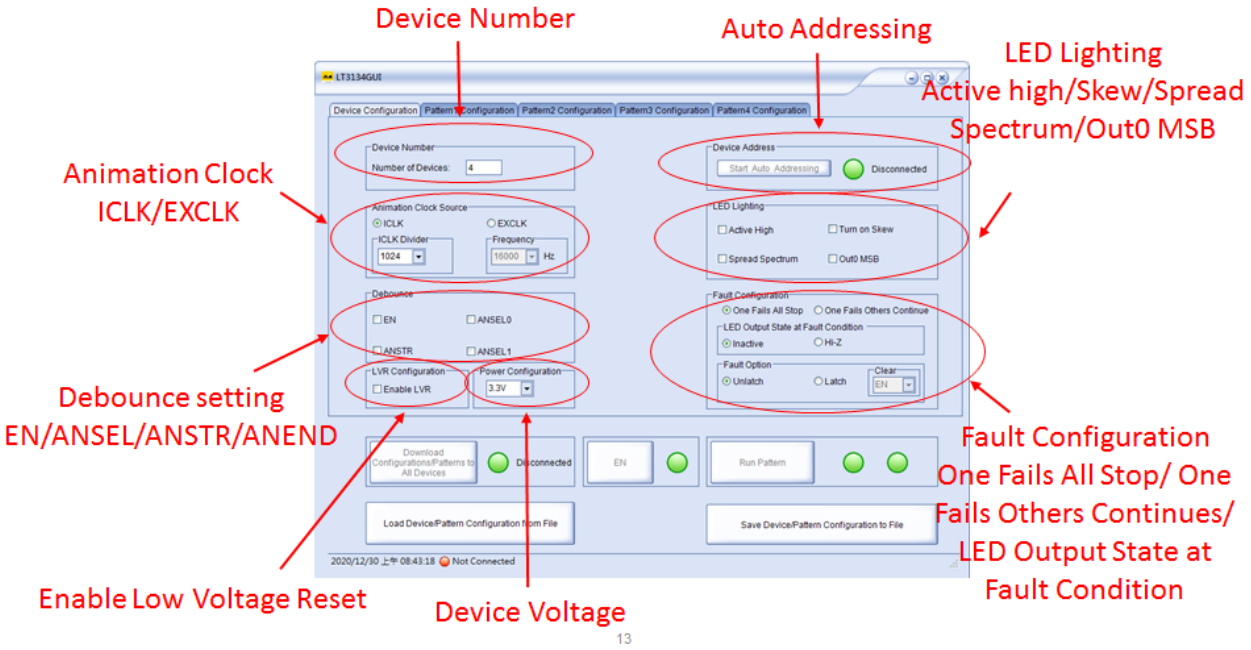
| Command No. | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Description |
|---|---|---|---|---|---|
| | CMD[3] | CMD[2] | CMD[1] | CMD[0] | |
| 0 | 0 | 0 | 0 | 0 | SAPD-RESET |
| 1 | 0 | 0 | 0 | 1 | SAPD |
| 2 | 0 | 0 | 1 | 0 | SAPD-END |
| 3 | 0 | 0 | 1 | 1 | ISP IFB FF |
| 4 | 0 | 1 | 0 | 0 | ISP IFB CF |
| 5 | 0 | 1 | 0 | 1 | ISP FF |
| 6 | 0 | 1 | 1 | 0 | ISP CF |
| 7 | 0 | 1 | 1 | 1 | MCU Part Number |
| 8 | 1 | 0 | 0 | 0 | Firmware version |

Bit 7 – 4 are all 0

**GUI Features**

- Animation Clock Source
  - ICLK(16000khz)
  - EXCLK(1khz)
- Debounce setting for EN/ANSEL/ANSTR/ANEND
  - Debounce time 530usec
- LED Lighting
  - Active High: When Pattern Bit[11-0] output on/off bit is 1, push-pull drivers high level, and vice versa.
  - Turn on Skew:
  - Spread Spectrum Enable: spread spectrum frequency change.
  - Out0 MSB: Push-Pull output 0 to port 11 start with Pattern Bit[11-0] MSB.
- Fault Configuration
  - One fails all stop/One fail others continue
  - LED status at Fault condition
  - Inactive/Hi-Z
- Vector Clock
  - Programmable clock divider
- Global dimming at end of animation
  - Delay after the Last Vector
  - Dimming step Duration
  - Dimming Duty per step
- Synchronous Signal
  - Synchronous
  - Cascading

## GUI Device Configuration

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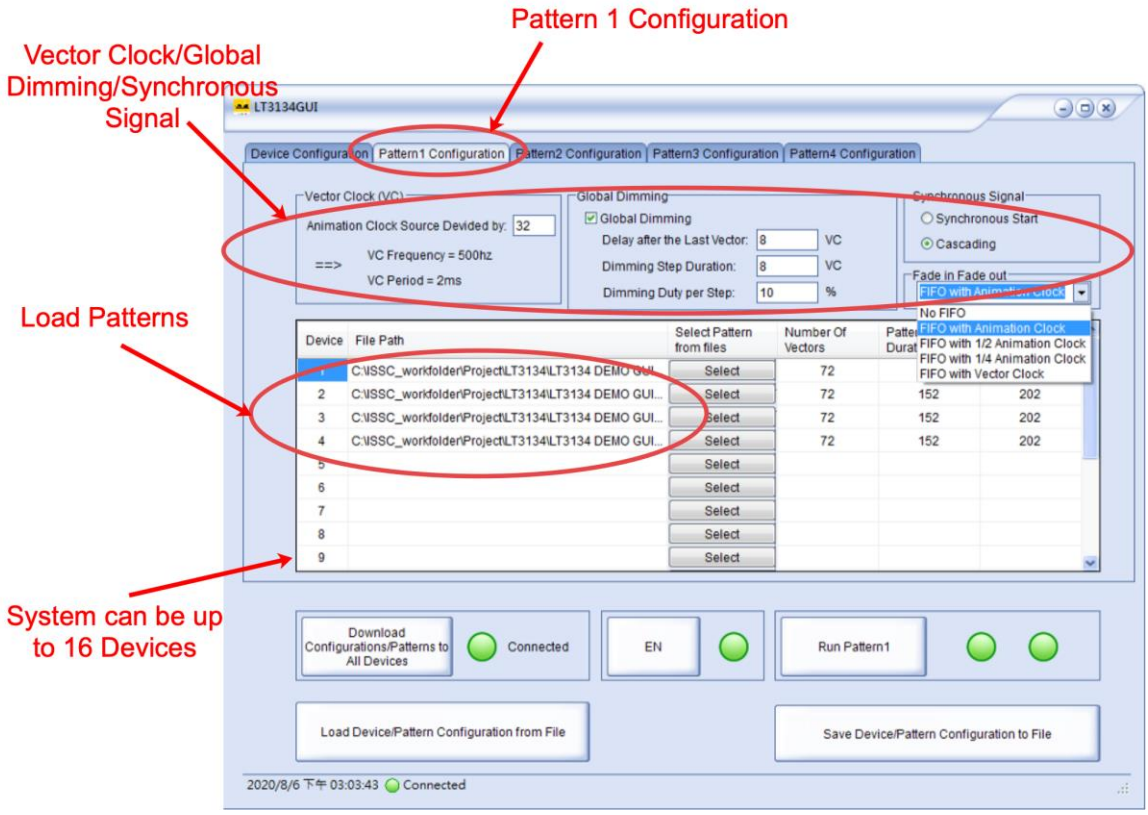
## GUI Patterns Configuration



## CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| Preheat & Soak<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

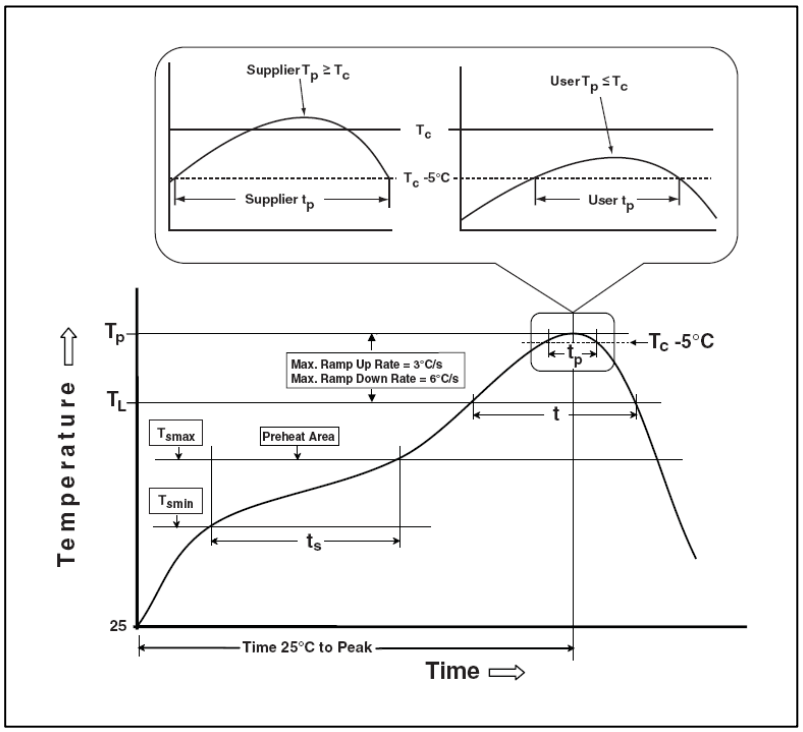
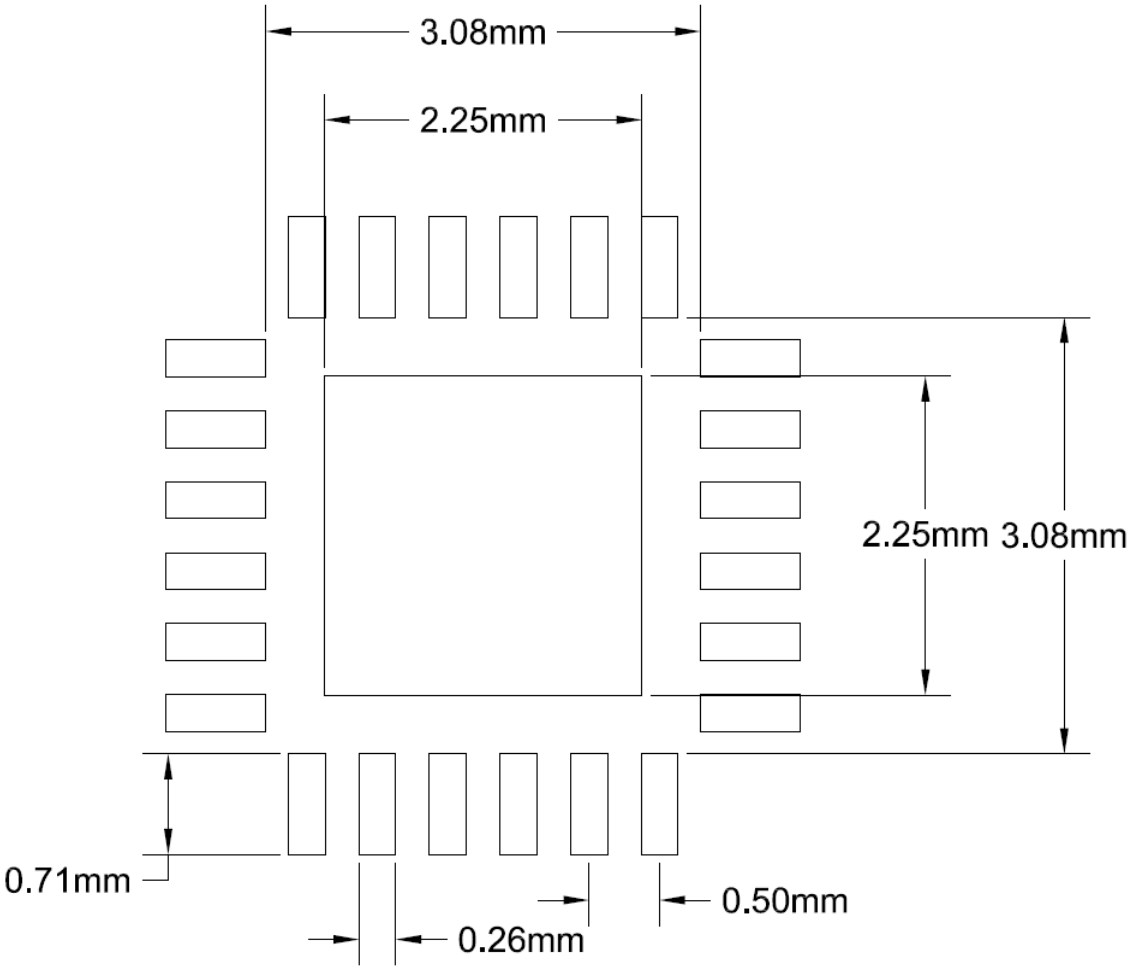



Figure 15 Classification Profile

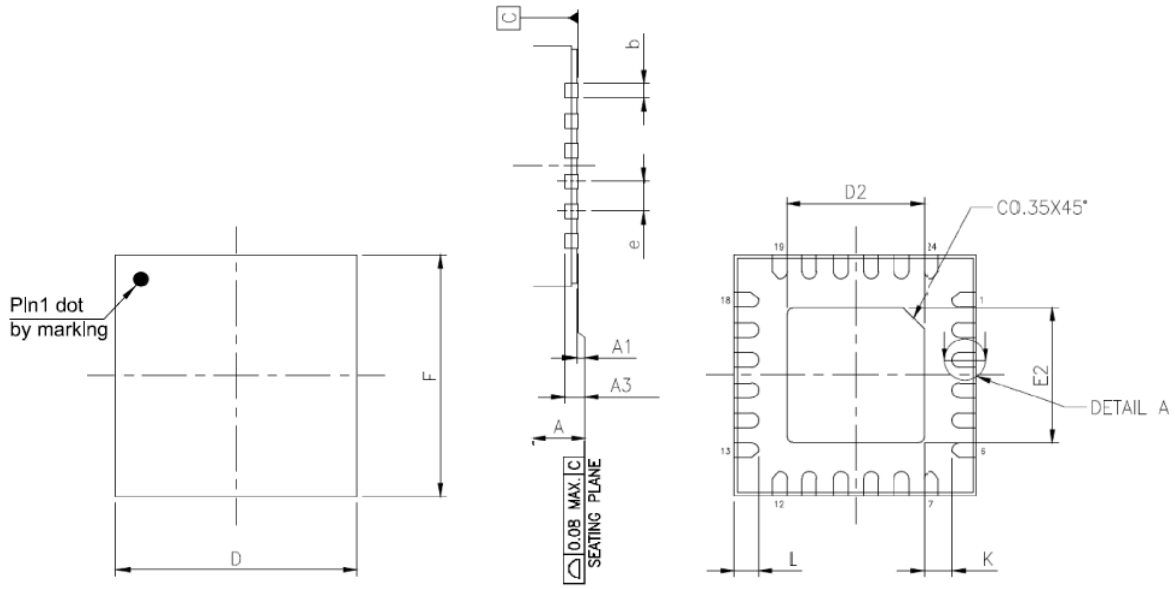
## PACKAGE INFORMATION

### Wettable Flank QFN-24

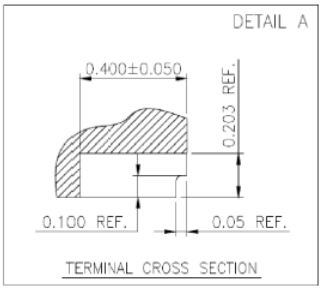
### RECOMMENDED LAND PATTERN



## POD




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203REF | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 4.0BSC | |
| E | | 4.0BSC | |
| D2 | 2.20 | 2.25 | 2.30 |
| E2 | 2.20 | 2.25 | 2.30 |
| L | 0.35 | 0.40 | 0.45 |
| e | | 0.50BSC | |
| K | 0.20 | - | - |




NOTE:

CONTROLLING DIMENSION: MM

REFERENCE DOCUMENT: JEDEC MO-220