IS32LT3959

HIGH VOLTAGE ASYNCHRONOUS BUCK, BOOST AND BUCK-BOOST LED LIGHTING CONTROLLER

November 2021

GENERAL DESCRIPTION

The IS32LT3959 is a wide voltage range asynchronous, multi-topology PWM controller that employs a single inductor to provide excellent constant high current regulation to LEDs with a cathode ground reference. In a Buck-Boost topology, a regulated output current is maintained when the input voltage is either less or greater than the desired output LED string forward voltage, making it especially suitable for automotive applications, where this wide input voltage variation is expected. With a 150kHz~650kHz programmable switching frequency that can be adjusted with an external resistor or synchronized by an external clock, optimum inductor and capacitor(s) can be achieved while maintaining a high efficiency. The controller integrates a spread spectrum function that efficiently reduces the overall EMI profile.

The IS32LT3959 can also be configured for single switch Buck or Boost operation for lower BOM cost and higher efficiency.

The IS32LT3959 supports both analog and digital dimming. It can be dimmed using an external analog input or digitally using either an external PWM or the internal PWM generator. For analog dimming, a DC voltage in the range of 0.4V~2.4V is applied to the ADIM pin. For digital PWM dimming, apply either an external PWM signal on the EN/PWM pin or enable the integrated PWM generator. The device features robust protection functions with fault flag reporting.

The IS32LT3959 is available in eTSSOP-28 package with an exposed pad for enhanced thermal dissipation.

FEATURES

- Wide input voltage: 4.5V to 55V
- Buck, Boost and Buck-boost topologies with LED string cathode reference to GND
- Additional output current regulator to prevent rush current
- ±3% output current accuracy over -40°C~+150°C junction temperature
- Integrated PWM generator:
  - Frequency programmable: 100Hz~2kHz
  - Duty cycle programmable: 5%~95%
- Flexible dimming: analog, external PWM or internal PWM
- Integrated PMOS driver to enable PWM dimming, fault protection and output current regulator
- Adjustable operating frequency: 150kHz-650kHz
  - Spread spectrum for EMI profile optimization
  - External clock synchronization capability
- Internal fixed soft start to avoid inrush current
- 1.5μA shutdown supply current
- Integrated bootstrap diode
- Built-in robust protections with fault reporting:
  - Over voltage protection
  - Secondary over voltage protection
  - LED string open/shorted
  - Output over current
  - Input over current
  - FS/SYNC pin open/shorted
  - FPWM pin open/shorted
  - Thermal shutdown
- AEC-Q100 Qualified
- Operating temperature range from -40°C ~ +150°C junction temperature

APPLICATIONS

- Automotive exterior light applications:
  - Headlight
  - Daytime Running Lamp (DRL)
  - Fog Lamp
  - Turn signal light

TYPICAL APPLICATION CIRCUIT

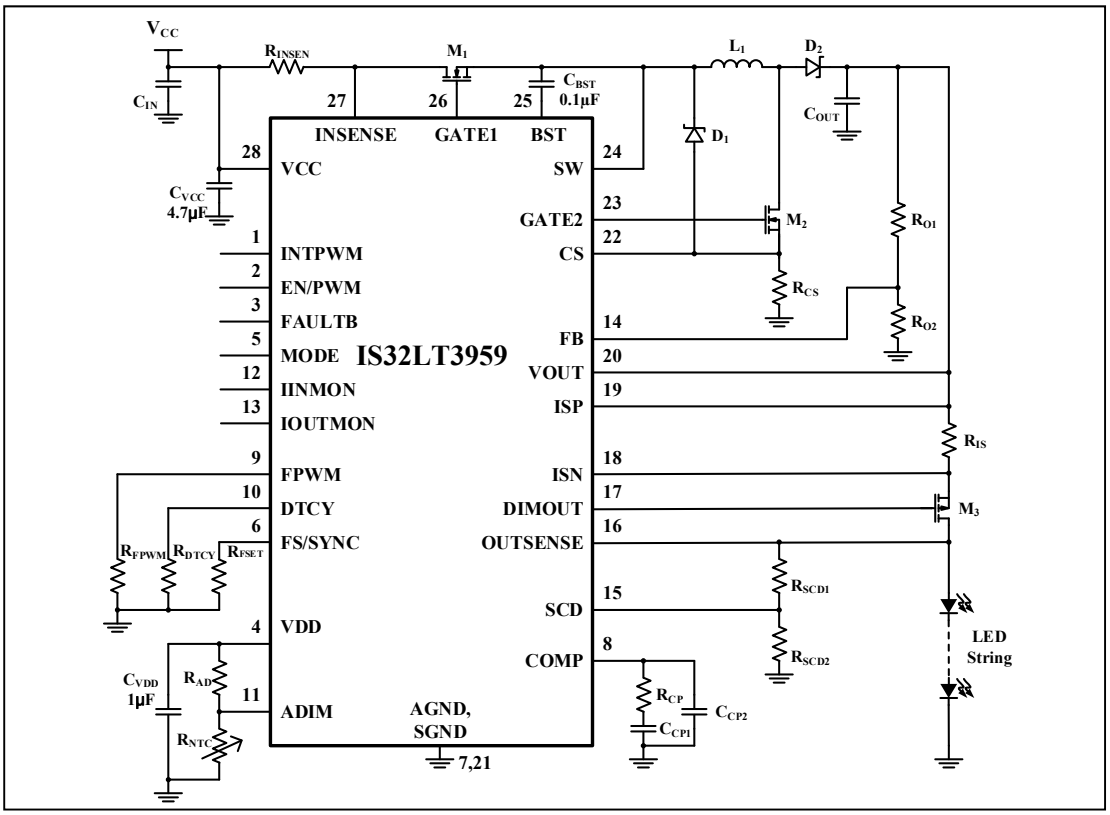


Figure 1 Typical Application Circuit (Buck-Boost Topology)

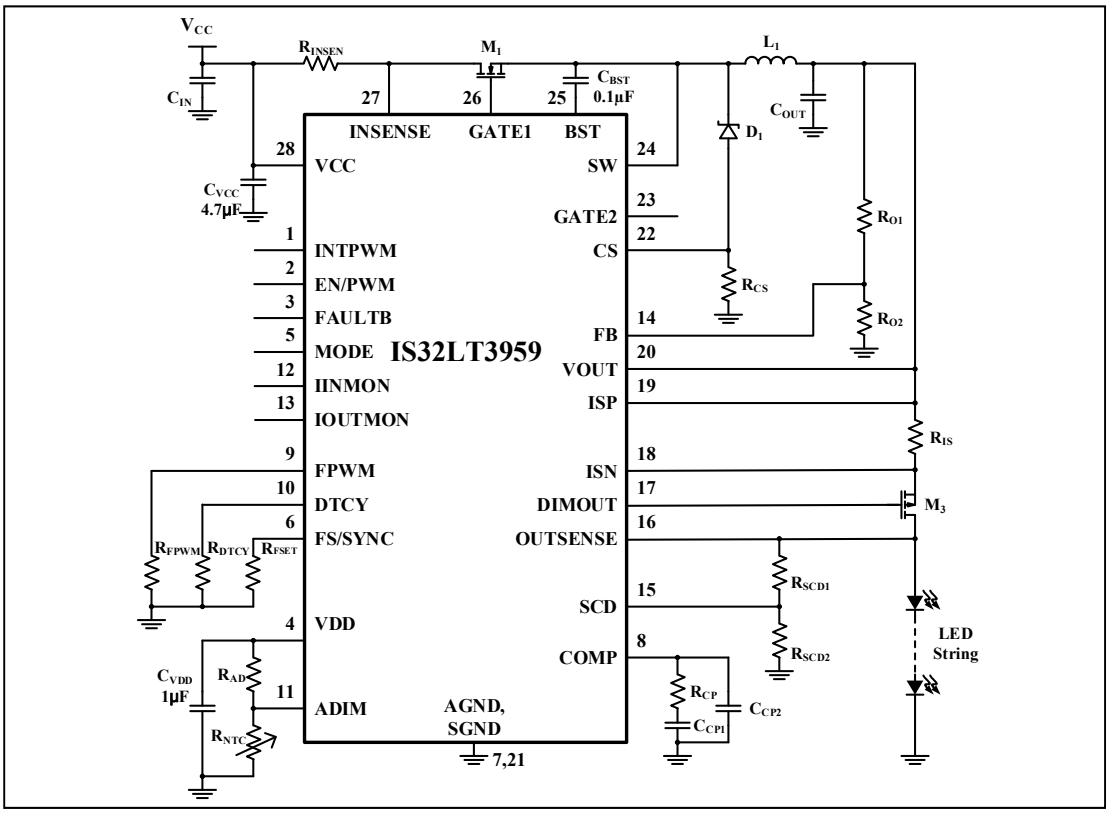


Figure 2 Typical Application Circuit (Buck Topology)

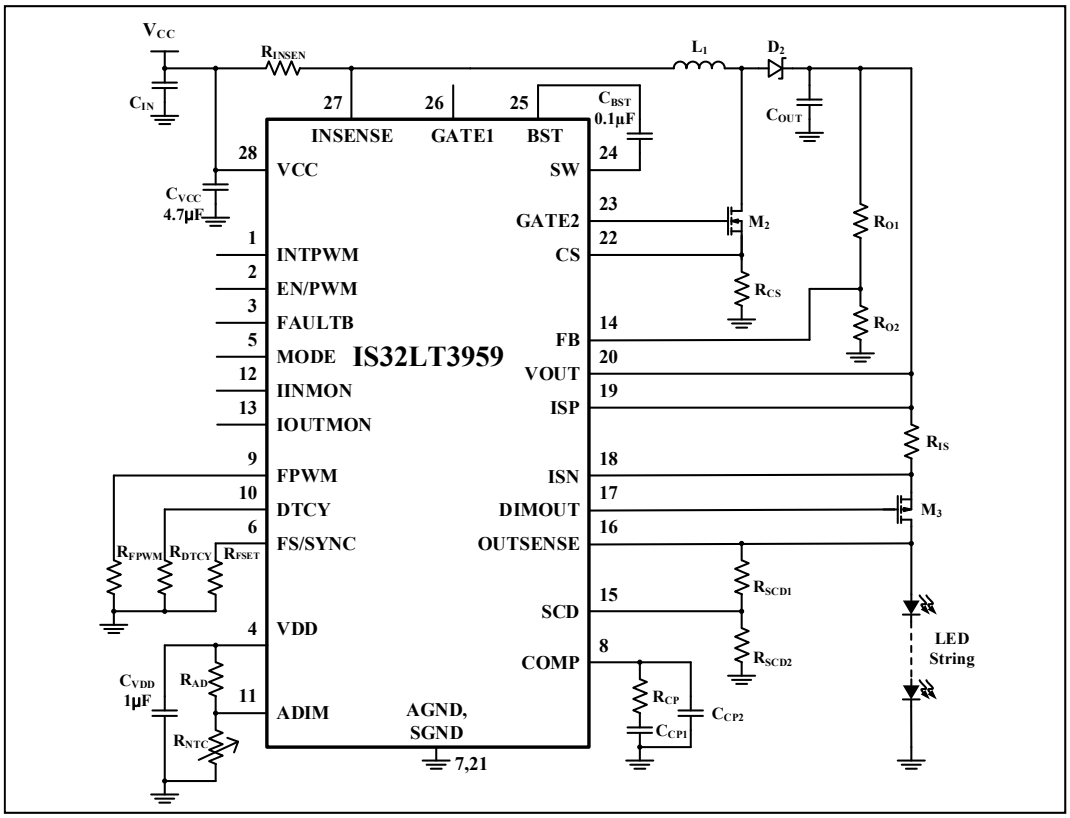
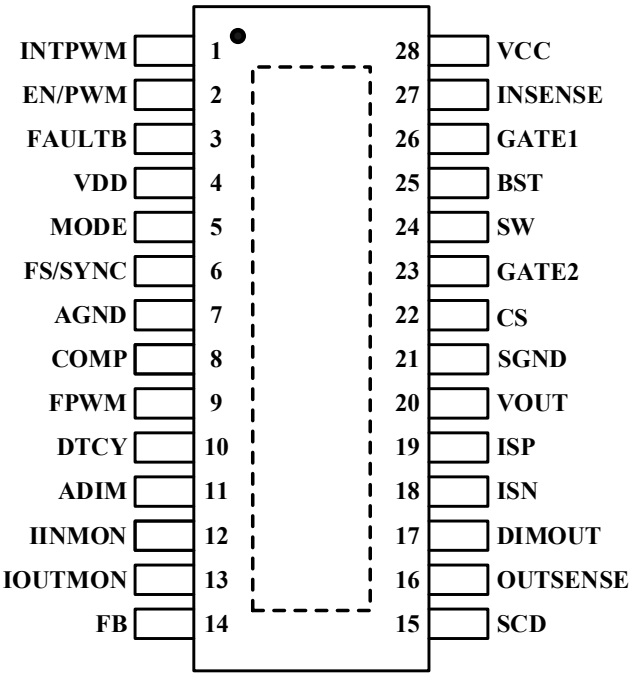


Figure 3 Typical Application Circuit (Boost Topology)

PIN CONFIGURATION

Package	Pin Configurations (Top view)
eTSSOP-28	

PIN DESCRIPTION

No.	Pin	Function
1	INTPWM	Internal PWM generator control pin with an internal 200kΩ pull-down resister. Pulling this pin high disables the internal PWM to achieve 100% LED brightness. Pulling this pin low or left unconnected enables the internal PWM generator to dim the LED string brightness.
2	EN/PWM	Enable and external PWM dimming pin with an internal 200kΩ pull-down resister. Pulling down below 0.8V for over 30ms (Typ.) will shut down the IC. For external PWM dimming, drive this pin with a digital pulse from 0V to a voltage greater than 2V and modulate the pulse width to control LED string brightness.
3	FAULTB	Open drain fault flag output pin. Active low to report a fault condition. Requires an external pull-up.
4	VDD	Internal LDO 6V output. Needs an external capacitor (1μF) to GND placed close to this pin.
5	MODE	External PMOS current regulator function select pin. Connect to VDD to enable or to ground to disable.
6	FS/SYNC	An external resistor on this pin sets the operating frequency range from 150kHz-650kHz. Connect an external clock signal to synchronize the operating frequency with an external source.
7	AGND	Analog ground.
8	COMP	Loop compensation pin.
9	FPWM	Connect an external resistor to GND to set the internal PWM generator frequency in the range of 100Hz to 2kHz.
10	DTCY	Connect an external resistor to GND to set the internal PWM generator duty cycle.
11	ADIM	Analog dimming voltage input. The analog dimming range is 0.4V~2.4V. When the pin voltage is between 2.4V<V_{ADIM}<6V, the output is full current and zero current when V_{ADIM}<0.4V. When 0.4V<V_{ADIM}<2.4V, analog dimming will be achieved. This pin cannot be left floating. Connect it to VDD via a 10kΩ resistor if not used.
12	IINMON	Input current monitor output pin.
13	IOUTMON	Output current monitor output pin.
14	FB	Output voltage feedback pin. This pin is used for output over voltage detection.
15	SCD	Single LED or LED string short detection pin. Do not floating. Tied to VOUT if not used.
16	OUTSENSE	Output voltage sensing pin for PMOS constant current regulator.
17	DIMOUT	Drive an external PMOS for dimming control of LED string, over current protection and output constant current regulation function.
18	ISN	The LED current sense amplifier negative input.
19	ISP	The LED current sense amplifier positive input.
20	VOUT	Output supply pin. This pin must be tied to the power output to determine the buck, boost, or buck-boost operating mode. It also serves as the positive rail of DIMOUT driver.
21	SGND	Driver and current sense ground. It must be directly connected to the ground terminal of the current sense resistor, R_{CS}, to ensure precise sensing.
22	CS	Low-side NMOS current sense and over current detect pin.
23	GATE2	Gate drive to the external low-side NMOS.
24	SW	High-side NMOS source pin.
25	BST	High-side NMOS bootstrap floating driver supply. The BST pin has an integrated bootstrap Schottky diode from an internal 5.5V (Typ.) linear regulator and requires an external bootstrap capacitor (0.1μF) to the SW pin. The BST pin swings from a diode voltage drop below 5.5V to (V_{SW} + 5.5V).
26	GATE1	Gate drive to the external high-side NMOS.
27	INSENSE	Input current sense pin.
28	VCC	Power supply pin.
	Thermal Pad	Connected to large PCB ground plane using multiple vias for good thermal performance.

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3959-ZLA3-TR	eTSSOP-28, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Voltage at VCC, INSENSE, GATE1, SW, INTPWM, ISP, ISN, DIMOUT, FAULTB, SCD, OUTSENSE, VOUT, EN/PWM pins	-0.3V~+60V
Voltage at GATE2, MODE, VDD, FPWM, COMP, FS/SYNC, ADIM, FB, DTCY, CS, IINMON, IOUTMON pins	-0.3V~+6.6V
Voltage at BST pin	-0.3V~+66V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Junction temperature, T_{JMAX}	+150°C
Storage temperature, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, $P_{D(MAX)}$	3.99W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	31.3°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	11.08°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The specifications are at T_J =T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J=T_A= 25°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Input voltage range		4.5		55	V
I_{CC}	Quiescent current	Gate switch off			5	mA
I_{SD}	Shutdown current	EN/PWM=Low for longer than t_{DELAY}		1.5	8	μA
V_{UVLO}	VCC under voltage lock out	V_{CC} falling	3.8	4	4.2	V
V_{UVLO_HY}	VCC under voltage lock out hysteresis			200		mV
V_{DD}	VDD regulator output voltage	I_{VDD}=5mA	5.8	6	6.2	V
I_{VDD_LM}	VDD output current limit	V_{CC}=8V and V_{DD}=4V	25	45		mA
V_{DD_UV}	VDD under voltage lock out	Voltage falling		3.5		V
V_{DD_UVHY}	VDD under voltage lock out hysteresis			0.5		V
V_{BSTUV}	BST-SW under voltage lockout	Voltage rising, GATE1 starts switching		3.6		V
V_{BSTUV_HY}	BST-SW under voltage lockout hysteresis			300		mv
V_{BST_RF}	BST-SW refresh voltage	BOOT start refresh pulse at BOOST mode		3.9		V
t_{SS}	Internal soft-start time		3.5	5		ms

ELECTRICAL CHARACTERISTICS (CONTINUED)

The specifications are at T_J =T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J=T_A= 25°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{OUT}/V_{CC}	Mode transfer from buck to buck-boost		0.745	0.775	0.805	
	Mode transfer from buck-boost to buck		0.67	0.7	0.73	
	Mode transfer from buck-boost to boost		1.27	1.3	1.33	
	Mode transfer from boost to buck-boost		1.195	1.225	1.255	
Oscillator						
f_{SW}	Operating frequency	R_{FSET}=125kΩ	360	400	440	kHz
f_{SYNC}	Synchronous frequency range		150		650	kHz
$V_{FS/SYNC}$	FS/SYNC pin voltage			1		V
V_{IH_SYNC}	FS/SYNC input high threshold		2.0			V
V_{IL_SYNC}	FS/SYNC input low threshold				0.4	V
t_{ON_SYNC}	Synchronization input minimum on-time		300			ns
t_{OFF_SYNC}	Synchronization input minimum off-time		300			ns
SS	Spread spectrum range	(Note 2)		±10		%
f_{SS}	Spread spectrum frequency	(Note 2)		500		Hz
t_{BK_MINON}	Buck minimum ON-time		120	160	200	ns
t_{BK_MINOFF}	Buck minimum OFF-time		120	160	200	ns
t_{BT_MINON}	Boost minimum ON-time		120	160	200	ns
t_{BT_MINOFF}	Boost minimum OFF-time		110	145	180	ns
Current Regulation						
V_{SENSE}	Output current sense threshold (V_{ISP}-V_{ISN})	V_{ADIM}>2.6V, MODE=Low, V_{ISN}= 12V	194	200	206	mV
		V_{ADIM}>2.6V, MODE=High, V_{ISN}= 12V	194	200	206	
	Output current sense threshold (V_{ISP}-V_{ISN}) with analog dimming down to 20% level	V_{ADIM}=0.1333×V_{DD}, MODE=Low, V_{ISN}= 12V, T_J=T_A=+25°C	38.5	40	41.5	mV
		V_{ADIM}=0.1333×V_{DD}, MODE=Low, V_{ISN}= 12V, T_J=T_A=-40°C~ +125°C	36.5	40	43.5	
I_{BIAS_ISP}	ISP pin bias current	V_{ISP}=V_{ISN}=12V		60		μA
I_{BIAS_ISN}	ISN pin bias current	V_{ISP}=V_{ISN}=12V		80		μA
V_{DO_TH}	Output PMOS constant current regulator dropout voltage threshold, including (V_{ISP}-V_{ISN})	V_{ADIM}>2.6V, MODE=High	650	720	800	mv

ELECTRICAL CHARACTERISTICS (CONTINUED)

The specifications are at T_J =T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J=T_A= 25°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I_{BIAS_DO}	Output PMOS constant current regulator gate driver bias current	MODE=High, (V_{ISP}-V_{ISN})=0V		145		μA
I_{BIAS_OS}	OUTSENSE pin bias current	(V_{ISP}-V_{ISN})=200mV, MODE=High, V_{OUT}=$V_{OUTSENSE}$=12V		32		μA
gm_{EA}	Transconductance amplifier gm			455		uS
G_{CS}	The gain from CS to EA COMP out	BUCK		30		
		BOOST		27.5		
Gate Driver						
R_{GATE_PU}	GATE1/2 pins pull-up resistance			3.5		Ω
R_{GATE_PD}	GATE1/2 pins pull-down resistance			2.5		Ω
t_{R_GATE}	GATE1/2 turn on rising time	C_L= 3.3nF		40		ns
t_{F_GATE}	GATE1/2 turn off falling time	C_L = 3.3nF		30		ns
V_{PMOS_GS}	PMOS gate to source drive voltage (V_{OUT}-V_{DIMOUT})	MODE=Low	5.4	6	6.6	V
t_{R_DIMOUT}	DIMOUT turn on falling time	C_L= 3.3nF		100		ns
t_{F_DIMOUT}	DIMOUT turn off rising time	C_L = 3.3nF		100		ns
Current Monitor						
$V_{IOUTMON}$	IOUTMON pin output voltage	(V_{ISP}-V_{ISN})=200mV	1.15	1.2	1.25	V
V_{IINMON}	IINMON pin output voltage	(V_{CC}-$V_{INSENSE}$)=80mV		1		V
Fault Protection						
V_{SENSE_OC}	Output over current protection threshold (V_{ISP}-V_{ISN})		300	350	400	mV
V_{CS_TH1}	Current limit threshold	Buck valley	-77	-67	-57	mV
		Boost peak	67	77	87	
V_{CS_TH2}	Secondary current limit threshold	Buck peak	-125	-110	-95	mV
		Boost peak	95	110	125	
V_{OVP_TH1}	Over voltage protection threshold of FB pin	Voltage rising	1.28	1.33	1.38	V
$V_{OVP\_TH1\_HY}$	Over voltage protection hysteresis of FB pin			80		mV
V_{OVP_TH2}	Secondary over voltage protection threshold via VOUT pin	Voltage rising		58		V
$V_{OVP\_TH2\_HY}$	Secondary over voltage protection hysteresis via VOUT pin			5		V
V_{IN_OCTH}	Input over current protection threshold (V_{CC}-$V_{INSENSE}$)		60	80	100	mV

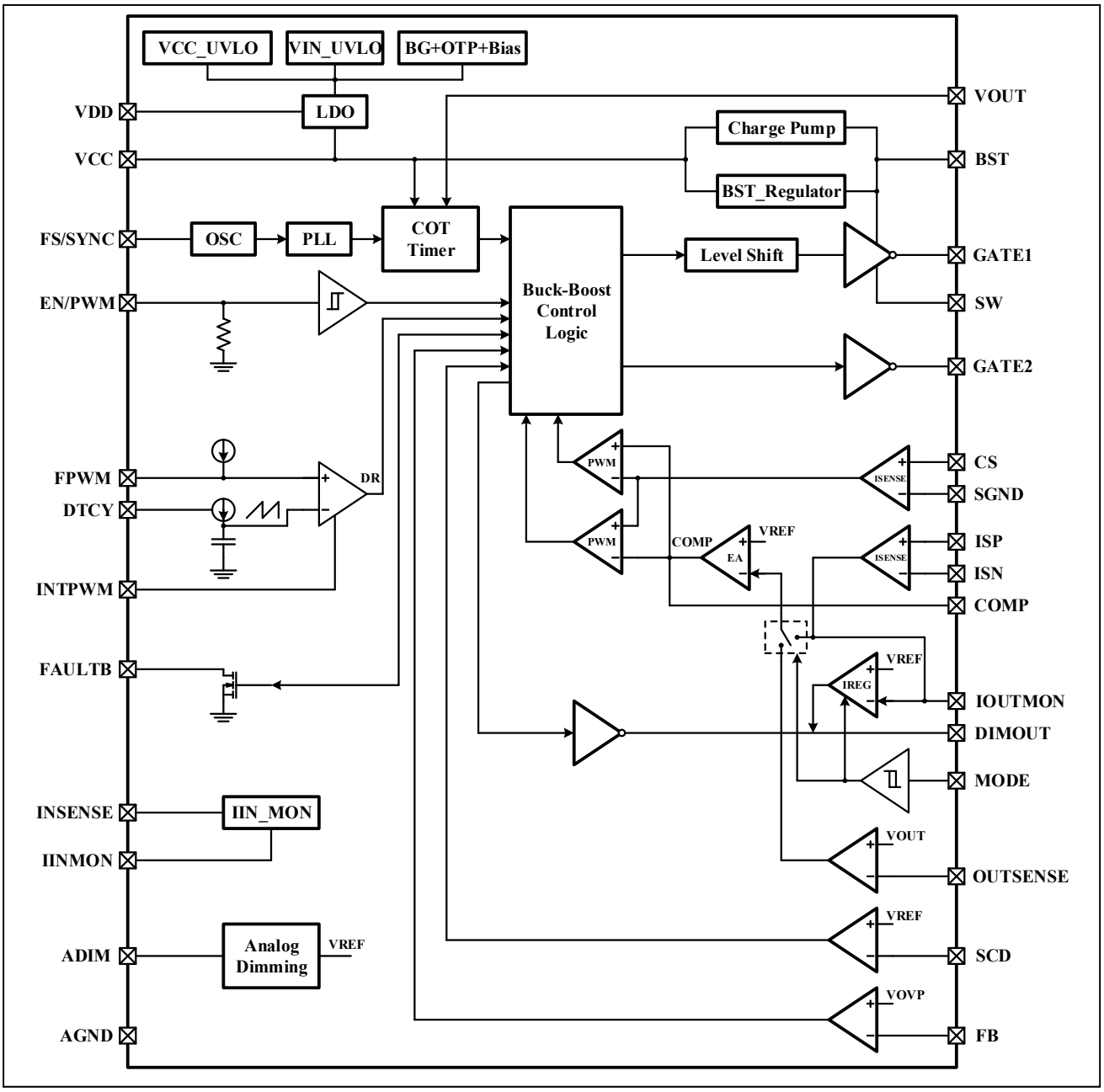
ELECTRICAL CHARACTERISTICS (CONTINUED)

The specifications are at T_J =T_A= -40°C ~ +150°C, V_{CC}= 12V, unless otherwise noted. Typical values are at T_J=T_A= 25°C.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I_{BIAS_INS}	INSENSE pin bias current	V_{CC}=$V_{INSENSE}$=12V		110		μA
t_{SKIP}	Fault protection reset time (Hiccup time)		115	130	145	ms
V_{SCD_TH}	Output LED shorted detection threshold	Voltage falling	1.12	1.15	1.18	V
$V_{SCD\_TH\_HY}$	Output LED shorted detection hysteresis			50		mV
V_{FAULTB_LOW}	FAULTB pull-low voltage	I_{FAULTB} = 1mA		100	200	mV
I_{FAULTB}	FAULTB pin leakage current	No fault condition			1	μA
T_{SD}	Thermal shutdown protection	(Note 2)		170		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 2)		20		°C
Inputs Parameter						
V_{ADIM}	Analog dimming range		0.4		2.4	V
V_{ADIM_FULL}	Analog dimming fully on threshold		2.6			V
V_{ADIM_BF}	Analog dimming blocks output LED short fault detection threshold			0.6		V
V_{ADIM_BFHY}	Analog dimming blocks output LED short fault detection hysteresis			50		mV
V_{IH}	Input high threshold on INTPWM, EN/PWM, MODE pins		2			V
V_{IL}	Input low threshold on INTPWM, EN/PWM, MODE pins				0.8	V
R_{PD}	EN/PWM, INTPWM and MODE pins internal pull-down resistor			200		kΩ
t_{DELAY}	Low voltage persist time on EN/PWM pin to shutdown IC		24	30	40	ms
Internal PWM Generator						
V_{FPWM}	FPWM pin output voltage			0.8		V
f_{PWM_RG}	Internal PWM frequency range		0.1		2	kHz
f_{PWM}	Internal PWM frequency	R_{FPWM}= 40kΩ	450	500	550	Hz
I_{DTCY}	DTCY pin output current			100		μA
D_{PWM5}	Internal PWM duty cycle	R_{DTCY}=1.8kΩ, R_{FPWM}=40kΩ	4.5	5	5.5	%
D_{PWM50}		R_{DTCY}=18kΩ, R_{FPWM}=40kΩ	47	50	53	
D_{PWM80}		R_{DTCY}=28.8KΩ, R_{FPWM}=40kΩ	76	80	84	

Note 2: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

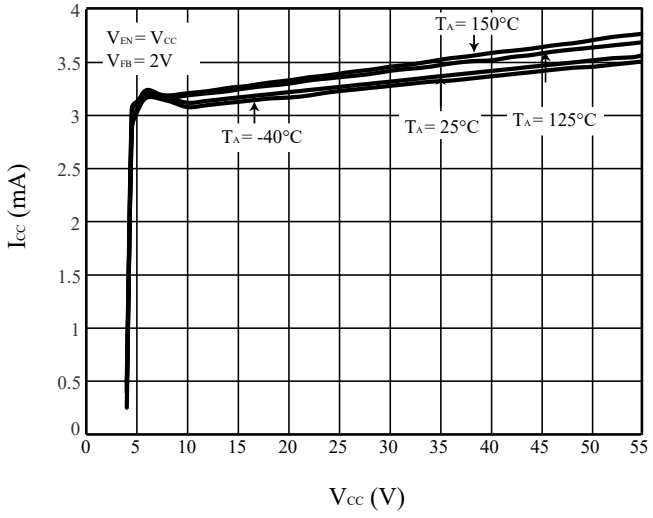


Figure 4 I_{CC} vs. V_{CC}

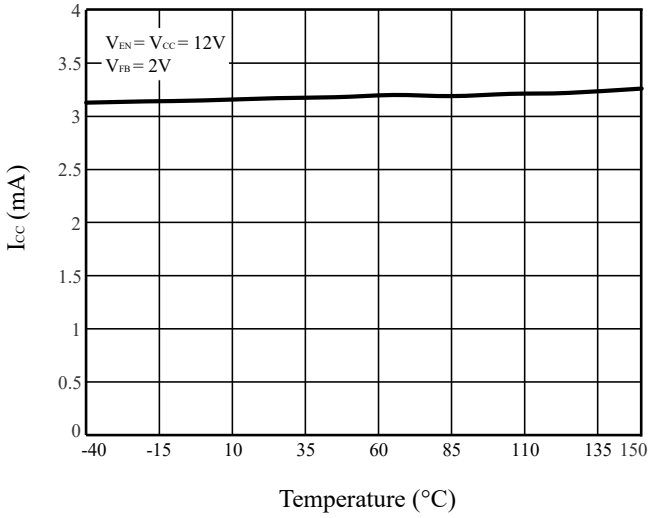


Figure 5 I_{CC} vs. Temperature

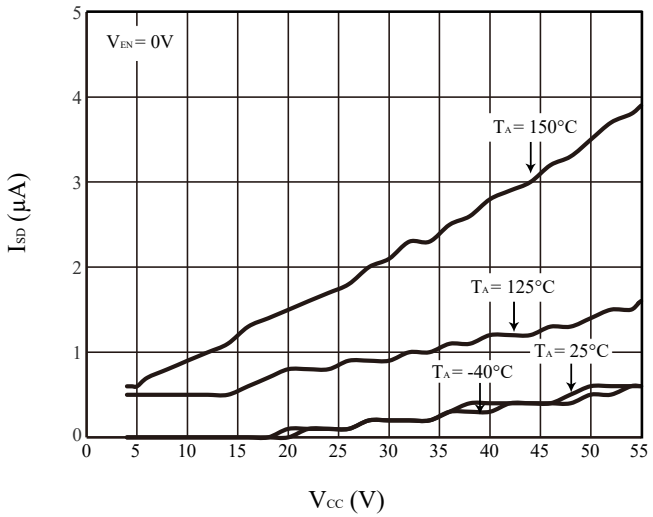


Figure 6 I_{SD} vs. V_{CC}

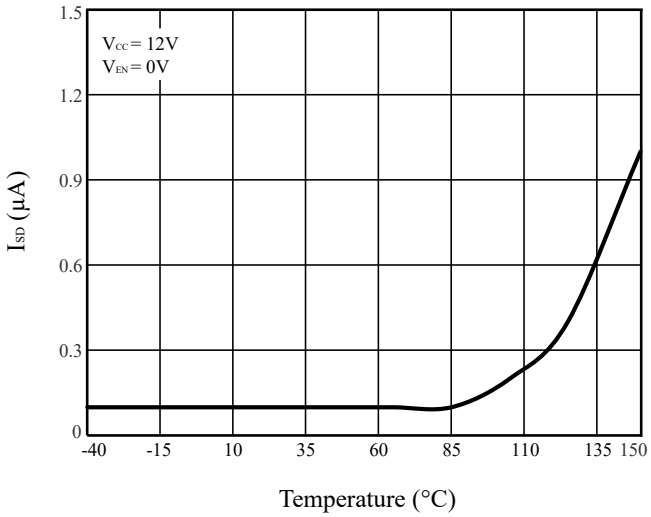


Figure 7 I_{SD} vs. Temperature

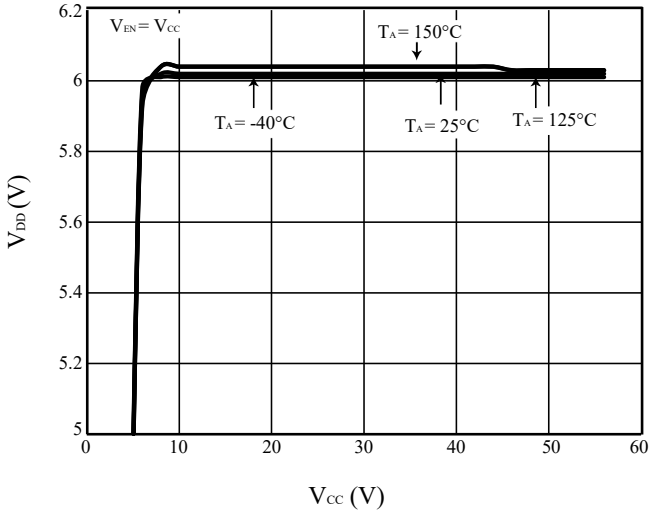


Figure 8 V_{DD} vs. V_{CC}

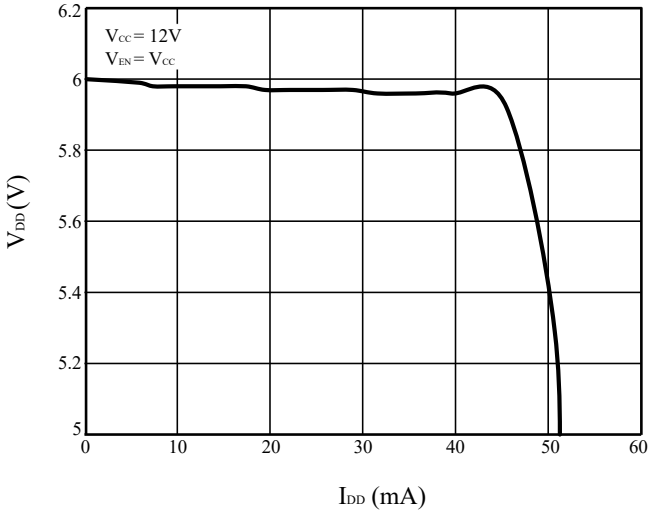


Figure 9 V_{DD} vs. I_{DD}

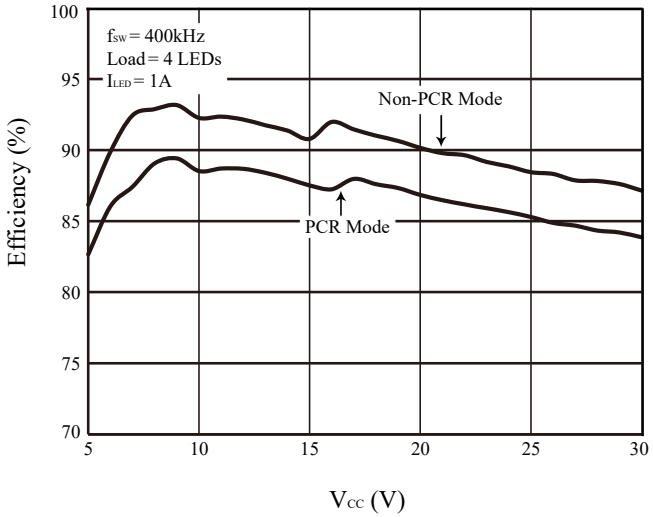


Figure 10 Efficiency vs. V_{CC}

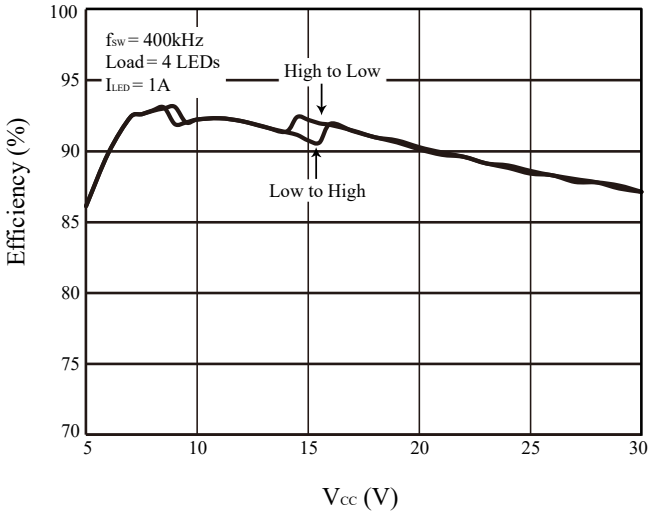


Figure 11 Efficiency vs. V_{CC}

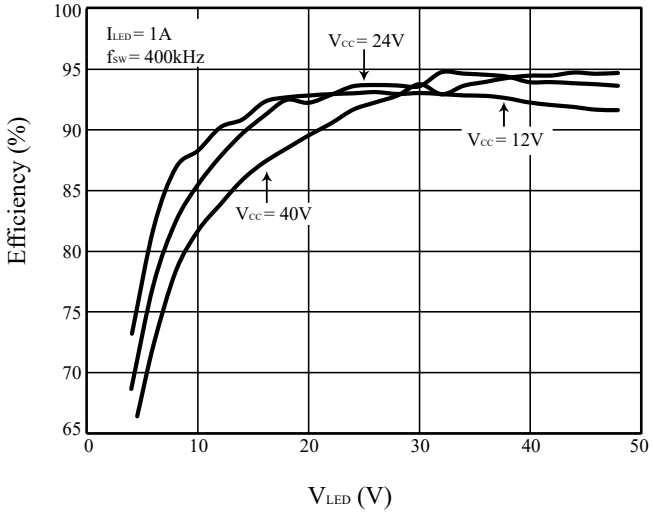


Figure 12 Efficiency vs. V_{LED}

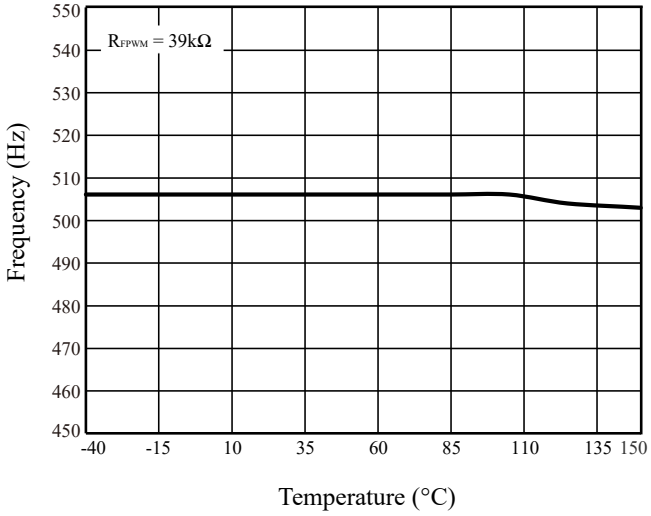


Figure 13 Internal PWM Frequency vs. Temperature

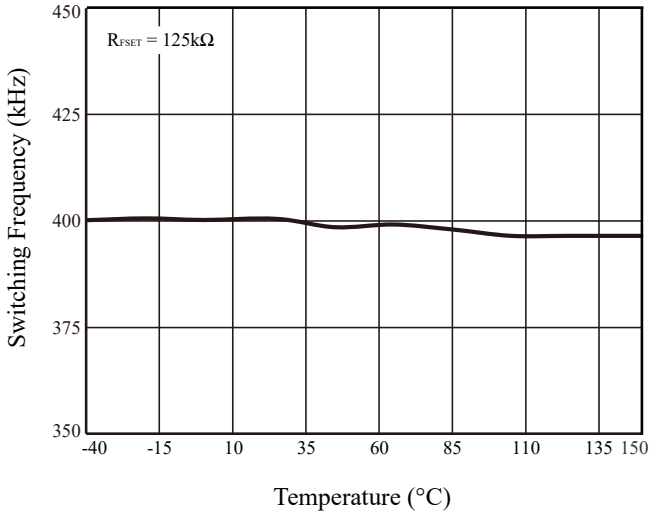


Figure 14 Switching Frequency vs. Temperature

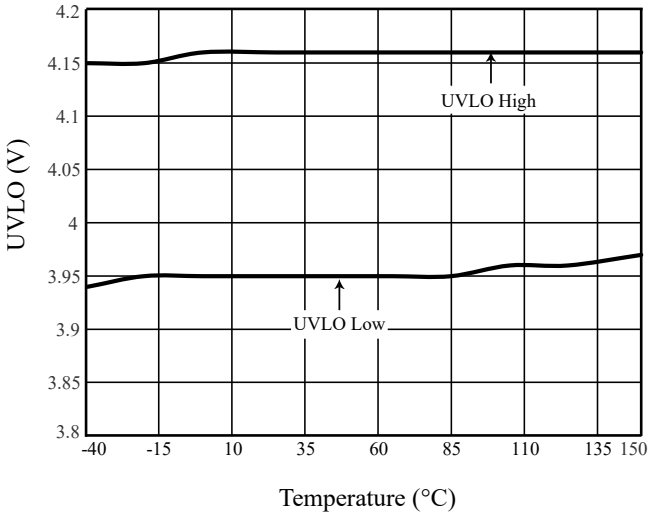


Figure 15 UVLO vs. Temperature

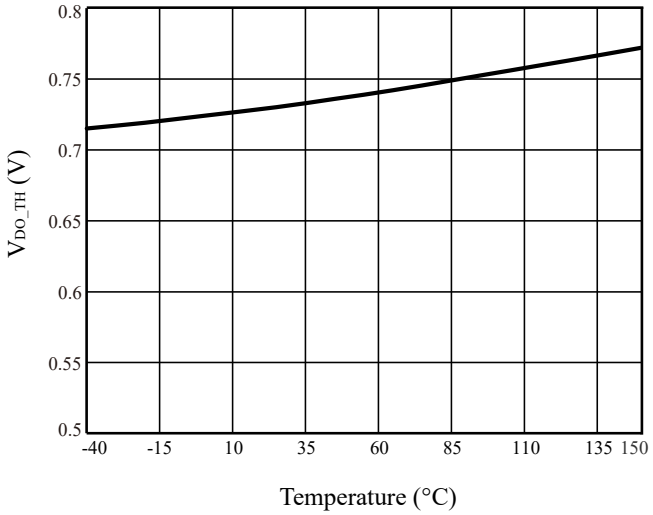


Figure 16 V_{DO_TH} vs. Temperature

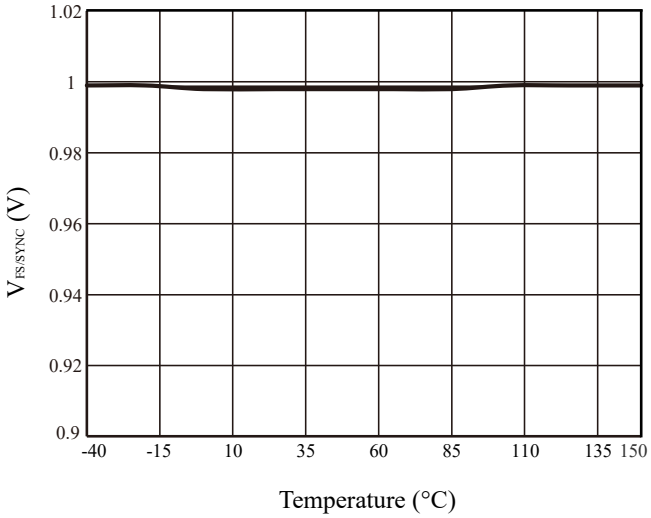


Figure 17 $V_{FS/SYNC}$ vs. Temperature

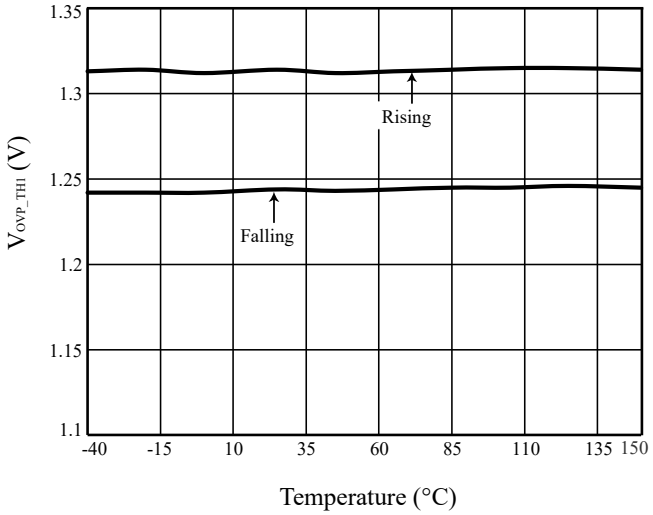


Figure 18 V_{OVP_TH1} vs. Temperature

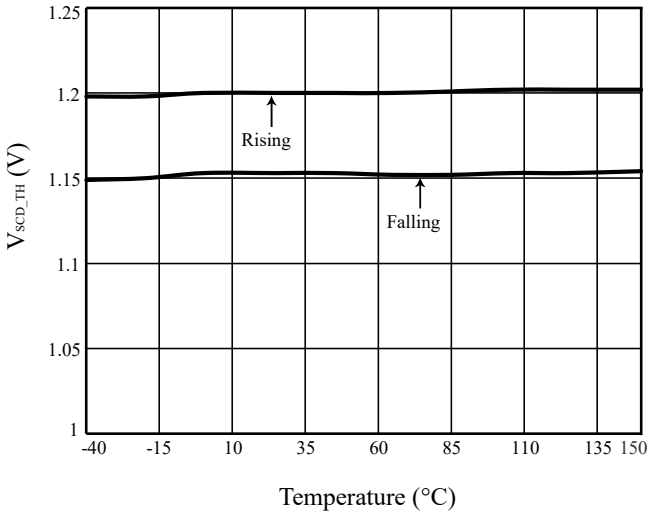


Figure 19 V_{SCD_TH} vs. Temperature

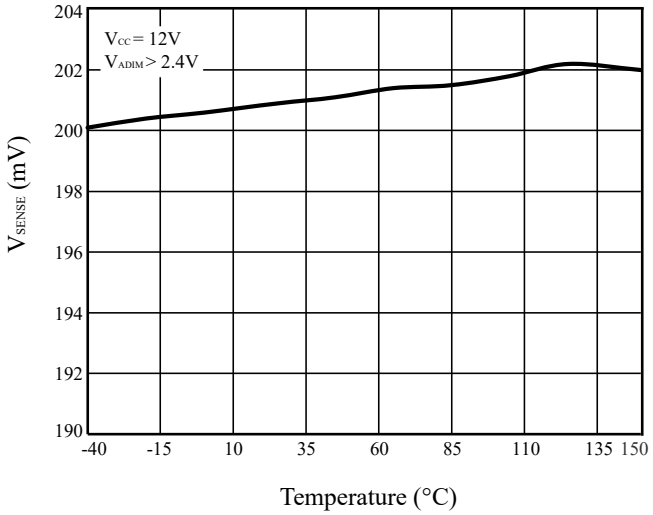


Figure 20 V_{SENSE} vs. Temperature

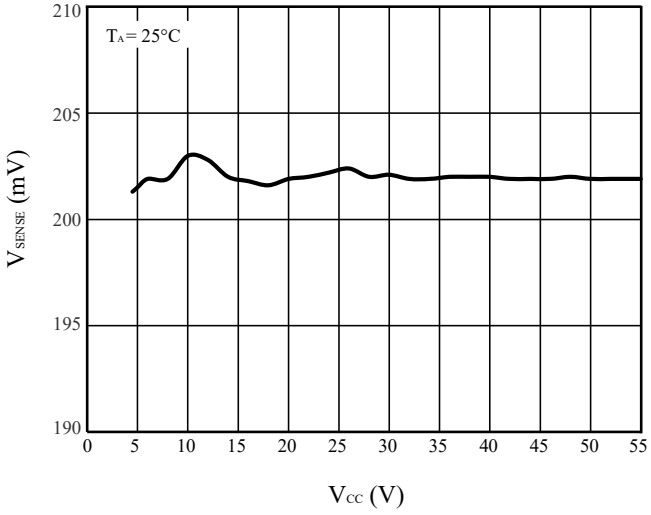


Figure 21 V_{SENSE} vs. V_{CC}

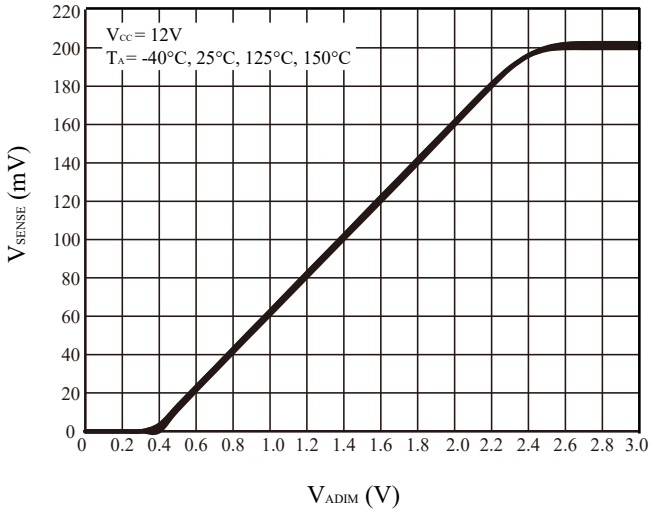


Figure 22 V_{SENSE} vs. V_{ADIM}

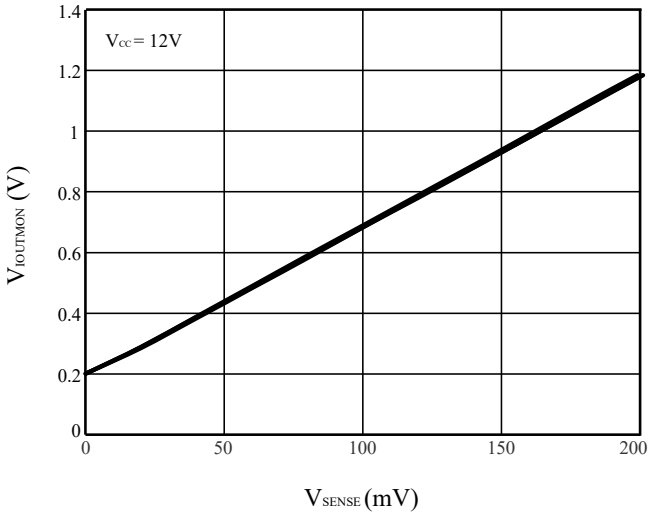


Figure 23 $V_{IOUTMON}$ vs. V_{SENSE}

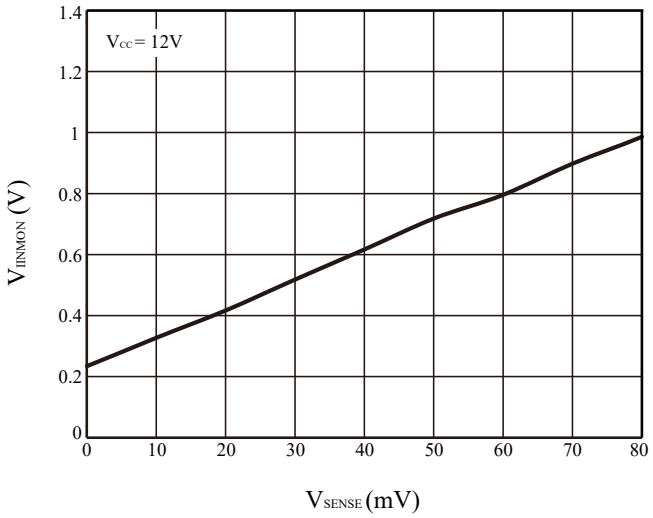


Figure 24 V_{IINMON} vs. V_{SENSE}

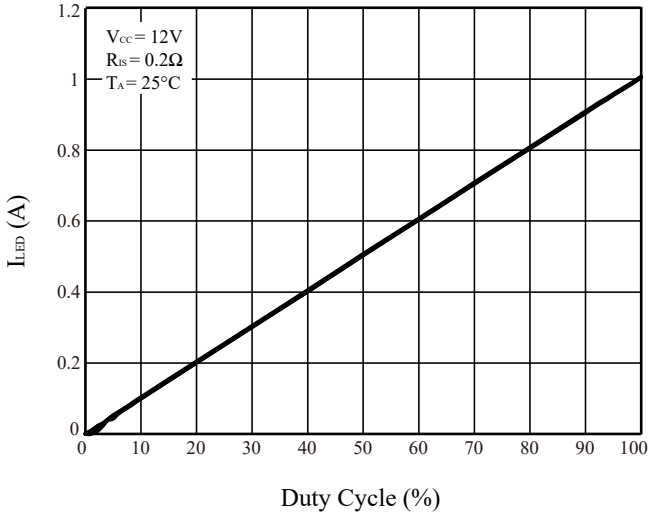


Figure 25 I_{LED} vs. External PWM Duty Cycle

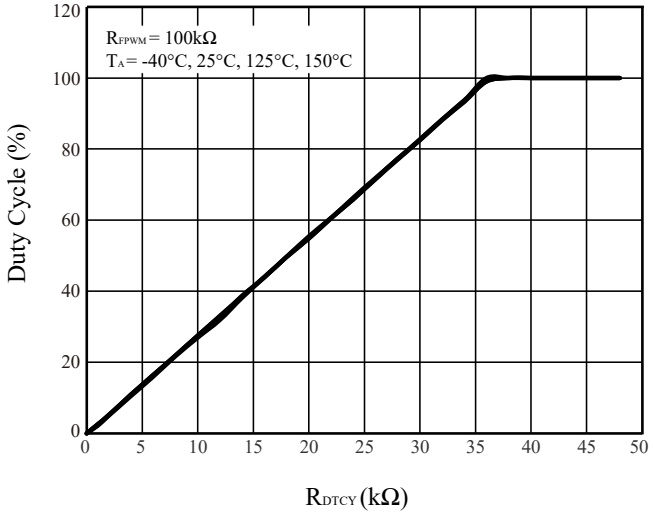


Figure 26 Internal PWM Duty Cycle vs. R_{DTCY}

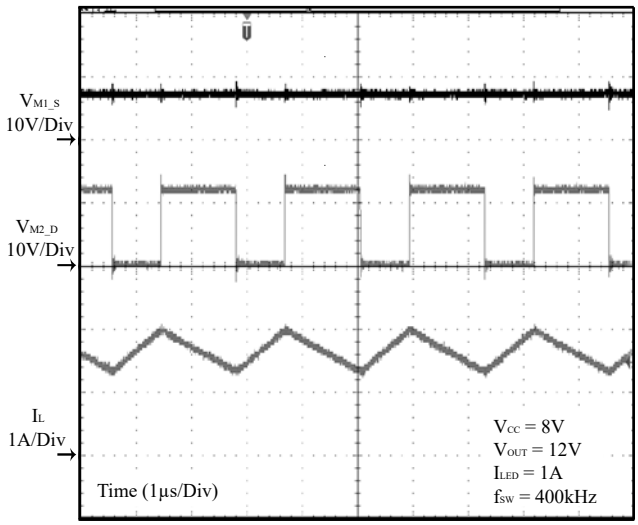


Figure 27 Switching Waveforms (Boost Region)

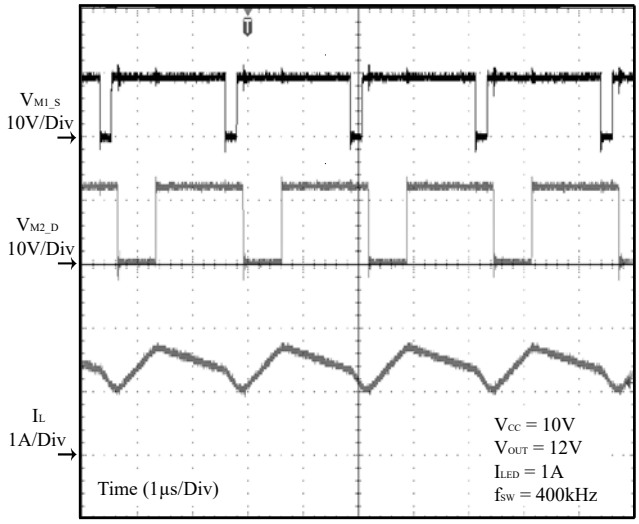


Figure 28 Switching Waveforms (Buck-Boost Region)

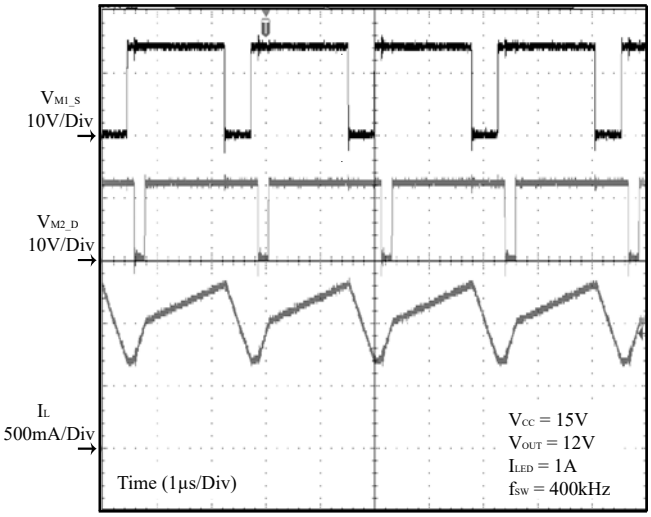


Figure 29 Switching Waveforms (Buck-Boost Region)

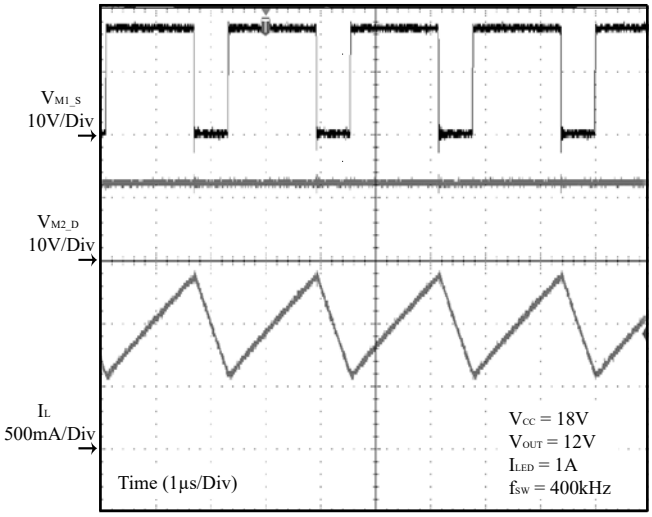


Figure 30 Switching Waveforms (Buck Region)

APPLICATION INFORMATION

The IS32LT3959 is a multi-topology PWM controller with constant ON-Time Buck and constant OFF-Time Boost combination control scheme to support step-up/down LED driver. With a single inductor, it is able to provide a constant current to an LED string whose string forward voltage is within the operating input voltage range. The multi-topology architecture provides a seamless transition between Buck, Buck-Boost, and Boost operating modes.

For the Buck-Boost topology, the IS32LT3959 needs two external power switches and two power Schottky diodes, but only one inductor as shown in Figure 1.

Figure 31 shows a simplified diagram of how the two switches and two Schottky diodes are connected to inductor L_1, output current sense resistor R_{IS}, peak/valley current sense resistor R_{CS}, and the input over current sense resistor R_{INSEN}. The output current sense resistor R_{IS} is connected to ISP and ISN pins to detect the output current. The current sense resistor R_{CS} is connected to the CS pin and provide inductor current information for both peak current detection of Boost control loop and reverse valley current detection of Buck control loop. The input current sense resistor R_{INSEN} connected to the VCC and INSENSE pins serves as a secondary protection to protect input over current fault. The operating region is decided by the V_{OUT}/V_{CC} voltage ratio. The IS32LT3959 controls the power switches for a smooth transition between the regions. The hysteresis is added to prevent jittering between regions. As Figure 32.

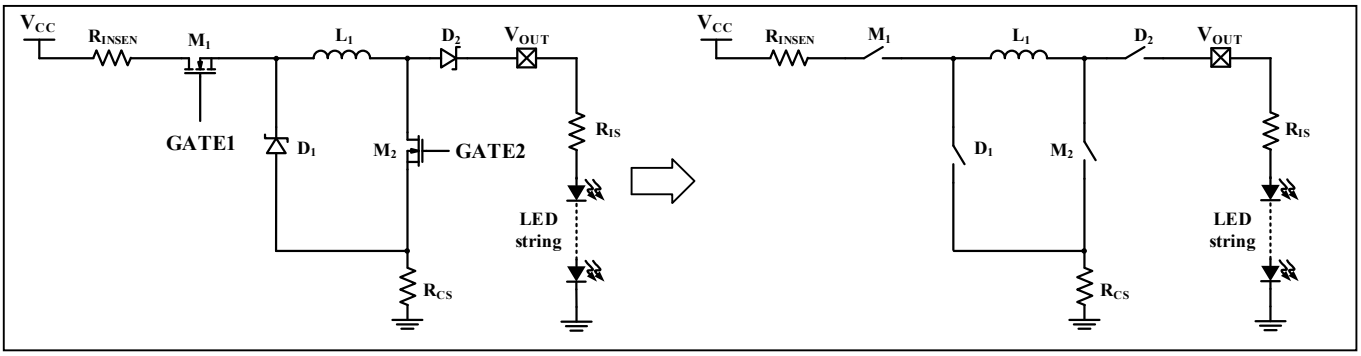


Figure 31 Simplified Diagram of Buck-Boost Topology

As Figure 32, there are three operating regions decided by the V_{OUT}/V_{CC} voltage ratio: (1) the operating mode is constant ON-Time Buck region, (2) and (3) the operating mode is constant ON-Time Buck and peak current Boost combination control Buck-Boost region, (4) the operating mode is constant OFF-Time Boost region. The following sections give detailed description for each state with waveforms.

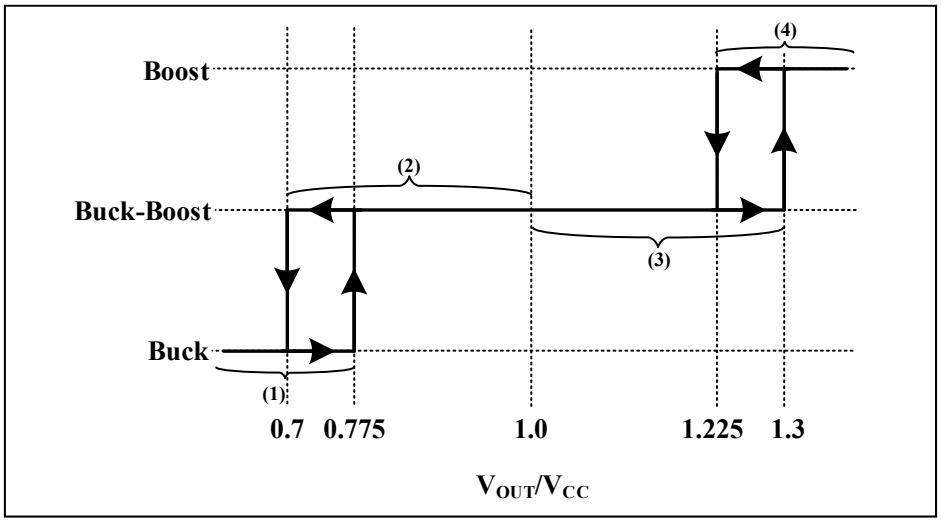


Figure 32 Operating Regions vs. V_{OUT}/V_{CC} Voltage Ratio

BUCK REGION (V_{CC} >> V_{OUT})

When the power supply voltage V_{CC} is much greater than the output voltage V_{OUT}, the IS32LT3959 uses constant ON-Time and valley current control in Buck region (Figure 33). The switch M_2 is always off and the Schottky diode D_2 is always active. At the beginning of each cycle, the switch M_1 is turned on and the current ramps up through the switch M_1, the inductor L_1, the Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string. When the constant ON-Time of the Buck control loop is expired, the switch M_1 is turned off and the recirculating Schottky diode D_1 is active. So the current ramps down through the current sense resistor R_{CS}, the recirculating Schottky diode D_1, the inductor L_1, the Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string. Once the current hits the valley current threshold of the Buck control loop, detected by the current sense resistor R_{CS} in series with D_1, the switch M_1 is turned on again. The next cycle starts and repeats the above control.

When operating in the Buck region both M_2 and D_2 can be omitted since switch M_2 is always off and Schottky diode D_2 is always active. It behaves like a typical asynchronous Buck regulator. As Figure 2 topology.

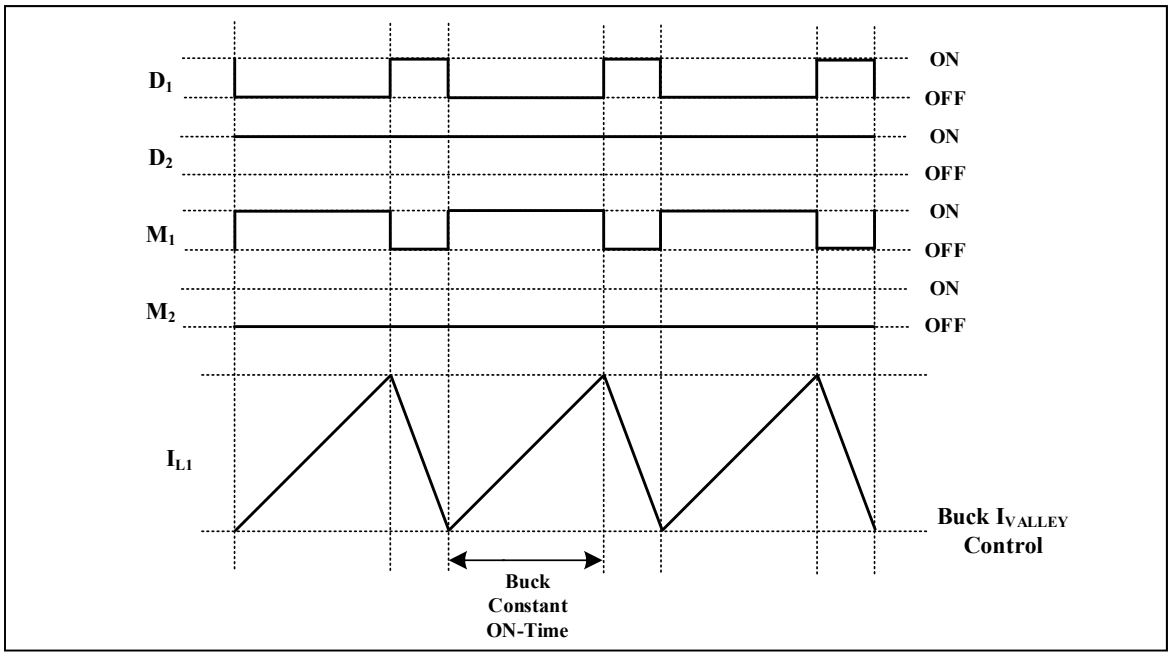


Figure 33 Buck Region (V_{CC} >> V_{OUT} Region)

BUCK-BOOST REGION (V_{CC} ~> V_{OUT})

When the power supply voltage V_{CC} is slightly higher than the output voltage V_{OUT}, the IS32LT3959 uses constant ON-Time Buck and peak current Boost combination control in Buck-Boost region (Figure 34). At the beginning of each cycle, both of the switches M_1 and M_2 are turned on and both of the Schottky diodes D_1 and D_2 are in off state. The current ramps up through the switch M_1, the inductor L_1, the switch M_2 and the current sense resistor R_{CS} to ground. When the current hits the peak current threshold of the Boost control loop, (detected by the current sense resistor R_{CS} in series with the switch M_2,) switch M_2 is turned off and the Schottky diode D_2 is active. The current keeps slowly ramping up through switch M_1, inductor L_1, Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string until switch M_1 is turned off because the constant ON-Time of the Buck control loop has expired. Then the current fast ramps down through the current sense resistor R_{CS}, Schottky diode D_1, inductor L_1, Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string. Once the current hits the valley current threshold of the Buck control loop, (detected by the current sense resistor R_{CS} in series with D_1,) both switches M_1 and M_2 are turned on again. The next cycle starts and repeats the above sequences.

Note that there is a 100ns (Typ.) dead-time control at the beginning of each cycle. Switch M_2 is delayed for 100ns (Typ.) and turned on after switch M_1 has turned on, this helps minimize switching noise. The dead-time is ignored in Figure 34 waveform.

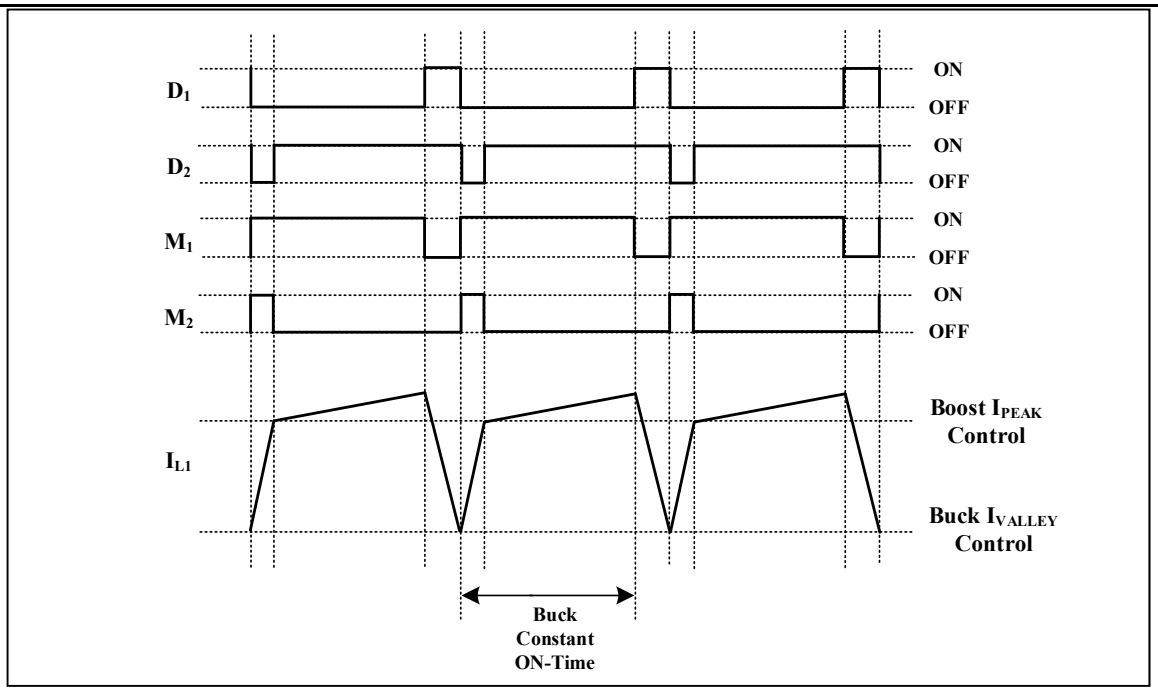


Figure 34 Buck-Boost Region (V_{CC} ~> V_{OUT} Region)

BUCK-BOOST REGION (V_{CC} <~ V_{OUT})

When the power supply voltage V_{CC} is slightly lower than the output voltage V_{OUT}, the IS32LT3959 uses constant ON-Time Buck and peak current Boost combination control in Buck-Boost region (Figure 35). At the beginning of each cycle, both of the switches M_1 and M_2 are turned on and both of the Schottky diodes D_1 and D_2 are in off state. The current ramps up through switch M_1, inductor L_1, switch M_2 and the current sense resistor R_{CS} to ground. Once the current hits the peak current threshold of the Boost control loop, (detected by the current sense resistor R_{CS} in series with the switch M_2,) switch M_2 is turned off and Schottky diode D_2 is active. The current starts to slowly ramp down through switch M_1, inductor L_1, Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string until the constant ON-Time of the Buck control loop has expired and switch M_1 is turned off. Then the recirculating Schottky diode D_1 is active. The current fast ramps down through current sense resistor R_{CS}, Schottky diode D_1, inductor L_1, Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string. Once the current hits the valley current threshold of the Buck control loop, (detected by the current sense resistor R_{CS} in series with D_1,) both of the switches M_1 and M_2 are turned on again. The next cycle starts and repeats the above sequences.

Note that there is a 100ns (Typ.) dead-time control at the beginning of each cycle. The switch M_2 is delayed for 100ns (Typ.) and turned on after switch M_1 has turned on, this helps minimize switching noise. The dead-time is ignored in Figure 35 waveform.

BOOST REGION (V_{CC} << V_{OUT})

When the power supply voltage V_{CC} is much lower than the output voltage V_{OUT}, the IS32LT3959 uses constant OFF-Time and peak current control in Boost region (Figure 36). The switch M_1 is always on and the Schottky diode D_1 is always in off state. At the beginning of each cycle, the switch M_2 is turned on and the current ramps up through the switch M_1, the inductor L_1, the current sense resistor R_{CS} and the switch M_2 to ground. When the current hits the peak current threshold of the Boost control loop, detected by the current sense resistor R_{CS} in series with M_2, the switch M_2 is turned off and the recirculating Schottky diode D_2 is active. So the current ramps down through the switch M_1, the inductor L_1, the Schottky diode D_2 and the output current sense resistor R_{IS} into the LED string. The switch M_2 keeps off until the constant OFF-Time of the Boost control loop being expired and it turns on again. The next cycle starts and repeats the above control.

When operating in the Boost region, both of M_1 and D_1 can be omitted since switch M_1 is always on and Schottky diode D_1 is always in off state. It behaves like a typical asynchronous Boost regulator. As Figure 3 topology.

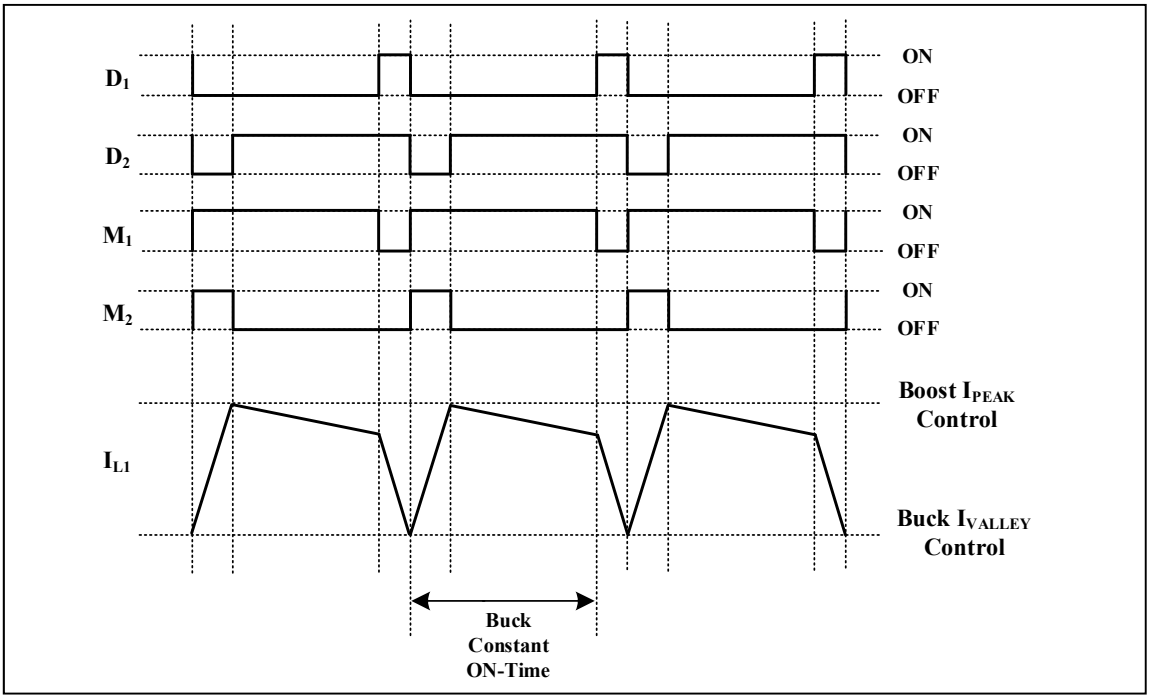


Figure 35 Buck-Boost Region (V_{CC} <~ V_{OUT} Region)

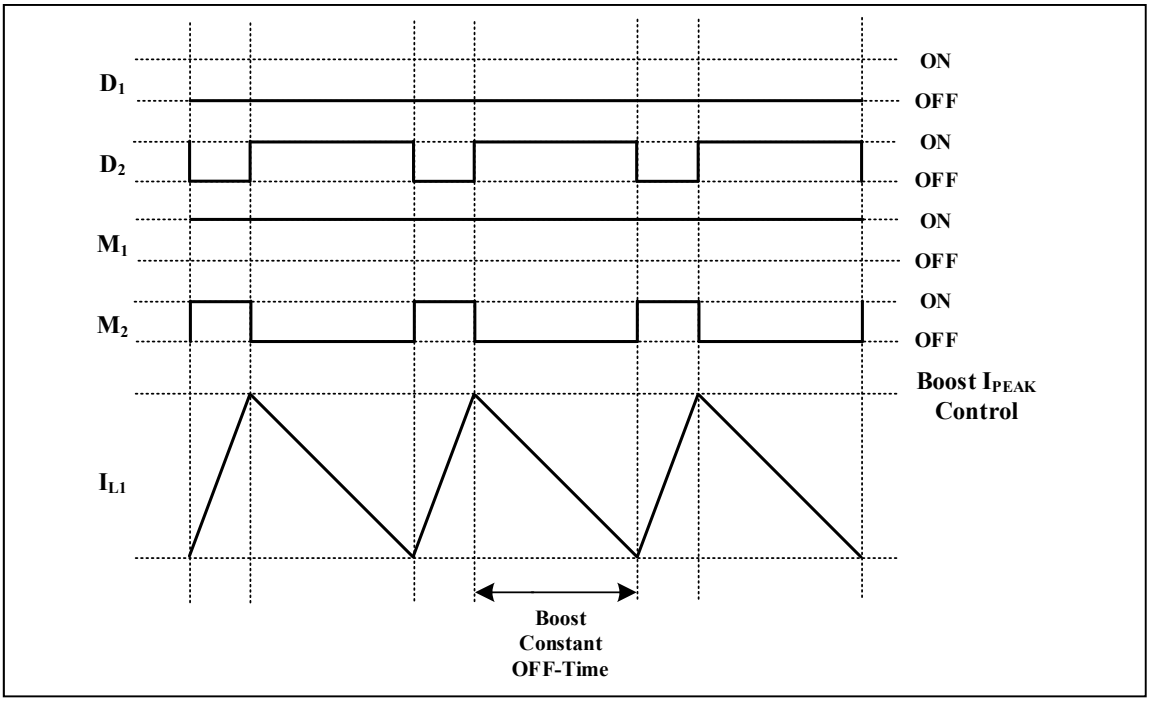


Figure 36 Boost Region (V_{CC} << V_{OUT} Region)

VCC UNDER VOLTAGE LOCKOUT (UVLO)

IS32LT3959 features an under voltage lockout (UVLO) function on the VCC pin to prevent unintended operation at too low input voltages. UVLO threshold is an internally fixed value and cannot be adjusted. The device disables the output when the V_{CC} voltage drops below V_{UVLO} (Typ. 4.0V), and resumes normal operation when the V_{CC} voltage rises above (V_{UVLO}+V_{UVLO_HY}) (Typ. 4.2V).

INTERNAL LINEAR REGULATORS

The device integrates a linear regulator (VDD) with 6.0V (Typ.) and I_{VDD_LM} current capability to power internal circuitry and low-side NMOS gate driver (GATE2) in the IS32LT3959. During operation, the external low-side NMOS will draw transient high current from this linear regulator. Therefore, a 1μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND; it must be placed as close to VDD pin as possible. This regulator also has the UVLO feature. The

device disables the output when the V_{DD} voltage drops below V_{DD_UV} (Typ. 3.5V), and resumes normal operation with soft-start process when the V_{DD} voltage rises above (V_{DD_UV}+V_{DD_UVHY}) (Typ. 4.0V). This helps protect the external low-side NMOS from excessive power consumption due to relatively higher $Rds_{(ON)}$ resulting from insufficient gate drive voltage. An I_{VDD_LM} current limit (Min. 25mA) on VDD pin protects the IS32LT3959 from excessive power dissipation at high input voltage.

VDD can be used to bias an external low current circuit requiring a reference supply, such as pulling up bias voltage for ADIM and FAULTB pins. However, to ensure stable operation of the IS32LT3959, it is not recommended to power high current external devices with the VDD pin.

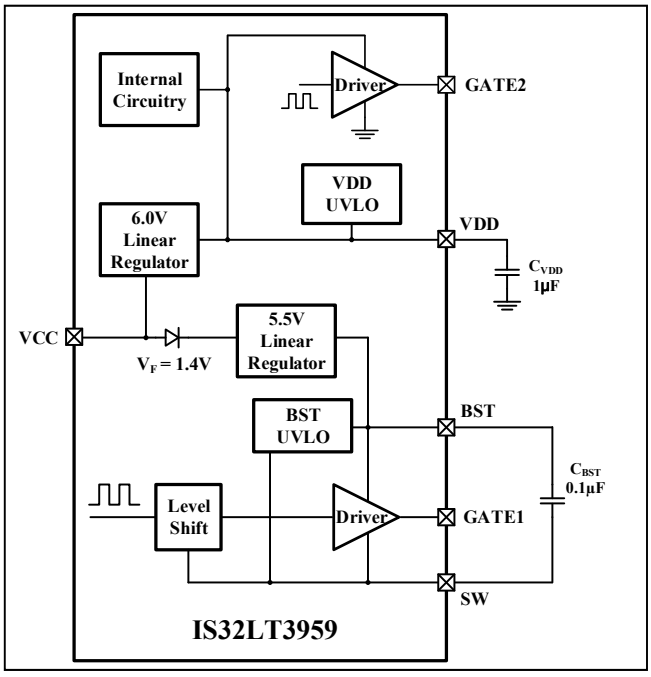


Figure 37 Linear Regulator

Besides the 6.0V linear regulator, there is another internal 5.5V linear regulator for the high-side NMOS driver (GATE1). During operation, the external high-side NMOS will draw transient high current from this linear regulator. Therefore, a 0.1µF low ESR, X7R type ceramic, floating bootstrap capacitor is necessary from BST pin to SW pin; it must be placed as close to BST and SW pins as possible. This regulator is monitored by a separate under voltage lockout circuit, BST UVLO, whose threshold voltage refers to SW pin. The device stops switching when the (V_{BST}-V_{SW}) voltage drops below (V_{BSTUV}-V_{BSTUV_HY}) (Typ. 3.3V), and resumes normal operation when the (V_{BST}-V_{SW}) voltage rises above V_{BSTUV} (Typ. 3.6V). This helps protect the external high-side NMOS from excessive power consumption due to relatively higher $Rds_{(ON)}$ resulting from insufficient gate drive voltage.

These two linear regulators will be supplied to the GATE1/2 pins to drive power NMOSs. The required driving current can be calculated from the following Equation (1):

$$I_{GATE} = f_{SW} \times (Q_{G1} + Q_{G2}) \qquad (1)$$

Where f_{SW} is operating frequency of IS32LT3959 and Q_{G1} and Q_{G2} are the total gate charge of power switches, M_1 and M_2.

Choosing power NMOSs with lower Q_G will improve the efficiency and allow higher switching frequency. Moreover, if the analog dimming voltage of the ADIM pin is biased from VDD pin, a too large Q_G NMOS will draw excessive current from the VDD linear regulator may result in more error to the analog dimming accuracy due I_{VDD_LM} current limit of the linear regulator.

It is important to consider the NMOS threshold voltage when operating in the dropout region when the input voltage (V_{CC}) is below the regulation level of these two regulators. If the device is required to operate at an input voltage less than 7V, recommend power NMOSs with a threshold voltage ($V_{GS(th)}$) below 3V and add an external BST diode from the VDD pin to BST pin which can enhance the high-side NMOS driving and improve the efficiency. The recommended external BST diode is 1N4148.

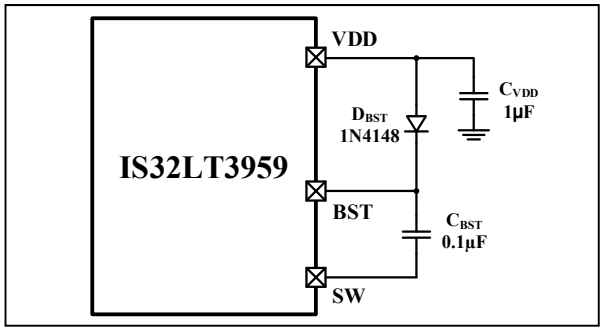


Figure 38 External BST Diode

ENABLE AND SHUTDOWN

The EN/PWM pin is an enable input for the device, pull it higher than V_{IH} to enable the device; pull it lower than V_{IL} for longer than t_{DELAY} to force the device into shutdown mode with an ultra-low shutdown current. The EN/PWM pin has an internal 200kΩ (Typ.) pull-down resistor to ground. If the shutdown function is not implemented, connect the EN/PWM pin to the VCC pin via a 10kΩ resistor.

SOFT-START

The IS32LT3959 provides a built-in soft-start function. The function of soft-start is made for the regulator to gradually reach the steady state operating point, thus dampening the inrush current to an acceptable value at startup. When the device starts, the internal circuitry generates a soft-start voltage ramping from 0V to V_{DD}. When it is lower than the internal reference of error amplifier (EA), the soft-start voltage overrides EA's reference so the EA uses the soft-start voltage as the reference. Once the soft-start voltage exceeds EA's

reference, EA's reference regains loop control. The soft-start period time is internally fixed at 5ms (Typ.) and not adjustable.

OPERATING FREQUENCY

The operating frequency of the device is programmable from 150kHz to 650kHz range using a single resistor R_{FSET} connected between FS/SYNC pin to ground. Selection of the operating frequency is a tradeoff between overall conversion efficiency and component size. Higher frequency operation results in smaller component sizes but increases the switching losses and power NMOS gate driving current, and may not allow sufficiently high or low duty cycle due to minimum ON-Time and minimum OFF-Time limitation. Lower frequency gives better efficiency performance but results in larger component sizes. In automotive applications, an operating frequency of 400kHz is a good compromise between component size and efficiency. It makes the system easier to filter switching noise from sensitive frequency bands and pass EMI tests.

To set a desired frequency, the resistor value can be calculated by Equation (2):

$$R_{FSET} = \frac{5 \times 10^4}{f_{SW} - 12} - 3.5 \qquad (2)$$

(74.9kΩ ≤ R_{FSET} ≤ 358.8kΩ)

Where R_{FSET} is in kΩ. f_{SW} is the operating frequency in kHz.

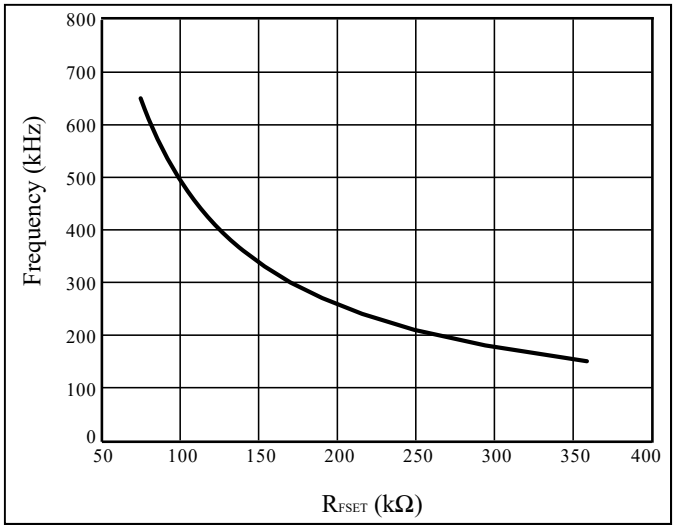


Figure 39 f_{SW} vs. R_{FSET}

If the FS/SYNC pin is connected to an extremely low or high value resistor, equivalent to an open or shorted to ground condition, the operating frequency will be internally clamped to 400kHz with spread spectrum disabled.

FREQUENCY SYNCHRONIZATION

The FS/SYNC pin can also be used as a synchronization input, allowing the IS32LT3959 to operate with an external clock in the range of 150kHz to 650kHz as long as its pulse width satisfies the requirements of t_{ON_SYNC} and t_{OFF_SYNC}, and its voltage level satisfies V_{IH_SYNC} and V_{IL_SYNC}. When an external synchronization clock is applied to the FS/SYNC pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of external clock. When an external synchronization clock is detected, Figure 40 shows the timing for a synchronization clock into the IS32LT3959 at 500kHz. Any pulse with a duty cycle of 15% to 85% at 500kHz can be used to synchronize the IC. However, driving FS/SYNC pin with a 50% duty cycle waveform is always a good choice.

Table 1 Synchronization Duty Cycle Range

SYNC Clock Frequency(kHz)	Duty Cycle Range (%)
650	19.5 ~ 80.5
500	15 ~ 85
400	12 ~ 88
300	9 ~ 91
250	7.5 ~ 92.5
150	4.5 ~ 95.5

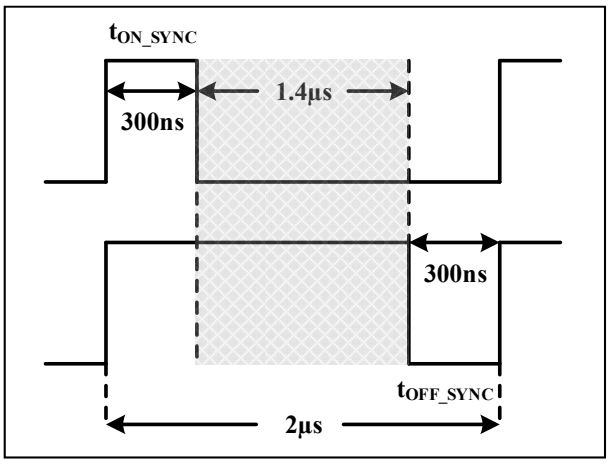


Figure 40 SYNC Pulse On And Off Time Requirements

SPREAD SPECTRUM

In switching topologies, EMI is a major concern. To optimize the EMI performance, the IS32LT3959 includes a spread spectrum feature, which is a 500Hz (Typ.) with ±10% (Typ.) operating frequency jitter. Spread spectrum effectively spreads the total electromagnetic emitting energy from a narrow band to a wide band lowering in the process the peak energy of EMI profile. Spread spectrum, reduces filter size and cost to pass EMI regulatory test. Note that when FS/SYNC pin is open or shorted to ground, spread spectrum function is disabled.

OUTPUT CURRENT SETTING

The IS32LT3959 regulates the LED current using

external current sense resistor, R_{IS}, in series with the LED string and connecting to ISP and ISN pins. The IS32LT3959 supports two current regulation modes, PMOS Current Regulator (PCR) and non-PCR, which is selected by the MODE pin. The output LED current of both modes is set by selecting the values of the output current sense resistor, R_{IS}, according to the following Equation (3):

$$I_{LED} = \frac{V_{SENSE}}{R_{IS}} \qquad (3)$$

In order to have an accurate output current, precision resistors with a good temperature-coefficient are preferred (±1% recommended). The R_{IS} resistor should be placed as close as possible to the IS32LT3959 device with minimal trace length to ISP and ISN pins. When the output current is high, the power rating of R_{IS} should also be considered. A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

PCR Mode (MODE=VDD):

If the MODE pin is connected to the VDD pin for high logic input, the device will operate in PCR mode whose output includes two control loops. As Figure 41. One loop is output constant current regulation loop, in which the device controls the external PMOS M_3 by the DIMOUT pin to operate as a constant current regulator whose output current is sensed and regulated via the current sense resistor R_{IS}. If PWM dimming and analog dimming are not enabled, the internal current sense voltage threshold V_{SENSE} of R_{IS}, which is equal to (V_{ISP}-V_{ISN}), is 200mV (Typ.). At the meantime, another loop, DC-DC control loop, independently operates as a constant voltage regulator to regulate the voltage drop between the VOUT and OUTSENSE pins at the threshold V_{DO_TH} (Typ. 720mV). Then the output voltage of the DC-DC control loop is equal to:

$$V_{OUT} = V_{DO\_TH} + V_{LED} \qquad (4)$$

The V_{DO_TH} provides a sufficient drop out voltage for the PMOS constant current regulator which optimizes the power consumption on the PMOS. The maximum power consumption on the PMOS is:

$$P_{PMOS} = \left(V_{DO\_TH} - V_{SENSE}\right) \times I_{LED} \qquad (5)$$

The larger the output LED current, the higher the power consumption on the PMOS. When the desired output current is high, the power rating of the PMOS should be carefully considered to sustain the maximum power dissipation on it.

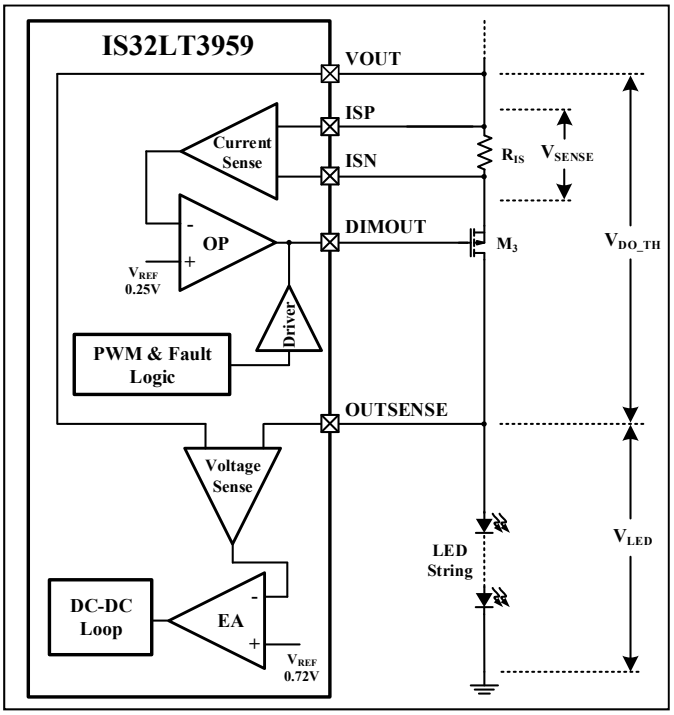


Figure 41 PCR Mode Output Control Loops

Non-PCR Mode (MODE=GND):

If the MODE pin is connected to GND for low logic input, the device will operate in non-PCR mode whose output has only a single control loop, DC-DC control loop. As Figure 42. There is no longer a constant voltage regulator loop. The DC-DC control loop operates as a constant current regulator, whose output current is sensed and regulated via the current sense resistor R_{IS}, to provide a constant current to the LED string. If PWM dimming and analog dimming are not enabled, the internal current sense voltage threshold V_{SENSE} of R_{IS}, which is equal to (V_{ISP}-V_{ISN}), is 200mV (Typ.). In this mode, the DIMOUT pin switches between V_{OUT} and (V_{OUT} - V_{PMOS_GS}) to drive the PMOS M_3 to operate as a switch either fully OFF or ON. Therefore, the power consumption on the PMOS is much lower than the PCR mode. The maximum power consumption on the PMOS is:

$$P_{PMOS} = R_{DS\_ON} \times I_{LED}^{2} \qquad (6)$$

The output voltage of the DC-DC control loop is equal to:

$$V_{OUT} = V_{SENSE} + R_{DS\_ON} \times I_{LED} + V_{LED} \qquad (7)$$

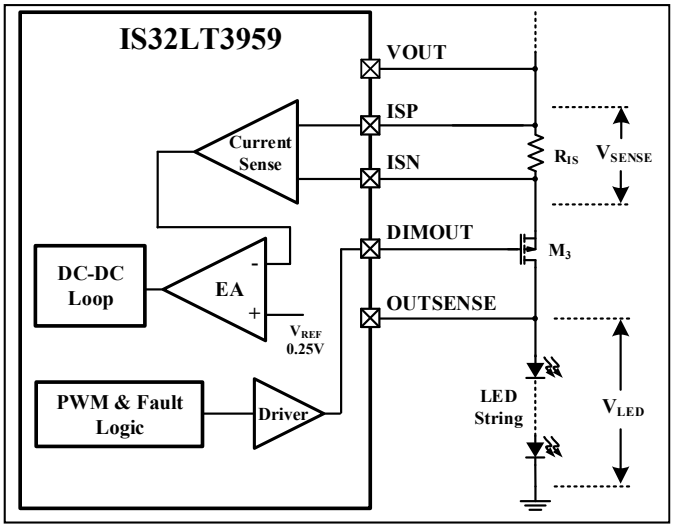


Figure 42 Non-PCR Mode Output Control Loop

The PMOS constant current regulation loop of the PCR mode performs much faster transient response than the DC-DC constant current regulation loop of non-PCR mode. Therefore, the PCR mode provides better load transient response which is able to efficiently decrease the current overshoot caused by a sudden change in LED string voltage. However, the PCR mode results in more power dissipation on the PMOS M_3 that lowers overall system efficiency.

In both current regulation modes, the DIMOUT pin is also controlled by the logic circuit of PWM and fault detection to switch the gate of PMOS M_3 between V_{OUT} and (V_{OUT}-V_{PMOS_GS}) to implement PWM dimming and fault protection. Leave the DIMOUT pin not connected (floating) if it is unused.

ANALOG DIMMING

The IS32LT3959 offers an analog dimming input pin, ADIM, whose dimming voltage range is 0.4V to 2.4V. The current sense voltage threshold, V_{SENSE}, can be regulated by the ADIM pin voltage. If the ADIM pin is pulled up above 2.4V, analog dimming is disabled and the output current is in full and given by Equation (3). When the ADIM voltage is driven below 2.4V, V_{ADIM} will proportionally control the current sense voltage threshold V_{SENSE} resulting in a change in the output LED current as given by Equation (8):

$$I_{LED\_ADIM} = \frac{V_{ADIM} - 0.4V}{2V} \times \frac{V_{SENSE}}{R_{IS}} \qquad (8)$$

Note that the relative current accuracy decreases with the decreasing current sense voltage threshold due to the offset of the internal circuit. Therefore, the recommended minimum analog dimming level is around 10%.

The output current will be turned off if the ADIM pin is pulled down below 0.4V.

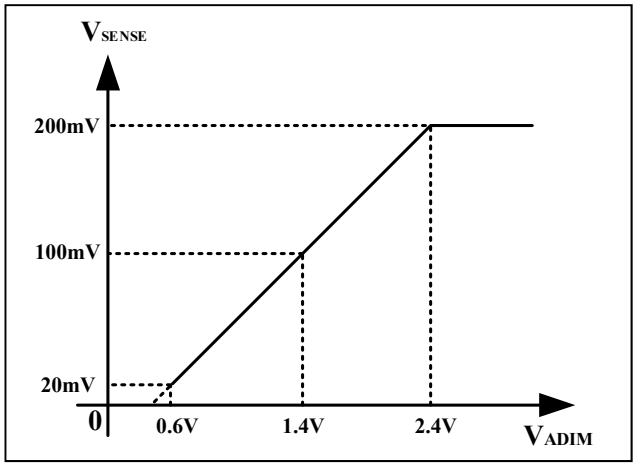


Figure 43 Analog Dimming

Never leave the ADIM pin unconnected (floating). If the analog dimming function is not implemented, connect the ADIM pin to a voltage level within 2.4V to 6V, or the VDD pin via a 10kΩ resistor.

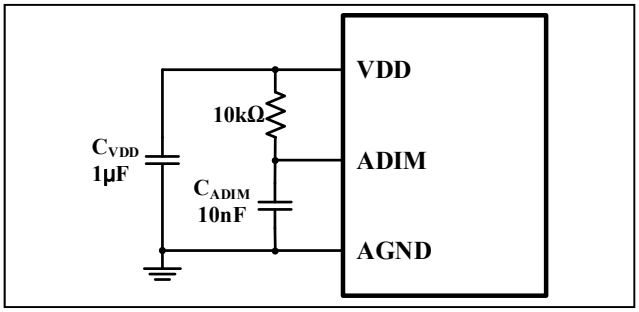


Figure 44 ADIM Pin Unused

It is recommended to add a 10nF ceramic capacitor from the ADIM pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the ADIM pin as possible. The following are some application scenarios for use of the analog dimming function.

LED Binning:

The ADIM pin can be used to fine tune the output current during mass-production. LEDs are typically sorted into various bins of different luminous intensity and forward voltage. To correct the brightness deviation during mass-production, the mean output current can be adjusted by adjusting the voltage level on the ADIM pin. As shown in Figure 45, fix the R_{ADIM1} value and solder different value R_{BIN} resistor to adjust and maintain the same lumen output across different LED bins. This R_{BIN} resistor can be placed on the LED board.

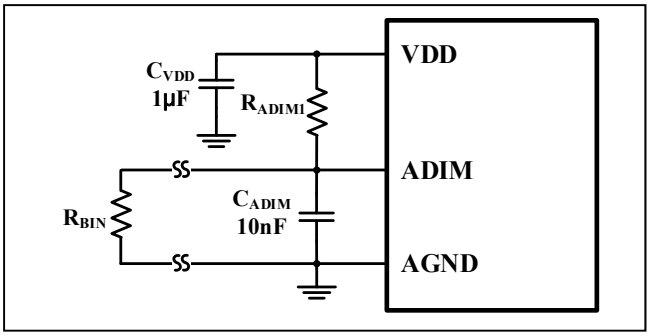


Figure 45 Analog Dimming for LED Binning

Over Temperature Thermal Roll Off:

The ADIM pin can also be used in conjunction with a NTC thermistor to provide over temperature current roll off protection for the LED load or the system. As Figure 46.

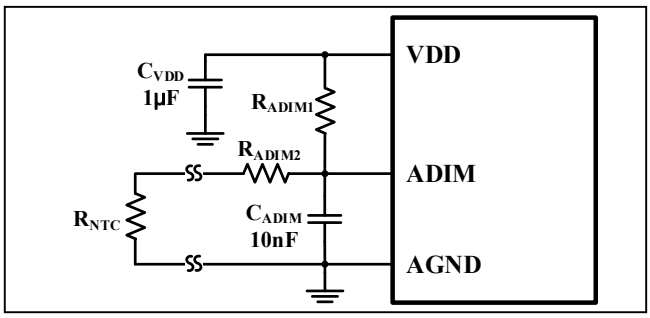


Figure 46 Analog Dimming for Thermal Roll Off Protection

For example, assume the desired current roll off temperature threshold is T_R and the NTC thermistor resistance is R_{NTCR} at this temperature (R_{NTCR} can be found in the NTC thermistor datasheet), then R_{ADIM1} and R_{ADIM2} can be calculated by:

$$R_{ADIM1} = \frac{(R_{NTCR} + R_{ADIM2}) \times (V_{DD} - 2.4V)}{2.4V} \quad (9)$$

For a given NTC thermistor, the R_{ADIM1} resistor will adjust the current roll off temperature threshold. The larger R_{ADIM1} the lower the current roll off temperature threshold. The R_{ADIM2} resistor is optional to be used to adjust current roll off slope. The larger R_{ADIM2} the flatter the current roll off slope. If R_{ADIM2} is not used, tie the NTC thermistor directly to ADIM pin.

The NTC thermistor should be placed next to the component to be monitored. Such as the LED board, beside the power MOSFET, and so on.

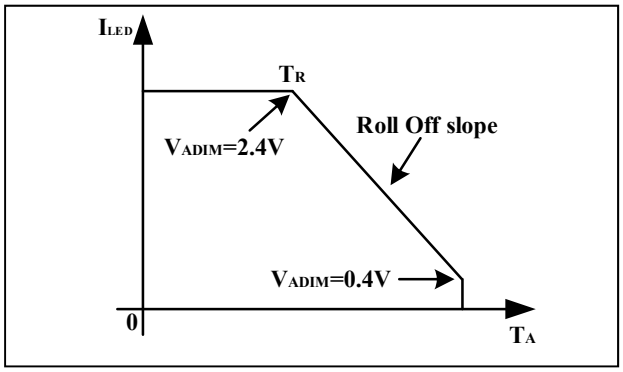


Figure 47 Thermal Roll Off Protection

Dual Brightness Level Output:

In automotive applications, some lamps require a dual brightness output. For instance, the daytime running light (DRL) and the position light (POL) can both use the same LED string, since these two lamps won't be active at the same time. The DRL is active in the daytime, while POL is active with lower brightness in the nighttime. Two brightness levels are selected by two independent power supply rails. The analog dimming can be used for this dual brightness output function.

As Figure 48. When the input logic to the GATE of the NMOS Q_1 is high, R_{ADIM3} resistor is shorted by Q_1. The output current is determined by the resistor divider R_{ADIM1} and R_{ADIM2}. If the GATE of the NMOS Q_1 is pulled low, the output current is determined by the resistor divider R_{ADIM1}, R_{ADIM2} and R_{ADIM3} the result is a higher brightness.

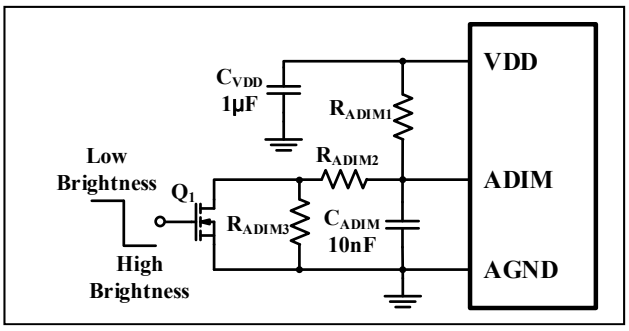


Figure 48 Analog Dimming for Dual Brightness Output

PWM DIMMING

IS32LT3959 supports two PWM (Pulse Width Modulation) dimming approaches: external PWM dimming by an external PWM signal applied on the EN/PWM pin and internal PWM dimming by an integrated PWM generator.

Note that both PWM dimming modes CANNOT be active at the same time, otherwise it will cause an LED flickering issue.

EXTERNAL PWM DIMMING

Besides enable and shutdown function, the EN/PWM pin also supports an external PWM signal to implement pulse-width modulation of the output current.

The DIMOUT pin is a buffered output following the PWM signal applied on the EN/PWM pin which drives the gate of the PMOS, M_3. When the EN/PWM signal voltage is greater than logic high threshold V_{IH}, the switching is enabled and the M_3 is turned on. When the EN/PWM voltage is lower than the logic low threshold V_{IL}, the switching is disabled and the M_3 is turned off. The LED string is dimmed by modulating the duty cycle of PWM signal to vary the LED average current. Apply a low PWM signal frequency with a higher device switching frequency will result in best dimming performance. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{EXTPWM} \qquad (10)$$

Where, D_{EXTPWM} is the external PWM signal duty cycle in %.

The high-side series connected PMOS M_3 driven by the DIMOUT pin is recommended for a precise PWM dimming function. The M_3 will disconnect the LED string during PWM low to prevent the VOUT node from discharging which will minimize the recovery time when the PWM goes back high. This shorter recovery time results in better dimming linearity and a stable loop regulation during low PWM duty cycles. Both are critical for ensuring control loop regulation during steady-state operation and to minimize LED current overshoot once PWM returns to a high level.

The EN/PWM pin has an internal 200kΩ (Typ.) pull-down resistor to ground. If external PWM dimming is not implemented, connect the EN/PWM pin to the VCC pin via a 10kΩ resistor.

INTERNAL PWM DIMMING

IS32LT3959 integrates a PWM generator which is controlled by the INTPWM pin. If the INTPWM pin is pulled high ($V_{INTPWM} \geq V_{IH}$), the internal PWM generator is disabled to get 100% output current which is set by the output current sense resistor, R_{IS}. Once the INTPWM pin is pulled low ($V_{INTPWM} \leq V_{IL}$), the internal PWM generator is enabled, which drives the switching and the PMOS M_3 to dim the output by its duty cycle. The internal PWM duty cycle can be programmed by a single resistor, R_{DTCY}, connected from DTCY pin to GND:

$$D_{INTPWM} = \frac{0.1 \times R_{DTCY}}{3.6} \qquad (11)$$

Where, D_{INTPWM} is the internal PWM duty cycle in % and R_{DTCY} is in kΩ.

To get better current accuracy, 1% resistors with good temperature-coefficient are recommended. The recommended internal PWM duty cycle setting range is 5%~95%. The lower duty cycle results in lower output current accuracy due to the error caused by the output current rising and falling response time. The PWM dimming output current is calculated by:

$$I_{LED\_PWM} = I_{LED} \times D_{INTPWM} \qquad (12)$$

When the internal PWM duty cycle is set by the DTYC pin, the internal PWM frequency is programmed by another single resistor, R_{FPWM}, connected from FPWM pin to GND. The PWM frequency can be set in a range of 100Hz~2kHz. Considering the output current rising and falling response time, a lower PWM frequency is helpful to get better output accuracy. A 100Hz~500Hz PWM frequency is recommended. The resistor value of R_{FPWM} can be calculated as follows:

$$f_{INTPWM} = \frac{2 \times 10^4}{R_{FPWM}} \qquad (13)$$

Where, f_{INTPWM} is the desired PWM frequency in Hz and R_{FPWM} is in kΩ.

With internal PWM dimming, the IS32LT3959 is able to easily implement dual brightness outputs by controlling the INTPWM pin. As Figure 49. When the PS2 rail supplies power, the INTPWM pin is pulled high to get high brightness (full current output). When only the PS1 rail supplies power, the INTPWM is pulled low by the internal pull-down resistor to get low brightness (internal PWM dimming output).

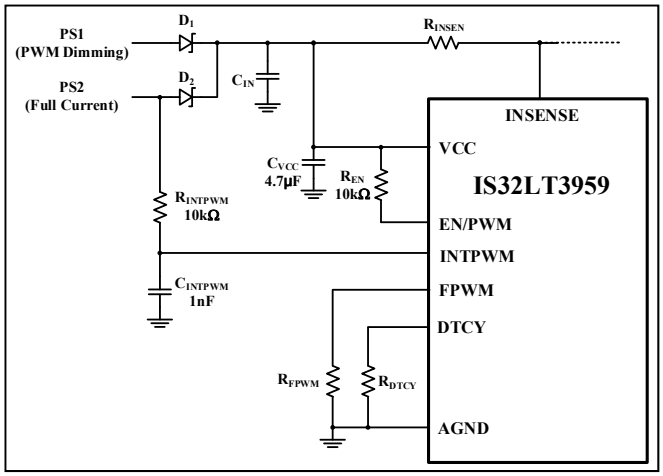


Figure 49 Dual Brightness Output Application

The INTPWM pin has an internal 200kΩ (Typ.) pull-down resistor to ground. If internal PWM dimming is not implemented, connect the INTPWM pin to the VCC pin via a 10kΩ resistor.

INDUCTOR SELECTION

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of a smaller inductor value. If the operating frequency is decided, inductor value involves trade-offs in performance. Larger inductance reduces inductor current ripple resulting in a smaller output current ripple, however it also brings in unwanted parasitic resistance that degrades performance. The inductor value determination is based on the operating frequency, output current, allowable inductor current ripple, and input voltage and output voltage. Use the following

equations to estimate the approximate inductor value:

For Boost:

$$L_{BOOST} \geq \frac{V_{CC\_MIN} \times (V_{OUT} - V_{CC\_MIN})}{f_{SW} \times \Delta I_L \times V_{OUT}} \quad (14)$$

For Buck:

$$L_{BUCK} \geq \frac{V_{OUT} \times (V_{CC\_MAX} - V_{OUT})}{f_{SW} \times \Delta I_L \times V_{CC\_MAX}} \quad (15)$$

Where V_{CC_MIN} is the minimum input voltage in volts, V_{CC_MAX} is the maximum input voltage in volts, f_{SW} is the operating frequency in hertz. ΔI_L is allowable inductor peak to peak ripple current in Amp. The inductor value has a direct effect on ripple current. In the Boost region, to keep the circuit in Continuous Conductive Mode (CCM), the maximum inductor current ripple ΔI_L should be chosen less than twice the input average current at the minimum input voltage. In the Buck region, to keep the circuit in Continuous Conductive Mode (CCM), the maximum inductor current ripple ΔI_L should be chosen less than twice the output LED current. The highest current ripple happens in the Buck region at maximum input voltage. If the application requires all operating regions, calculate the inductor value based on the Buck's Equation (15).

For high efficiency, choose an inductor with low core loss. The inductor should have a low DC resistance to reduce the I^2R losses, and its rating current must be greater than the maximum input average current and saturation current greater than maximum inductor peak current with some safety margin. To minimize radiated EMI noise, a shielded inductor is always a good choice.

SWITCH CURRENT SENSE RESISTOR R_{CS} SELECTION

When the input voltage is much lower than the output voltage V_{OUT}, the IS32LT3959 operates in constant OFF-Time and inductor peak current control Boost mode. In Boost operation, the switch M_1 is always on. In the switch M_2 on phase, the inductor current ramps up through the switch M_2 and the current sense resistor R_{CS} to ground. The inductor peak current control is detected by the current sense resistor R_{CS} connected in series with the switch M_2. As Figure 50.

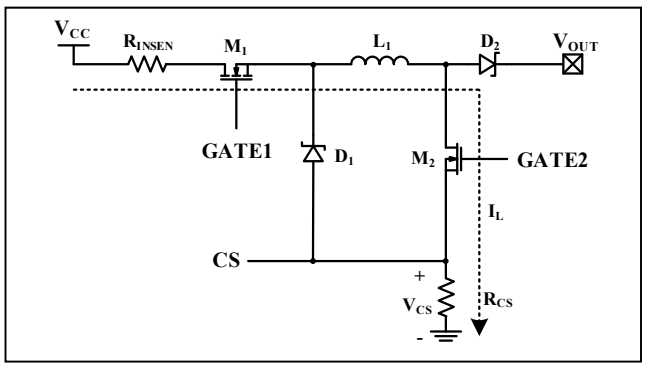


Figure 50 Boost Peak Current Detection in M_2 On Phase

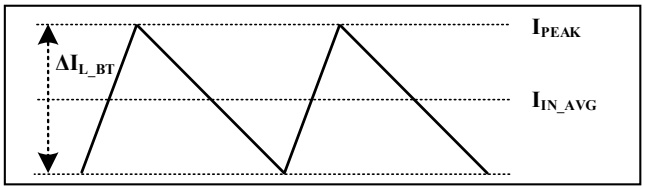


Figure 51 Boost Inductor Current

The inductor current in the Boost operation is shown in Figure 51. The maximum input average current happens at the minimum input voltage V_{CC_MIN}. Therefore the maximum inductor peak current, I_{PEAK_BTMAX}, can be given by:

$$I_{PEAK\_BTMAX} = I_{IN\_AVG\_MAX} + \frac{\Delta I_{L\_BT}}{2} = \frac{V_{OUT} \times I_{LED}}{\eta \times V_{CC\_MIN}} + \frac{\Delta I_{L\_BT}}{2} \quad (16)$$

Where, $I_{IN\_AVG\_MAX}$ is the maximum input average current at the minimum input voltage V_{CC_MIN}. η is the assumed circuit efficiency, choose 0.9. ΔI_{L_BT} is the inductor current ripple at the minimum input voltage in Boost operation and can be calculated as:

$$\Delta I_{L\_BT} = \frac{V_{CC\_MIN} \times (V_{OUT} - V_{CC\_MIN})}{f_{SW} \times L \times V_{OUT}} \quad (17)$$

The inductor peak current limit protection threshold is set by the R_{CS} value, which is cycle-by-cycle protection. Once the inductor peak current hits the current limit threshold, the GATE2 immediately pulls low to turn off the low-side power NMOS until the next switching cycle. If the inductor peak current keeps hitting the peak current limit and persists for longer than 2.5ms (Typ.) time frame, the IS32LT3959 will trigger hiccup protection, stop switching for t_{SKIP} and restart with the soft-start sequence. The hiccup will repeat until the peak current limit condition is removed.

Therefore, the R_{CS} value should be properly chosen to make sure that the inductor peak current limit protection is higher than the maximum inductor peak current with same safe margin, 30% recommended. So the current sense resistor R_{CS} in Boost operation can be calculated by the following Equation (18):

$$R_{CS\_BT} = \frac{V_{CS\_TH1}}{1.3 \times I_{PEAK\_BTMAX}} \quad (18)$$

V_{CS_TH1} is peak current limit threshold, typical 77mV for Boost operation.

Besides the inductor peak current limit, the CS pin has a secondary peak current limit threshold, typical 110mV for Boost operation. Once the inductor peak current hits the secondary current limit, the hiccup protection is triggered directly.

When the input voltage is much higher than the output

voltage, the IS32LT3959 operates in constant ON-Time and inductor valley current control Buck mode. In Buck operation, the switch M_2 is always off. In the switch M_1 off phase, the inductor current ramps down through the current sense resistor R_{CS} and the Schottky diode D_1, the inductor L_1 and the Schottky diode D_2 into the output loading. The inductor valley current control is detected by the current sense resistor R_{CS} connected in series with the Schottky diode D_1. As Figure 52.

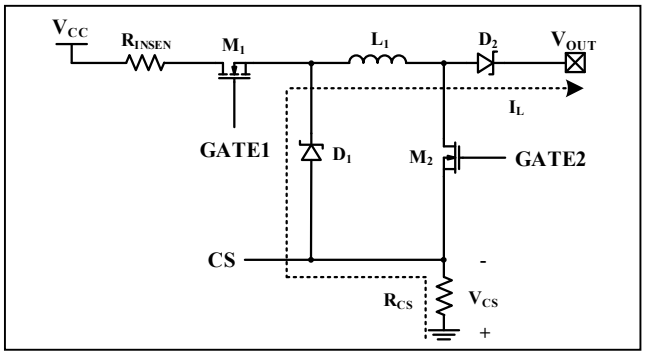


Figure 52 Buck Valley Current Detection in M_1 Off Phase

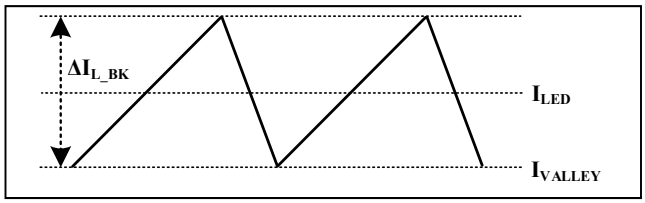


Figure 53 Buck Inductor Current

The inductor current in the Buck operation is shown in Figure 53. In theory, the maximum inductor valley current will never exceed the output LED current.

The cycle-by-cycle inductor valley current limit protection threshold is also set by the R_{CS} value. Once the inductor valley current exceeds the valley current limit, the high-side NMOS keeps off state to clamp the inductor valley current at the valley current limit threshold. If the inductor valley current persists at the valley current limit for longer than 2.5ms (Typ.), the IS32LT3959 will trigger hiccup protection, stop switching for t_{SKIP} and restart with the soft-start sequence. The hiccup will repeat until the valley current limit condition is removed. Similar to the Boost operation, the CS pin has a secondary peak current limit threshold, typical -110mV for Buck operation. Once the inductor peak current hits the secondary current limit, the hiccup protection is triggered directly.

Therefore, the R_{CS} resistor value in Buck operation can be chosen to make sure that the inductor valley current limit protection around the output LED current plus a 20% safe margin. So the current sense resistor R_{CS} in Buck operation can be calculated by the following Equation (19)

$$R_{CS\_BK} = \frac{|V_{CS\_TH1}|}{1.2 \times I_{LED}} \qquad (19)$$

Where, V_{CS_TH1} is valley current limit threshold, typical -67mV for Buck operation.

If the application requires only Buck operation (Figure 2 topology), the R_{CS} value can be calculated by the Buck Equation (19). If the application requires other operating regions (Figure 1 or 3 topology), calculate R_{CS} value based on the Boost Equation (18). Recommend use of ±1% precision type resistors for best accuracy. It should be placed as close as possible to the IS32LT3959 device to ensure stable operation.

DIODES SELECTION

To select D_1 and D_2, the reverse recovery characteristics and forward voltage drop are particular important characteristics to be considered. To achieve high efficiency, Schottky type diodes with low forward voltage drop and fast recovery time are a good choice. Fast recovery time minimizes the peak instantaneous power during turn-on transition of the power switches. Low forward voltage drop has a significant impact on the conversion efficiency, especially for applications with low output voltage. The reverse breakdown voltage rating of both diodes should be selected to be greater than V_{CC_MAX} and V_{OVP1} together with overshoot voltage due to the ringing caused by parasitic inductances and capacitances, therefore keeping a 20% safety margin. The current rating of both diodes should be greater than the maximum output load current with some safety margin. A conservative design would allow at least two times of the maximum output LED current.

POWER NMOS SELECTION

The IS32LT3959 requires two external power NMOSs, one for high-side switch (M_1) and another for low-side switch (M_2). Important parameters for the power NMOSs are the drain to source breakdown voltage $V_{(BR)DSS}$, the gate threshold voltage $V_{GS(th)}$, drain to source on-resistance $R_{DS(on)}$, and drain to source current capability.

The $V_{(BR)DSS}$ must be greater than V_{CC_MAX} and V_{OVP1} together with overshoot voltage due to the ringing caused by parasitic inductances and capacitances, therefore keeping a 20% safety margin. The gate drive voltage is sourced from the internal linear regulator, 6.0V (Typ.) for the low-side NMOS and 5.5V (Typ.) for the high-side NMOS. Consequently, low gate threshold voltage type NMOSs should be chosen to make sure the internal linear regulator voltage is sufficient to drive the NMOSs into full saturation.

The consideration of the $R_{DS(ON)}$ of power NMOSs is usually secondary because the switching loss dominates the power lost, especially at high operating frequency. Power NMOSs with lower Q_G and $R_{DS(ON)}$ achieves higher efficiency and lower power losses. The continuous current rating of the selected power NMOSs should be higher than the input average current of Boost operation and the maximum current rating should be higher than the peak current limit protection level of

Boost operation.

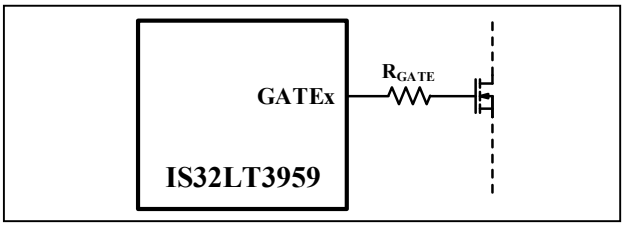


Figure 54 GATE Buffer Resistor

A buffer resistor (Figure 54) can be considered to be added in series with the gate driving that slows down the switching rising and falling edge to minimize EMI. However, it increases the switching loss and degrades the efficiency at the same time. So the value should not be too large; ten ohms is a good starting point. Please choose a proper value to compromise for both EMI test result and thermal performance.

POWER PMOS PWM SWITCH SELECTION

A high side PMOS PWM switch M_3 is recommended in most applications to maximize the PWM dimming ratio and protect the LED string during fault conditions. In PCR mode, the PMOS M_3 is essential.

Compared to a low-side NMOS PWM switch, the high-side PMOS PWM switch allows a single wire to the LED string cathode and ground return path through the chassis. For proper operation, its drain to source breakdown voltage rating $V_{(BR)DSS}$ should exceed the V_{OVP1} set by the FB pin, the absolute value of its gate threshold voltage $V_{GS(TH)}$ should be less than 3V, and its current rating I_D should be above I_{LED}.

INPUT AND OUTPUT CAPACITORS

Input and output capacitors are necessary to suppress voltage ripple caused by switched current. The use of low ESR capacitors is preferred to be used to efficiently reduce voltage ripple. Ceramic capacitors have excellent ESR characteristics and are good choice for input and output capacitors. A parallel combination of multiple ceramic capacitors is typically used to achieve ultra-low ESR and high capacitance. X7R type ceramic capacitors are recommended, as it retains the nominal capacitance value over wide voltage and temperature ranges. The ceramic capacitors should be placed near the driver input and output. It's a good practice to put an additional 0.1μF~0.47μF ceramic capacitor on the input and output of the driver to absorb high frequency switching spike. Ceramic capacitors, of at least 1μF, should also be placed from VCC to GND and VOUT to GND as close to the IS32LT3959 pins as possible.

In the Buck operation, the input current is periodically interrupted with the on and off toggling of the high-side switch. When the high-side switch turns on, the input current into the high-side switch steps from zero to the valley of the inductor current waveform, then ramps up to the peak value, and then drops to the zero as the high-side switch turns off. The input capacitors must supply most of the input current during the high-side switch on phase. Therefore, the input capacitors should be capable to handle the maximum RMS current in the Buck operation:

$$I_{INBK\_RMS} = I_{LED} \times \sqrt{\left(1 - \frac{V_{OUT}}{V_{CC}}\right) \times \frac{V_{OUT}}{V_{CC}}} \qquad (20)$$

The formula has a maximum at $V_{CC}=2\times V_{OUT}$, where $I_{INBK\_RMS}=I_{LED}/2$.

In the Boost operation, since the input current is uninterrupted, the demand for input capacitors is much less than in Buck mode. However, the output current of the Boost mode is periodically interrupted with the on and off toggling of the low-side switch. When the low-side switch turns off, the output current through the output Schottky diode D_2 steps from zero to the peak of the inductor current waveform, then ramps down to the valley value, and then drops to the zero as the low-side switch turns on. The output capacitors must supply the entire output current during the low-side switch on phase. For this reason, the selection of the output capacitor is based on the Boost operation. Both bulk capacitance and ESR must be considered to ensure allowable output ripple voltage. The capacitance of the Boost mode can be estimated by:

$$C_{OUT\_MIN} = \frac{I_{LED} \times \left(V_{OUT} - V_{CC\_MIN}\right)}{\Delta V_{OUT\_RIP} \times f_{SW} \times V_{OUT}} \qquad (21)$$

$$ESR_{MAX} = \frac{\Delta V_{OUT\_RIP} \times V_{CC\_MIN}}{V_{OUT} \times I_{OUT\_MAX}} \qquad (22)$$

Where ΔV_{OUT_RIP} is allowable output ripple voltage. ESR_{MAX} is the maximum ESR of the output capacitors.

Note that the effective capacitance of ceramic capacitors decreases with DC bias. For larger bulk values of capacitance and lower cost, low ESR type electrolytic capacitors are usually used to be connected in parallel with the ceramic capacitors. However, electrolytic capacitors have poor tolerance, especially over temperature, and the selected value should be selected larger than the calculated value to allow for temperature variation.

INPUT AND OUTPUT CURRENT MONITOR OUTPUT

The IINMON pin voltage represents the input average current of the system measured by the VCC and INSENSE pins connected to the current sense resistor R_{INSEN}, while the IOUTMON pin voltage represents the output LED average current measured by the ISP and ISN pins connected to the output current sense resistor R_{IS}. They can be connected to an external host to implement input and output status tracking. The linear relationship between the current monitor output voltage and the voltage across the current sense resistors is:

$$V_{IINMON} = \left(V_{CC} - V_{INSENSE}\right) \times 10 + 0.2V \qquad (23)$$

$$V_{IOUTMON} = (V_{ISP} - V_{ISN}) \times 5 + 0.2V \quad (24)$$

The maximum output voltage of the IINMON and IOUTMON pins can be close to V_{DD}, 6V. If the voltage rating of the host's I/O is lower than 6V, a resistor divider can be used to reduce the IMON pin output voltage. The recommended resistor divider value is several tens of kΩ. If the current monitor function is not implemented, please leave them floating.

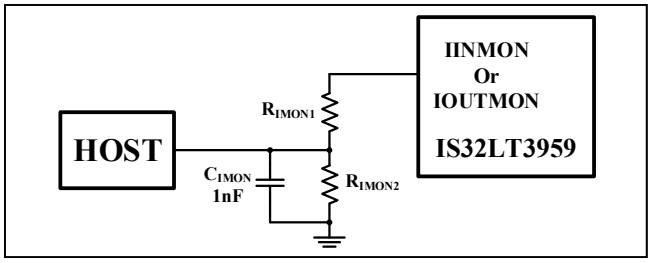


Figure 55 IINMON and IOUTMON to Host

LOOP COMPENSATION

The IS32LT3959 uses an internal transconductance error amplifier with COMP pin output that compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the COMP pin are set to optimize control loop response and stability. For typical applications, a 100nF or higher compensation capacitor at COMP pin is needed, and a series resistor 1.5kΩ should always be used to increase the slew rate on the COMP pin to maintain tighter regulation of the output current during fast transients on the input supply of the driver.

FAULT PROTECTION AND REPORTING

For added system reliability, the IS32LT3959 integrates various fault detection and protection circuitry for LED string open/short detection, output over voltage, input/output over current, FS/SYNC and FPWM pins open/short detection and over temperature conditions. The open drain pin FAULTB can be used as a fault condition flag. When it's monitored by a host, a pull-up resistor (R_{PU}, 47kΩ recommended) from the FAULTB pin to the supply of the host is required (Figure 56). It is pulled low to report a fault condition. Table 2 briefly describes the typical protection trigger conditions and device behavior.

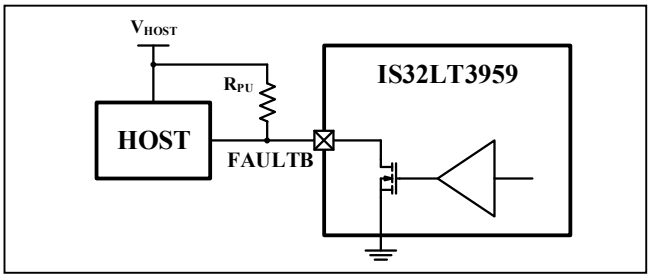


Figure 56 Host Monitors The Fault Reporting

INPUT CURRENT LIMIT

The IS32LT3959 has a standalone input over current monitor circuit which can be programmed with a current sense resistor R_{INSEN} connected in series with power supply, between VCC and INSENSE pins. When the voltage across R_{INSEN} hits the over current protection threshold V_{IN_OCTH} (Typ. 80mV), the high-side power switch M_1 will be turned off immediately. The input current limit must be set greater than the inductor peak current limit of the Boost operation, with a recommended 30% safety margin.

$$I_{IN\_LIM} = 1.3 \times \frac{V_{CS\_TH1}}{R_{CS}} \quad (25)$$

So

$$R_{INSEN} = \frac{V_{IN\_OCTH} \times R_{CS}}{1.3 \times V_{CS\_TH1}} \quad (26)$$

Where, V_{CS_TH1} is peak current limit threshold, typical 77mV for Boost.

In Boost topology (as Figure 3), since the high-side switch M_1 is omitted, the input current limit function will not be available. If the VOUT is shorted to ground, the input power supply V_{CC} is shorted by the inductor L_1 and the Schottky diode D_2 to ground. The uncontrolled huge current I_{SHORT} may damage the components as well as power supply. As Figure 57.

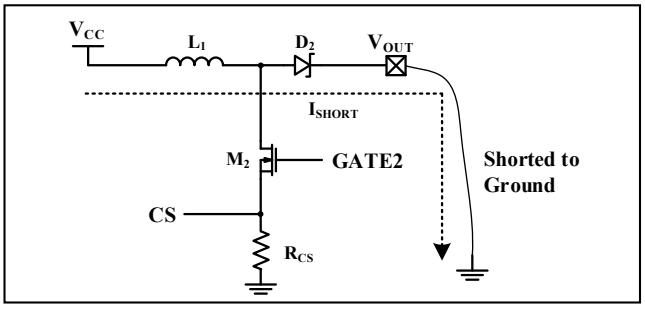


Figure 57 Output Shorted to Ground of Boost Topology

To avoid this fault condition, the Buck-Boost topology can be considered for the Boost applications.

If the application requires only Buck operation (Figure 2 topology), the input current limit can be set 3 times above the output LED current. So the R_{INSEN} value can be calculated by the following Equation (27):

$$R_{INSEN} = \frac{V_{IN\_OCTH}}{3 \times I_{LED}} \quad (27)$$

If the application requires only Buck operation (Figure 2 topology), the R_{INSEN} value can be calculated by the Buck Equation (27). If the application requires other operating regions (Figure 1 or 3 topology), calculate R_{INSEN} value based on the Boost Equation (26).

If the input current limit function is unused, directly connect the INSENSE pin to the VCC pin.

LED OPEN AND OUTPUT OVER VOLTAGE PROTECTION

The LED open protection is achieved using Over Voltage Protection (OVP). In the case of the LED string open, the driver keeps switching and charging the output capacitor to higher voltage. When the output voltage reaches the programmed OVP voltage (V_{OVP1}), IS32LT3959 immediately stops switching and pulls the FAULTB pin low to report the fault condition. The switching will not restart until the output voltage drops below the hysteresis voltage. To make sure the chip functions properly, the resistor divider (R_{O1}, R_{O2}) at the OVP pin must be set greater than the output voltage V_{OUT}, with a recommended 20% safe margin. The OVP voltage V_{OVP1} is programmed using Equation (28).

$$V_{OVP1} = \frac{V_{OVP\_TH1} \times (R_{O1} + R_{O2})}{R_{O2}} = 1.2 \times V_{OUT} \qquad (28)$$

±1% precision type resistor should be used for best accuracy. The resistor divider should be placed as close as possible to the FB pin to ensure stable operation. It is recommended to connect a 1nF ceramic capacitor from the FB pin to GND to avoid unexpected noise coupling into this pin.

Besides the programmable OVP (V_{OVP1}), the IS32LT3959 also provides a secondary Over Voltage Protection through VOUT pin to avoid accidental IC damage, caused for example by an error on FB resistor divider value. This secondary OVP protection is internally fixed threshold V_{OVP_TH2} (Typ. 58V). In case the VOUT pin voltage hits V_{OVP_TH2}, the IS32LT3959 will stop switching immediately and pulls the FAULTB pin low to report the fault condition. It will only resume operation once the output voltage drops below (V_{OVP_TH2}-$V_{OVP\_TH2\_HY}$) (Typ. 53V). This protection is provided to prevent catastrophic failures from accidental device over voltage breakdown.

LED SHORT AND OUTPUT OVER CURRENT PROTECTION

A resistor divider on the SCD pin, R_{SCD1} and R_{SCD2}, is connected in parallel with the LED string. When the LED string is either partially shorted or whole string shorted, the SCD pin voltage, V_{SCD}, drops down. If the V_{SCD} drops below the output LED shorted detection threshold V_{SCD_TH}, the device will pull the FAULTB pin low to report the fault condition. For partial LED string short detection, choose the R_{SCD1} and R_{SCD2} resistor divider using the following Equation:

$$V_{SF\_SHORT} < V_{SCD\_TH} \times \frac{R_{SCD1} + R_{SCD2}}{R_{SCD2}} < V_{SF\_NORM} \qquad (29)$$

Where, V_{SF_NORM} is LED string voltage in normal state. V_{SF_SHORT} is LED string voltage in partial short circuit condition. Recommend to choose 10kΩ for the R_{SCD2} and calculate the R_{SCD1} according to above equation. The resistors R_{SCD1} and R_{SCD2} should be ±1% tolerance with good temperature characteristic to ensure accurate detection.

Once the short circuit fault condition is removed and the SCD pin voltage rises above (V_{SCD_TH}+$V_{SCD\_TH\_HY}$), the FAULTB pin will resume to high impedance. Never leave the SCD pin floating. If the SCD pin is unused, please connect it to the VOUT pin via a 10kΩ resistor.

The device monitors the LED string voltage via the SCD pin to report LED short fault condition, while the LED short fault protection action is implemented by the detecting output current sense resistor R_{IS} and voltage drop between VOUT pin and OUTSENSE pin to control the PMOS M_3.

In the PCR mode (MODE=VDD), when the LED string is shorted, the output PMOS constant current regulator keeps regulating the output current at set point (I_{LED}) to gradually discharge the output capacitor C_{OUT}, however the voltage drop between VOUT pin and OUTSENSE pin, V_{DO}, rises rapidly. If the V_{DO} rises above 1.5V (Typ.) and persists for longer than 2.5ms (Typ.), the device will decrease the output current to 20% of I_{LED} to reduce the power consumption on the PMOS M_3, and pull the FAULTB pin low to report the fault condition. The output current and the FAULTB pin state will resume when the LED string short fault condition is removed.

In the non-PCR mode (MODE=GND), when the LED string is shorted, the device controls the PMOS M_3 to clamp the output current at 1.33 (Typ.) times of I_{LED} to gradually discharge the output capacitor C_{OUT}. If either the current clamping persists for longer than 2.5ms (Typ.) or the V_{DO} rises above 1.5V (Typ.) for longer than 2.5ms (Typ.), the device will trigger hiccup protection and pull the FAULTB pin low to report the fault condition. The hiccup will repeat until the LED string short fault condition is removed.

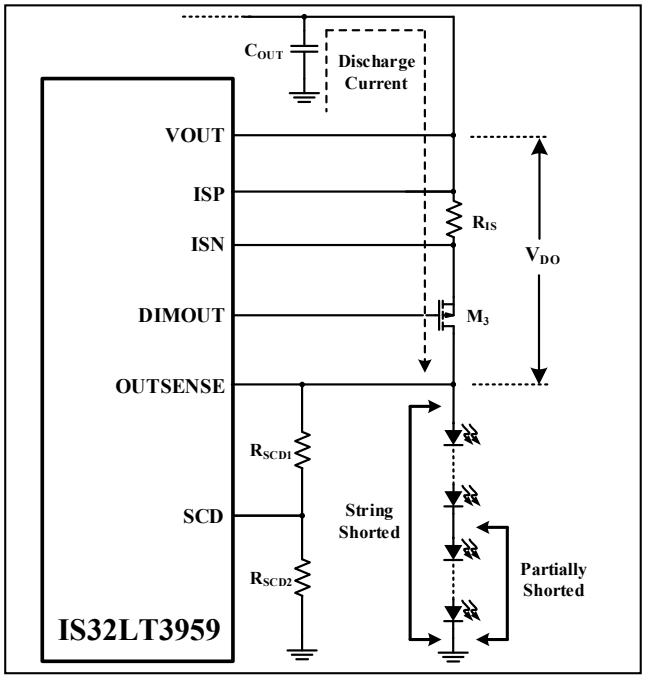


Figure 58 LED Short Protection

In case of the PMOS M_3 is not able to clamp the output current and the voltage across the output current sense resistor R_{IS}, (V_{ISP}-V_{ISN}), exceeds output over current protection threshold V_{SENSE_OC} for longer than 12μs (Typ.), the device will trigger hiccup protection and pull the FAULTB pin low to report the fault condition. The hiccup will repeat until the output over current fault condition is removed.

THERMAL SHUTDOWN PROTECTION

The temperature of the die is monitored to protect the device from damage when the maximum junction temperature is exceeded. If the die temperature exceeds the thermal shutdown temperature of 170°C (Typ.) the device will stop switching to enter standby mode and pulls the FAULTB pin low to report the fault condition. After a thermal shutdown event, the IS32LT3959 will not try to restart until its die temperature has reduced to less than 150°C (Typ.).

Table 2 Fault Actions

Fault Type	Fault Condition	Driver Action	FAULTB Pin	Fault Reset
LED Open (OVP)	$V_{FB} > V_{OVP\_TH1}$	Stops switching, pulls DIMOUT pin high and resets COMP to zero.	Pull low	$V_{FB} < (V_{OVP\_TH1}$-$V_{OVP\_TH1\_HY})$
LED Short (Output Over Current)	$V_{SCD} < V_{SCD\_TH}$	No action, only pulls FAULTB pin low.	Pull low	$V_{SCD} > (V_{SCD\_TH}+V_{SCD\_TH\_HY})$
	Output current clamped at I_{LED}x1.33 (Typ.)	If this fault condition persists longer than 2.5ms (Typ.), stops switching and hiccups with a t_{SKIP} period.		Output current drops below I_{LED}x1.33 (Typ.)
	$V_{DO} > 1.5V$ (Typ.)	If this fault condition persists longer than 2.5ms (Typ.), stops switching and hiccups with a t_{SKIP} period.		$V_{DO} < 1.5V$ (Typ.)
	$(V_{ISP}$-$V_{ISN}) > V_{SENSE\_OC}$	If this fault condition persists for longer than 12μs (Typ.), stops switching and hiccups with t_{SKIP} period time.		$(V_{ISP}$-$V_{ISN}) < V_{SENSE\_OC}$
Thermal Shutdown	$T_J > T_{SD}$	Stops switching, pulls DIMOUT pin high and resets COMP to zero.	Pull low	$T_J < (T_{SD}$-$T_{SD\_HY})$
VOUT Short to GND (Input Over Current)	$V_{CS} \geq V_{CS\_TH1}$	If this fault condition persists longer than 2.5ms (Typ.), stops switching and hiccups with a t_{SKIP} period time.	Pull low	$V_{CS} < V_{CS\_TH1}$
	$V_{CS} \geq V_{CS\_TH2}$	Stops switching and hiccups with a t_{SKIP} period time.		$V_{CS} < V_{CS\_TH2}$
	$(V_{CC}$-$V_{INSENSE}) \geq V_{IN\_OCTH}$	Turns off high-side NMOS, COMP high clamps. If this fault condition persists for longer than 2.5ms (Typ.), stops switching and hiccups with t_{SKIP} period time.		$(V_{CC}$-$V_{INSENSE}) < V_{IN\_OCTH}$
FS/SYNC Pin Open/Short	$V_{FS/SYNC} > 1.6V$ (Typ.) or < 0.6V (Typ.)	Operates with default 400kHz (Typ.) switching frequency.	Pull low	0.6V (Typ.) < $V_{FS/SYNC}$ < 1.6V (Typ.)
FPWM Pin Open/Short	$R_{FPWM} > 400k\Omega$ (Typ.) or < 6kΩ (Typ.)	Disables the internal PWM generator and gets full output current.	Pull low	6kΩ (Typ.) < R_{FPWM} < 400kΩ (Typ.)
Secondary OVP	$V_{OUT} > V_{OVP\_TH2}$	Stops switching, pulls DIMOUT pin high and resets COMP to zero.	Pull low	$V_{OUT} < (V_{OVP\_TH2}$-$V_{OVP\_TH2\_HY})$

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, PCB layout is a very critical design phase. If layout is not carefully done, operation instability as well as EMI problems may arise.

The high dV/dt surface and dI/dt loops are big noise emission sources. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage very compact. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

Please design the PCB layout according to following considerations.

(1) Wide and short traces should be used for connection of the high current paths that helps achieve better efficiency and EMI performance. Such as the traces for power supply, inductor L_1, power switches M_1, M_2 and M_3, Schottky diodes D_1 and D_2, current sense resistor R_{CS}, R_{IS} and R_{INSEN}, output to LED string, ground.

(2) Minimize the PCB area of the switching current loops. The input capacitors C_{IN}, inductor L_1, power switches M_1 and M_2, Schottky diodes D_1 and D_2, current sense resistor R_{CS}, and output capacitors C_{OUT} should be placed as close to each other as possible and the trace connections between them should be as short and wide as possible.

(3) The (-) terminals of the input capacitors C_{IN} should be connected as close as possible to the (-) terminals of the output capacitors C_{OUT}.

(4) Connect the bootstrap capacitor, C_{BST}, close to the BST and SW pins.

(5) The output OVP setting resistor divider, R_{O1} and R_{O2}, must be placed as close to FB and AGND pins as possible.

(6) The LED short detection resistor divider, R_{SCD1} and R_{SCD2}, must be placed as close to SCD and AGND pins as possible.

(7) The ground of the current sense resistor, R_{CS}, should be directly connected to SGND pin by a separate trace to prevent SGND plane jitter and ensure precise sensing.

(8) To avoid ground jitter, the parameter setting components should be placed close to the corresponding pins and return to the AGND pin, and keep their trace length to the pins as short as possible. On the other side, to prevent the noise coupling, the traces of these components should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for best accuracy and stability.

(9) The capacitors C_{VCC} and C_{VDD} should be placed as close as possible to VCC and VDD pin for good filtering.

(10) In practice, if the LED string is far away from the driver board and connected through long cables, the parasitic inductance in the cables will form a LC-resonant circuit with the C_{OUT}. In the case of hot plugging the output connector or an unreliable connector, this LC-resonant circuit will crease oscillation on the OUTSENSE pin due to the C_{OUT} fast discharging. This oscillation could subject the OUTSENSE pin to negative spike voltages exceeding their Absolute Maximum Ratings that may permanently damage the OUTSENSE pin. Add a 60V/1A Schottky diode D_P from the OUTSENSE pin to GND (placed close to OUTSENSE pin) to avoid this negative spike voltage. Figure 59.

Note that hot plugging the output connector is a non-standard operation; please avoid hot plugging during mass-production. Ensure that connections to the output connector are made solid and reliable.

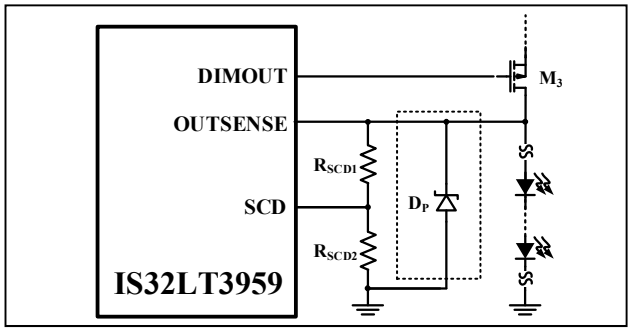


Figure 59 Schottky Diode for Hot Plugging Protection

(11) Flood all unused areas on all layers with copper that reduces the temperature rise of the power components. Connect the copper areas to GND.

(12) All thermal pads on the back of IS32LT3959, the Schottky diodes and the power NMOSs package must be soldered to a sufficient size of copper plane with sufficient vias to conduct the heat to opposite side PCB for adequate cooling.

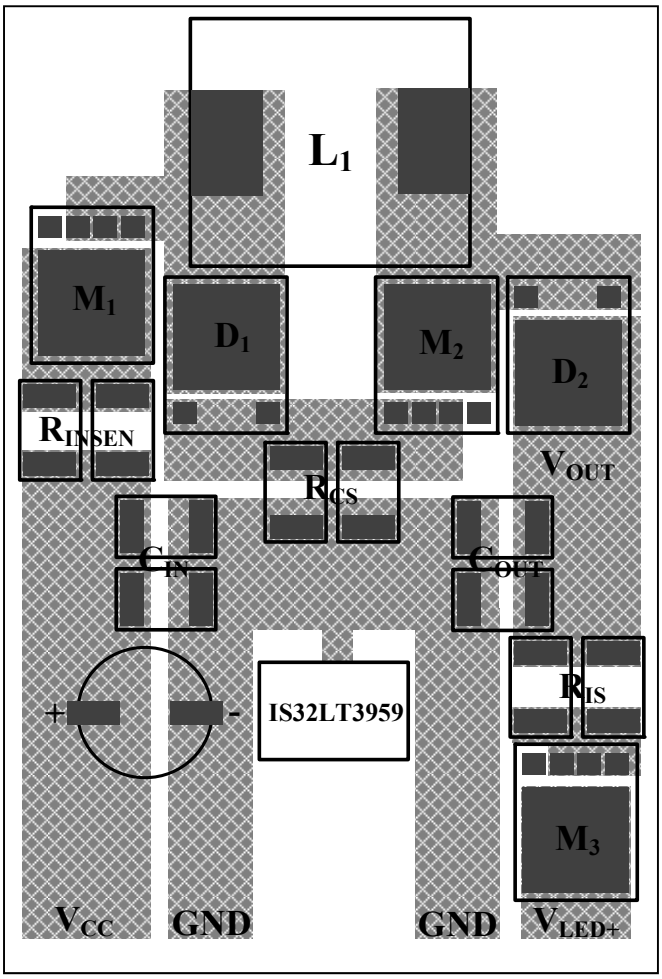


Figure 60 PCB Layout Example

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (30):

$$P_D = V_{CC} \times (I_{CC} + f_{SW} \times (Q_{G1} + Q_{G2})) \qquad (30)$$

And,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (31)$$

Where f_{SW} is the operating frequency. Q_{G1} and Q_{G2} are

the total gate charge of M_1 and M_2.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (32):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (32)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{31.3°C/W} \approx 3.99W \qquad (33)$$

for eTSSOP-28 package.

Figure 61, shows the power derating of the IS32LT3959 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

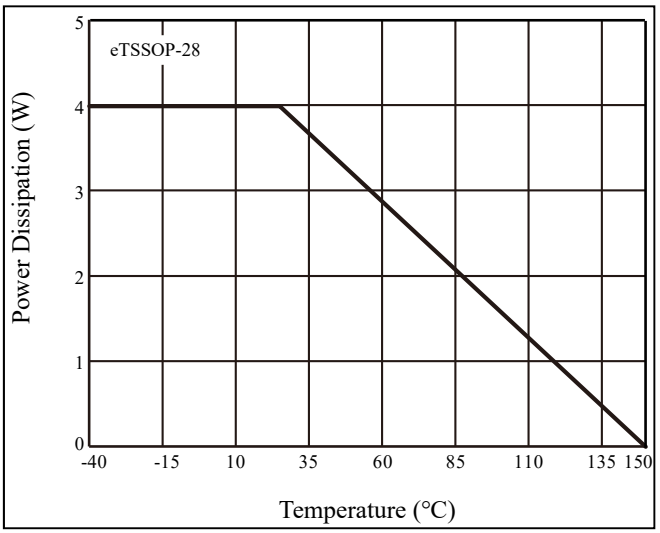


Figure 61 Dissipation Curve

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

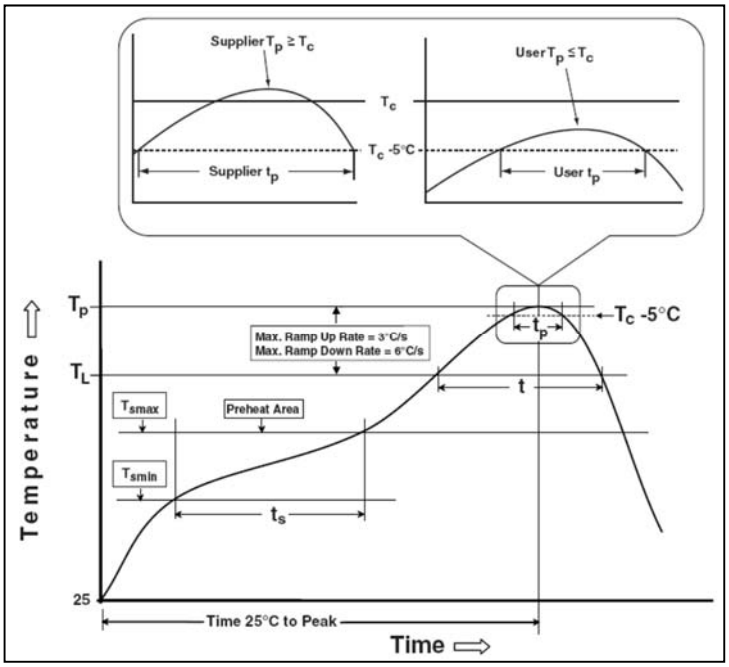
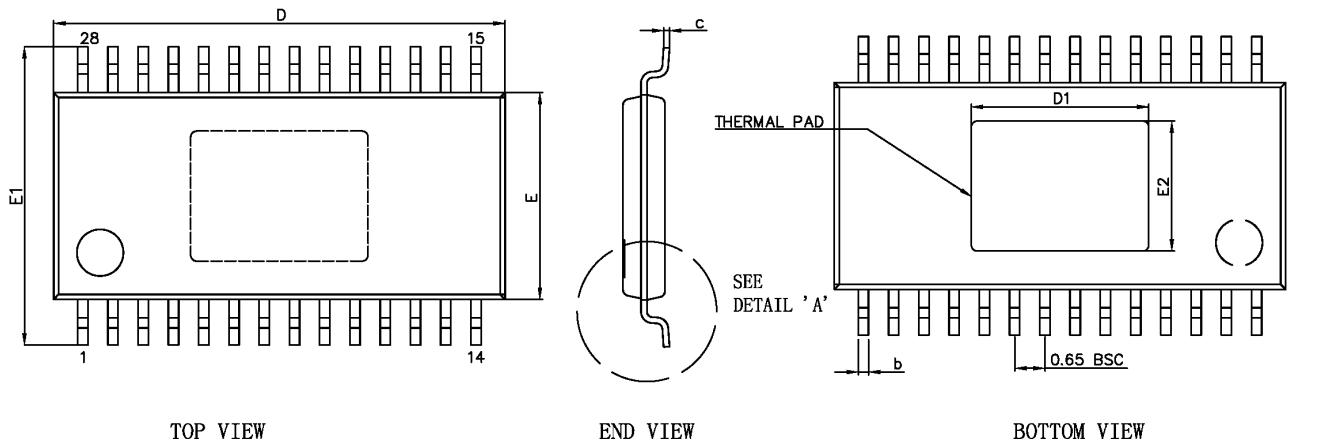


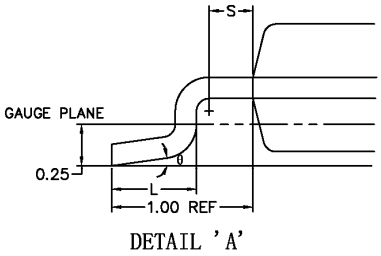
Figure 62 Classification Profile

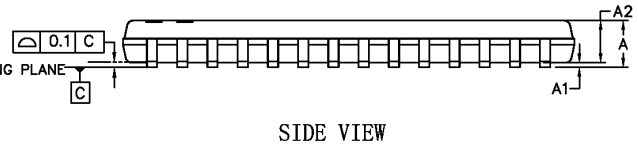
PACKAGE INFORMATION

eTSSOP-28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	9.60	9.70	9.80
D1	2.84	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

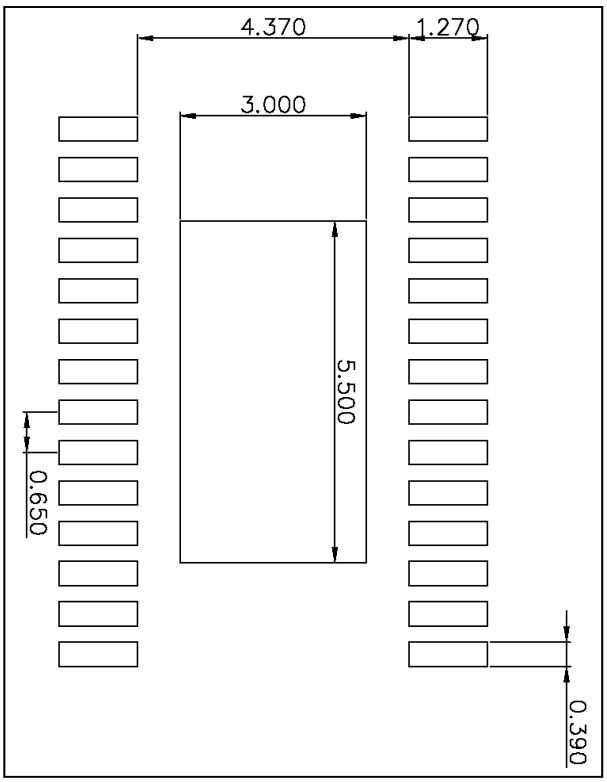




NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

eTSSOP-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.