

IS32LT3965

1.5-AMPERE PWM DIMMABLE SYNCHRONOUS BUCK LED DRIVER WITH LED THERMAL PROTECTION AND FAULT REPORTING

May 2023

GENERAL DESCRIPTION

The IS32LT3965 is a synchronous DC/DC switching LED driver that integrates high-side and low-side N-channel MOSFETs to operate in a Buck configuration. The device can operate from a wide input voltage between 3.8V and 38V and provides a constant current of up to 1.5A for driving a single LED or multiple series connected LEDs.

The external resistor, R_{IS} , is used to set a constant LED output current, while allowing the output voltage to be automatically adjusted for a variety of LED configurations.

The IS32LT3965 operates in a fixed frequency mode during switching, up to 2.2MHz. There is an external resistor connected between the VCC and TON pins used to configure the on-time (switching frequency). The switching frequency is dithered in spread spectrum operation which spreads the electromagnetic energy over a wider frequency band. This function is helpful for optimizing EMI performance.

A logic input PWM signal applied to the enable (EN/PWM) pin will adjust the average LED current by its PWM duty cycle. The EN/PWM pin also can be used to program an additional UVLO protection. The analog dimming pin ICTRL can implement LED dimming or LED string thermal roll-off protection.

True average output current operation is achieved with fast transient response by using cycle-by-cycle, controlled on-time method.

The IS32LT3965 is available in a WFCQFN-14 (3mm × 4mm) package with wettable flanks. It operates from 3.8V to 38V over the temperature range of -40°C to +125°C.

FEATURES

- Wide input voltage supply from 3.8V to 38V
- High-side sense and true average output current control, up to 1.5A maximum over temperature range
- Operating frequency up to 2.2MHz
- Forced Continuous Conduction Mode (FCCM) operation
- Integrated high-side and low-side MOSFET switches
- Cycle-by-cycle current limit
- Dimming via PWM logic input or analog voltage
 - Supports LED thermal roll-off or LED binning
- Internal control loop compensation
- Externally programmable undervoltage lockout (UVLO)
- 1µA low power shutdown
- Spread spectrum to optimize EMI
- Robust fault protection and reporting function:
 - Pin-to-GND short
 - Component open/short faults
 - LED string open/short
 - Junction thermal roll-off
 - Thermal shutdown
 - Shared fault flag for multiple device operation to comply with “one-fail-all-fail” function
- AEC-Q100 Qualified
- RoHS & Halogen-Free Compliance
- TSCA Compliance

APPLICATIONS

- Logo lamp
- License plate lights
- Interior lights
- Turn/stop lights
- Front and rear fog lights

IS32LT3965

TYPICAL APPLICATION CIRCUIT

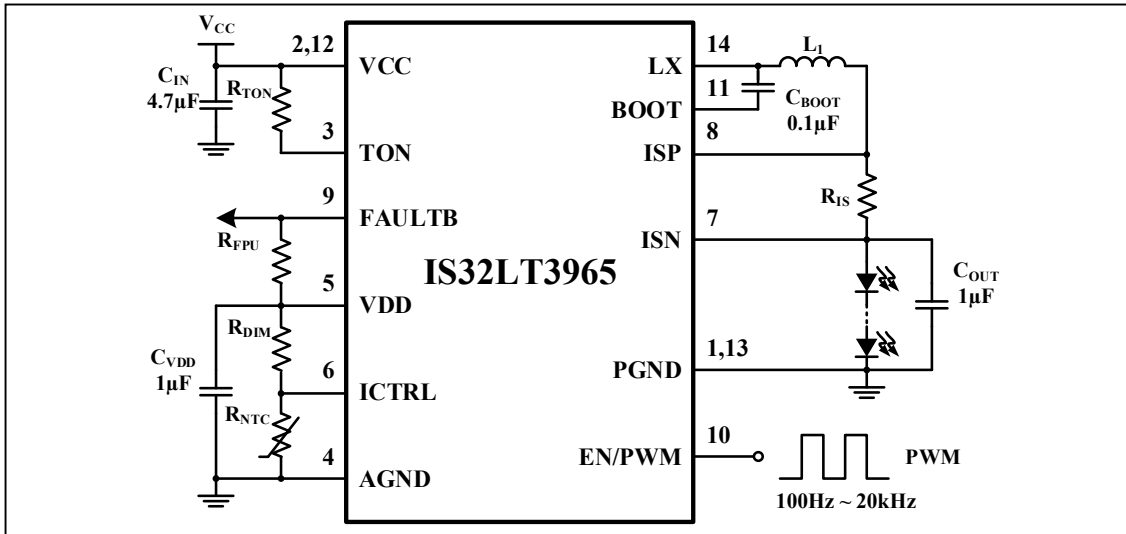
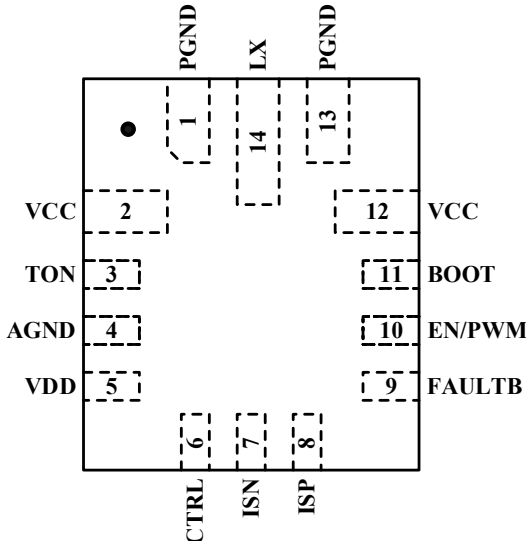


Figure 1 Typical Application Circuit

IS32LT3965

PIN CONFIGURATION

Package	Pin Configuration (Top View)
WFCQFN-14	

PIN DESCRIPTION

No.	Pin	Description
1,13	PGND	Power ground.
2,12	VCC	Power supply input. Connect a bypass capacitor C_{IN} to ground. The path from C_{IN} to PGND and VCC pins should be as short as possible.
3	TON	On-time setting. Connect a resistor from this pin to VCC pin to set the regulator controlled on-time (switching frequency).
4	AGND	Signal ground.
5	VDD	Internal 5V (Typ.) regulator output pin. Connect a $1\mu\text{F}$ X7R ceramic capacitor from this pin to AGND. This capacitor must be placed as close to VDD pin as possible.
6	ICTRL	Analog dimming pin.
7	ISN	LED current sense negative input.
8	ISP	LED current sense positive input.
9	FAULTB	Open drain I/O diagnostic pin. Active low output driven by the device when it detects a fault condition. As an input, this pin will accept an externally generated FAULTB signal to disable the device output to satisfy the "One-Fail-All-Fail" function. Note this pin requires an external pull up resistor (R_{FPU}). Do not allow to float.
10	EN/PWM	Enable and PWM dimming pin. Pull up above V_{ENTH} to enable and below ($V_{ENTH} - V_{ENTH_HY}$) to disable. Input a 100Hz~20kHz PWM signal to dim the LED brightness. This pin also can be used in conjunction with external resistor divider to set external UVLO for VCC.
11	BOOT	Internal MOSFET gate driver bootstrap. Connect a $0.1\mu\text{F}$ X7R ceramic capacitor from this pin to LX pin.
14	LX	Internal high-side and low-side MOSFET switches output. Connect this pin to the inductor.

IS32LT3965

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3965-QWCLA3-TR	WFCQFN-14, Lead-free	2500

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

IS32LT3965

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Input voltage, V_{CC} (Note 2)	-0.3V ~ +42V
Bootstrap to switching voltage, ($V_{BOOT} - V_{LX}$)	-0.3V ~ +6.0V
Switching voltage, V_{LX} (Steady state)	-0.6V ~ $V_{CC} + 0.3V$
Switching voltage, V_{LX} (Transient < 10ns)	-3.0V
EN/PWM, TON, FAULTB, ISN and ISP voltage, $V_{EN/PWM}$, V_{TON} , V_{FAULTB} , V_{ISN} and V_{ISP}	-0.3V ~ $V_{CC} + 0.3V$
VDD and ICTRL voltage, V_{DD} and V_{CTRL}	-0.3V ~ 6.0V
Power dissipation, $P_{D(MAX)}$	2.33W
Operating temperature, $T_A = T_J$	-40°C ~ +150°C
Storage temperature, T_{STG}	-65°C ~ +150°C
Maximum operating junction temperature, T_{JMAX}	+150°C
Junction Package thermal resistance, junction to ambient (4-layer standard test PCB based on JEDEC 51-2A), θ_{JA}	53.7°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JEDEC 51-8), θ_{JP}	17.7°C/W
ESD (HBM)	±2kV
ESD (CDM)	±750V

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: A maximum of 44V can be sustained at this pin for a duration of $\leq 2s$.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 24V$, $T_J = T_A = -40^\circ C \sim +150^\circ C$, Typical values are at $T_J = 25^\circ C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Input supply voltage		3.8		38	V
V_{UVLO}	VCC undervoltage-lockout threshold	V_{CC} rising	3.3	3.5	3.7	V
V_{UVLO_HY}	VCC undervoltage-lockout hysteresis	V_{CC} falling		250		mV
I_{CC}	VCC pin supply current	$(V_{ISP} - V_{ISN}) = 0.5V$, EN/PWM= High, LX= GND		0.7	1	mA
I_{SD}	VCC pin shutdown current	EN/PWM= GND for $> t_{PWML}$		1	5	μA
V_{DD}	Regulator output voltage	$I_{DD} < 5mA$, $V_{CC} > 6V$	4.85	5.0	5.15	V
I_{DD_LIM}	Regulator output current limit	$V_{CC} = 12V$, $V_{DD} = 0V$	20			mA
I_{HSLIM}	High-side switch current limit threshold	$V_{CC} = 12V$	2.5	3	3.5	A
I_{LSLIM}	Low-side switch reverse current limit threshold	$V_{CC} = 12V$		1		A
t_{OCP}	Over Current Protection (OCP) hiccup time	$V_{CC} = 12V$ (Note 3)		10		ms
$R_{DS(on)_HS}$	High-side switch on-resistance	$V_{BOOT} = V_{CC} + 4.3V$, $I_{LX} = 1A$, $V_{CC} = 12V$		0.2	0.4	Ω
$R_{DS(on)_LS}$	Low-side switch on-resistance	$I_{LX} = 1A$, $V_{CC} = 12V$		0.1	0.25	Ω
V_{BTUV}	BOOT undervoltage-lockout threshold	V_{BOOT} to V_{LX} increasing $V_{CC} = 12V$		2.76		V
V_{BTUV_HY}	BOOT undervoltage-lockout hysteresis	V_{BOOT} to V_{LX} decreasing $V_{CC} = 12V$		350		mV
t_{OFF_MIN}	Switching minimum off-time	$(V_{ISP} - V_{ISN}) = 0V$		70	90	ns
t_{ON_MIN}	Switching minimum on-time			60	80	ns

IS32LT3965

ELECTRICAL CHARACTERISTICS (CONTINUE)

$V_{CC}=24V$, $T_A=T_J=-40^{\circ}C \sim +150^{\circ}C$, Typical values are at $T_J=25^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Selected on-time	$V_{CC}=24V$, $V_{OUT}=12V$, $R_{TON}=580k\Omega$	900	1000	1100	ns
		$V_{CC}=24V$, $V_{OUT}=12V$, $R_{TON}=115k\Omega$	225	245	265	ns
Regulation Comparator And Error Amplifier						
V_{IS}	Load current sense regulation threshold without analog dimming ($V_{ISP}-V_{ISN}$)	($V_{ISP}-V_{ISN}$) falling, LX turns on, $V_{ICTRL}>2.4V$, $V_{ISN}>2.5V$, $T_J=-40^{\circ}C \sim 125^{\circ}C$	195	200	205	mV
$V_{IS_{10}}$	Load current sense regulation threshold at 10% analog dimming ($V_{ISP}-V_{ISN}$)	($V_{ISP}-V_{ISN}$) falling, LX turns on, $V_{ICTRL}=0.96V$, $V_{ISN}>2.5V$, $T_J=-40^{\circ}C \sim 125^{\circ}C$	17.5	20	22.5	mV
I_{ISP}	ISP pin bias current	$V_{ISP}=12.2V$, $V_{ISN}=12V$		190		μA
I_{ISN}	ISN pin bias current	$V_{ISP}=12.2V$, $V_{ISN}=12V$		100		μA
Fault Output						
V_{FAULTB}	FAULTB pin pull down voltage	Fault condition, sink current $I_{OL}=5mA$		0.1	0.2	V
I_{LK_FAULTB}	FAULTB pin leakage current	No fault condition, pull up to 12V			1	μA
t_{DELAY}	FAULTB report/recover delay time			10		ms
V_{FAULTB_IH}	FAULTB pin input high enable threshold		1.4			V
V_{FAULTB_IL}	FAULTB pin input low disable threshold				0.4	V
Enable And ICTRL						
V_{ENTH}	EN/PWM pin threshold voltage	Voltage rising	1.15	1.20	1.25	V
V_{ENTH_HY}	EN/PWM pin threshold voltage hysteresis	Voltage falling		100		mV
t_{PWML}	Duration EN/PWM pin kept low to shut down the device		100	130	160	ms
t_{PWH}	Duration EN/PWM pin kept high to quit from shutdown mode			25	50	μs
t_{PWMSW}	The latency of EN/PWM pull high to IC starts switching			100	150	μs
V_{ICTRL_RG}	Analog dimming range		0.88		2.4	V
V_{ICTRL_MAX}	Analog dimming fully on threshold		2.3	2.4	2.5	V
V_{ICTRL_OFF}	ICTRL force output off threshold	Voltage falling		0.4		V
V_{ICTRL_OFFHY}	ICTRL force output off hysteresis	Voltage rising		200		mV
I_{ICTRL}	ICTRL pin input current	$V_{ICTRL} > 2.4V$		-25		nA
		$V_{ICTRL} < 2.4V$		0		

IS32LT3965

ELECTRICAL CHARACTERISTICS (CONTINUE)

$V_{CC} = 24V$, $T_A = T_J = -40^{\circ}C \sim +150^{\circ}C$, Typical values are at $T_J = 25^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Thermal Protection						
T_{RO}	Thermal roll-off activation temperature	(Note 3)		150		$^{\circ}C$
T_{SD}	Thermal shutdown threshold	(Note 3)		170		$^{\circ}C$
T_{SDHYS}	Thermal shutdown hysteresis	(Note 3)		20		$^{\circ}C$

Note 3: Guaranteed by design.

IS32LT3965

TYPICAL PERFORMANCE CHARACTERISTICS

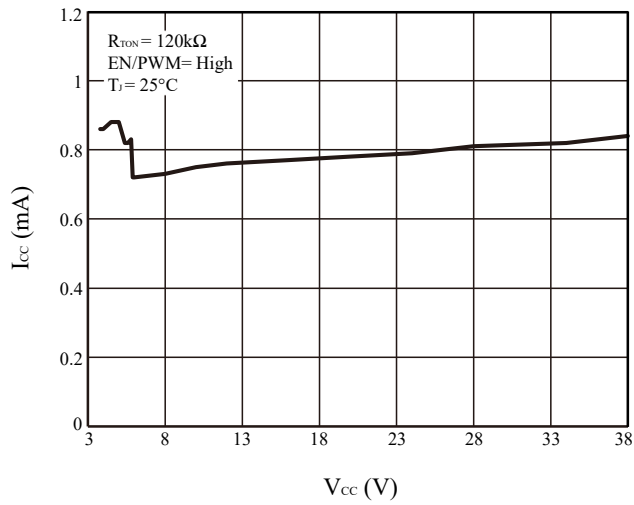


Figure 2 I_{CC} vs. V_{CC}

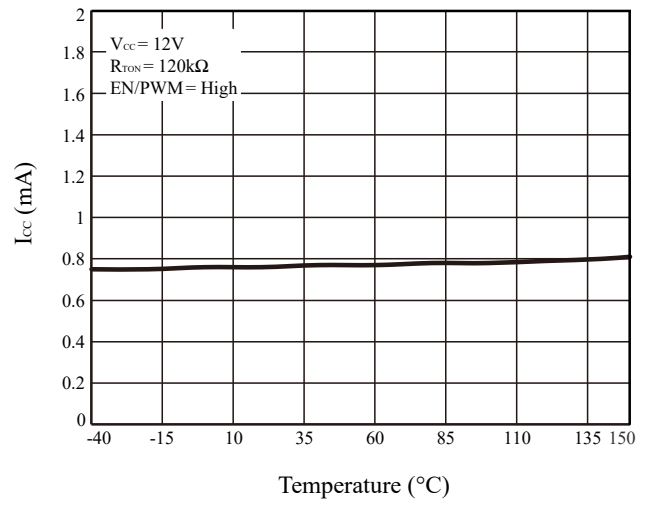


Figure 3 I_{CC} vs. Temperature

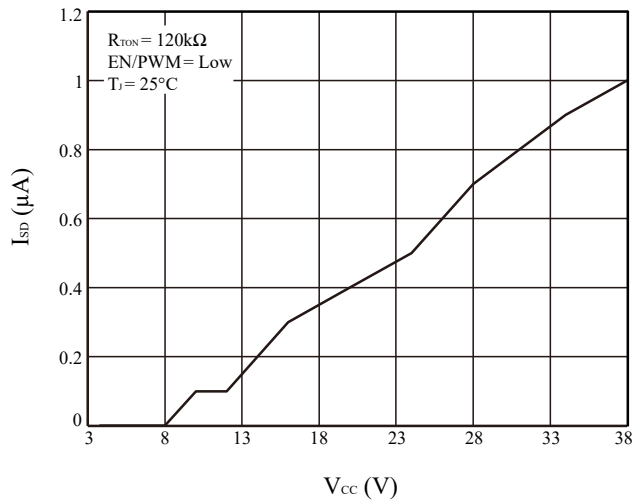


Figure 4 I_{SD} vs. V_{CC}

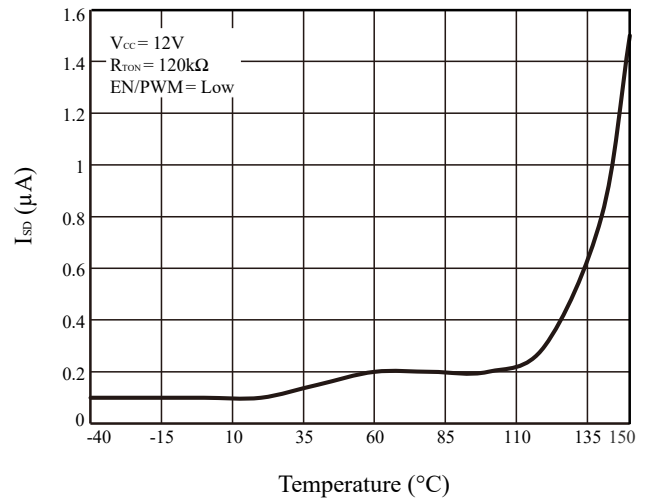


Figure 5 I_{SD} vs. Temperature

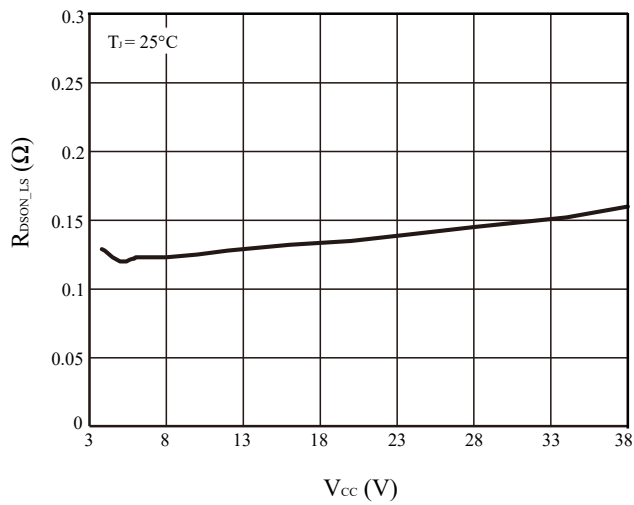


Figure 6 R_{DS(on)_LS} vs. V_{CC}

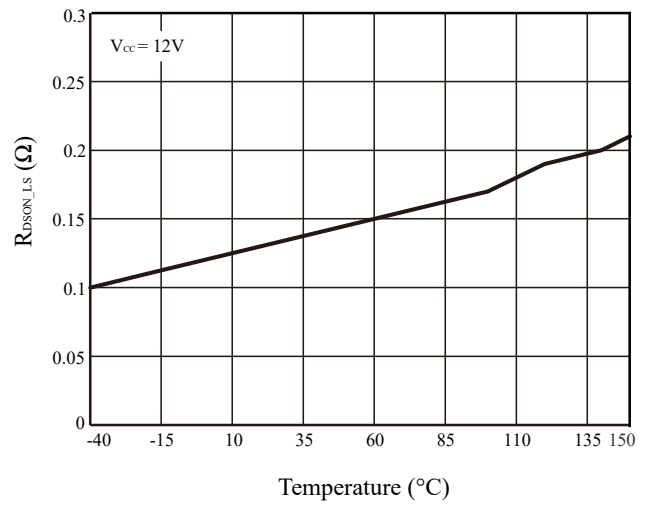


Figure 7 R_{DS(on)_LS} vs. Temperature

IS32LT3965

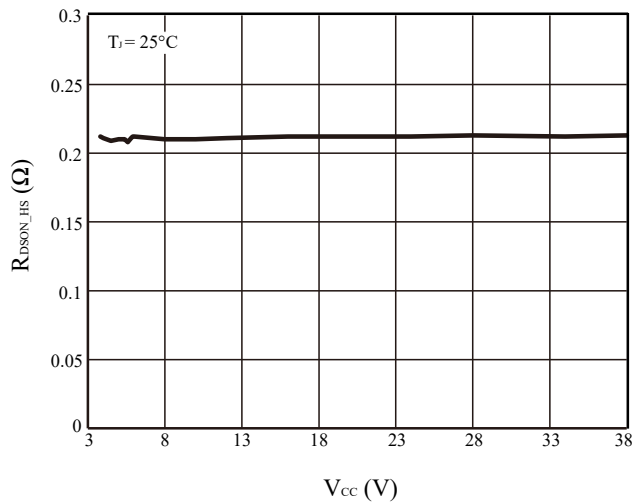


Figure 8 R_{DSON_HS} vs. V_{CC}

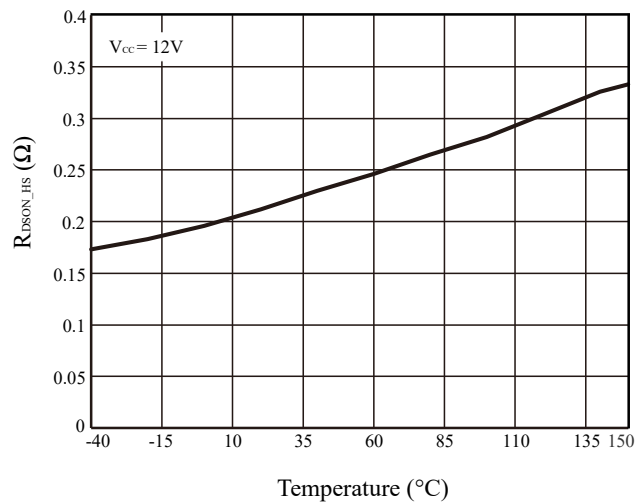


Figure 9 R_{DSON_HS} vs. Temperature

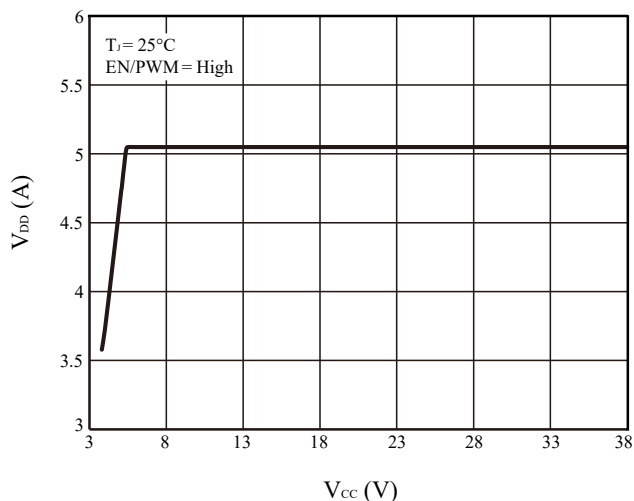


Figure 10 V_{DD} vs. V_{CC}

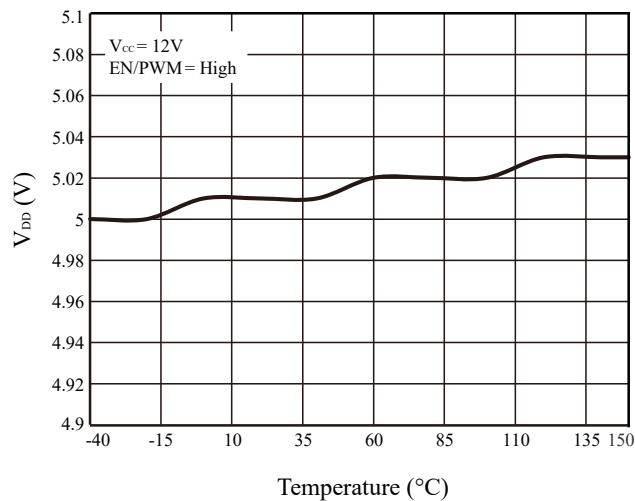


Figure 11 V_{DD} vs. Temperature

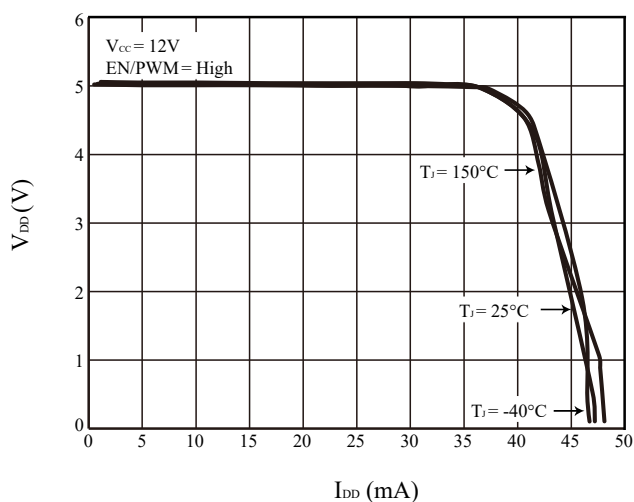


Figure 12 V_{DD} vs. I_{DD}

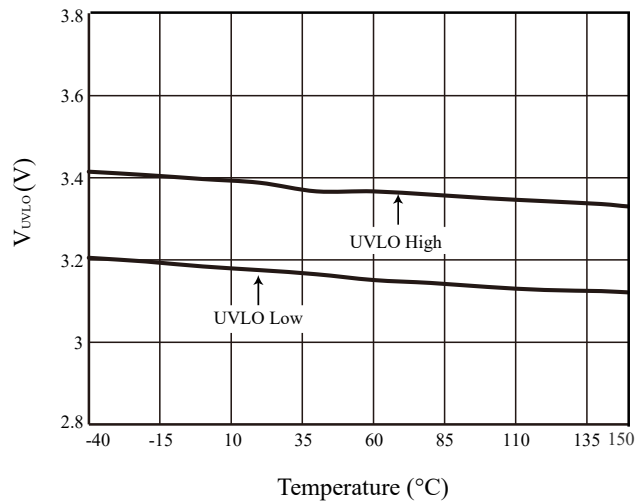


Figure 13 V_{UVLO} vs. Temperature

IS32LT3965

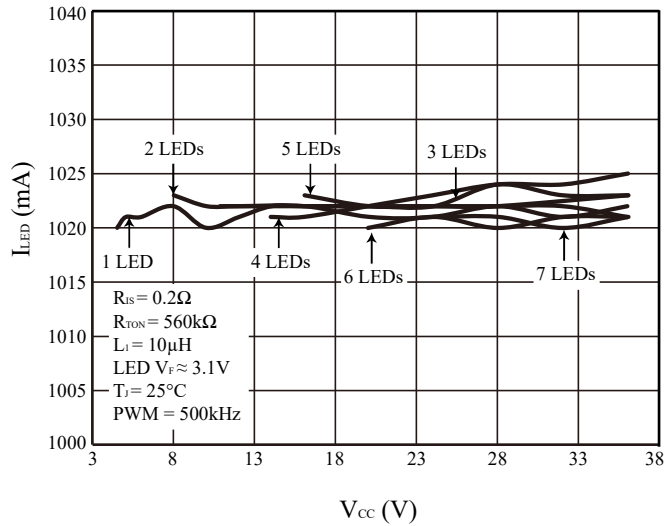


Figure 14 I_{LED} vs. V_{CC}

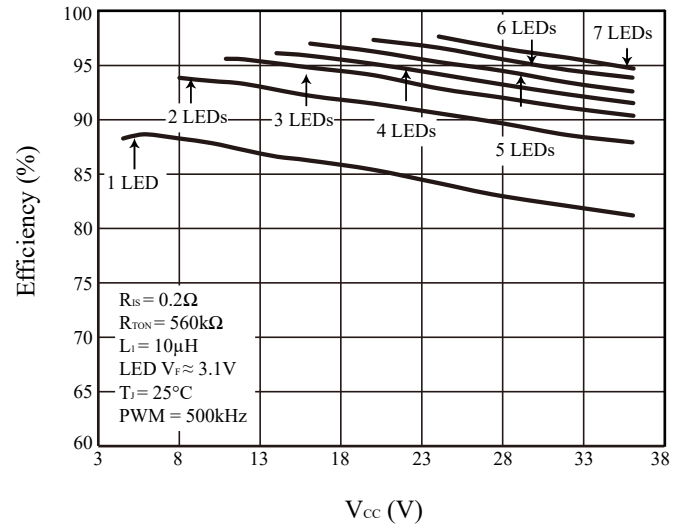


Figure 15 Efficiency vs. V_{CC}

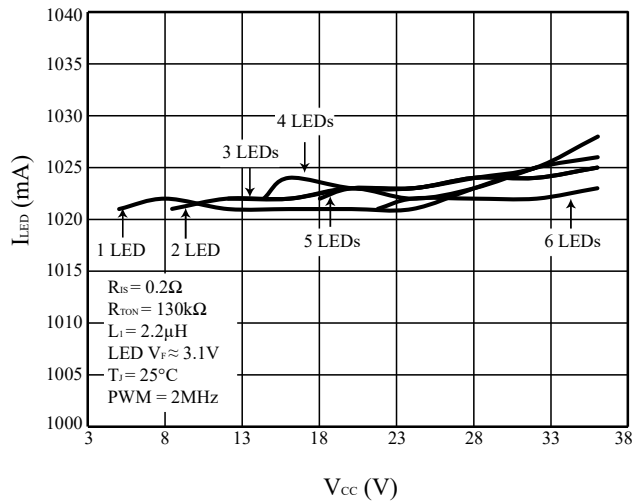


Figure 16 I_{LED} vs. V_{CC}

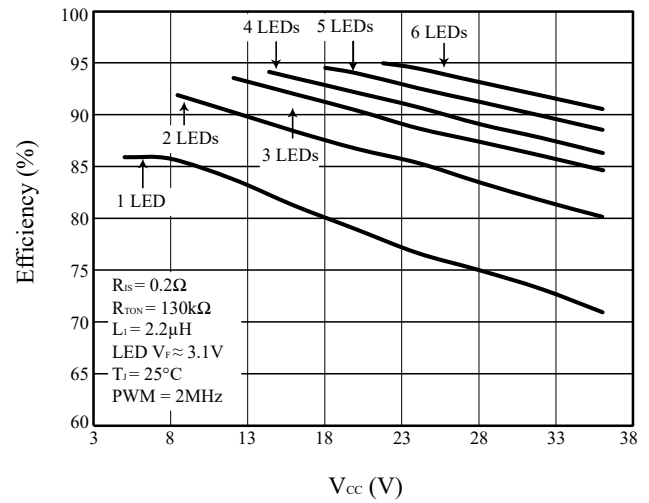


Figure 17 Efficiency vs. V_{CC}

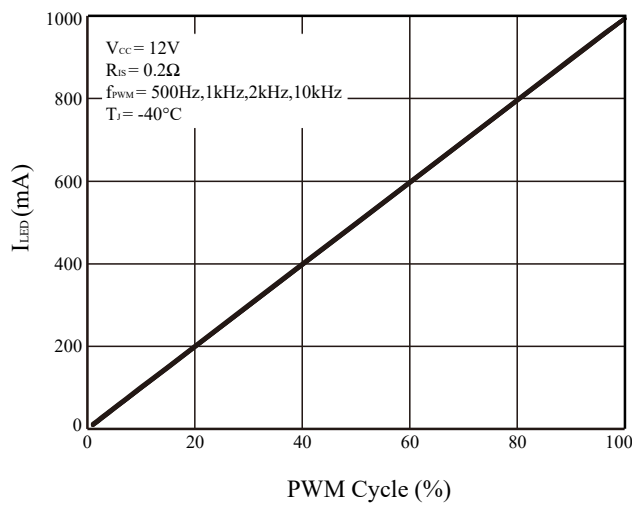


Figure 18 I_{LED} vs. PWM Cycle

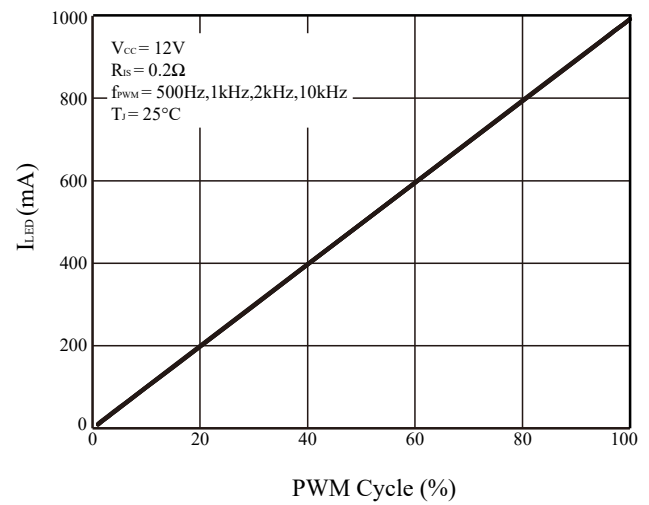


Figure 19 I_{LED} vs. PWM Cycle

IS32LT3965

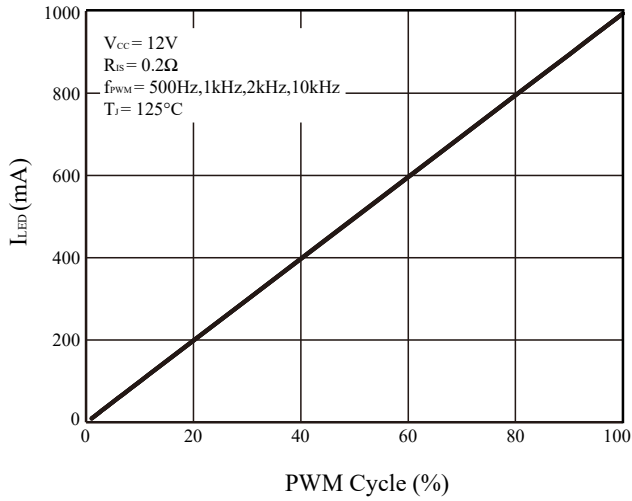


Figure 20 I_{LED} vs. PWM Cycle

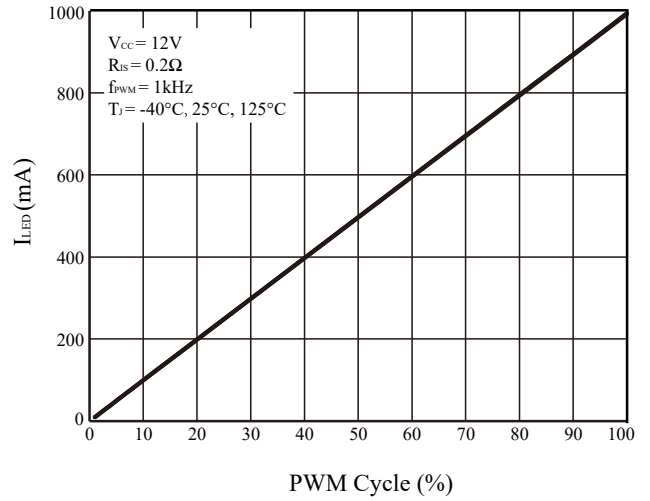


Figure 21 I_{LED} vs. PWM Cycle

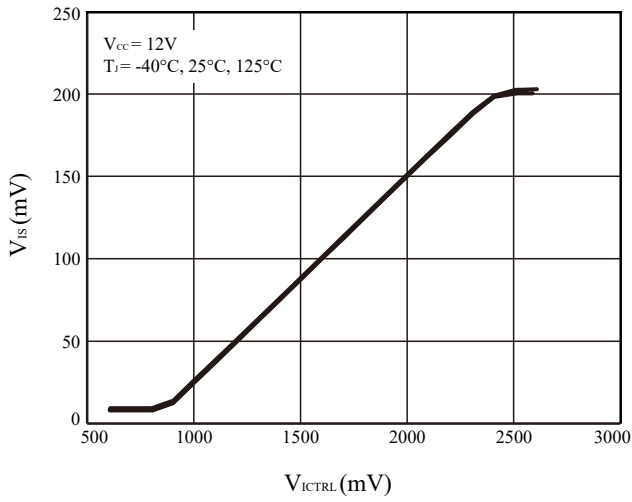


Figure 22 V_{IS} vs. V_{ICTRL}

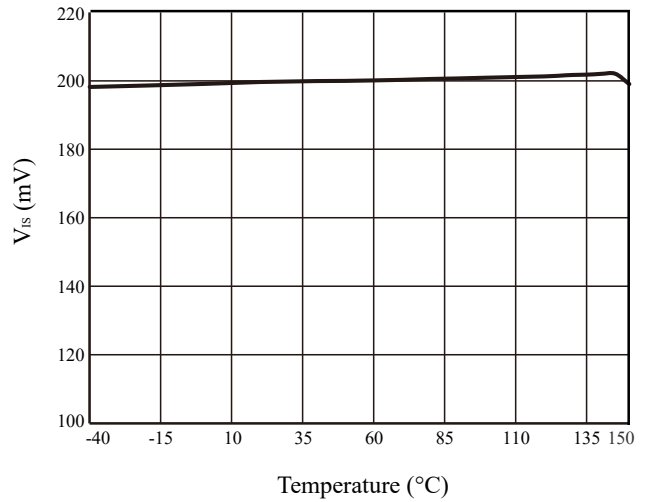


Figure 23 V_{IS} vs. Temperature

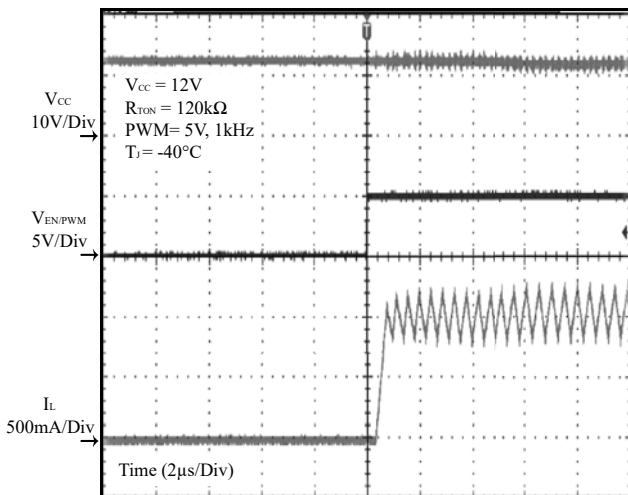


Figure 24 PWM On

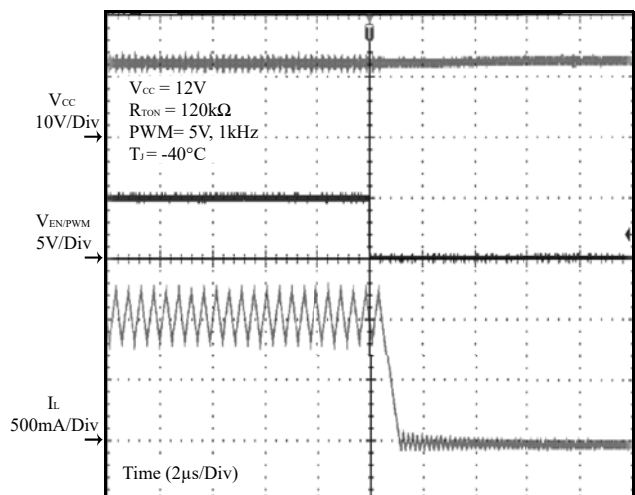


Figure 25 PWM Off

IS32LT3965

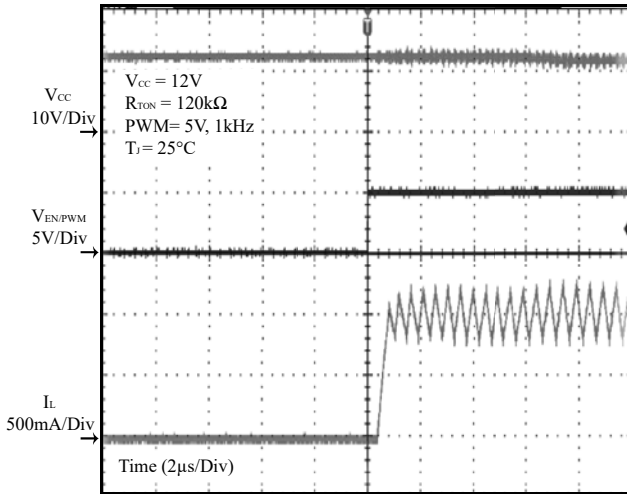


Figure 26 PWM On

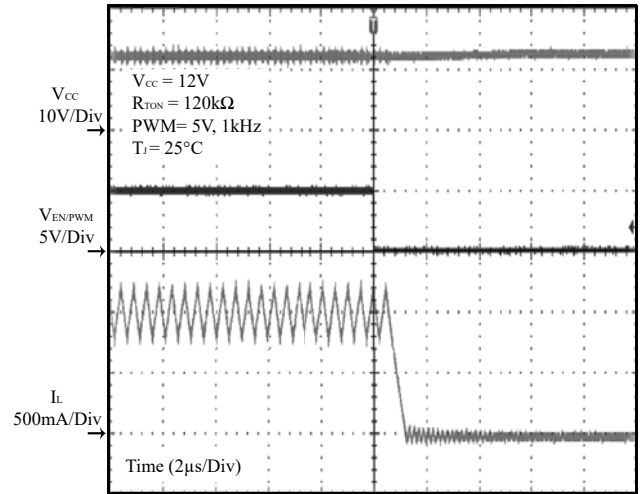


Figure 27 PWM Off

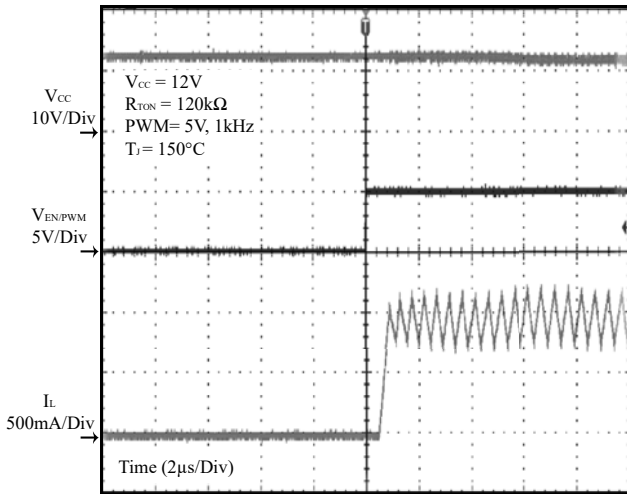


Figure 28 PWM On

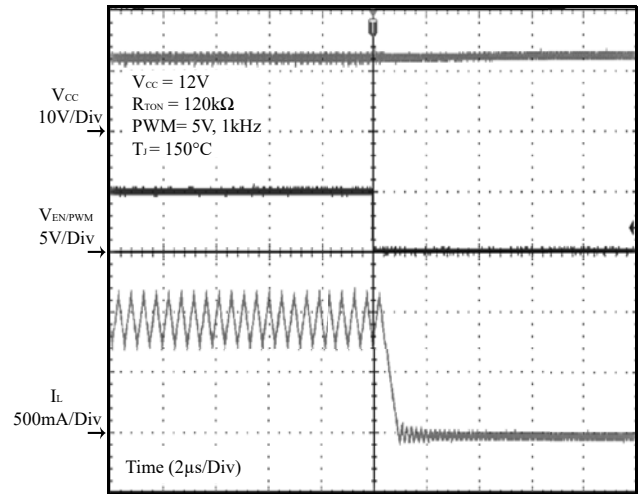


Figure 29 PWM Off

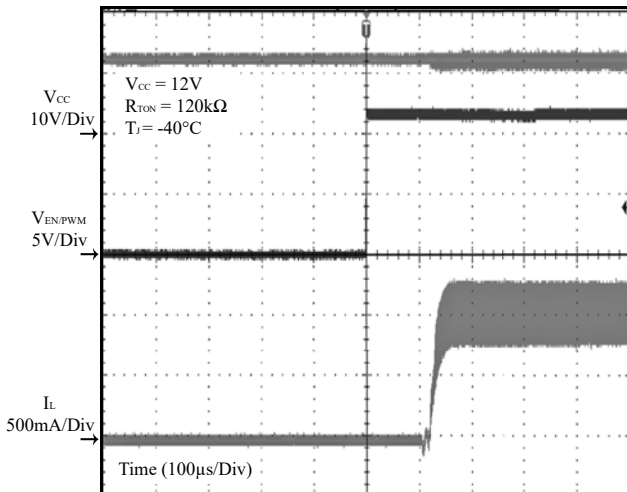


Figure 30 EN/PWM Enable

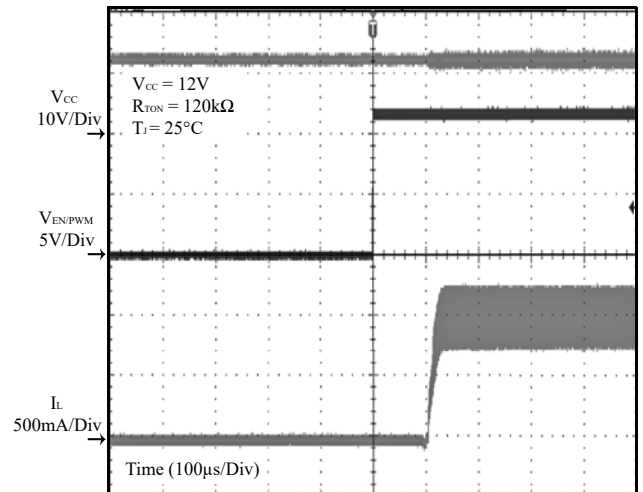


Figure 31 EN/PWM Enable

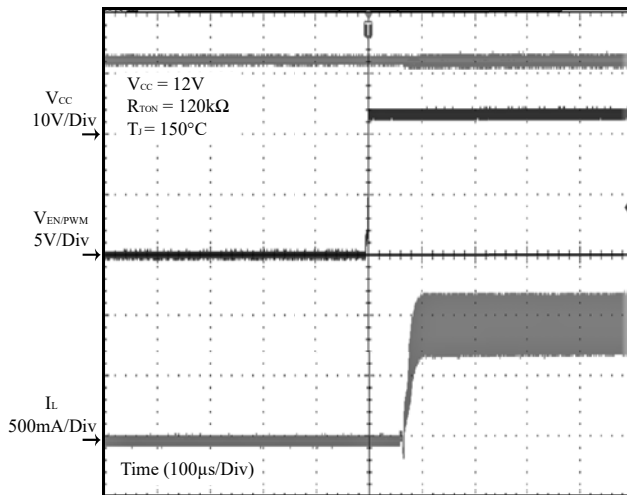
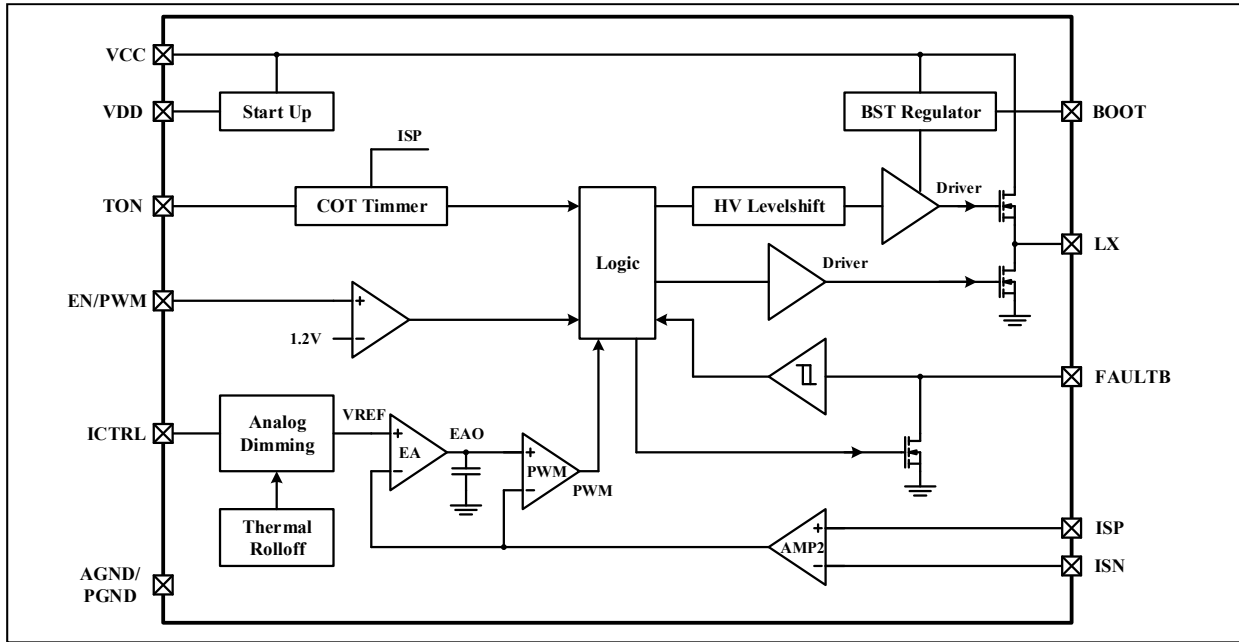


Figure 32 EN/PWM Enable

IS32LT3965

FUNCTIONAL BLOCK DIAGRAM



IS32LT3965

APPLICATION INFORMATION

DESCRIPTION

The IS32LT3965 is a synchronous Buck LED driver with wide input voltage, low reference voltage, quick output response and excellent PWM/analog dimming performance, which is ideal for driving a high-current LED string. It uses average current mode control to maintain constant LED current for consistent brightness.

UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3965 features an undervoltage-lockout (UVLO) function on the VCC pin. This is a fixed value which cannot be adjusted. The device is enabled when the VCC voltage rises to exceed V_{UVLO} (Typ. 3.5V), and disabled when the VCC voltage falls below ($V_{UVLO} - V_{UVLO_HY}$) (Typ. 3.25V).

Besides this internal, fixed UVLO, it may be desirable to externally set a higher UVLO threshold for some applications. A precise UVLO threshold voltage can be set by using a resistor voltage divider between VCC and GND with the center connected to the EN/PWM pin.

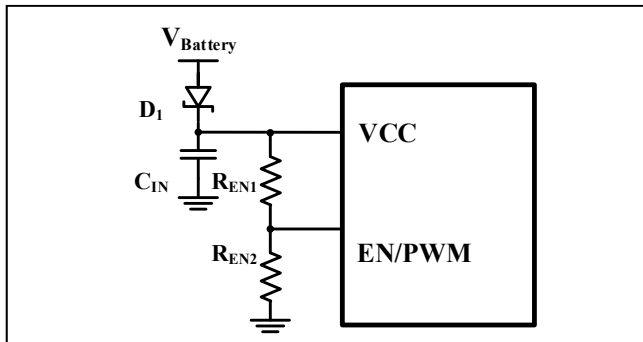


Figure 33 External UVLO for VCC

The external UVLO threshold voltage can be computed by the following Equations:

$$V_{UVLO_EXTR} = V_{ENTH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \quad (1)$$

$$V_{UVLO_EXTF} = (V_{ENTH} - V_{ENTH_HY}) \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \quad (2)$$

The output source is enabled when the VCC voltage exceeds V_{UVLO_EXTR} , and disabled when the VCC voltage falls below V_{UVLO_EXTF} .

It is recommended that R_{EN1} and R_{EN2} be 1% accuracy resistors with good temperature characteristics to ensure a precise detection. On the PCB layout, this resistor divider must be placed as close as possible to the EN/PWM pin to avoid noise coupling into the UVLO detection.

VDD

The IS32LT3965 integrates a 5V linear regulator with I_{DD_LIM} current limit to power the internal control circuits. Its output is the VDD pin which requires a 1 μ F low ESR,

X7R type ceramic capacitor from VDD to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, it can be used to supply the reference voltage for the ICTRL input or for the pullup resistor used with the FAULTB output.

BOOTSTRAP CIRCUIT

The gate driver of the integrated high-side MOSFET requires a voltage above VCC as an input power supply. As in below circuit diagram, there is another dedicated internal 5.4V LDO which is the power supply of the gate driver. The BOOT pin is internally connected to the output of the 5.4V LDO. Connect a ceramic capacitor between BOOT and LX pins. The VCC supplies the power to the 5.4V LDO which charges the C_{BOOT} capacitor during high-side MOSFET off cycles. Then in high-side MOSFET on cycles, the C_{BOOT} charge voltage is used to boost the BOOT pin to 5.4V higher than LX pin.

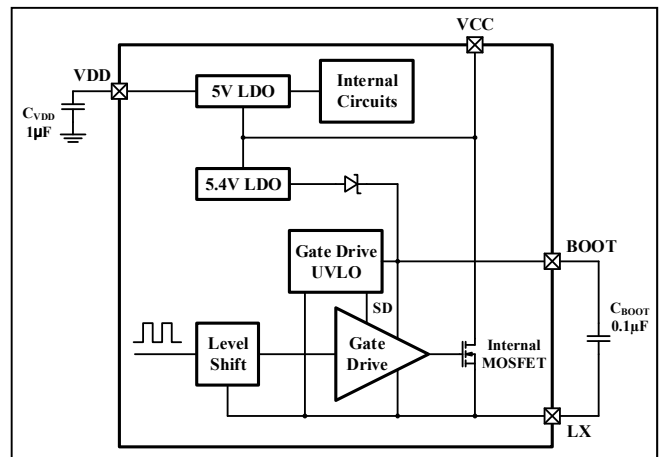


Figure 34 LDOs and Bootstrap Circuit

A 0.1 μ F X7R ceramic capacitor will work well in most applications. The gate driver also has an undervoltage-lockout detection. The gate driver is enabled when the voltage on the C_{BOOT} rises to above V_{BTUV} (Typ. 2.76V), and disabled when the voltage on the C_{BOOT} drops below ($V_{BTUV} - V_{BTUV_HY}$) (Typ. 2.41V).

OUTPUT CURRENT SETTING

The LED current is configured by an external sense resistor, R_{IS} , with a value determined by the following Equation (3):

$$I_{LED} = \frac{V_{IS}}{R_{IS}} \quad (3)$$

Where the analog dimming function is disabled ($V_{CTRL} > 2.4V$) and $V_{IS} = 0.2V$ (Typ.).

Note that $R_{IS} = 0.133\Omega$ is the minimum allowed value for the sense resistor in order to maintain the switch current below the specified maximum value.

IS32LT3965

Table 1 R_{IS} Resistance Versus Output Current

R _{IS} (Ω)	Nominal Average Output Current (mA)
0.3	667
0.2	1000
0.133	1500

The resistor R_{IS} should be a 1% resistor with enough power tolerance and good temperature characteristic to ensure accurate and stable output current.

ENABLE AND PWM DIMMING

A high logic signal (>V_{ENTH}) on the EN/PWM pin will enable the IC. The buck driver ramps up the LED current to a target level which is set by external resistor, R_{IS}.

When the EN/PWM pin goes from high to low, the buck driver will turn off, but the IC remains in standby mode for up to t_{PWML}. When the EN/PWM pin goes high within this period, the LED current will turn on immediately. Sending a PWM (pulse-width modulation) signal to the EN/PWM pin will result in dimming of the LED. The resulting LED brightness is proportional to the duty cycle of the PWM signal. A practical range for PWM dimming frequency is between 100Hz and 20kHz.

There is an inherent PWM turn on delay time of about 500ns during continuous PWM dimming. A high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. At a 200Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower.

If the EN/PWM pin is kept low for at least t_{PWML}, the IC enters shutdown mode to reduce power consumption. The next high signal on EN/PWM will initialize a full startup sequence, which includes a shutdown quit time, t_{PWMH}, and a startup latency, t_{PWMSW}. This startup sequence does not happen in a typical PWM dimming operation.

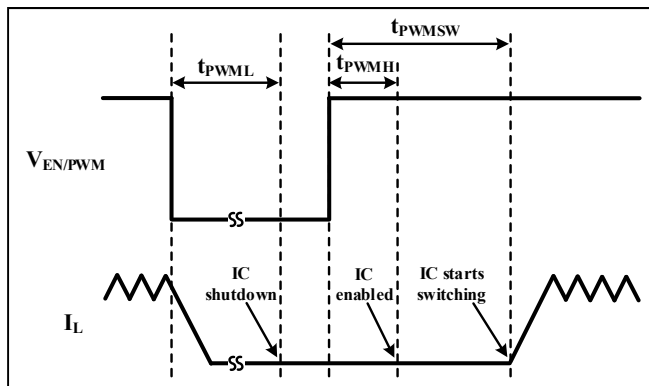


Figure 35 Device Shutdown and Enable

The EN/PWM pin is high impedance and high-voltage tolerant and can be connected directly to the VCC pin

if the EN/PWM pin is unused. However, a series resistor (recommended value of 10kΩ) is required to limit the current flowing into the EN/PWM pin if it is higher than the V_{CC} voltage at any time. If EN/PWM is driven with PWM logic input, the series resistor is not necessary.

ANALOG DIMMING

The IS32LT3965 also offers an analog dimming function on input pin, ICTRL, whose dimming voltage range is V_{ICTRL_RG} (0.88V to 2.4V). The current sense voltage threshold, V_{IS}, can be regulated by the ICTRL pin voltage. If the ICTRL pin is pulled up above V_{ICTRL_MAX} (typical 2.4V), analog dimming is disabled, and the output current is given by Equation (3). When the ICTRL voltage (V_{ICTRL}) is driven within 0.88V to V_{ICTRL_MAX}, V_{ICTRL} will proportionally control the current sense voltage threshold V_{IS} resulting in a linear change in the output current as given by Equation (4):

$$I_{LED_ICTRL} = \frac{V_{ICTRL} - 0.8V}{1.6V} \times \frac{V_{IS}}{R_{IS}} \quad (4)$$

$$(0.88V \leq V_{ICTRL} \leq 2.4V)$$

When the ICTRL pin voltage is driven below 0.88V, the current sense voltage threshold is clamped at 10mV (Typ.). The ICTRL pin features a forcing output off threshold, V_{ICTRL_OFF} (typical 0.4V). Pulling the ICTRL pin below V_{ICTRL_OFF} can completely turn off the output.

Note that the relative current accuracy decreases with the decreasing current sense voltage threshold due to the offset of the internal circuit. Therefore, the recommended minimum analog dimming level is around 10%. At low analog dimming level (such as below 20%), the inductor current ripple will be too large compared to the average current. To improve the dimming linearity, please choose a proper inductor value to get smaller inductor current ripple. Basically, a current ripple of 10%~50% of full output current is a good choice for analog dimming.

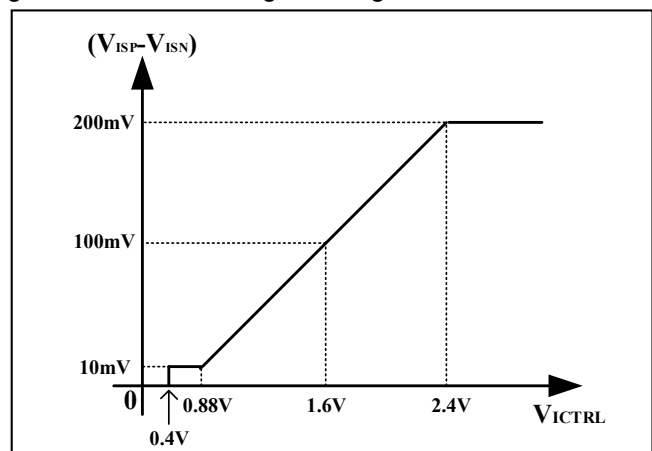


Figure 36 Analog Dimming Graph

Never leave the ICTRL pin floating. If the analog dimming function is not implemented, connect the

IS32LT3965

ICTRL pin either to a voltage level within 2.6V to 6V, or the VDD pin via a resistor (recommended value is 10kΩ).

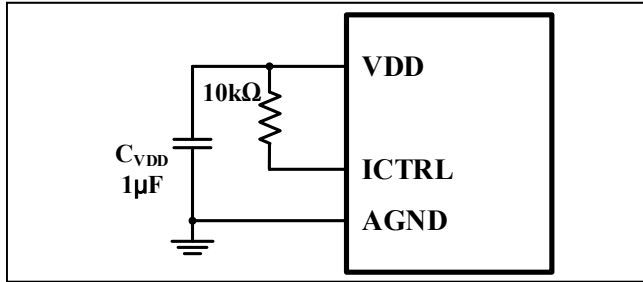


Figure 37 ICTRL Pin Unused

It is recommended to add a 10nF ceramic capacitor from the ICTRL pin to GND to bypass any high frequency noise, especially if the analog voltage level comes from a long copper trace. This 10nF capacitor should be placed as close to the ICTRL pin as possible. The following are some application scenarios for use of the analog dimming function.

LED Binning:

The ICTRL pin can be used to fine tune the output current during mass-production. LEDs are typically sorted into various bins of different luminous intensity and forward voltage. To correct the brightness deviation during mass-production, the mean output current can be adjusted by adjusting the voltage level on the ICTRL pin. As shown in Figure 38, fix the R_{ICTRL1} value and solder different value R_{BIN} resistor to adjust and maintain the same lumen output across different LED bins. This R_{BIN} resistor can be placed on the LED board.

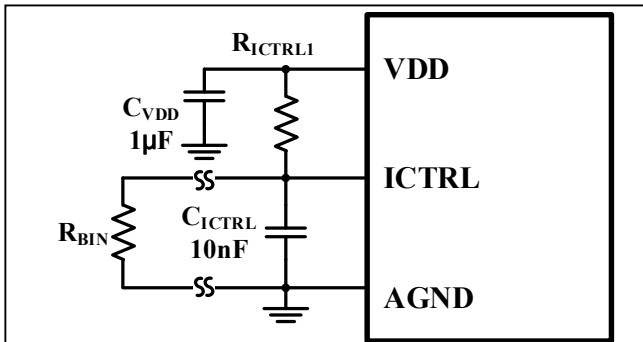


Figure 38 Analog Dimming For LED Binning

Over Temperature Thermal Roll-off:

The ICTRL pin can also be used in conjunction with a NTC thermistor to provide over temperature current roll-off protection for the LED load or the system. As shown in Figure 39.

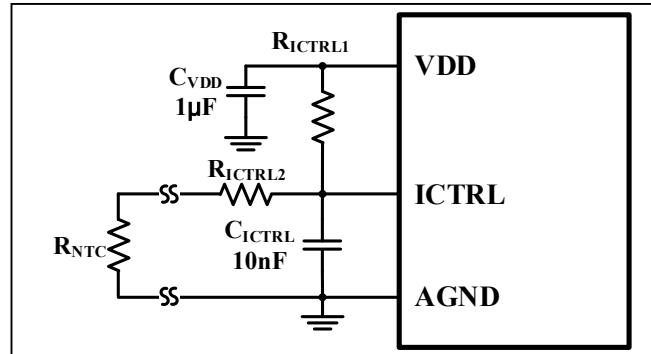


Figure 39 ICTRL Pin with NTC for Thermal Roll-off Protection

For example, assume the desired current roll-off temperature threshold is T_R and the NTC thermistor resistance is R_{NTCR} at this temperature (R_{NTCR} can be found in the NTC thermistor datasheet), then R_{ICTRL1} and R_{ICTRL2} can be calculated by:

$$R_{ICTRL1} = \frac{(R_{NTCR} + R_{ICTRL2}) \times (V_{DD} - 2.4V)}{2.4V} \quad (5)$$

For a given NTC thermistor, the R_{ICTRL1} resistor will adjust the current roll-off temperature threshold. The larger R_{ICTRL1} the lower the current roll-off temperature threshold. The R_{ICTRL2} resistor is optionally used to adjust the current derating slope. The larger the R_{ICTRL2} the flatter the current derating slope. If R_{ICTRL2} is not used, tie the NTC thermistor directly to ICTRL pin.

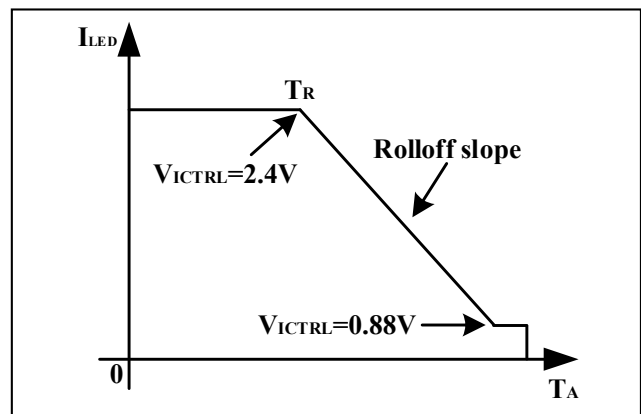


Figure 40 Analog Dimming For Thermal Roll-off Protection

The NTC thermistor should be placed next to the component to be monitored. Such as the LED board, beside the power MOSFET, and so on.

Dual Brightness Level Output:

In automotive applications, some lamps require a dual brightness output. For instance, the daytime running light (DRL) and the position light (POL) can both use the same LED string, since these two lamps won't be active at the same time. The DRL is active in the daytime, while POL is active with lower brightness in the nighttime. Two brightness levels are selected by two independent power supply rails. The analog dimming can be used for this dual brightness output function.

IS32LT3965

As shown in Figure 41. When the input logic to the GATE of the MOSFET Q₁ is high, R_{ICTRL3} resistor is shorted by Q₁. The output current is determined by the resistor divider R_{ICTRL1} and R_{ICTRL2}. If the GATE of the switch Q₁ is pulled low, the output current is determined by the resistor divider R_{ICTRL1}, R_{ICTRL2} and R_{ICTRL3} resulting in a higher brightness.

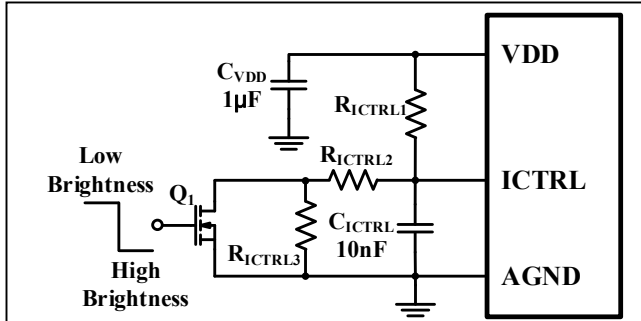


Figure 41 ICTRL Pin for Dual Brightness Output

INPUT CAPACITOR

The input capacitor provides the transient pulse current, which is approximately equal to I_{LED}, to the inductor of the converter when the high-side MOSFET is on. An X7R type ceramic capacitor is a good choice for the input bypass capacitor to handle the ripple current since it has a very low equivalent series resistance (ESR) and low equivalent series inductance (ESL). Use the following equation to estimate the approximate capacitance:

$$C_{VCC_MIN} = \frac{I_{LED} \times t_{ON}}{\Delta V_{CC}} \quad (6)$$

Where, ΔV_{CC} is the acceptable input voltage ripple, generally choose 5%-10% of input voltage. t_{ON} is on-time of the high-side MOSFET in μs. A minimum input capacitance of 2X C_{VCC_MIN} is recommended for most applications.

OUTPUT CAPACITOR

The ISP/ISN pins need a certain amount of voltage ripple to keep control loop stability. A capacitor must be added across the LEDs but excluding the R_{IS} resistor. As shown in Figure 42. This capacitor will reduce the LED current ripple while maintaining the same average current. Meanwhile, this capacitor also helps to reduce the common mode noise on ISP/ISN pins that improves the line regulation accuracy of the output current. The reduction of the LED current ripple by the capacitor depends on several factors: capacitor value, inductor current ripple, operating frequency, output voltage, etc. To support FCCM mode operation, the output capacitor value must be equal or larger than 1μF. A 1μF~2.2μF capacitor is sufficient for most applications. However, the output capacitor brings in more delay time of LED current during PWM dimming that will degrade the dimming contrast. An output capacitor that is too large is not recommended.

The output capacitor is used to filter the LED current ripple to an acceptable level. The equivalent series resistance (ESR), equivalent series inductance (ESL) and capacitance of the capacitor contribute to the output current ripple. Therefore, a low-ESR X7R type capacitor should be used.

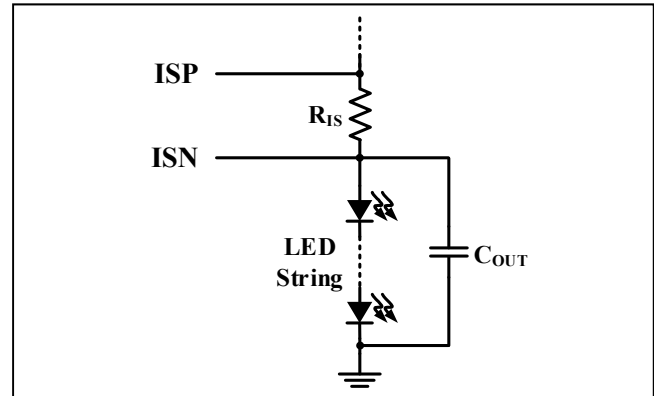


Figure 42 Output Capacitor Excluding R_{IS}

FREQUENCY SELECTION

During switching the IS32LT3965 operates in a constant on-time mode. The on-time is adjusted by the external resistor, R_{TON}, which is connected between the VCC and TON pins.

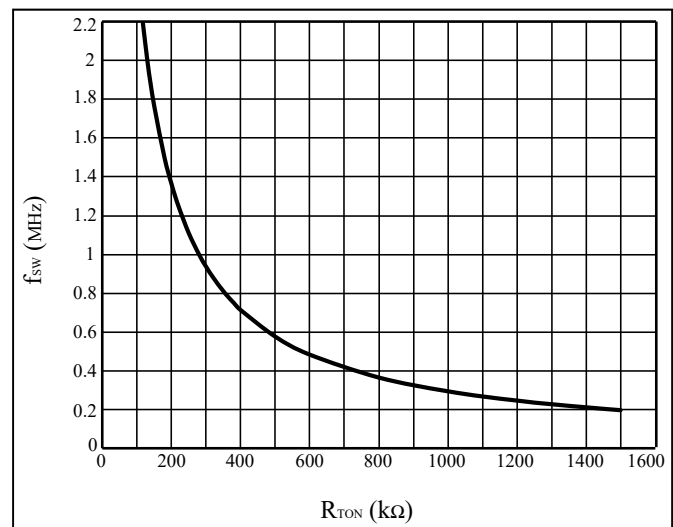


Figure 43 Operating Frequency vs. R_{TON} Resistance

The approximate operating frequency can be calculated by below Equation (7):

$$f_{SW} = \frac{1}{k \times (R_{TON} + R_{INT}) + 0.037} \quad (7)$$

Where k= 0.00333, with f_{SW} in MHz, R_{TON} and R_{INT} (internal resistance = 20kΩ) in kΩ.

Higher frequency operation results in smaller component size but increases the switching losses. It may also increase the high-side MOSFET gate driving current and may not allow sufficient high or low duty cycle. Lower frequency gives better performance but results in larger component size. In automotive applications, an operating frequency of 400kHz or

IS32LT3965

2.2MHz is good choice to compromise for both component size and efficiency while keeping the switching noise out of the sensitive frequency bands to easily pass EMI test.

SPREAD SPECTRUM

A switch mode controller can be troublesome when EMI is concerned. To optimize the EMI performance, the IS32LT3965 includes a spread spectrum feature, which has a 600Hz with $\pm 5\%$ operating frequency jitter. The spread spectrum can spread the total electromagnetic emitting energy onto a wider frequency range to significantly degrade the EMI energy peaks. With spread spectrum, the EMI test can pass with smaller sized and lower cost filter circuit.

MINIMUM AND MAXIMUM OUTPUT VOLTAGE

The output voltage of a buck converter is approximately given as below:

$$V_{OUT} = V_{CC} \times D \quad (8)$$

Where D is the operating duty cycle.

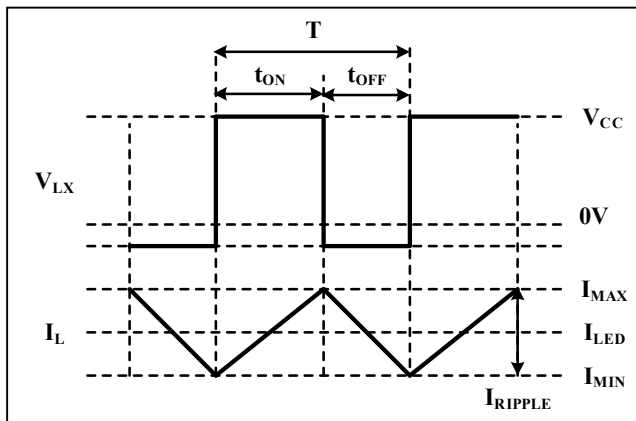


Figure 44 Operating Waveform

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (9)$$

So,

$$V_{OUT} = V_{CC} \times \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{CC} \times t_{ON} \times f_{SW} \quad (10)$$

Where t_{ON} and t_{OFF} are the turn-on and turn-off time of high-side MOSFET. Note that due to the spread spectrum function, f_{SW} should be increased by 5% ($105\% \times f_{SW}$) to account for the maximum of operating frequency.

According to above equation, the output voltage depends on the operating frequency and the high-side MOSFET turn-on time. When the frequency is set, the maximum output voltage is limited by the switching minimum off-time t_{OFF_MIN} , about 90ns. For example, if the input voltage is 12V and the operating frequency $f_{SW}=1\text{MHz}$, the maximum output voltage is:

$$V_{OUT} = 12V \times (0.952\mu s - 90ns) \times 1.05\text{MHz} = 10.86V \quad (11)$$

Assume the forward voltage of each LED is 3.2V, the device can drive up to 3 LEDs in series.

The minimum output voltage is limited by the switching minimum on-time t_{ON_MIN} , about 80ns, once the frequency is set. For example, if the input voltage is 12V and the operating frequency $f_{SW}=1\text{MHz}$, the minimum output voltage is:

$$V_{OUT} = 12V \times 80ns \times 1.05\text{MHz} = 1.008V \quad (12)$$

This means the device can drive a low forward voltage LED, such as a RED color LED. So under the condition of $V_{CC}=12V$ and $f_{SW}=1\text{MHz}$, the output voltage range is about 1.008V~10.86V. Exceeding this range, the operation will be clamped and the output current cannot reach the set value.

In a typical application, the output voltage is affected by other operating parameters, such as output current, $R_{DS(ON)}$ of the high-side and low-side MOSFETs, DRC of the inductor, parasitic resistance of the PCB traces, and the forward voltage of the diode. Therefore, the output voltage range could vary from the calculation. The more precision equation is given by:

$$V_{OUT} = (V_{CC} - I_{LED} \times R_{DS(ON_HS)}) \times D - R_L \times I_{LED} - (I_{LED} \times R_{DS(ON_LS)}) \times (1 - D) \quad (13)$$

Where, $R_{DS(ON_HS)}$ is the static drain-source on resistance of the high-side MOSFET, $R_{DS(ON_LS)}$ is the static drain-source on resistance of the low-side MOSFET, and R_L is the inductor DC resistance.

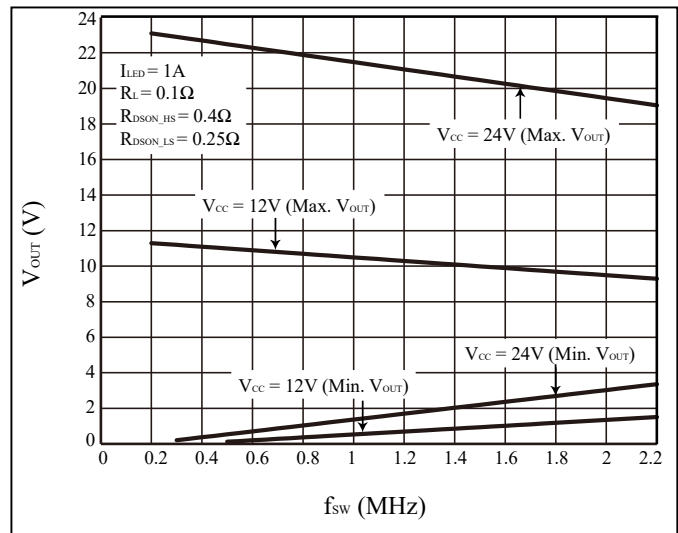


Figure 45 Minimum and Maximum Output Voltage versus Operating Frequency (minimum $t_{ON}=80\text{ns}$ and minimum $t_{OFF}=90\text{ns}$)

IS32LT3965

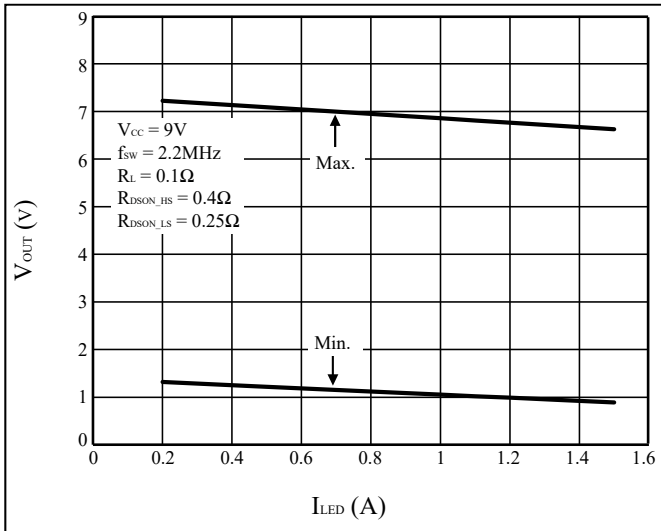


Figure 46 Minimum and Maximum Output Voltage versus LED Current (minimum $t_{ON}=80ns$ and minimum $t_{OFF}=90ns$)

Figure 45 shows how the minimum and maximum output voltages vary with the operating frequency at 12V and 24V input. Figure 46 shows how the minimum and maximum output voltages vary with the LED current at 9V input (assuming $R_{DS(on)_{HS}}=0.4\Omega$, $R_{DS(on)_{LS}}=0.25\Omega$ and inductor DCR $R_L=0.1\Omega$). Note that due to spread spectrum the f_{SW} should use the maximum operating frequency, $105\% \times f_{SW}$.

When the output voltage is lower than the minimum t_{ON} time of the device, the device will automatically extend the operating t_{OFF} time to maintain the set output LED current at all times. However, the operating frequency will decrease accordingly to a lower level to keep the duty cycle in correct regulation.

To achieve wider output voltage range and flexible output configuration, a lower operating frequency should be considered.

HIGH-SIDE MOSFET PEAK CURRENT LIMIT

To protect itself, the IS32LT3965 integrates an Over Current Protection (OCP) detection circuit to monitor the current through the high-side MOSFET during switch on. Whenever the current exceeds the OCP current threshold, I_{HSLIM} , the device will immediately turn off the high-side MOSFET for t_{OCP} and restart again. The device will remain in this hiccup mode until the current drops below I_{HSLIM} .

FCCM OPERATION

The IS32LT3965 uses Forced Continuous Conduction Mode (FCCM) to ensure the device always operates with fixed frequency from a light-load to full-load range (such as analog dimming application). The advantage of FCCM is the controllable frequency and low output current ripple at light-load.

INDUCTOR

Inductor value involves trade-offs in performance. A larger inductance reduces inductor current ripple;

however, it also brings in unwanted parasitic resistance that degrades efficiency. A smaller inductance has compact size and lower cost but introduces higher ripple in the LED string. Use the following equation to estimate the approximate inductor value:

$$L = \frac{(V_{CC} - V_{LED}) \times V_{LED}}{f_{SW} \times \Delta I_L \times V_{CC}} \quad (14)$$

Where V_{CC} is the minimum input voltage in volts, V_{LED} is the total forward voltage of LED string in volts, f_{SW} is the operation frequency in hertz and ΔI_L is the current ripple in the inductor. Select an inductor with a rated current greater than the output average current and the saturation current over the Over Current Protection (OCP) current threshold I_{HSLIM} .

Since the IS32LT3965 is a Continuous Conduction Mode (CCM) buck driver the ΔI_L must be smaller than 200% of the average output current.

$$\Delta I_L < 2 \times I_{LED} \quad (15)$$

Besides, the peak current of the inductor, I_{L_PK} , must be smaller than I_{HSLIM} to prevent the IS32LT3965 from triggering OCP, especially when the output current is set to a high level.

$$I_{L_PK} = I_{LED} + \frac{\Delta I_L}{2} < I_{HSLIM} \quad (16)$$

To ensure system stability, the ΔI_L must be higher than 10% of the average output current. The limit on the highest current ripple percentage allowed is 200%. However, to get better current accuracy and analog dimming performance, it is recommended to choose an inductor current ripple ΔI_L between 10% and 50% of the average output current.

$$0.1 \times I_{LED} \leq \Delta I_L \leq 0.5 \times I_{LED} \quad (17)$$

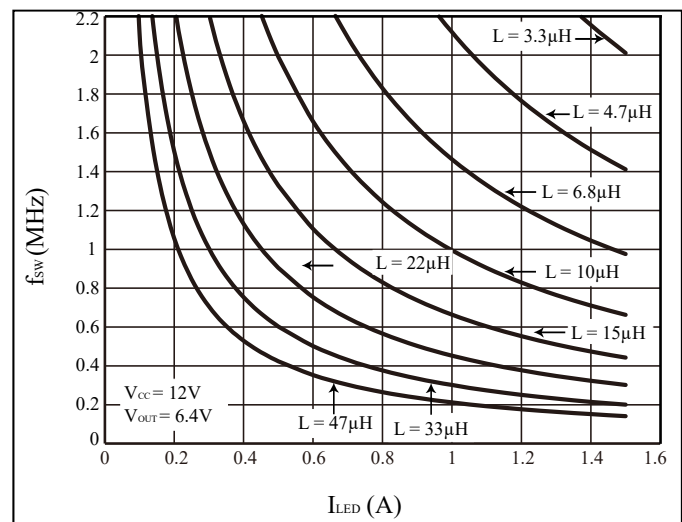


Figure 47 Inductance Selection Based On 30% Current Ripple

Figure 47 shows inductor selection based on the operating frequency and LED current at 30% inductor

IS32LT3965

current ripple. If a lower operating frequency is used, either a larger inductance or current ripple should be used.

FAULT HANDLING

The IS32LT3965 is designed to detect the following faults and report via open drain FAULTB pin:

- Pin open
- Pin-to-ground short
- Output LED string open and short
- External component open or short
- Thermal shutdown

Please check Table 2 for the details of the fault actions.

The FAULTB pin is an open drain structure. If the device detects a fault condition, the FAULTB pin will go low to report the fault condition, which can be monitored by an external host. The FAULTB pin supports both input and output functions. Externally pulling FAULTB pin low will disable the device. For lighting systems with multiple IS32LT3965 drivers that requires the complete lighting system to shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the “one fail all fail” operating requirement.

Note that this pin requires an external pull up resistor (R_{FPU}) for normal operation. Do not allow to float. The recommended R_{FPU} value is 10k Ω .

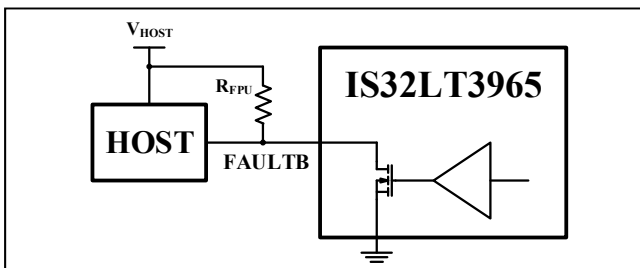


Figure 48 Host Monitors The Fault Reporting

THERMAL SHUTDOWN PROTECTION

To protect the IC from damage due to high power dissipation, the temperature of the die is monitored. If the die temperature exceeds the thermal shutdown temperature of 170°C (Typ.) then the device will shut down, and the output current is shut off and FAULTB pin pulls low. After a thermal shutdown event, the IS32LT3965 will not try to restart until its temperature has reduced to less than 150°C (Typ.). The FAULTB pin will recover once the IC restarts.

THERMAL ROLL-OFF PROTECTION

The device integrates the thermal shutdown protection to prevent the device from overheating. In addition, to prevent the LEDs from flickering due to rapid thermal changes, the device also includes a thermal roll-off feature to reduce power dissipation at high junction temperature.

The output current will be equal to the set value I_{LED} as long as the junction temperature of the IC remains below thermal roll-off temperature threshold T_{RO} . If the junction temperature exceeds the threshold, the output current begins to reduce at a rate of about typical 2% of I_{LED} per °C following the junction temperature ramping up until thermal shutdown protection. Thermal roll-off protection won't be reported by the fault reporting pin.

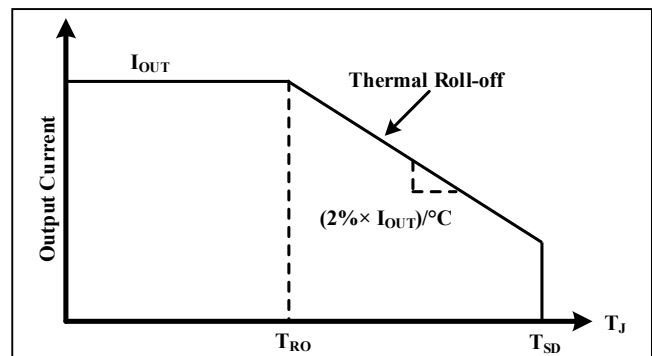


Figure 49 Thermal Roll-off

IS32LT3965

Table 2 Fault Actions

Fault Type	LED String	Detect Condition		FAULTB Pin		Fault Recovering
Inductor short	Dim	Trigger OCP. Turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low immediately		Inductor short removed. No OCP triggered and FAULTB pin recover after 10ms.
R _{IS} short	Dim	Trigger OCP. Turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low immediately		R _{IS} short removed. No OCP triggered and FAULTB pin recover after 10ms.
R _{IS} open	Off	Detect high differential sense voltage. Turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low after 20us deglitch time.		R _{IS} open removed. FAULTB pin recover after 10ms.
LED string open	Off	No PWM dimming:	Low R _{IS} voltage trigger EAO (Error Amplifier Output) high-clamp for 10ms.	No PWM dimming:	Pull Low after 10ms.	LED open removed. FAULTB pin recover after 10ms.
		PWM dimming:	Low R _{IS} voltage trigger EAO (Error Amplifier Output) high-clamp after 20us deglitch time and keeps for 16 PWM cycles.	PWM dimming:	Pull low after 16 PWM cycles.	
LED string short	Off	No PWM dimming:	Filter V _{LX} to get V _{OUT} , if V _{OUT} <1.45V for 10ms	No PWM dimming:	Pull Low after 10ms.	Short removed. V _{OUT} >1.65V for 10ms and FAULTB pin recover after 10ms.
		PWM dimming:	Filter V _{LX} to get V _{OUT} , if V _{OUT} <1.45V after 20μs deglitch time and keeps for 16 PWM cycles.	PWM dimming:	Pull low after 16 PWM cycles.	
BOOT capacitor open	Dim	V _{CC} -V _{LX} >2V at high-side MOSFET ON (High-side can't fully turn on). Turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low immediately		BOOT capacitor open removed, V _{CC} -V _{LX} <2V for 10ms and FAULTB pin recover.
BOOT capacitor short	Off	Bootstrap circuit UVLO and turn off high-side MOSFET immediately.		No PWM dimming:	Pull Low after 10ms.	BOOT capacitor short removed. Release from UVLO and FAULTB pin recover after 10ms
				PWM dimming:	Pull low after 16 PWM cycles.	
R _{TON} resistor open	Dim	On-time exceeds 20μs or trigger OCP, then turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low immediately		R _{TON} resistor open removed. No over 20us on-time or OCP triggered. FAULTB pin recover after 10ms
R _{TON} resistor short	Dim	The device operating at minimum on/off time, maybe trigger the other fault conditions.		No reporting		R _{TON} resistor short removed.
V _{OUT} /ISP short to GND	Off	Trigger OCP. Turn off high-side MOSFET immediately. Retry after 10ms.		Pull Low immediately		Short removed. FAULTB pin recover after 10ms.
Thermal Shutdown	Off	The die temperature exceeds 170°C		Pull Low immediately		The die temperature cools down below 150°C. FAULTB pin recovers after 10ms.

LAYOUT CONSIDERATIONS

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the operation could show instability as well as EMI problems.

The high dV/dt surface and dI/dt loops are big noise emission source. To optimize the EMI performance, keep the area size of all high switching frequency points with high voltage compact. Meantime, keep all traces carrying high current as short as possible to minimize the loops.

- (1) Wide traces should be used for connection of the high current paths that helps to achieve better efficiency and EMI performance. Such as the traces of power supply, inductor L₁, current sense

resistor R_{IS}, LED load and ground.

- (2) Keep the traces of the switching points shorter. The inductor L₁ should be placed as close to LX pin as possible and the traces of connection between them should be as short and wide as possible.
- (3) To avoid ground jitter, the components of parameter setting should be placed close to the corresponding pins and return to the AGND pin and keep the traces length to the pins as short as possible. On the other side, to prevent the noise coupling, the traces of R_{IS} should either be far away or be isolated from high-current paths and high-speed switching nodes. These practices are essential for better accuracy and stability.
- (4) The capacitors C_{IN} and C_{VDD} must be placed as

IS32LT3965

close as possible to VCC and VDD pins for good filtering.

- (5) Place the bootstrap capacitor C_{BOOT} close to BOOT pin and LX pin to ensure the traces are as short as possible.
- (6) The connection to the LED string should be kept short to minimize radiated emission. An output capacitor C_{OUT} is recommended to be used and placed on driver board to reduce the current ripple in the connecting cables.
- (7) In practice, if the LED string is far away from the driver board and connected through long cables, the parasitic inductance in the cables will form a LC-resonant circuit with the C_{OUT} . In the case of hot plugging the output connector or an unreliable connector, this LC-resonant circuit will create oscillation on ISN and ISP pins due to the C_{OUT} fast discharging. This oscillation could subject the ISN and ISP pins to negative spike voltage exceeding their Absolute Maximum Ratings that may permanently damage the ISN and ISP pins. To avoid the negative spike voltage, please consider adding a Schottky diode D_P in parallel with the C_{OUT} . Recommend a 40V/1A Schottky diode for D_P .

Note that hot plugging the output connector is a non-standard operation. Please avoid it during mass-production. And the connecting reliability of the output connector must be ensured as well.

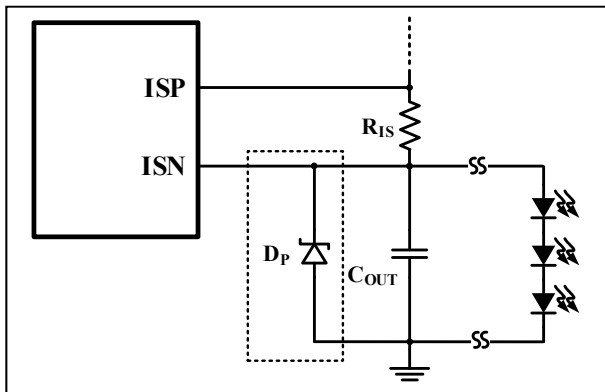


Figure 50 Schottky Diode for ISN/ISP Protection

- (8) The LX, VCC and PGND pins of device package must be soldered to a sufficient size of copper ground plane with sufficient vias to conduct the heat to opposite side of the PCB for adequate cooling.

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA} , determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt ($^{\circ}C/W$).

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (18):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (18)$$

Where $T_{J(MAX)}$ is the recommended maximum operating junction temperature.

So,

$$P_{D(MAX)} = \frac{150^{\circ}C - 25^{\circ}C}{53.7^{\circ}C/W} \approx 2.33W$$

Figure 51, shows the power derating of the IS32LT3965 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

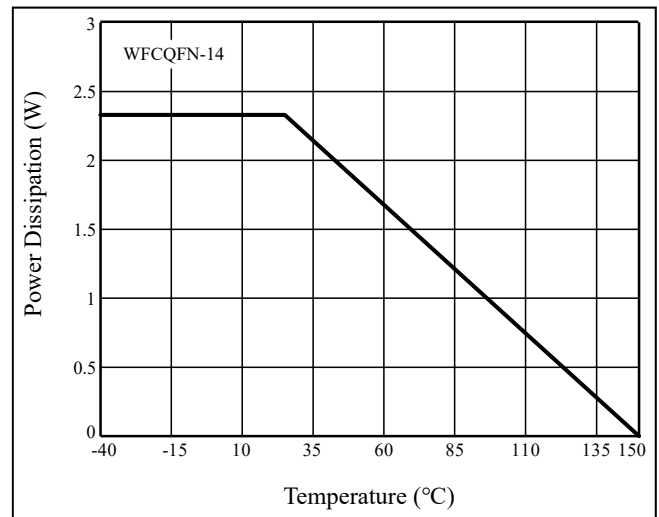


Figure 51 Dissipation Curve

The thermal resistance is achieved by mounting the IS32LT3965 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3965. The thermal resistance can be reduced by using a four-layer PCB board. A four-layer layout is strongly recommended to achieve better thermal and EMI performance.

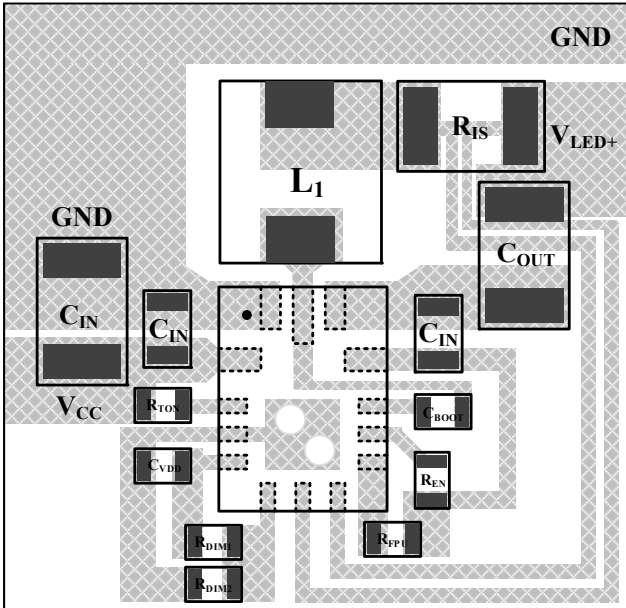


Figure 52 PCB Layout Example (Top Layer)

IS32LT3965

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

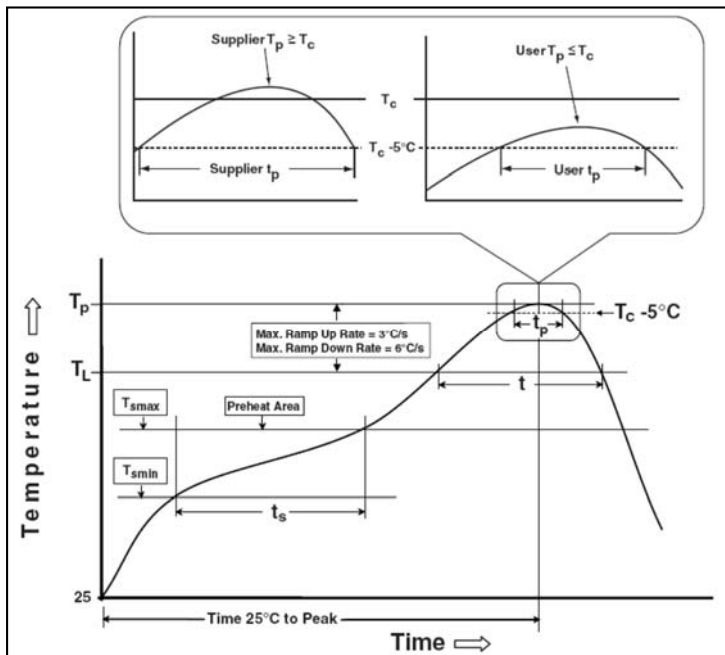
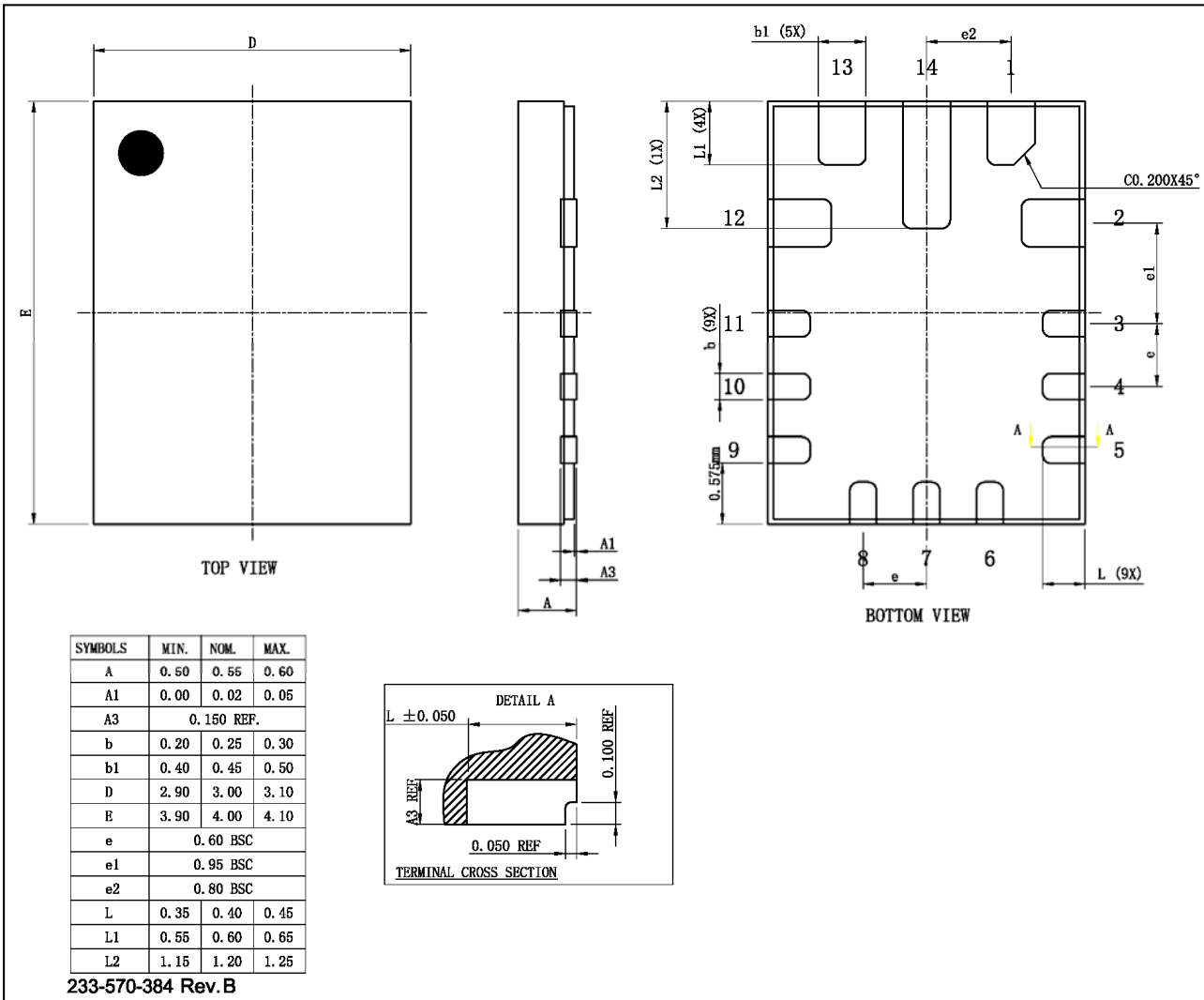


Figure 53 Classification Profile

IS32LT3965

PACKAGE INFORMATION

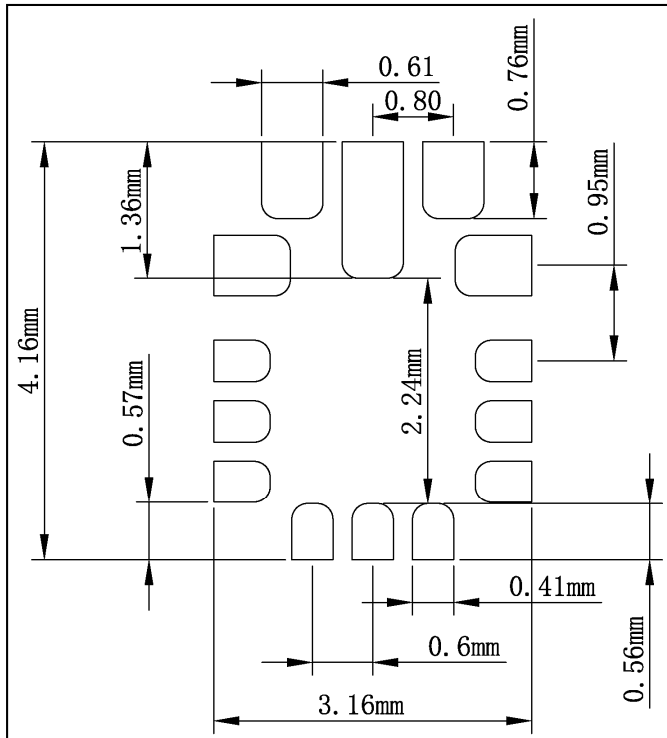
WFCQFN-14



IS32LT3965

RECOMMENDED LAND PATTERN

WFCQFN-14



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.