IS43/46LD16160B
IS43/46LD32800B

256Mb (x16, x32) Mobile LPDDR2 S4 SDRAM

PRELIMINARY INFORMATION
MARCH 2018

FEATURES

- Low-voltage Core and I/O Power Supplies VDD2 = 1.14-1.30V, VDDCA/VDDQ = 1.14-1.30V, VDD1 = 1.70-1.95V
- High Speed Un-terminated Logic(HSUL_12) I/O Interface
- Clock Frequency Range : 10MHz to 533MHz (data rate range : 20Mbps to 1066Mbps per I/O)
- Four-bit Pre-fetch DDR Architecture
- Multiplexed, double data rate, command/address inputs
- Four internal banks for concurrent operation
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable Read/Write latencies(RL/WL) and burst lengths(4,8 or 16)
- ZQ Calibration
- On-chip temperature sensor to control self refresh rate
- Partial –array self refresh(PASR)
- Deep power-down mode(DPD)
- Operation Temperature
  Commercial (T_C = 0°C to 85°C)
  Industrial (T_C = -40°C to 85°C)
  Automotive, A1 (T_C = -40°C to 85°C)
  Automotive, A2 (T_C = -40°C to 105°C)

OPTIONS

- Configuration:
  – 16Mx16 (4M x 16 x 4 banks)
  – 8Mx32 (2M x 32 x 4 banks)
  Package:
  – 134-ball BGA for x16 / x32
  – 168-ball PoP BGA for x32

DESCRIPTION

The IS43/46LD16160B/32800B is 256Mbit CMOS LPDDR2 DRAM. The device is organized as 4 banks of 4Meg words of 16bits or 2Meg words of 32bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4N prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 4n bits prefetched to achieve very high bandwidth.

ADDRESS TABLE

Parameter	8Mx32	16Mx16
Row Addresses	R0-R12	R0-R12
Column Addresses	C0-C7	C0-C8
Bank Addresses	BA0-BA1	BA0-BA1
Refresh Count	4096	4096

KEY TIMING PARAMETERS(1)

Speed Grade	Data Rate (Mb/s)	Write Latency	Read Latency	tRCD/ tRP(2)
-18	1066	4	8	Typical
-25	800	3	6	Typical
-3	667	2	5	Typical

Notes:
1. Other clock frequencies/data rates supported; please refer to AC timing tables.
2. Please contact ISSI for Fast t_{RCD}/t_{RP}.

BALL ASSIGNMENTS AND DESCRIPTIONS

134-ball FBGA (x32), 0.65mm pitch

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		VDD2	VDD1	DQ31	DQ29	DQ26	DNU	B
C	VDD1	VSS	RFU		VSS	VSSQ	VDDQ	DQ25	VSSQ	VDDQ	C
D	VSS	VDD2	ZQ		VDDQ	DQ30	DQ27	DQS3	DQS3#	VSSQ	D
E	VSSCA	CA9	CA8		DQ28	DQ24	DM3	DQ15	VDDQ	VSSQ	E
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ	F
G	VDD2	CA5	Vref(CA)		DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ	G
H	VDDCA	VSS	CK#		DM1	VDDQ					H
J	VSSCA	NC	CK		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)		J
K	CKE	RFU	RFU		DM0	VDDQ					K
L	CS#	RFU	RFU		DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ	L
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ	M
N	VSSCA	VDDCA	CA1		DQ19	DQ23	DM2	DQ0	VDDQ	VSSQ	N
P	VSS	VDD2	CA0		VDDQ	DQ17	DQ20	DQS2	DQS2#	VSSQ	P
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	DQ22	VSSQ	VDDQ	R
T	DNU	NC	NC		VDD2	VDD1	DQ16	DQ18	DQ21	DNU	T
U	DNU	DNU							DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	

DQ
CA
Power
Ground
No ball
ZQ
Clock
NC, DNU, RFU

Top View (ball down)

BALL ASSIGNMENTS AND DESCRIPTIONS

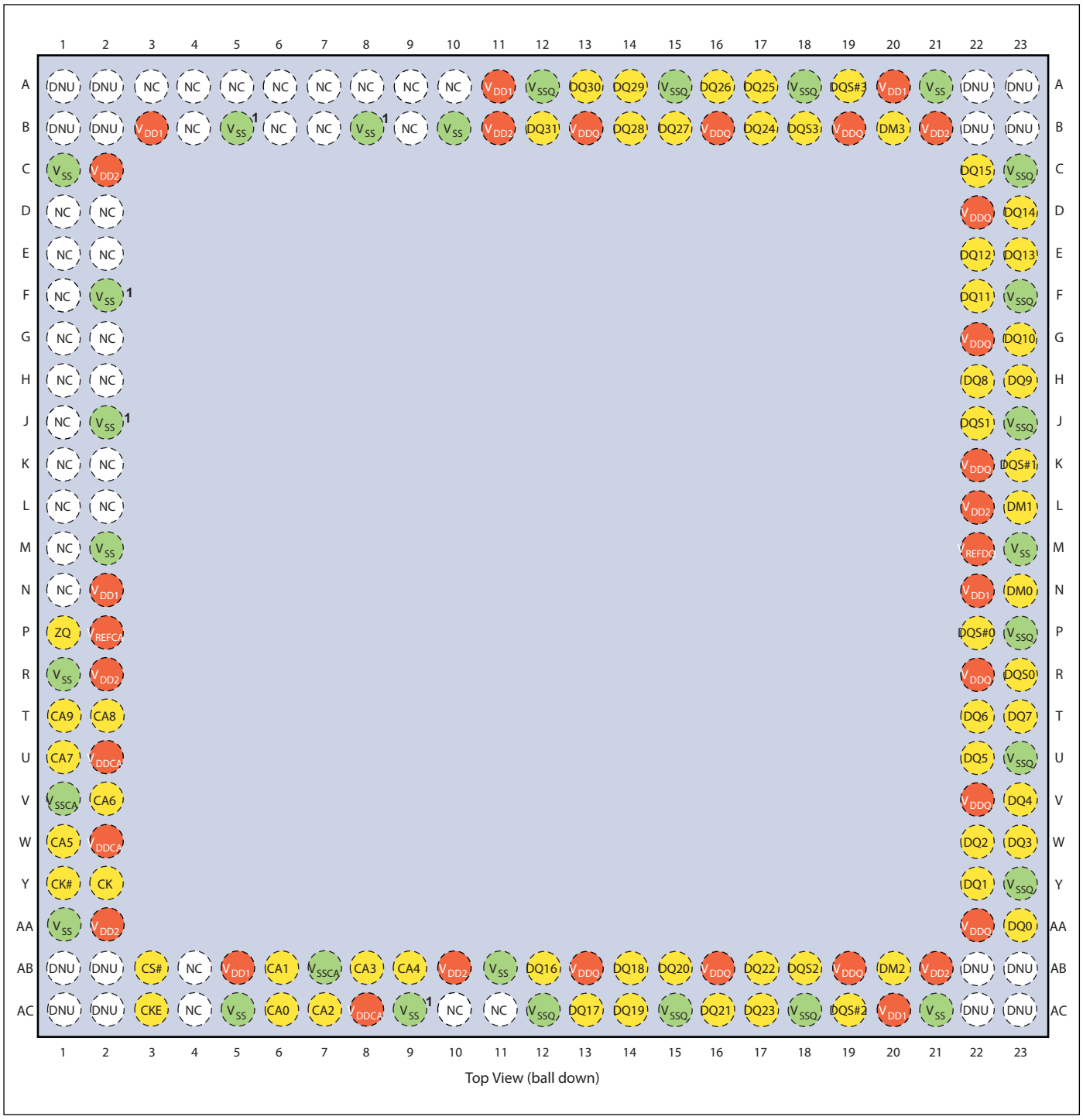
134-ball FBGA (x16), 0.65mm pitch

	1	2	3	4	5	6	7	8	9	10
A	DNU	DNU							DNU	DNU
B	DNU	NC	NC		VDD2	VDD1	NC	NC	NC	DNU
C	VDD1	VSS	RFU		VSS	VSSQ	VDDQ	NC	VSSQ	VDDQ
D	VSS	VDD2	ZQ		VDDQ	NC	NC	NC	NC	VSSQ
E	VSSCA	CA9	CA8		NC	NC	NC	DQ15	VDDQ	VSSQ
F	VDDCA	CA6	CA7		VSSQ	DQ11	DQ13	DQ14	DQ12	VDDQ
G	VDD2	CA5	Vref(CA)		DQS1#	DQS1	DQ10	DQ9	DQ8	VSSQ
H	VDDCA	VSS	CK#		DM1	VDDQ				
J	VSSCA	NC	CK		VSSQ	VDDQ	VDD2	VSS	Vref(DQ)	
K	CKE	RFU	RFU		DM0	VDDQ				
L	CS#	RFU	RFU		DQS0#	DQS0	DQ5	DQ6	DQ7	VSSQ
M	CA4	CA3	CA2		VSSQ	DQ4	DQ2	DQ1	DQ3	VDDQ
N	VSSCA	VDDCA	CA1		NC	NC	NC	DQ0	VDDQ	VSSQ
P	VSS	VDD2	CA0		VDDQ	NC	NC	NC	NC	VSSQ
R	VDD1	VSS	NC		VSS	VSSQ	VDDQ	NC	VSSQ	VDDQ
T	DNU	NC	NC		VDD2	VDD1	NC	NC	NC	DNU
U	DNU	DNU							DNU	DNU

DQ
CA
Power
Ground
No ball
ZQ
Clock
NC, DNU, RFU

Top View (ball down)

168-ball FBGA - 12mm x 12mm (x32), 0.5mm pitch



Note:
1. Balls labeled Vss[1] (at coordinates B5, B8, F2, J2, AC9) may be connected to Vss or left unconnected.
2. Balls indicated as (NC) are no connects.

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

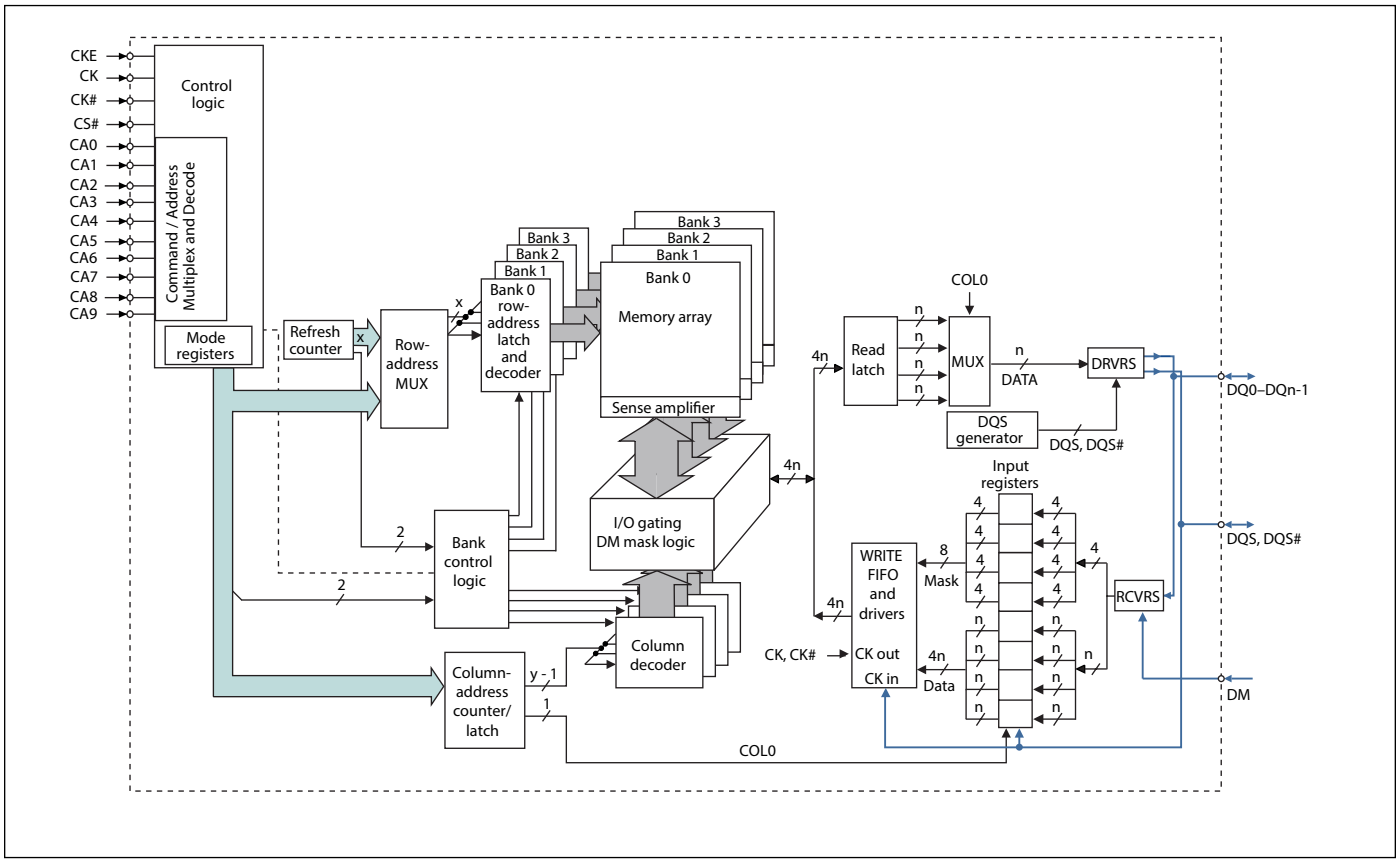
Pad Definition and Description

Name	Type	Description
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, CS# and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK and CK#. The positive Clock edge is defined by the crosspoint of a rising CK and a falling CK#. The negative Clock edge is defined by the crosspoint of a falling CK and a rising CK#.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS#	Input	Chip Select: CS# is considered part of the command code. See Command Truth Table for command code descriptions. CS# is sampled at the positive Clock edge.
CA0 - CA9	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	Data Inputs/Output: Bi-directional data bus
DQS0, DQS0#, DQS1, DQS1# (x16) DQS0 - DQS3, DQS0# - DQS3# (x32)	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. For x16, DQS0 and DQS0# correspond to the data on DQ0 - DQ7; DQS1 and DQS1# to the data on DQ8 - DQ15. For x32 DQS0 and DQS0# correspond to the data on DQ0 - DQ7, DQS1 and DQS1# to the data on DQ8 - DQ15, DQS2 and DQS2# to the data on DQ16 - DQ23, DQS3 and DQS3# to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	Input Data Mask: For LPDDR2 devices that do not support the DNV feature, DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS#). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.

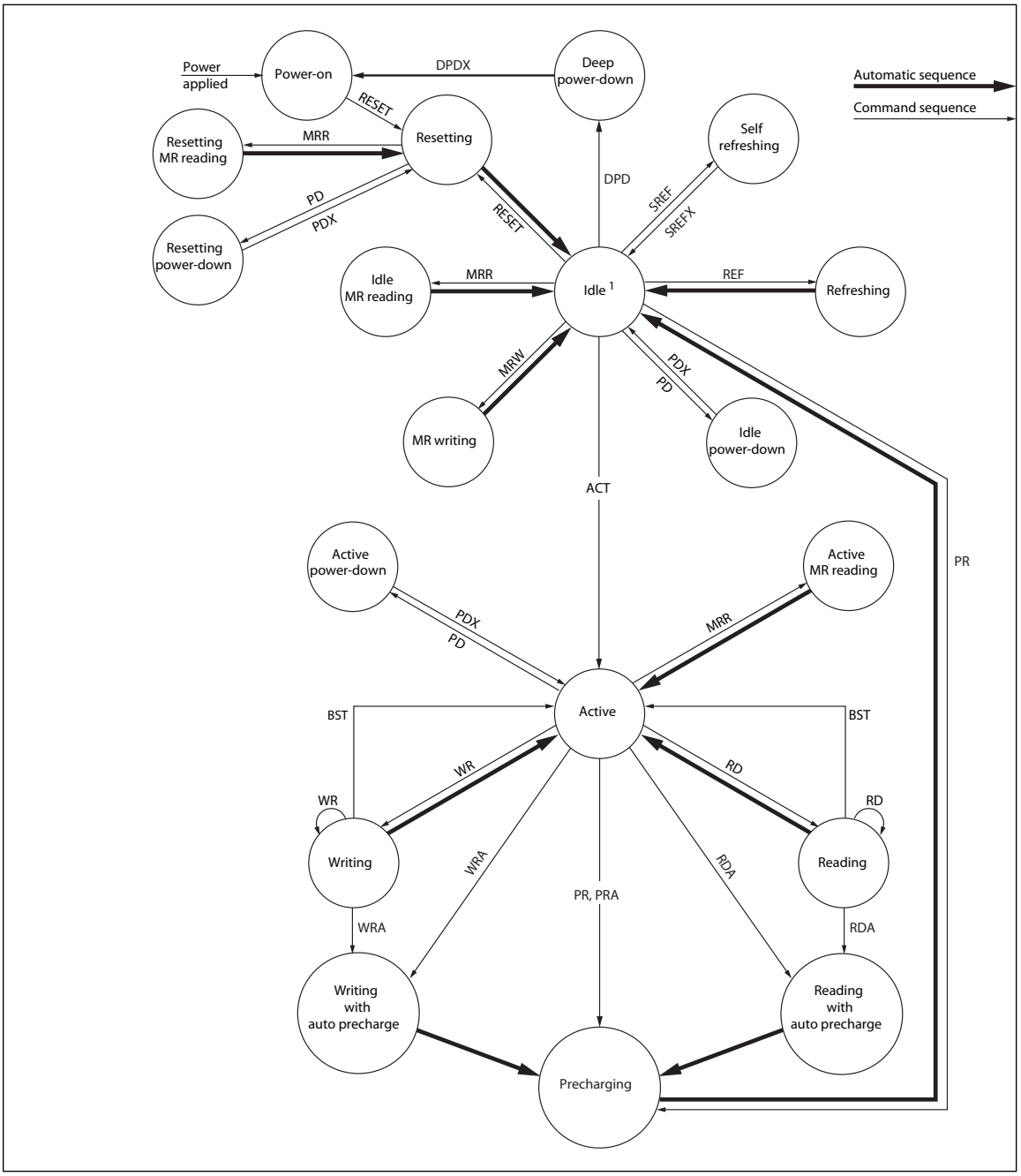
Name	Type	Description
V_{DD1}	Supply	Core Power Supply 1
V_{DD2}	Supply	Core Power Supply 2
V_{DDCA}	Supply	Input Receiver Power Supply: Power supply for CA0-9, CKE, CS#, CK, and CK# input buffers.
V_{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA0-9, CKE, CS#, CK, and CK# input buffers.
$V_{REF(DQ)}$	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all Data input buffers.
V_{SS}	Supply	Ground
V_{SSCA}	Supply	Ground for Input Receivers
V_{SSQ}	Supply	I/O Ground
ZQ	I/O	Reference Pin for Output Drive Strength Calibration

NOTE 1 Data includes DQ and DM.

FUNCTIONAL BLOCK DIAGRAM



SIMPLIFIED STATE DIAGRAM



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	PD	Enter Power Down	REF	Refresh
RD(A)	Read (w/ Autopre-charge)	PDX	Exit Power Down	SREF	Enter self refresh
WR(A)	Write (w/ Autopre-charge)	DPD	Enter Deep Power Down	SREFX	Exit self refresh
PR(A)	Precharge (All)	DPDX	Exit Deep Power Down		
MRW	Mode Register Write	BST	Burst Terminate		
MRR	Mode Register Read	RESET	Reset is achieved through MRW command		

Note: For LPDDR2-S4 SDRAM in the idle state, all banks are precharged.

FUNCTIONAL DESCRIPTION

LPDDR2-S4 is a high-speed SDRAM device internally configured as an 4-Bank memory. This device contains 268,435,456 bits (256 Megabit)

All LPDDR2 devices use a double data rate archiecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

This LPDDR2-S4 device also uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the memory device effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

POWER-UP AND INITIALIZATION

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for Power-up and Initialization.

1. Voltage ramp up sequence is required :

A. While applying power, attempt to maintain CKE below 0.2 x VDDCA and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. The voltage ramp time tINIT0 (Tb-Ta) must be no greater than 20 ms from Tb which is point for all supply and reference voltage are within their defined operating ranges , to Ta which is point for any power supply first reaches 300mV.

B. The following conditions apply for voltage ramp after Ta is reached,
− VDD1 must be greater than VDD2-200mV AND
− VDD1 and VDD2 must be greater than VDDCA-200mV AND
− VDD1 and VDD2 must be greater than VDDQ-200mV AND
− VREF must always be less than all other supply voltages
− The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV

2. Start clock and maintain stable condition.

Beginning at Tb, CKE must remain LOW for at least tINIT1 = 100 ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 × tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

Once the ramping of the supply voltages is complete (Tb), CKE must be maintained LOW. DQ, DM, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up

If any Mode Register Read (MRRs) are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). Mode Register Write (MRWs) can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters could have relaxed timings before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 = 200µs (Td).

3. RESET Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td).
An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands

4. Mode Register Reads and Device Auto Initialization (DAI) Polling:

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications.
Use the MRR command to poll the DAI bit and report when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set before proceeding.
As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured. After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding

5. ZQ Calibration

After tINIT5 (Tf), the MRR initialization calibration (ZQ_CAL) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR2 device exists on the same bus, the controller must not overlap MRR ZQ_CAL commands. The device is ready for normal operation after tZQINIT.

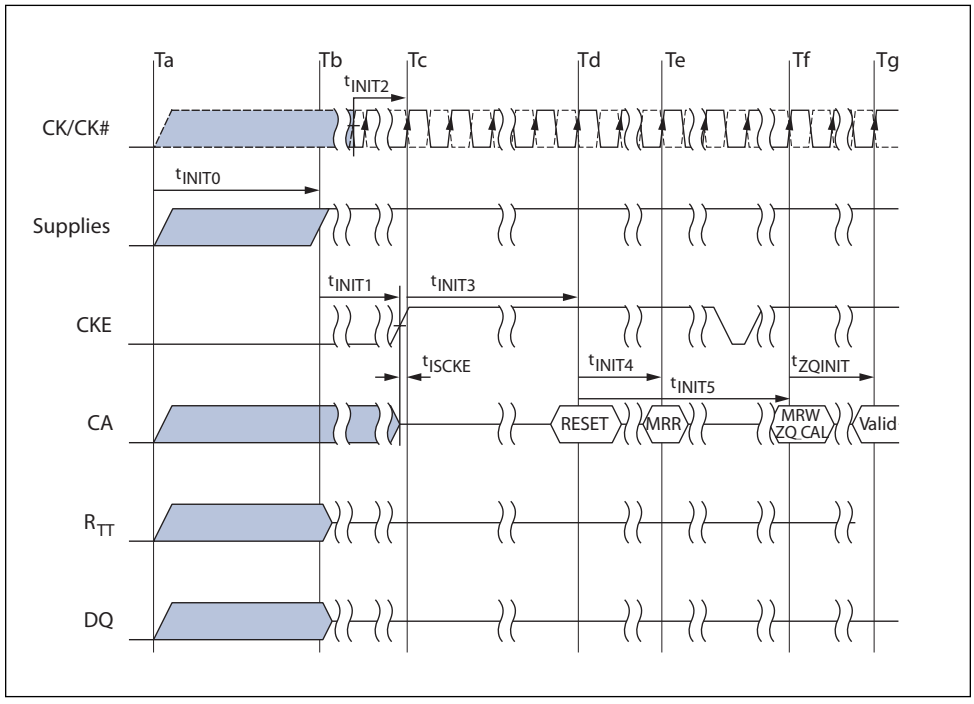
6. Normal Operation

After tZQINIT (Tg), MRW commands must be used to properly configure the memory . Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration
After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop Eventsll.

INITIALIZATION TIMING

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Power Ramp Time	-	20	ms
tINIT1	Minimum CKE low time after completion of power ramp	100	-	ns
tINIT2	Minimum stable clock before first CKE high	5	-	tCK
tINIT3	Minimum idle time after first CKE assertion	200	-	us
tINIT4	Minimum idle time after Reset command, this time will be about 2 x tRFCab + tRPab	1	-	us
tINIT5	Maximum duration of Device Auto-Initialization	-	10	us
tCKb	Clock cycle time during boot	18	100	ns
tZQINIT	ZQ initial calibration	1	-	us

Figure - Power Ramp and Initialization Sequence



Initialization After RESET (without voltage ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td

Power-Off Sequence

Use the following sequence to power off the device. Unless specified otherwise, this procedure is mandatory and applies to S4 devices.

While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off

Required Power Supply Conditions Between Tx and Tz:

• VDD1 must be greater than VDD2 - 200mV

• VDD1 must be greater than VDDCA - 200mV

• VDD1 must be greater than VDDQ - 200mV

• VREF must always be less than all other supply voltages

The voltage difference between VSS, VSSQ, and VSSCA must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

1.At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

2.After Tz , the device must power off. The time between Tx and Tz must not exceed 20ms. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignment

The MRR command is used to read from a register. The MRW command is used to write to a register.

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI
1	01_H	Device Feature1	W	nWR (for AP)			WC	BT	BL		
2	02_H	Device Feature2	W	(RFU)					RL & WL		
3	03_H	I/O Config-1	W	(RFU)					DS		
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11~15	$0B_H$~$0F_H$	(reserved)		(RFU)							

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
16	10_H	PASR_BANK	W	Bank Mask							
17	11_H	(Reserved)		(RFU)							
18-19	12_H-13_H	(Reserved)		(RFU)							

Mode Register Assignment

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
20-31	18_H-$1F_H$	Reserved									

Mode Register Assignment (Reset Command & RFU part)

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
32	20_H	DQ calibration pattern A	R	See "Data Calibration Pattern Description"							
33-39	21_H-27_H	(Do Not Use)									
40	28_H	DQ calibration pattern B	R	See "Data Calibration Pattern Description"							
41-47	29_H-$2F_H$	(Do Not Use)									
48-62	30_H-$3E_H$	(Reserved)		(RFU)							
63	$3F_H$	Reset	W	X							
64-126	40_H-$7E_H$	(Reserved)		(RFU)							
127	$7F_H$	(Do Not Use)									
128-190	80_H-BE_H	(Reserved for Vendor Use)		(RFU)							
191	BF_H	(Do Not Use)									
192-254	$C0_H$-FE_H	(Reserved for Vendor Use)		(RFU)							
255	FF_H	(Do Not Use)									

Notes:
1. RFU bits shall be set to '0' during Mode Register writes.
2.RFU bits shall be read as '0' during Mode Register reads.
3.All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4.All Mode Registers that are specified as RFU shall not be written.
5.See Vendor Device Datasheets for details on Vendor Specific Mode Registers.
6.Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)			RZQI		(RFU)	DI	DAI	
OP <4:3>		RZQI				Read-only		00_B: RZQ self test not supported 01_B: ZQ pin might be connected to V_{DDCA} or left floating 10_B: ZQ pin might be shorted to ground 11_B: ZQ pin self test compelte; no error condition detected
OP1		DI (Device Information)				Read-only		0_B: SDRAM 1_B: Do Not Use
OP0		DAI (Device Auto-Initialization Status)				Read-only		0_B: DAI complete 1_B: DAI still in progress

MR1_Devcie Feature 1 (MA<7:0> = 01_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
nWR (for AP)			WC	BT	BL			

OP<2:0>	BL (Burst Length)	Write-only	010_B: BL4 (default) 011_B: BL8 100_B: BL16 All others: reserved
OP3	BT[*1] (Burst Type)	Write-only	0_B: Sequential (default) 1_B: Interleaved
OP4	WC (Wrap)	Write-only	0_B: Wrap (default) 1_B: No wrap (allowed for SDRAM BL4 only)
OP<7:5>	nWR[*2]	Write-only	001_B: nWR=3 (default) 010_B: nWR=4 011_B: nWR=5 100_B: nWR=6 101_B: nWR=7 110_B: nWR=8 All others: reserved

Notes:
1. BL16, interleaved is not an official combination to be supported.
2. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK)

Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence													
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	x	0_B	0_B	wrap	any	4	0	1	2	3												
x	x	1_B	0_B				2	3	0	1												
x	x	x	0_B	nw	any		y	y+1	y+2	y+3												

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
x	0_B	0_B	0_B	wrap	seq	8	0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	4	5	6	7	0	1								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	0	1	2	3	4	5								
x	0_B	0_B	0_B		int		0	1	2	3	4	5	6	7								
x	0_B	1_B	0_B				2	3	0	1	6	7	4	5								
x	1_B	0_B	0_B				4	5	6	7	0	1	2	3								
x	1_B	1_B	0_B				6	7	4	5	2	3	0	1								
x	x	x	0_B	nw	any		illegal (not allowed)															
0_B	0_B	0_B	0_B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_B	0_B	1_B	0_B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_B	1_B	0_B	0_B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_B	1_B	1_B	0_B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_B	0_B	0_B	0_B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_B	0_B	1_B	0_B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_B	1_B	0_B	0_B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_B	1_B	1_B	0_B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
x	x	x	0_B		int		illegal (not allowed)															
x	x	x	0_B	nw	any		illegal (not allowed)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C1~C0.
3. For BL=8, the burst address represents C2~C0.
4. For BL=16, the burst address represents C3~C0.
5. For no-wrap, BL4, the burst must not cross the page boundary or the sub-page boundary.The variabley can start at any address with C0 equal to 0, but must not start at any address shown below

Non-Wrap Restrictions

Width	64Mb	128Mb/256Mb	512Mb/1Gb/2Gb	4Gb/8Gb
	Cannot cross full page boundary			
X16	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001	7FE, 7FF, 000, 001
X32	7E, 7F, 00, 01	FE, FF, 00, 01	1FE, 1FF, 000, 001	3FE, 3FF, 000, 001
	Cannot cross sub-page boundary			
X16	7E, 7F, 80, 81	0FE, 0FF, 100, 101	1FE, 1FF, 200, 201	3FE, 3FF, 400, 401
X32	none	none	None	none

Note: Non-wrap BL=4 data orders shown are prohibited.

MR2_Device Feature 2 (MA<7:0> = 02_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				RL & WL				
OP<3:0>		RL & WL (Read Latency & Write Latency)				Write-only		0001_B: RL3 / WL1 (default) 0010_B: RL4 / WL2 0011_B: RL5 / WL2 0100_B: RL6 / WL3 0101_B: RL7 / WL4 0110_B: RL8 / WL4 All others: reserved

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
(RFU)				DS				
OP<3:0>		DS (Drive Strength)				Write-only		0000_B: reserved 0001_B: 34.3 ohm typical 0010_B: 40.0 ohm typical (default) 0011_B: 48.0 ohm typical 0100_B: 60.0 ohm typical 0101_B: reserved 0110_B: 80.0 ohm typical 0111_B: 120.0 ohm typical All others: reserved

MR4_Device Temperature (MA<7:0> = 04_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
TUF	(RFU)				SDRAM Refresh Rate			
OP<2:0>		SDRAM Refresh Rate				Read-only		000_B: 4 x t_{REFI}, SDRAM Low Temp. operating limit exceeded 001_B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW 010_B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW, 011_B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW (<= 85C) 100_B: RFU

			101_B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, don't re-rate SDRAM AC timing 110_B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, derate SDRAM AC timing 111_B: SDRAM High temperature operating limit exceeded
OP7	TUF (Temperature Update Flag)	Read-only	0_B: (not used) 1_B: (always)

Notes:
1. A Mode Register Read from MR4 will reset OP7 to "0".
2. OP7 is reset to "0" at power-up.
3. If OP2 equals "1", the device temperature is greater than 85C.
4. OP7 is set to "1", if OP2~OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP<2:0> = 000B or 111B.
6. For specified operating temperature range and maximum operating temperature.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. The tDQSCK parameter must be derated Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in "Temperature Sensor"

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
LPDDR2 Manufacturer ID								
OP<7:0>	Manufacturer ID					Read-only		0001 1011B: ISSI All Others : Reserved

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID1								
OP<7:0>	Revision ID1					Read-only		00000000_B: A-version

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Revision ID2								
OP<7:0>	Revision ID2					Read-only		00000000_B: A-version

MR8_Basic Configuration 4 (MA<7:0> =08_H):

OP7	OP6	OP5	OP4O	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type	Read-only	00_B:S4 SDRAM
			01_B: Reserved
			10_B: Reserved
			11_B: Reserved
OP<5:0>	Density	Read-only	0000_B: 64Mb (Reserved)
			0001_B: 128Mb (Reserved)
			0010_B: **256Mb**
			0011_B: 512Mb (Reserved)
			0100_B: 1Gb (Reserved)
			0101_B: 2Gb (Reserved)
			0110_B: 4Gb (Reserved)
			0111_B: 8Gb (Reserved)
			1000_B: 16Gb (Reserved)
			1001_B: 32Gb (Reserved)
			All others: Reserved
OP<7:6>	I/O width	Read-only	00_B: x32
			01_B: x16
			10_B: x8 (Reserved)
			11_B: not used

MR9_Test Mode (MA<7:0> =09_H):

OP7	OP6	OP5	OP4O	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10_Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Calibration Code								
OP<7:0>		Calibration Code				Write-only		0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset All others: Reserved

Notes:
1. Host processor shall not write MR10 with “Reserved” values.
2. LPDDR2 devices shall ignore calibration command, when a “Reserved” values is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see “MRW ZQ Calibration Command”) or default
calibration (through the ZQ RESET command) is supported. If ZQ is connected to VDDCA, the device opeates with default calibration,
and ZQ calibration commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.
5. Devices that do not support calibration ignore the ZQ calibration command.

MR11:15_(Reserved) (MA<7:0> = $0B_H$- $0F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Bank Mask (4-Bank)								
OP<7:0>		Bank Mask Code				Write-only		0_B: refresh enable to the bank (=unmasked, default) 1_B: refresh blocked (=masked)

OP	Bank Mask	4 Bank
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3

Note: For 4-bank S4 SDRAM, only OP<3:0> are used.

MR17_(Reserved) (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR18:19_(Reserved) (MA<7:0> = 012_H- 013_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR20:31_(Do Not Use) (MA<7:0> = 014_H- $01F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR32_(DQ Calibration pattern A) (MA<7:0> = 020_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Read-only								See Data Calibration Pattern Description

MR33:39_(Do Not Use) (MA<7:0> = 021_H- 027_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR40_(DQ Calibration pattern B) (MA<7:0> = 028_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Read-only								See Data Calibration Pattern Description

MR41:47_(Do Not Use) (MA<7:0> = 029_H- $02F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR48:62_(Reserved) (MA<7:0> = 030_H- $03E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR63_Reset (MA<7:0> = $03F_H$): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
X								

Note: For additional information on MRW RESET, see “Mode Register Write Command” on Timing Spec.

MR64:126_(Reserved) (MA<7:0> = 040_H- $07E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR127_(Do Not Use) (MA<7:0> = $07F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR128:190_(Reserved for Vendor Use) (MA<7:0> = 080_H- $0BE_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR191_(Do Not Use) (MA<7:0> = $0BF_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

MR192:254_(Reserved for Vendor Use) (MA<7:0> = $0C0_H$- $0FE_H$):								
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
RFU								

MR255_(Do Not Use) (MA<7:0> = $0FF_H$):								
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	
Do Not Use								

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be powered down and then restarted using the specified initialization sequence before normal operation can continue.

Command Truth Table

Table 49: Command Truth Table

Notes 1–11 apply to all parameters conditions

Command	Command Pins			CA Pins										CK Edge
	CKE													
	CK(n-1)	CK(n)	CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
	H	H	X	MA6	MA7	X								↓
REFRESH (per bank)	H	H	L	L	L	H	L	X						↑
	H	H	X	X										↓
REFRESH (all banks)	H	H	L	L	L	H	H	X						↑
	H	H	X	X										↓
Enter self refresh	H	L	L	L	L	H	X							↑
	X	L	X	X										↓
ACTIVATE (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
	H	H	X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
WRITE (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
READ (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
	H	H	X	AP	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
PRECHARGE (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
	H	H	X	X										↓
BST	H	H	L	H	H	L	L	X						↑
	H	H	X	X										↓
Enter DPD	H	L	L	H	H	L	X							↑
	X	L	X	X										↓
NOP	H	H	L	H	H	H	X							↑
	H	H	X	X										↓
Maintain PD, SREF, DPD, (NOP)	L	L	L	H	H	H	X							↑
	L	L	X	X										↓

Command	Command Pins			CA Pins										CK Edge
	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK(n-1)	CK(n)												
NOP	H	H	H	X										↑
	H	H	X	X										↓
Maintain PD, SREF, DPD, (NOP)	L	L	H	X										↑
	L	L	X	X										↓
Enter power-down	H	L	H	X										↑
	X	L	X	X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
	X	H	X	X										↓

Note:
1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses (BA) determine which bank will be operated upon.
3.AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
4. X indicates a “Don’t Care” state, with a defined logic level, either HIGH (H) or LOW (L).
5. Self refresh exit and DPD exit are asynchronous.
6. VREF must be between 0 and VDDQ during self refresh and DPD operation.
7. CAxr refers to command/address bit “x” on the rising edge of clock.
8. CAxf refers to command/address bit “x” on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. Per-bank refresh is only supported in devices with eight banks.
11. The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero

CKE Truth Table

Device Current State*3	CKE_{n-1}*1	CKE_n*1	CS#2*	Command n*4	Operation n*4	Device Next State	Notes
Active Power Down	L	L	x	x	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	x	x	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	x	x	Maintain Resertting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	x	x	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	x	x	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	Enter Self-Refresh	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:
1.“CKEn” is the logic state of CKE at clock edge n; “CKEn-1” was the logic state of CKE at previous clock edge.
2. “CS#” is the logic state of CS# at the clock rising edge n;
3. “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
4. “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power- Down exit procedure must be followed as discussed in the DPD section of the Functional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least once during the tXSR period.
11. “x” means “Don’t care”.
12. Upon exiting Resetting Power Down, the device will return to the idle state if tINIT5 has expired.

Current State Bank n – Command to Bank n Truth Table

Current State	Command	Operation	Next State	Notes
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (AllBank)	7
	MRW	Load value from Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle / MR Reading	
	Reset	Begin Device Auto-initialization	Resetting	7,8
	Precharge	Deactivate row in bank or banks	Precharging	9,15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active / MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-initialization	Resetting	7,9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Notes:
1. Values in this table apply when both CKEn -1 and CKEn are HIGH, and after tXSR or tXP has been met, if the previous state was power-down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

Idle: The bank or banks have been precharged, and tRP has been met.

Active: A row in the bank has been activated, and tRCD has been met. No data bursts or accesses and no register acesses are in progress.

Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.

4. The states listed below must not be interrupted by a command issued to the same bank.

NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that bank's current state, and the definitions given in Current State Bank n to Command to Bank m Truth Table.

Precharge: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank is in the idle state.

Row activate: Starts with registration of an ACTIVATE command and ends when tRCD is met. After tRCD is met, the bank is in the active state.

READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states.

Refresh (per bank): Starts with registration of a REFRESH (per bank) command and ends when tRFCpb is met. After tRFCpb is met, the bank is in the idle state.
Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when tRFCab is met. After tRFCab is met,
the device is in the all banks idle state.
Idle MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in the all
banks idle state.
Resetting MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in
the all banks idle state.
Active MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the bank is in the active state.
MR writing: Starts with registration of the MRW command and ends when tMRW is met. After tMRW is met, the device is in the all banks idle state.
Precharging all: Starts with registration of a PRECHARGE ALL command and ends when
tRP is met. After tRP is met, the device is in the all banks idle state.

6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
10. If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.
11. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
12. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
13. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
14. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
15. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Current State Bank n to Command to Bank m Truth Table

Current State of Bank n	Command to Bank m	Operation	Next State for Bank m	Notes
Any	NOP	Continue previous operation	Current state of bank m	
Idle	Any	Any command supported to bank m	–	7
Row activating, active, or pre-charging	ACTIVATE	Select and activate row in bank m	Active	8
	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or active MR reading	11, 12, 13
	BST	READ or WRITE burst terminates an on-going READ/WRITE from/to bank m	Active	7
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 14
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9, 15
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank m	Reading	9, 16
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 14, 16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank m	Reading	9, 15, 16
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	MRW RESET	Begin device auto initialization	Resetting	17, 18
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:
1. This table applies when: the previous state was self refresh or power-down; after tXSR z or tXP has been met; and both CKEn -1 and CKEn are HIGH.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:

Idle: The bank has been precharged and tRP has been met.
Active: A row in the bank has been activated, tRCD has been met, no data bursts or accesses and no register accesses are in progress.
Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.
Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.

4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.
5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.
6. The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:

Idle MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the device is in the all banks idle state.
Reset MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the device is in the all banks idle state.
Active MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the bank is in the active state.
MRW: Starts with registration of the MRW command and ends when tMRW has been met. After tMRW is met, the device is in the all banks idle state.

7. BST is supported only if a READ or WRITE burst is ongoing.
8. tRRD must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m.
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. This command may or may not be bank-specific. If all banks are being precharged, they must be in a valid state for precharging.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank m depends on the current state of bank m (idle, row-activating,precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge Clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command

DM Operation Truth Table

Function	DM	DQ	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

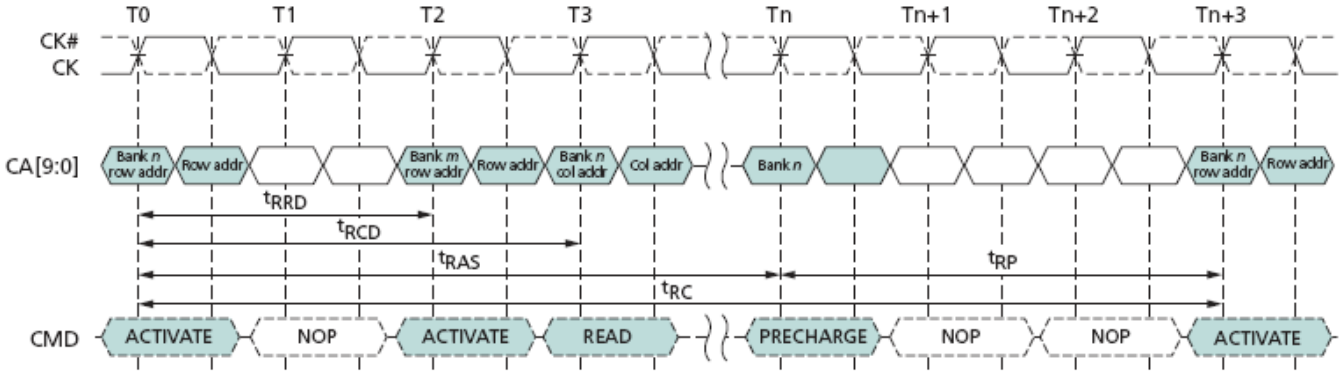
Note: Used to mask write data, and is provided simultaneously with the corresponding input data.

Command

Activate

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA[1:0] are used to select the desired bank.
Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed.
The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

ACTIVATE Command



Activate command cycle: ^{t}RCD=3, ^{t}RP=3, ^{t}RRD=2

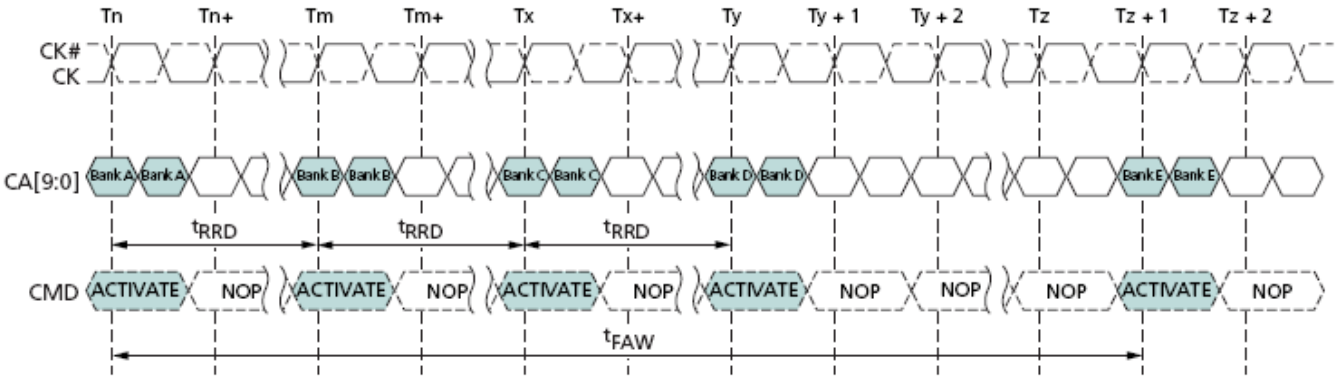
Notes:
1. tRCD = 3, tRP = 3, tRRD = 2.
2. A PRECHARGE ALL command uses tRPab timing, and a single-bank PRECHARGE command uses tRPpb timing. In this figure, tRP is used to denote either an all-bank PRECHARGE or a single-bank PRECHARGE

Certain restriction on operation of 8 bank devices must be observed, One rule restricts the number of sequential ACTIVATE commands that can be issued; the second provides additional RAS pre-charge time for a PRECHARGE ALL command.

• The 8-Bank Device Sequential Bank Activation Restriction:No more than four banks can be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. To convert to clocks, divide tFAW[ns] by tCK[ns], and round up to the next integer value. For example, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW.

• The 8-Bank Device PRECHARGE ALL Provision: tRP for a PRECHARGE ALL command must equal tRPab, which is greater than tRPpb

tFAW Timing (8-Bank Devices)



tFAW timing

Note: Exclusively for 8-bank devices. The product for this datasheet has 4-banks.

Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The LPDDR2 provide a fast column access operation .A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles.

For LPDDR2 –S4 devices, a new burst access must not interrupt the previous 4-bit burst operation when BL = 4.

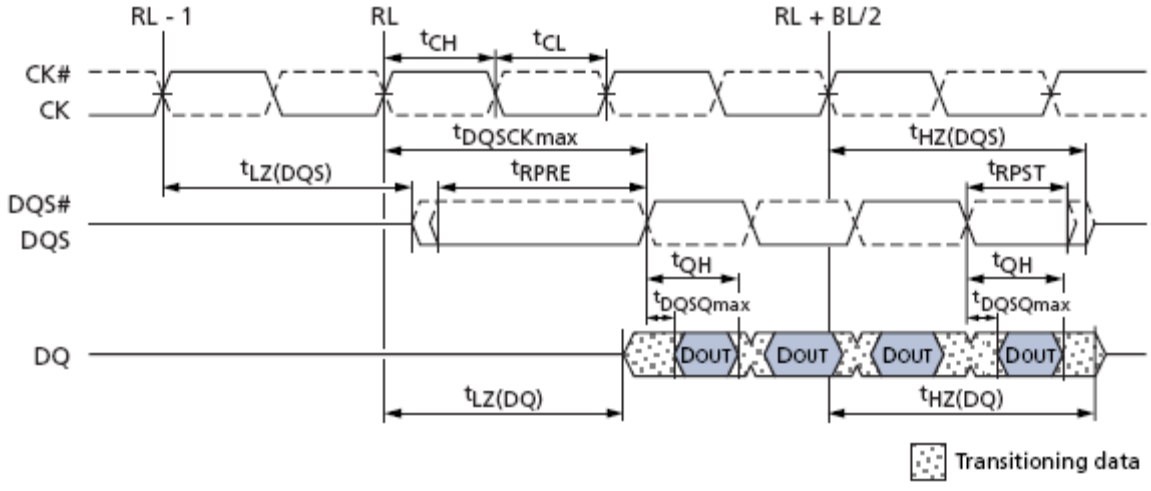
In case of BL = 8 or BL = 16, READs can be interrupted by READs and WRITEs can be interrupted by WRITEs, provided that the interrupt occurs on a 4-bit boundary and that tCCD is met.

Burst READ

The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW tRPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge aligned with the data strobe. The RL is programmed in the mode registers.

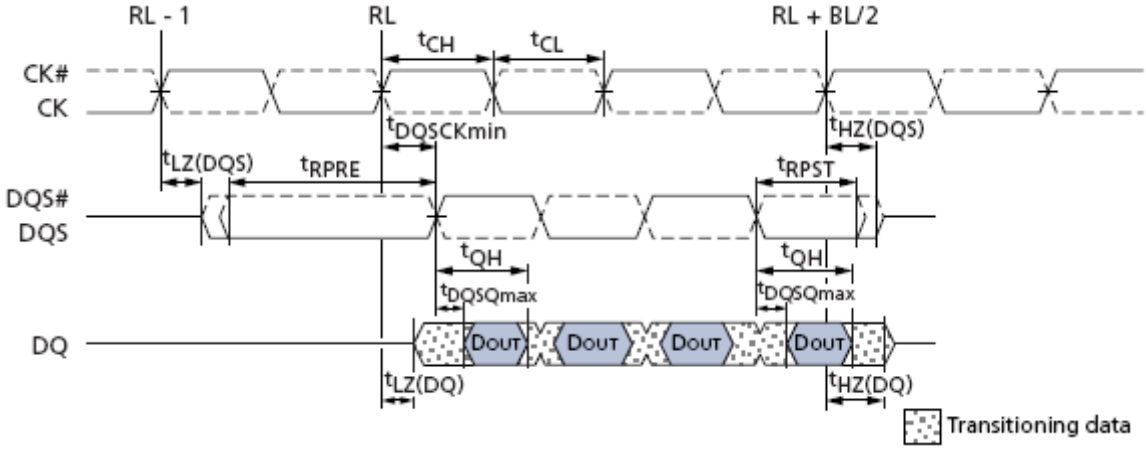
Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

Data Output (Read) Timing – tDQSCK (MAX)



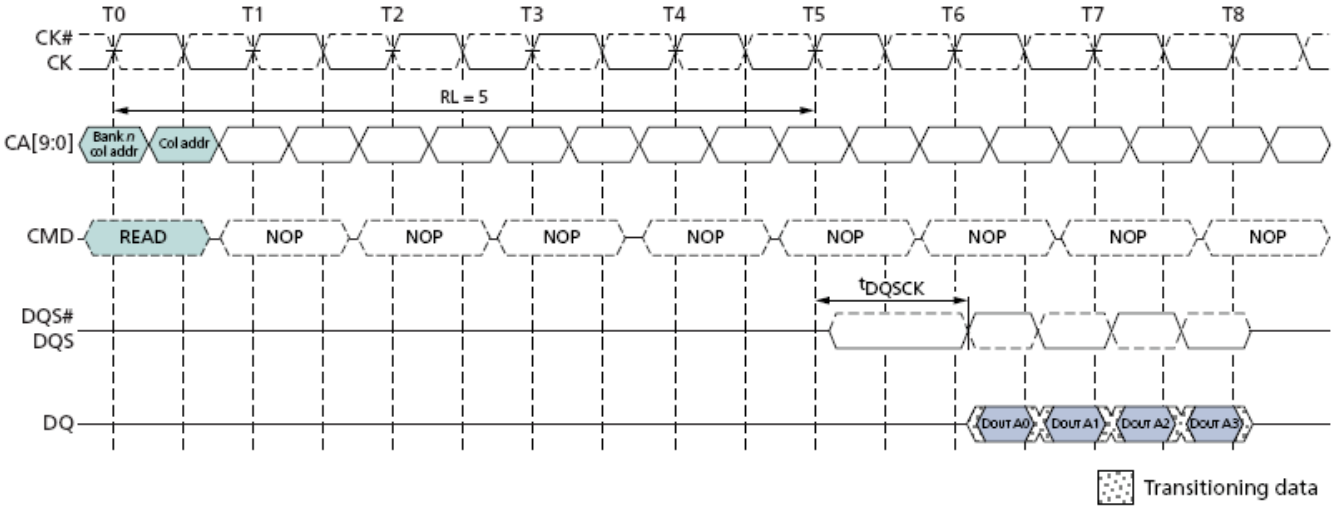
Notes:
1. tDQSCK can span multiple clock periods.
2. An effective burst length of 4 is shown

Data Output (Read) Timing– tDQSCK (MIN)

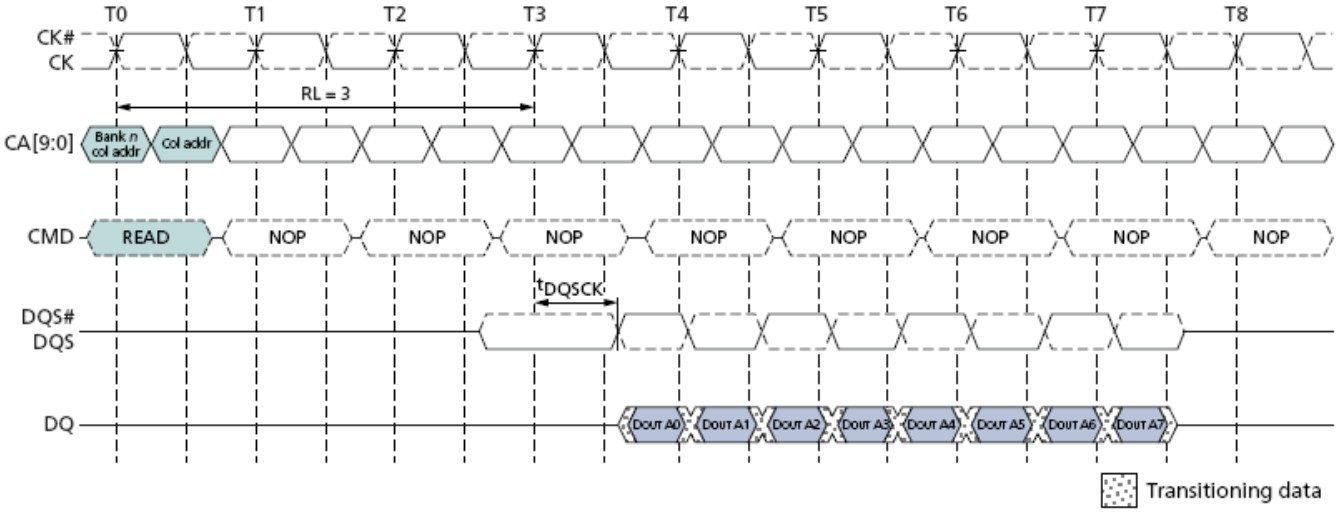


Note: An effective BL=4 is shown.

Burst READ – RL = 5, BL = 4, tDQSCK > tCK

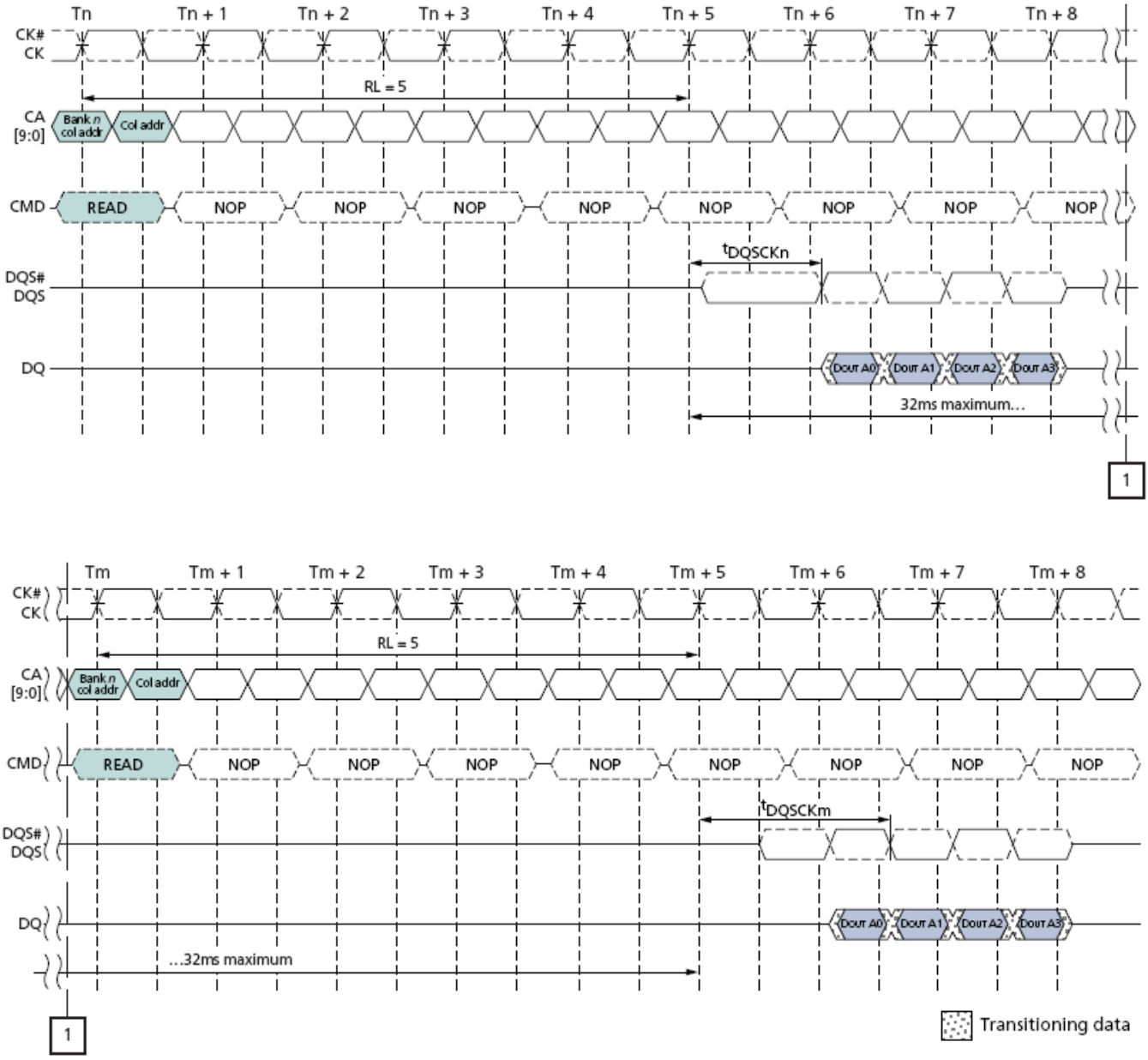


Burst READ – RL = 3, BL = 8, tDQSCK < tCK



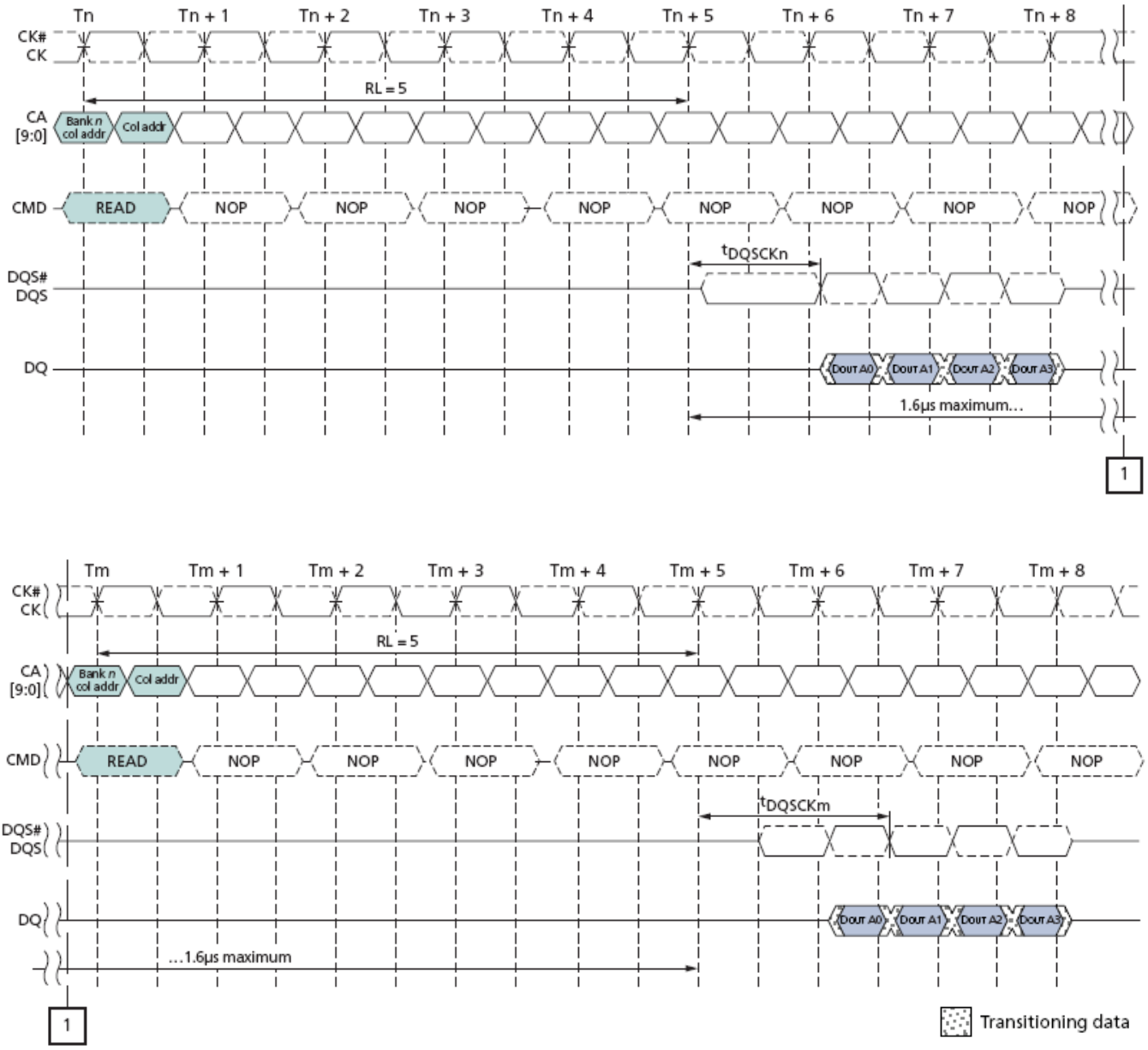
Burst Read: RL=3, BL=8, ^{t}DQSCK < ^{t}CK

tDQSCKDL Timing



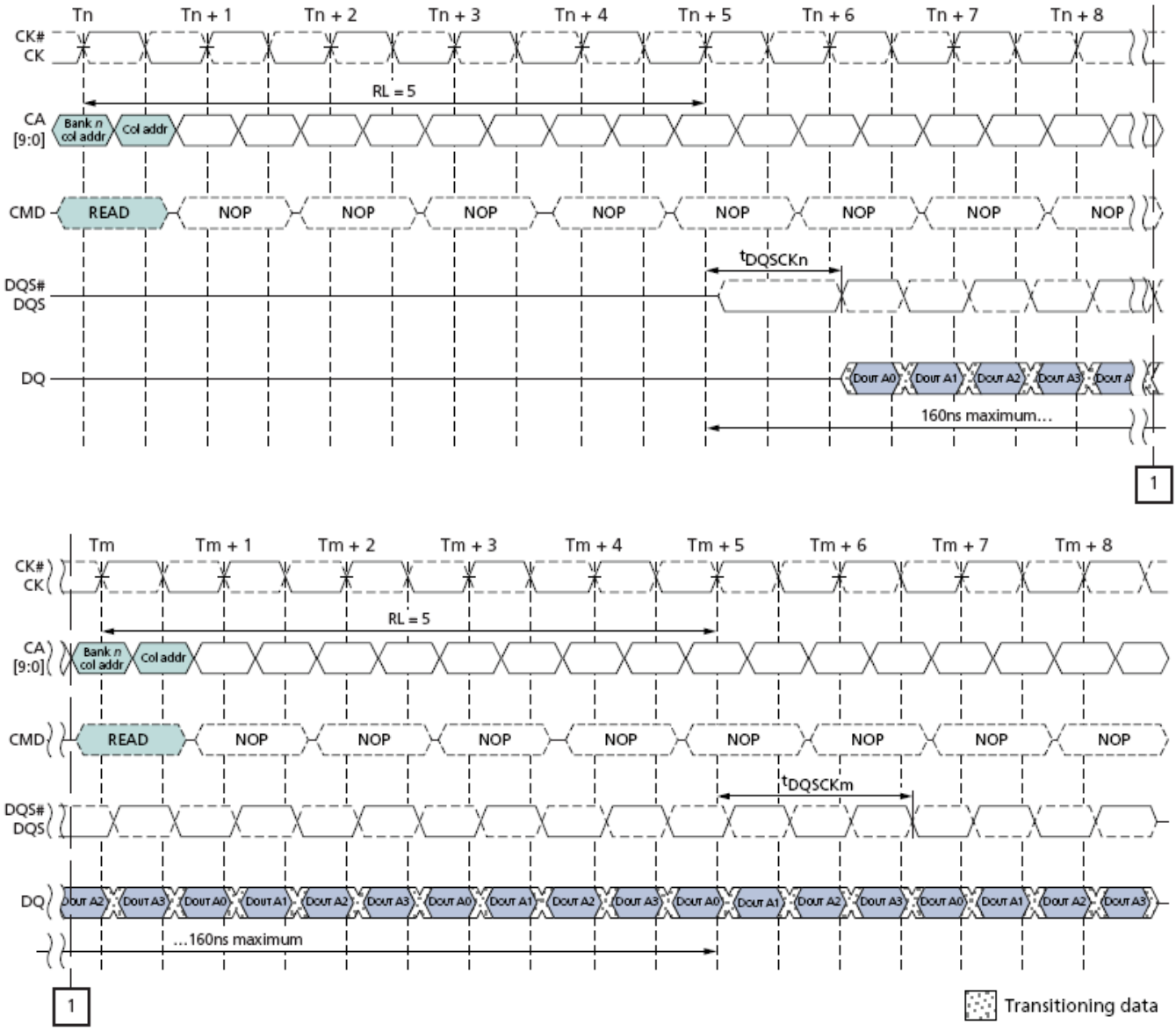
Notes:
1. tDQSCKDL = (tDQSCKn - tDQSCKm).
2. tDQSCKDL (MAX) is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair within any 32ms rolling window.

tDQSCKDM Timing



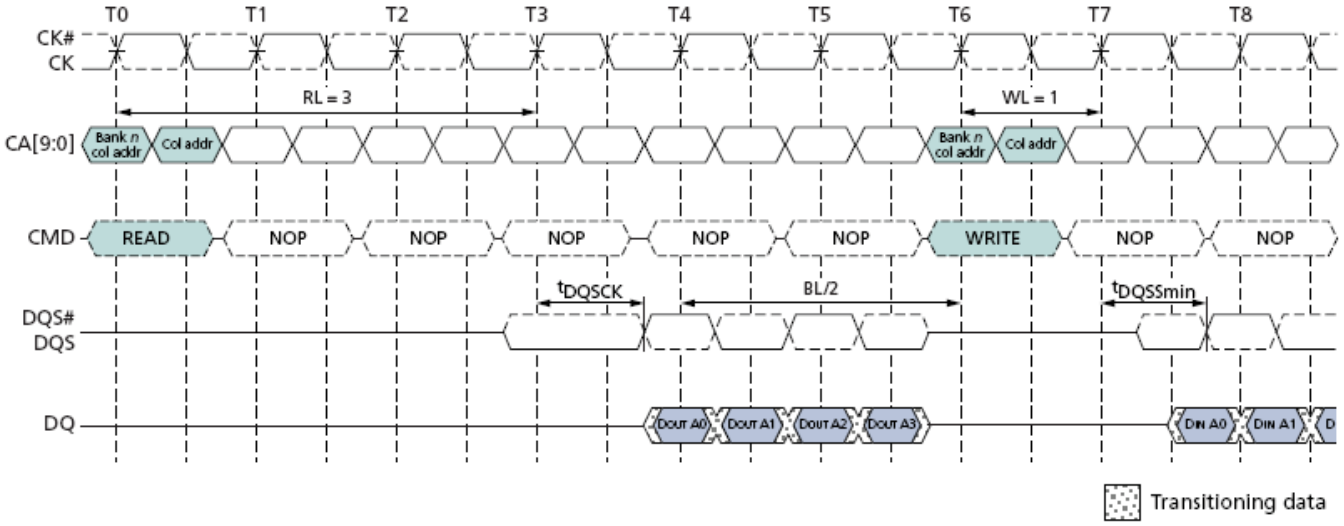
Notes:
1. tDQSCKDM = (tDQSCKn - tDQSCKm).
2. tDQSCKDM (MAX) is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair within any 1.6µs rolling window.

tDQSCKDS Timing



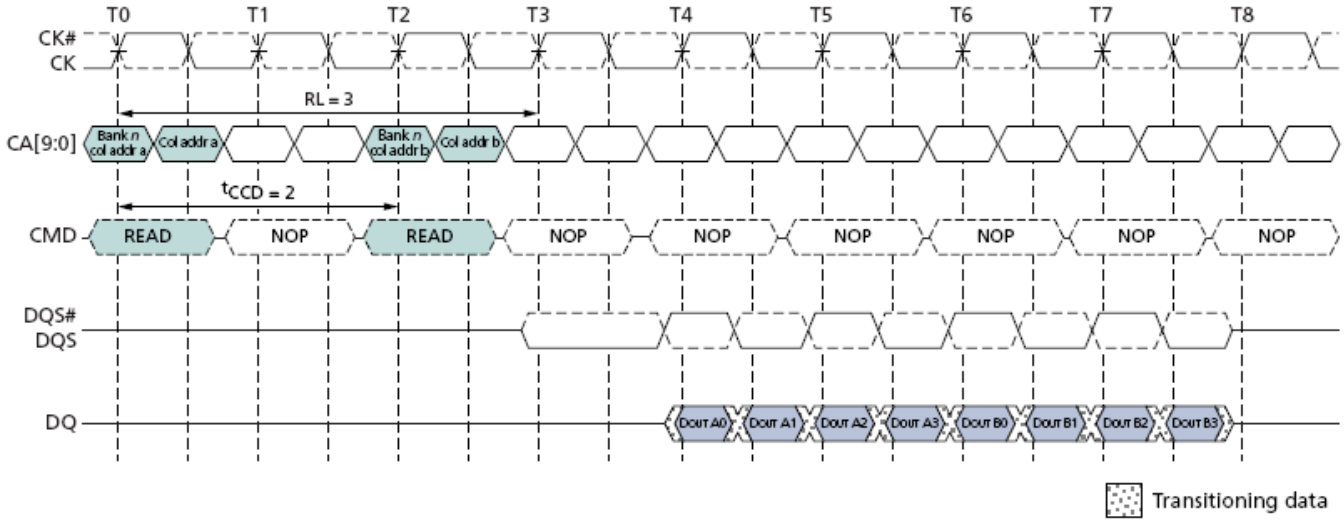
Notes:
1. tDQSCKDS = (tDQSCKn - tDQSCKm).
2. tDQSCKDS (MAX) is defined as the maximum of ABS (tDQSCKn - tDQSCKm) for any (tDQSCKn, tDQSCKm) pair for READs within a consecutive burst, within any 160ns rolling window.

Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4



The minimum time from the burst READ command to the burst WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE latency is RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 - WL clock cycles. Note that if a READ burst is truncated with a burst TERMINATE (BST) command, the effective burst length of the truncated READ burst should be used for BL when calculating the minimum READ-to-WRITE delay.

Seamless Burst READ – RL = 3, BL = 4, tCCD = 2



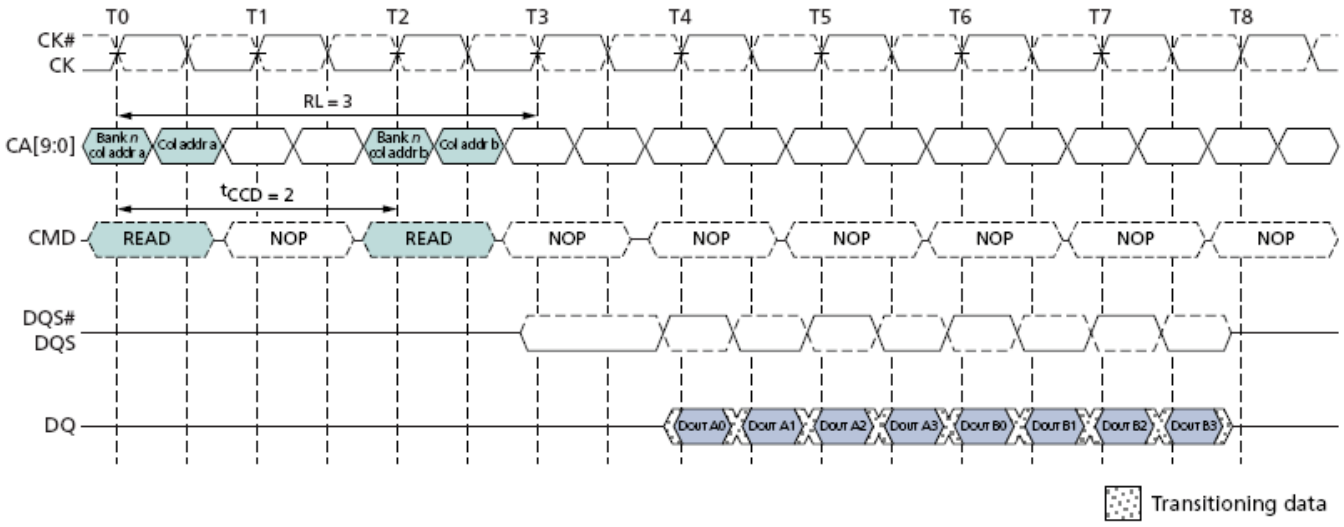
A seamless burst READ operation is supported by enabling a READ command at every other clock cycle for BL = 4 operation, every fourth clock cycle for BL = 8 operation, and every eighth clock cycle for BL = 16 operation. This operation is supported as long as the banks are activated, whether the accesses read the same or different banks.

READs Interrupted by a READ

For LP-DDR2-S4 devices, burst READ can be interrupted by another READ with a 4-bit burst boundary, provided that tCCD is met.

A burst READ can be interrupted by other READs on any subsequent clock, provided that tCCD is met.

READ Burst Interrupt Example – RL = 3, BL = 8, tCCD = 2



Note: READs can only be interrupted by other READs or the BST command.

Burst WRITE

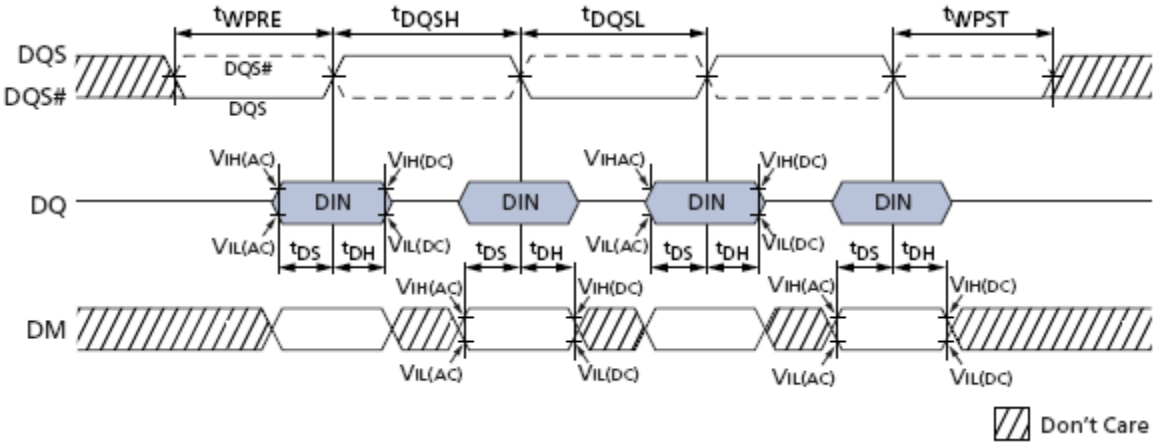
The burst WRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r–CA6r and CA1f–CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW tWPRE prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to

the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed.

After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued.

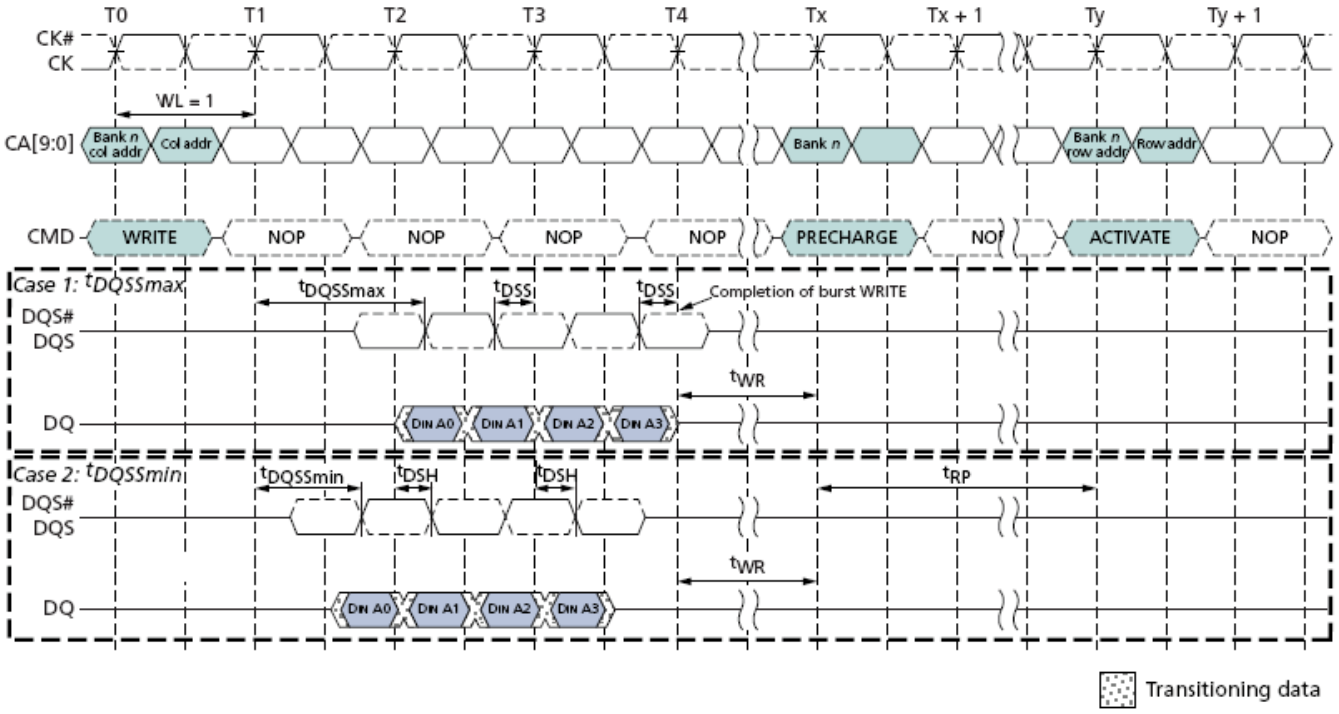
Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Data Input (WRITE) Timing

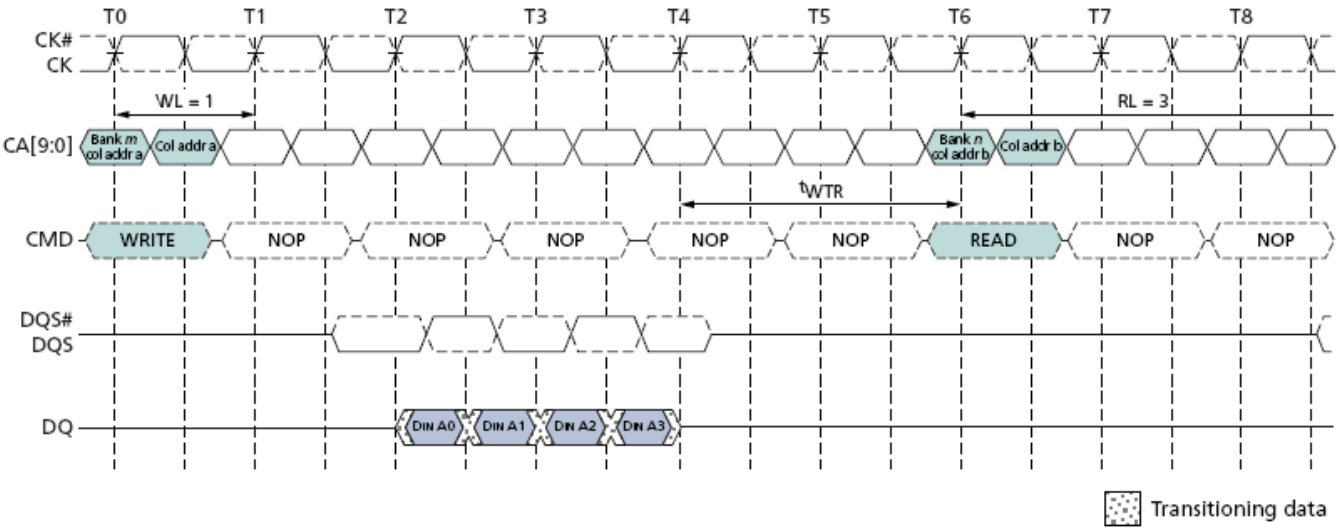


Data input (Write) timing

Burst WRITE – WL = 1, BL = 4

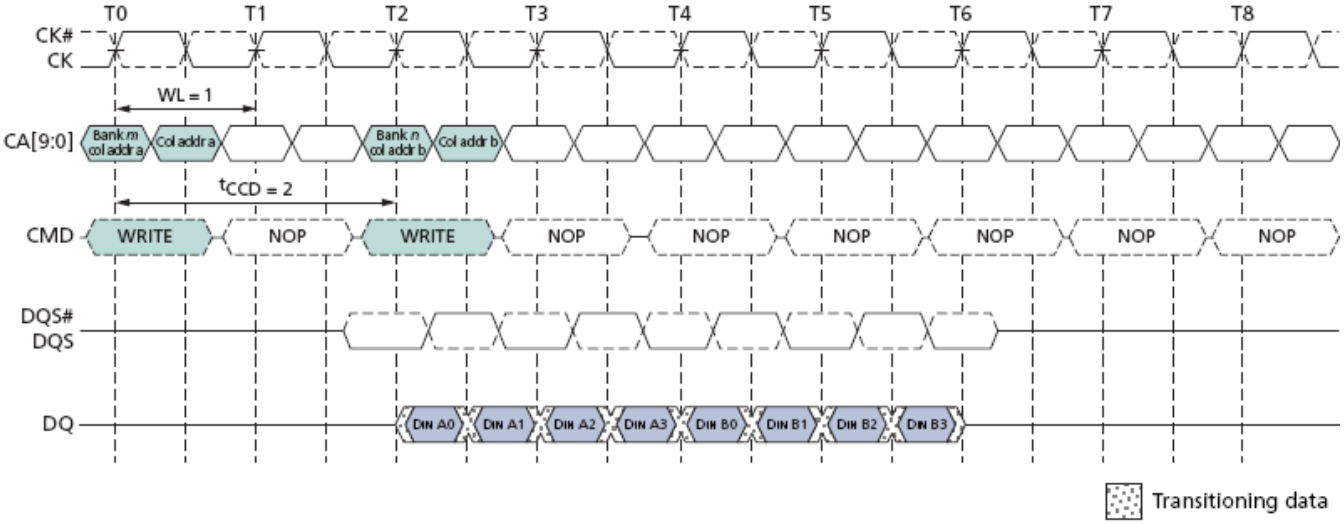


Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. tWTR starts at the rising edge of the clock after the last valid input data.
3. If a WRITE burst is truncated with a BST command, the effective burst length of the truncated WRITE burst should be used as BL to calculate the minimum WRITE-to-READ delay.

Seamless Burst WRITE – WL = 1, BL = 4, tCCD = 2



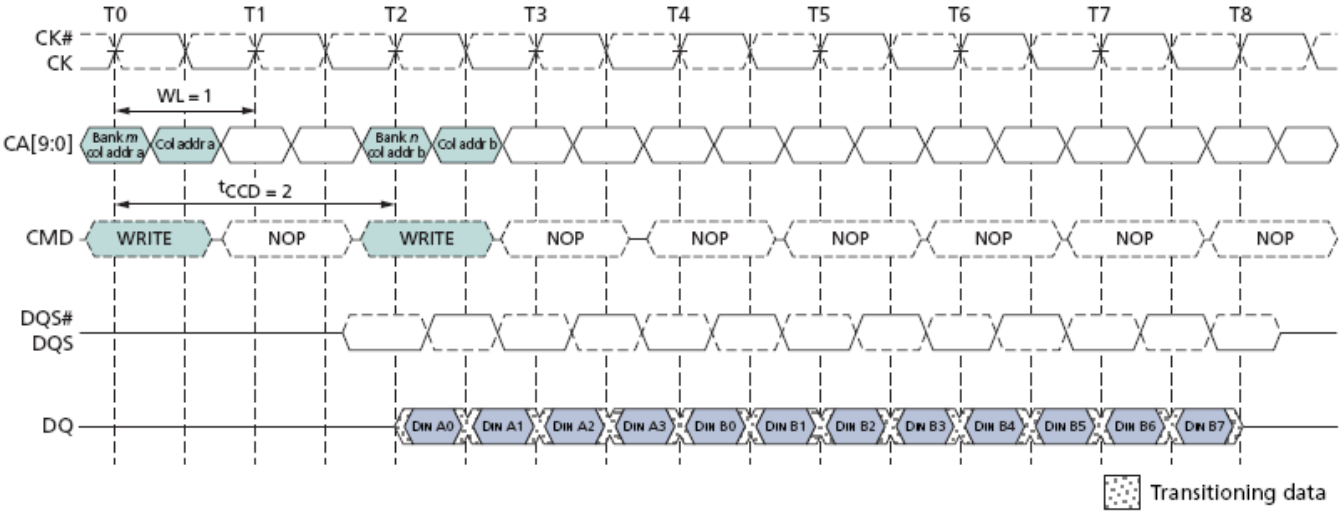
Note: The seamless burst WRITE operation is supported by enabling a WRITE command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is supported for any activated bank.

WRITEs Interrupted by a WRITE

For LPDDR2-S4 devices, a burst WRITE can only be interrupted by another WRITE with a 4-bit burst boundary, provided that tCCD (MIN) is met.

A WRITE burst interrupt can occur on any clock after the initial WRITE command, provided that tCCD (MIN) is met.

WRITE Burst Interrupt Timing – WL = 1, BL = 8, tCCD = 2



Notes:
1. WRITEs can only be interrupted by other WRITEs or the BST command.
2. The effective burst length of the first WRITE equals two times the number of clock cycles between the first WRITE and the interrupting WRITE

BURST TERMINATE (BST)

The BURST TERMINATE (BST) command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command.

The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

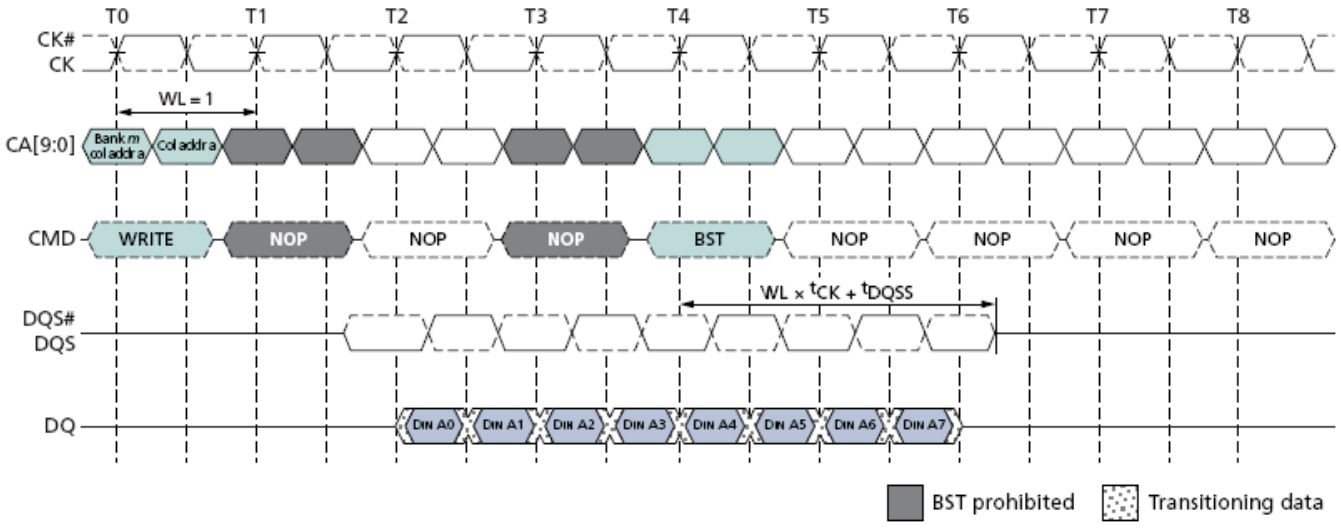
• Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).

• If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ to-WRITE or WRITE-to-READ delay.

• The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock where the BST command is issued. The BST command truncates an ongoing WRITE burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.

• The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

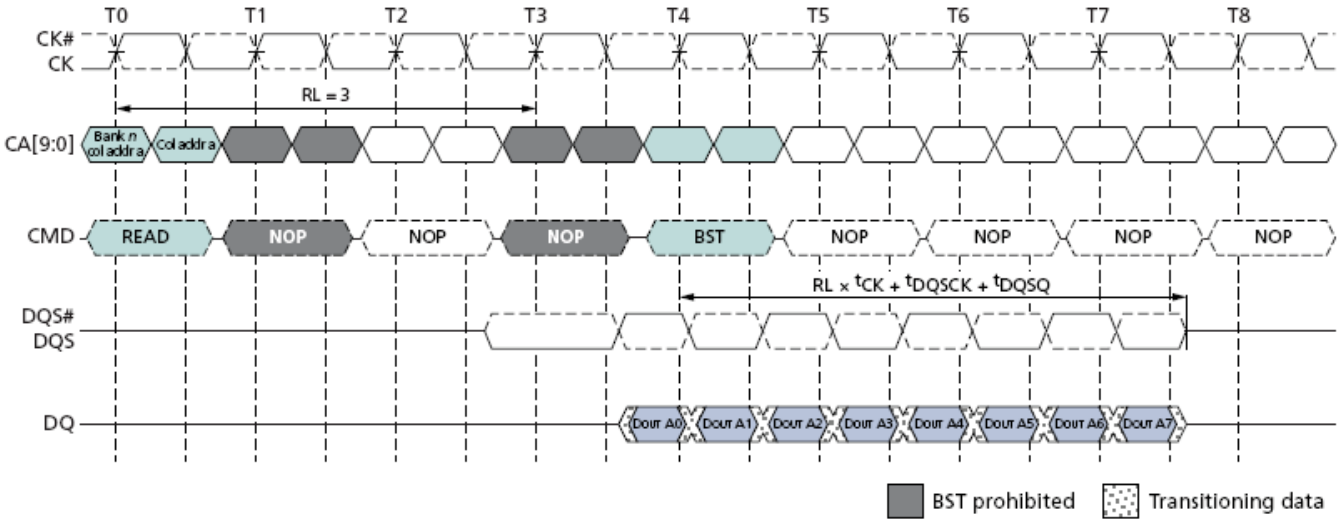
Burst WRITE Truncated by BST – WL = 1, BL = 16



Burst Write truncated by BST: WL=1, BL=16

Notes:
1. The BST command truncates an ongoing WRITE burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.
2. BST can only be issued an even number of clock cycles after the WRITE command.
3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command.

Burst READ Truncated by BST – RL = 3, BL = 16



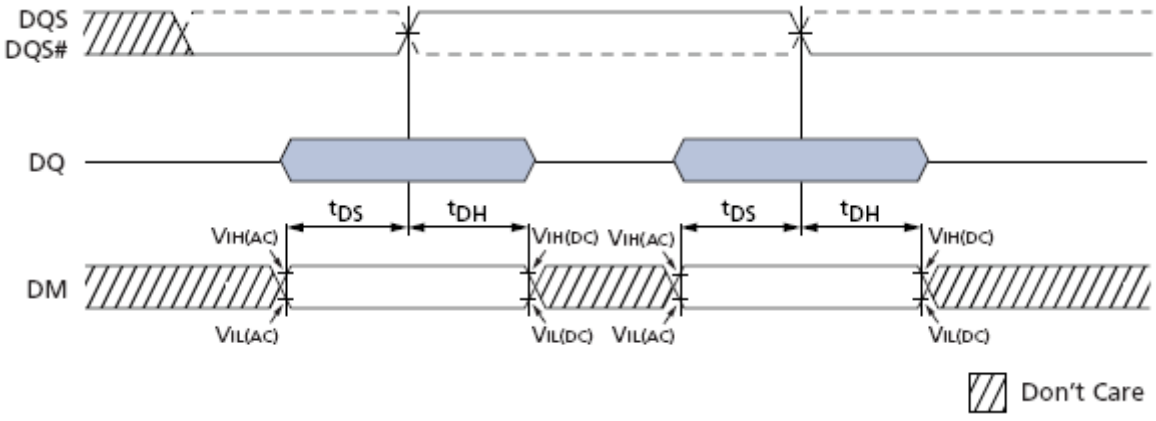
Notes:
1. The BST command truncates an ongoing READ burst (RL × tCK + tDQSCK + tDQSQ) after the rising edge of the clock where the BST command is issued.
2. BST can only be issued an even number of clock cycles after the READ command.
3. Additional BST commands are not supported after T4 and must not be issued until after the next READ or WRITE command

Write Data Mask

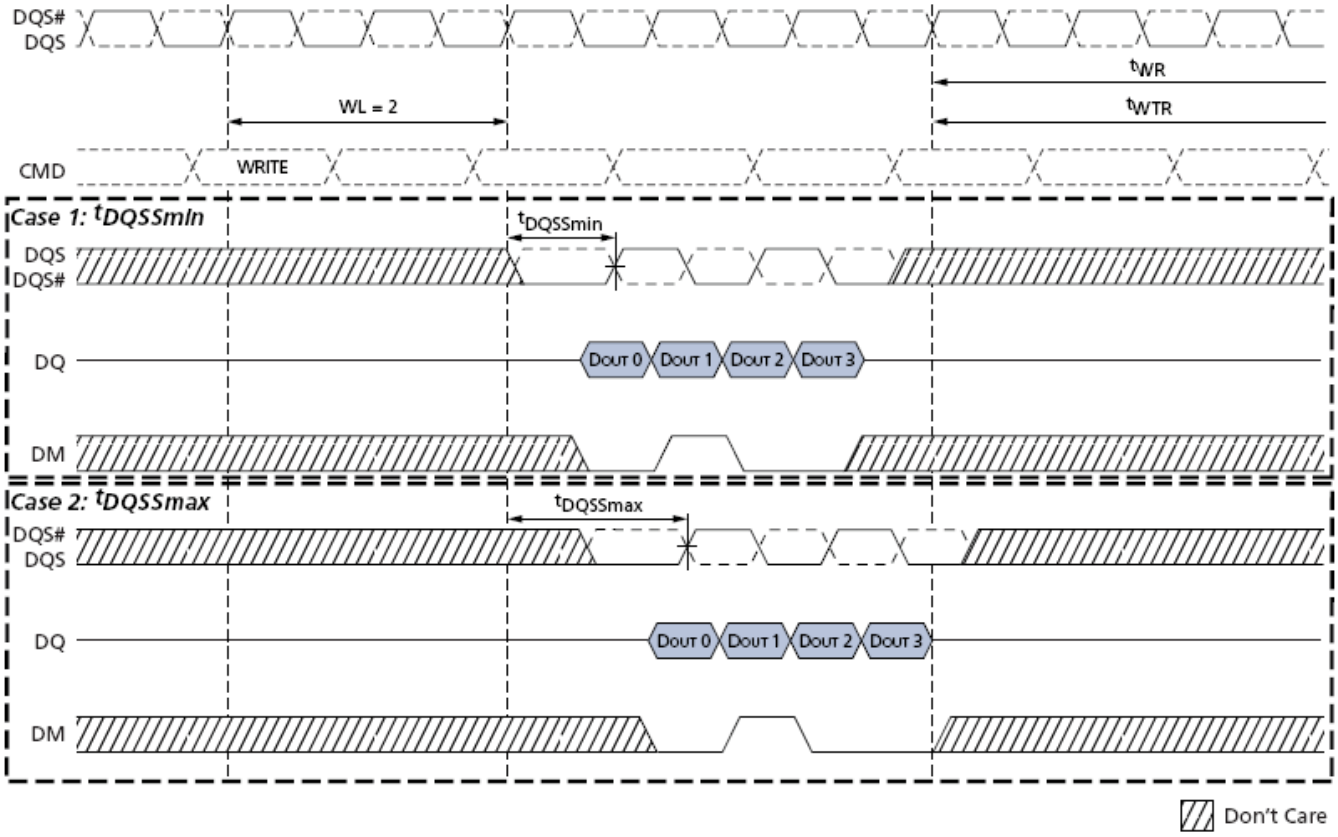
On LPDDR2 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing,

but are inputs only. Internal data mask loading is identical to data bit loading to ensure matched system timing.

Data Mask Timing



Write Data Mask – Second Data Bit Masked



PRECHARGE

The PRECHARGE command is used to precharge or close a bank that has been activated.

The PRECHARGE command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously.

This is a 4-bank device such that, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge; BA2 is not used. The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

This is a 4-bank device so, tRPab is equal to tRPpb.

Bank Selection for PRECHARGE by Address Bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 0 only
0	1	0	1	Bank 1 only
0	1	1	0	Bank 2 only
0	1	1	1	Bank 3 only
1	Don't care	Don't care	Don't care	All Banks

Bank selection for Precharge by address bits

READ Burst operation Followed by PRECHARGE

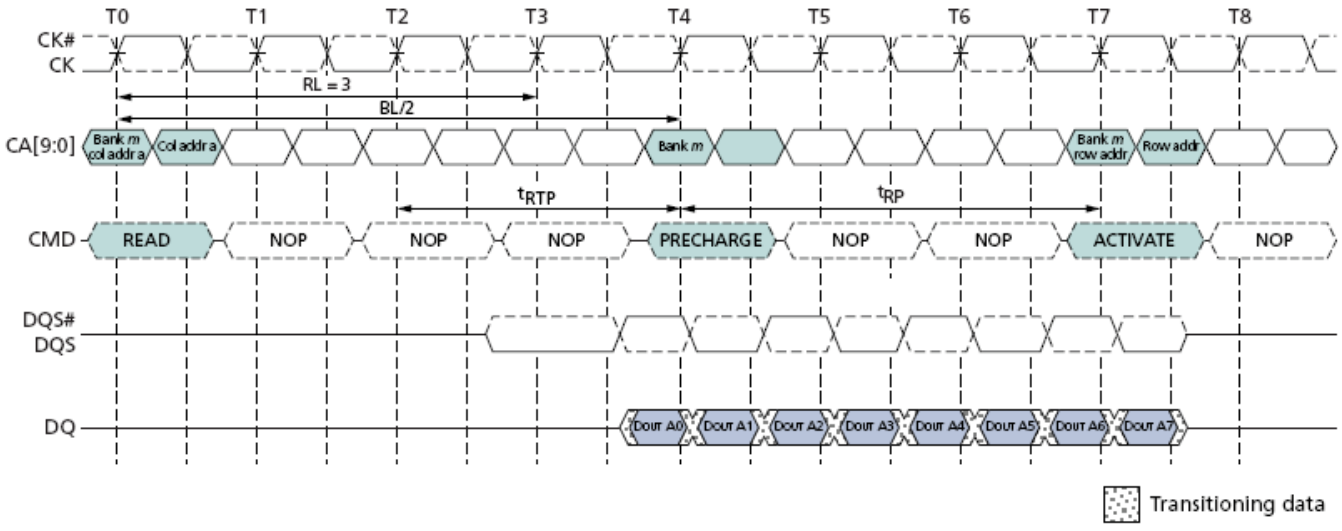
For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (tRP) has elapsed. A PRECHARGE command

cannot be issued until after tRAS is satisfied.

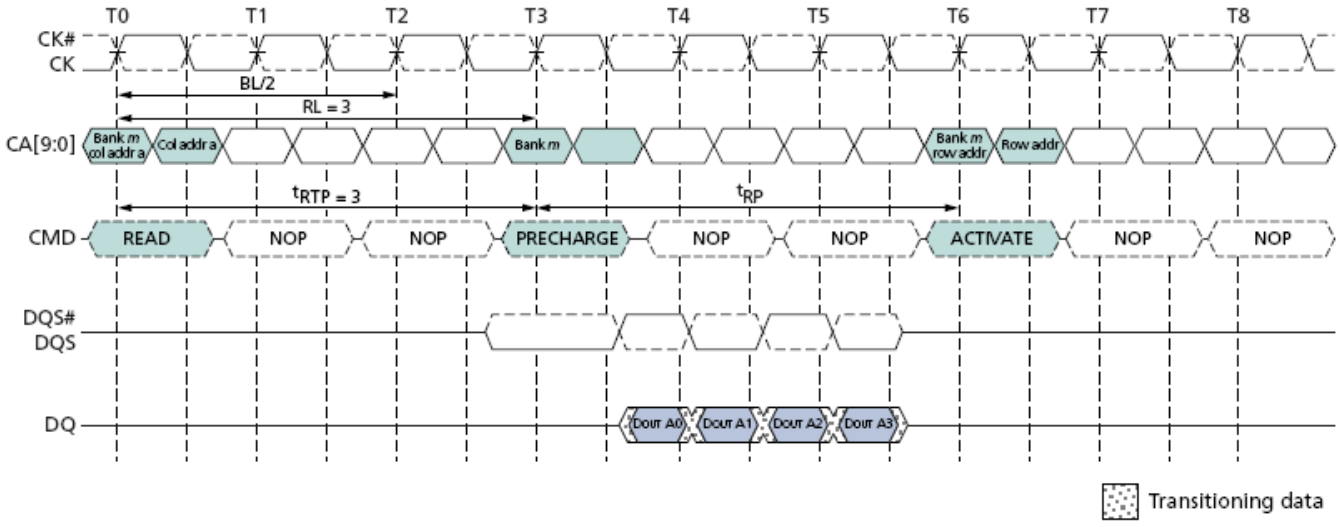
The minimum READ-to-PRECHARGE time (tRTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command. tRTP begins BL/2 - 2 clock cycles after the READ command.

If the burst is truncated by a BST command, the effective BL value is used to calculate when tRTP begins.

READ Burst Followed by PRECHARGE – RL = 3, BL = 8, RU(tRTP(MIN)/tCK) = 2



READ Burst Followed by PRECHARGE – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 3



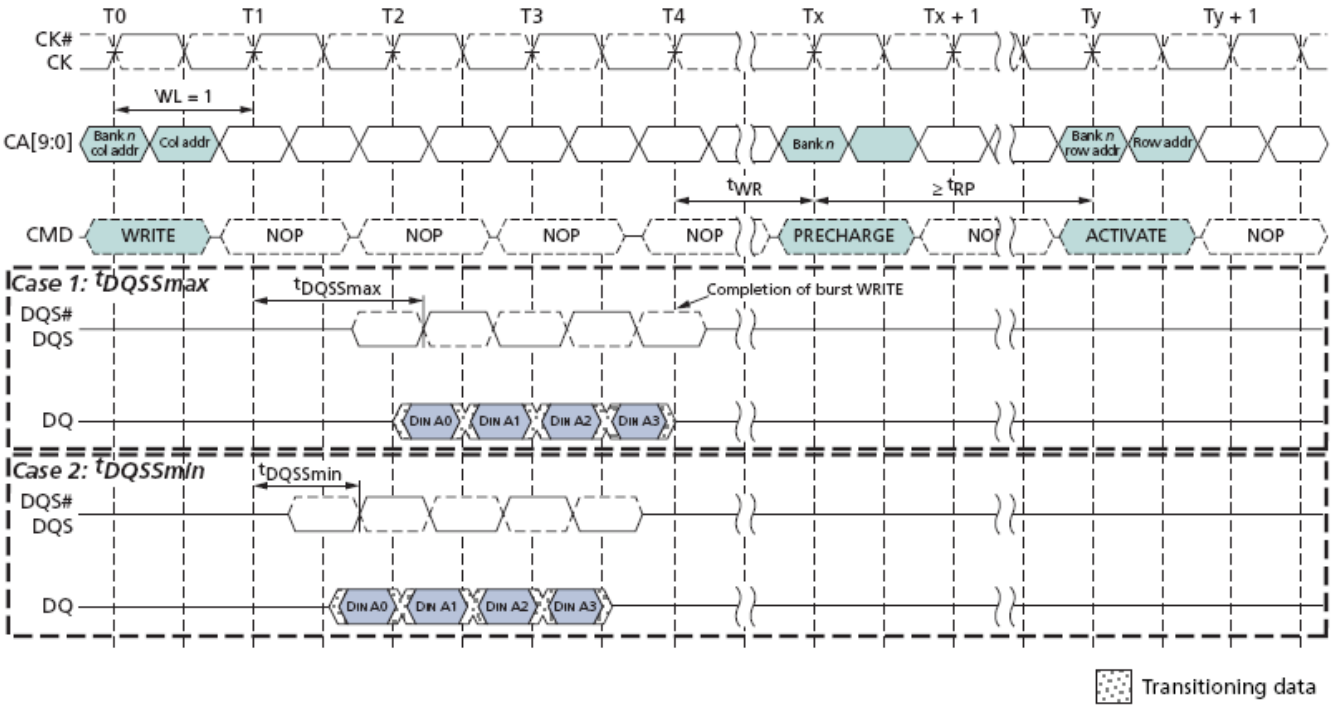
WRITE Burst operation Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the tWR delay.

These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.

WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

READ Burst with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.

These devices start an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations see following table.

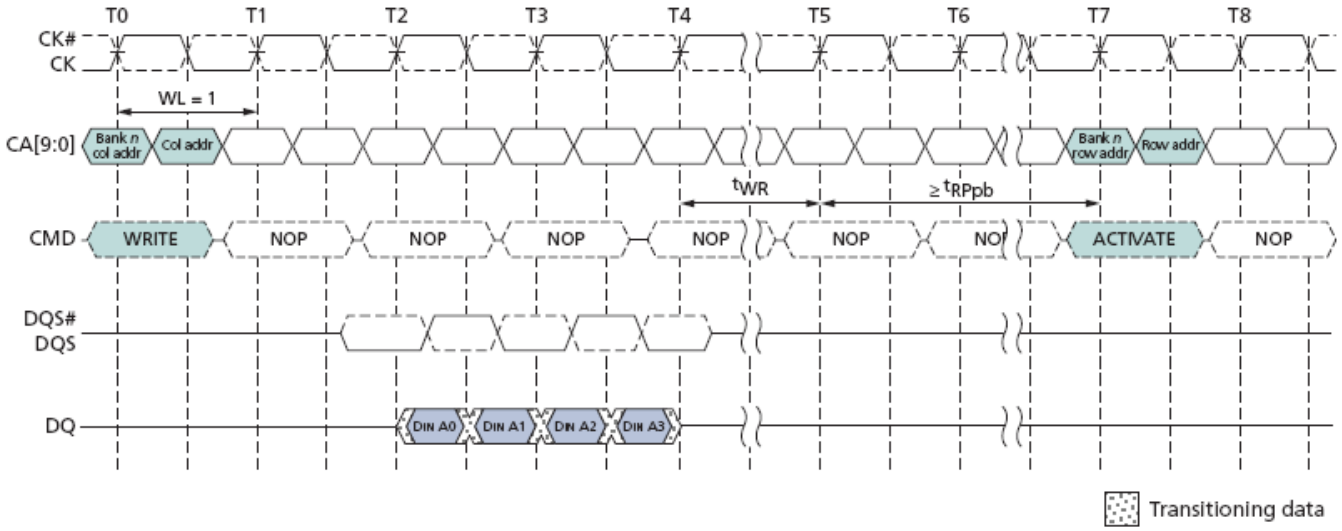
LPDDR2-S4: PRECHARGE and Auto Precharge Clarification

LPDDR2-S4: Precharge & Auto Precharge clarification				
From Command	**To Command**	**Minimum Delay between "From Command" to "To Command"**	**Unit**	**Notes**
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
	Precharge All	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
BST (for Reads)	Precharge (to same Bank as Read)	1	clks	1
	Precharge All	1	clks	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1,2
	Precharge All	BL/2 + max(2, RU(^{t}RTP/^{t}CK)) - 2	clks	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(RTP/ CK)) - 2 + RU(^{t}RP /^{t}CK)	clks	1
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(^{t}DQSCKmax/^{t}CK) - WL + 1	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	BL/2	clks	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + RU(^{t}WR/^{t}CK) + 1	clks	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Precharge All	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1	clks	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(^{t}WR/^{t}CK) + 1 + RU(^{t}RP$_{pb}$/^{t}CK)	clks	1
	Write or Write w/AP (same bank)	illegal	clks	3
	Write or Write w/AP (different bank)	BL/2	clks	3
	Read or Read w/AP (same bank)	illegal	clks	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(^{t}WTR/^{t}CK) + 1	clks	3
Precharge	Precharge (to same Bank as Precharge)	1	clks	1
	Precharge All	1	clks	1
Precharge All	Precharge	1	clks	1
	Precharge All	1	clks	1

Notes:
1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE command—either a one-bank PRECHARGE or PRECHARGE ALL—issued to that bank.
The PRECHARGE period is satisfied after tRP, depending on the latest PRECHARGE command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After READ with auto precharge, seamless READ operations to different banks are supported.
After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:
• The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
• The RAS cycle time (tRC) from the previous bank activation has been satisfied.

READ Burst with Auto Precharge – RL = 3, BL = 4, RU(tRTP(MIN)/tCK) = 2



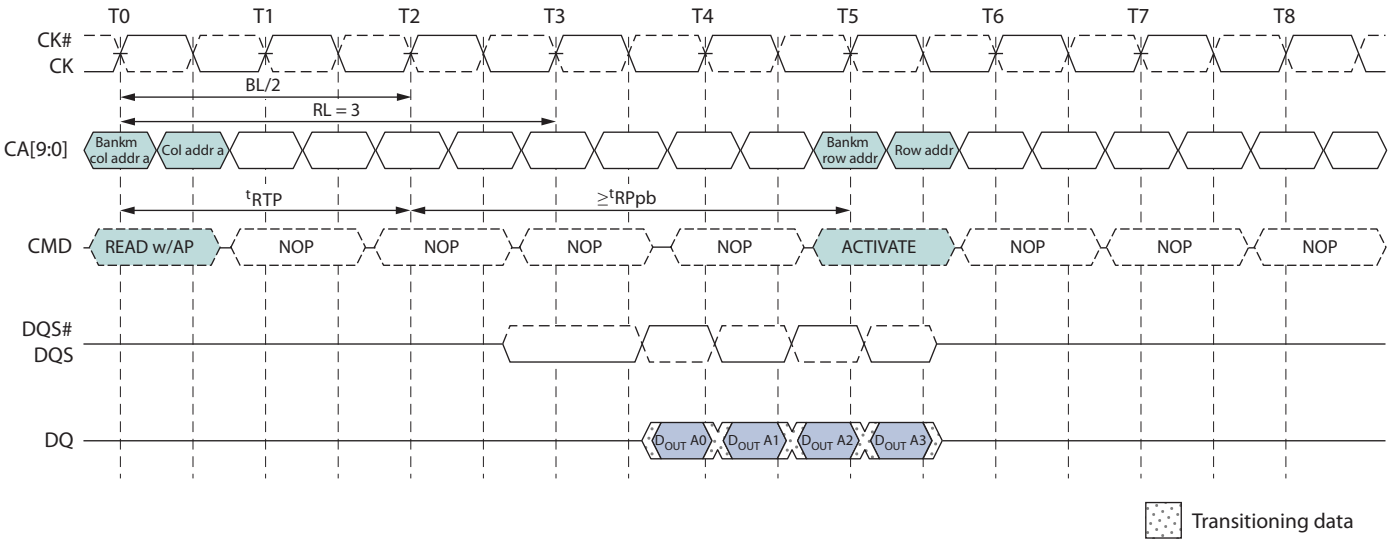
WRITE Burst operation Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the tWR delay.

These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.

The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For untruncated bursts, BL is the value set in the mode register. For truncated bursts, BL is the effective burst length.

WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4



REFRESH

The REFRESH command is initiated with CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of

the clock. Per-bank REFRESH is only supported in devices with eight banks.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-.... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET command or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command.

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

• tRFCab has been satisfied after the prior REFab command

• tRFCpb has been satisfied after the prior REFpb command

• tRP has been satisfied after the prior PRECHARGE command to that bank

• tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle.

During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or WRITE command.

When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

• tRFCpb must be satisfied before issuing a REFab command

• tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank

• tRRD must be satisfied before issuing an ACTIVATE command to a different bank

• tRFCpb must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE commands

After an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command

REFRESH Command Scheduling Separation Requirements

Command Scheduling Separations related to Refresh			
Symbol	**minimum delay from**	**to**	**Notes**
$^{t}RFC_{ab}$	REF_{ab}	REF_{ab}	
		Activate cmd to *any* bank .	
		REF_{pb}	
$^{t}RFC_{pb}$	REF_{pb}	REF_{ab}	
		Activate cmd to *same* bank as REF_{pb}	
		REF_{pb}	
^{t}RRD	REF_{pb}	Activate cmd to *different* bank than REF_{pb}	
	Activate	REF_{pb} affecting an idle bank (different bank than Activate)	1
		Activate cmd to *different* bank than prior Activate	

Note: A bank must be in the idle state before it is refreshed, so REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

The LPDDR2 devices provide significant flexibility in scheduling REFRESH commands as long as the required boundary conditions are met (see figure of tSRF Definition).

In the most straightforward implementations, a REFRESH command should be scheduled every tREFI. In this case, self refresh can be entered at any time.

Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 256Mb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by tREFBW), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: tREFW - (R/8) × tREFBW= tREFW - R × 4 × tRFCab.

For example, a 256Mb device at TC ≤ 85˚C can be operated without a refresh for up to 32ms - 4096 × 4 × 90ns ≈ 30ms.

Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in every rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern is shown in figure of Supported Transition from Repetitive REFRESH Burst .

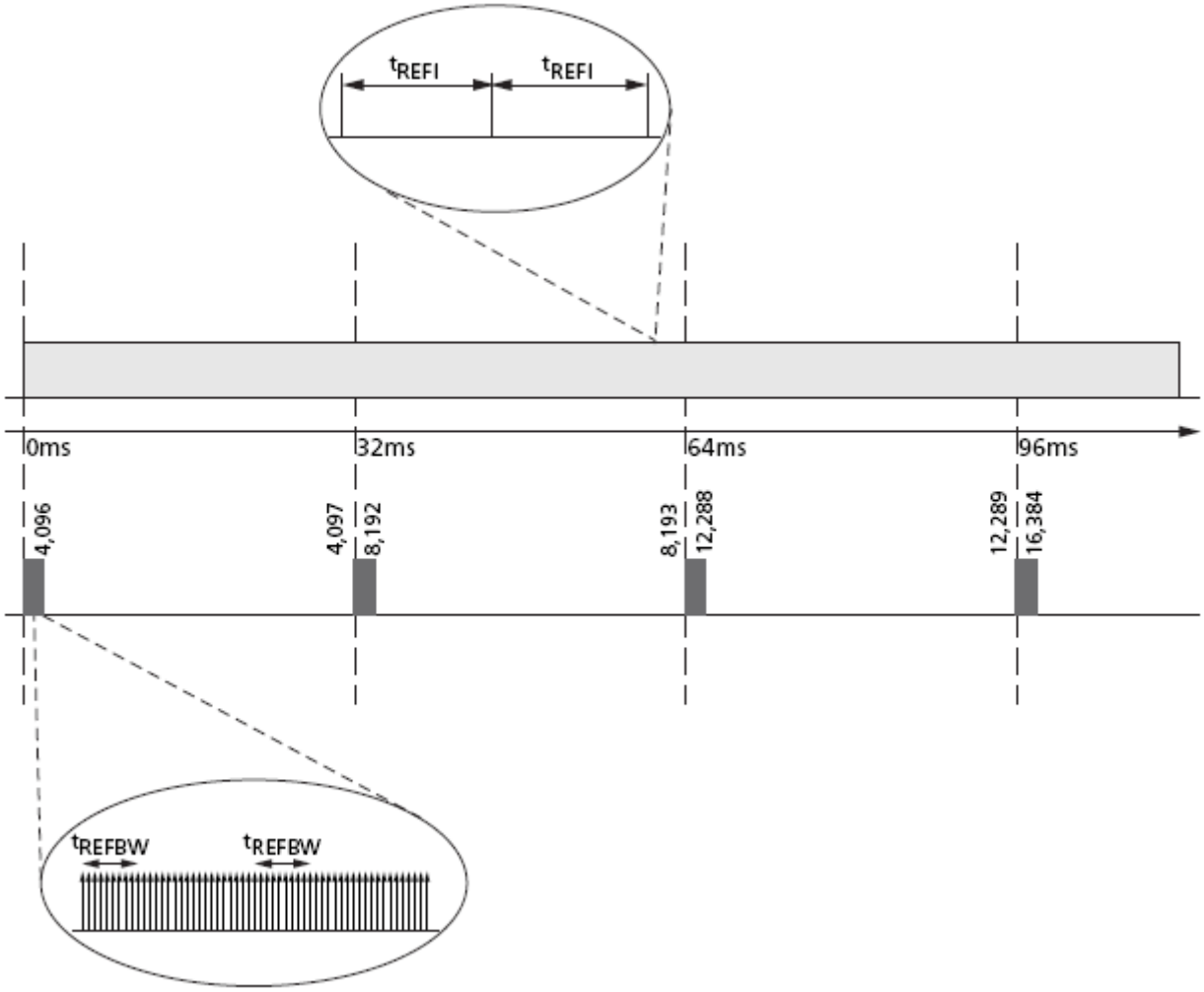
If this transition occurs immediately after the burst refresh phase, all rolling tREFW intervals will meet the minimum required number of REFRESH commands.

A nonsupported transition is shown in Figure of Nonsupported Transition from Repetitive REFRESH Burst . In this example, the regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling tREFW intervals, the minimum number of REFRESH commands is not satisfied.

Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed.

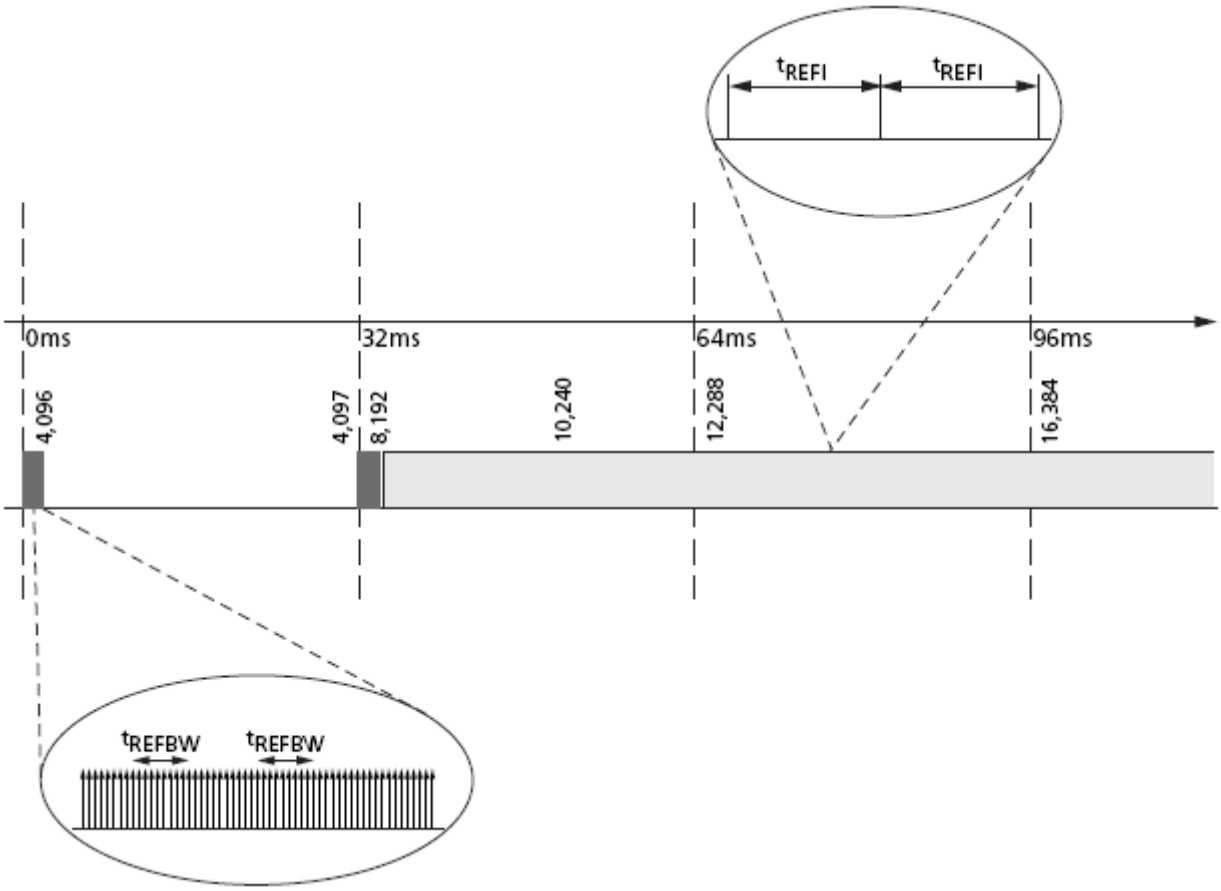
ISSI recommends entering self refresh mode immediately following the burst phase of a burst/pause refresh pattern; upon exiting self refresh, begin with the burst phase (see Figure of Recommended Self Refresh Entry and Exit).

Regular Distributed Refresh Pattern



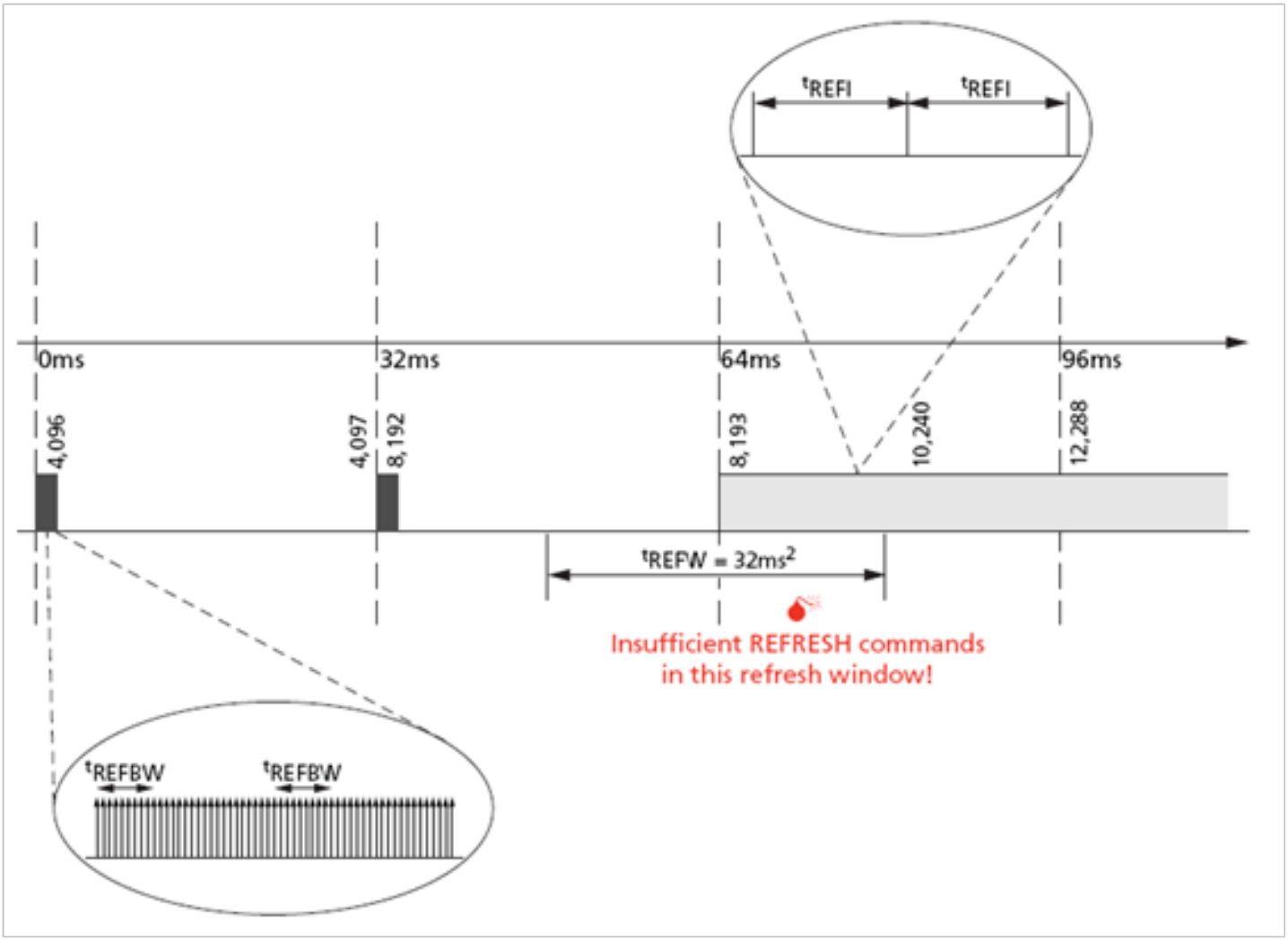
Notes:
1. Compared to repetitive burst REFRESH with subsequent REFRESH pause.
2. As an example, in a 512Mb LPDDR2 device at TC ≤ 85˚C, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 30ms without any REFRESH command.

Supported Transition from Repetitive REFRESH Burst



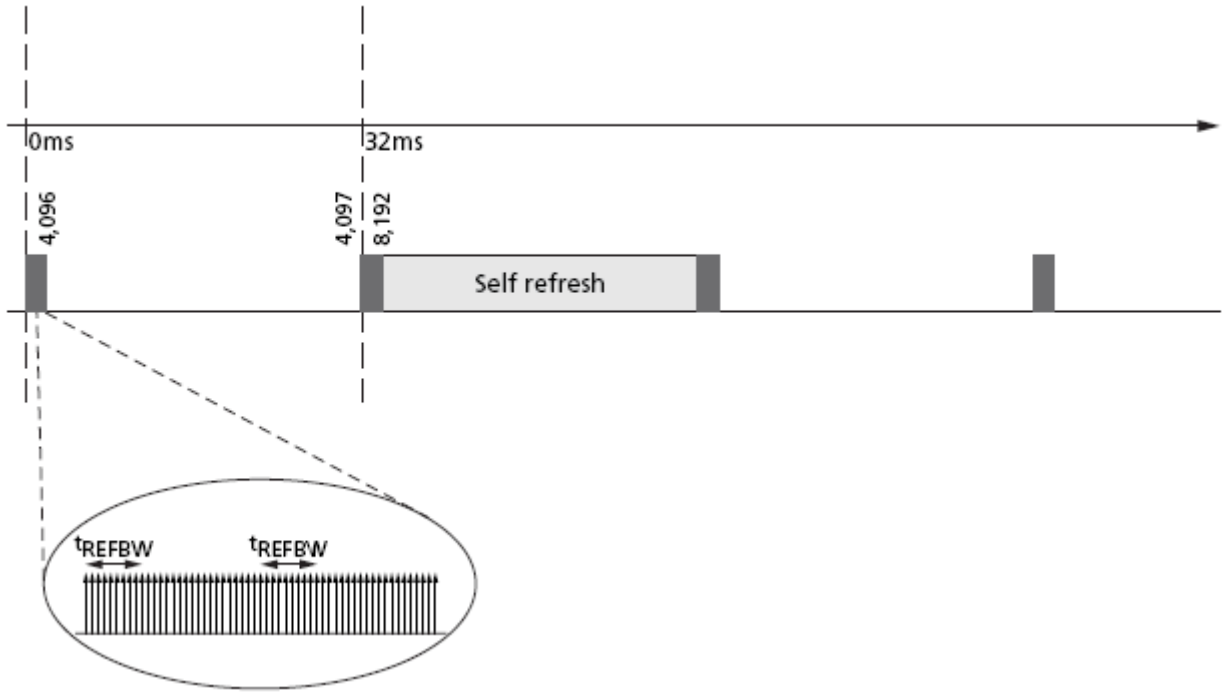
Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
2. As an example, in a 512Mb LPDDR2 device at TC ≤ 85˚C, the distributed refresh pattern has one REFRESH command per 7.8µs; the burst refresh pattern has one REFRESH command per 0.52µs, followed by ≈ 30ms without any REFRESH command

Nonsupported Transition from Repetitive REFRESH Burst



Notes:
1. Shown with subsequent REFRESH pause to regular distributed refresh pattern.
2. There are only ≈ 2048 REFRESH commands in the indicated tREFW window. This does not provide the required minimum number of REFRESH commands (R).

Recommended Self Refresh Entry and Exit



Note: In conjunction with a burst/pause refresh pattern

REFRESH Requirements

1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (tREFW = 32 ms @ MR4[2:0] = 011 or TC ≤ 85˚C). For actual values per density and the resulting average refresh interval (tREFI).

For tREFW and tREFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

For devices supporting per-bank REFRESH, a REFab command can be replaced by a full cycle of eight REFpb commands.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REFab commands can be issued in any rolling tREFBW (tREFBW = 4 × 8 × tRFCab). This condition does not apply if REFpb commands are used.

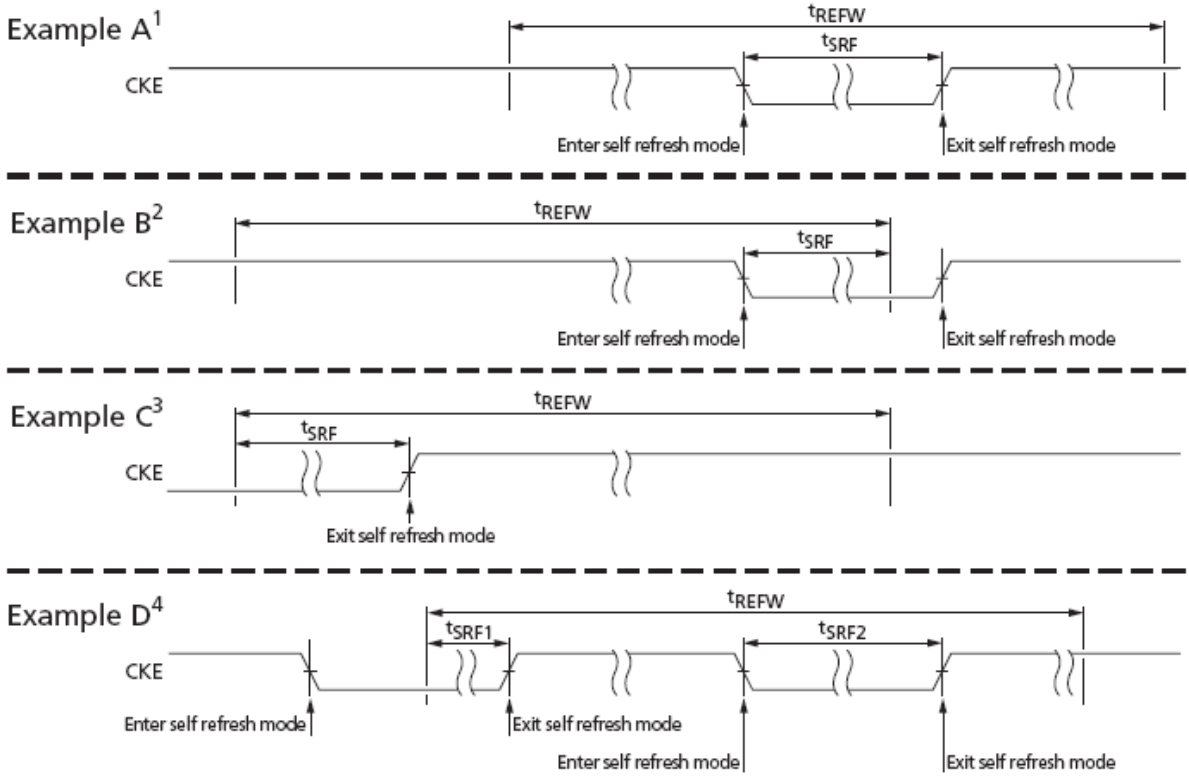
3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:

R' = RU tSRF / tREFI = R - RU × R x tSRF / tREFW

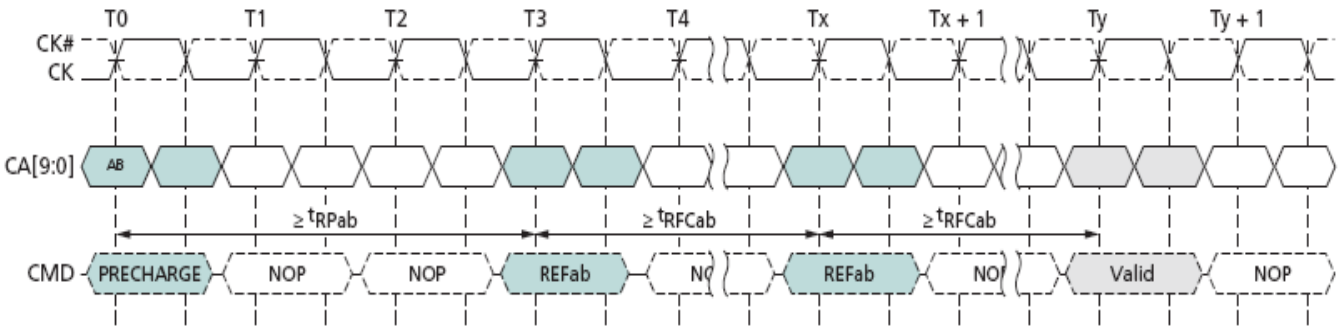
Where RU represents the round-up function.

tSRF Definition

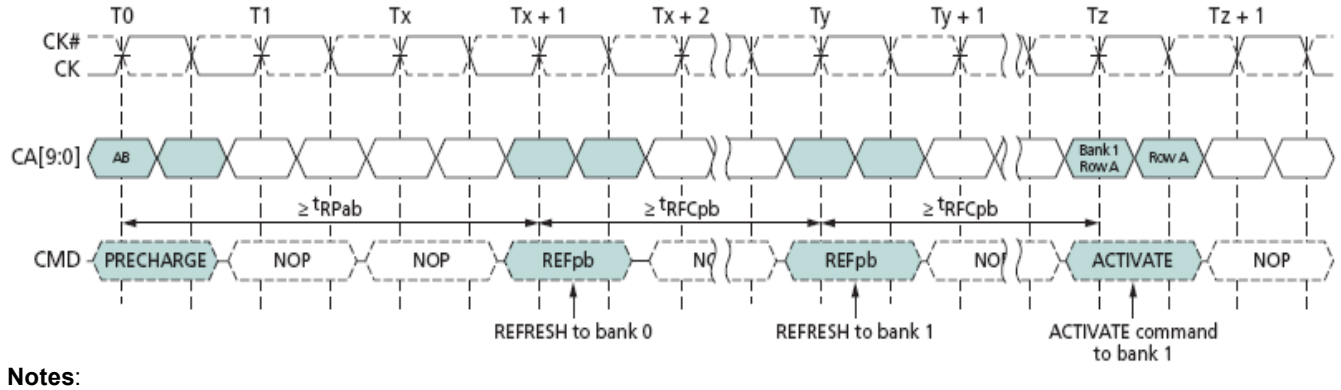


Notes:
1. Time in self refresh mode is fully enclosed in the refresh window (tREFW).
2. At self refresh entry.
3. At self refresh exit.
4. Several intervals in self refresh during one tREFW interval. In this example, tSRF = tSRF1 +tSRF2.

All-Bank REFRESH Operation



Per-Bank REFRESH Operation



Notes:
1. Prior to T0, the REFpb bank counter points to bank 0.
2. Operations to banks other than the bank being refreshed are supported during the tRFCpb period

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock.

CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. A NOP command must be driven in the clock cycle following the SELF REFRESH command.

After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode. LPDDR2-S4 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption

when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range.

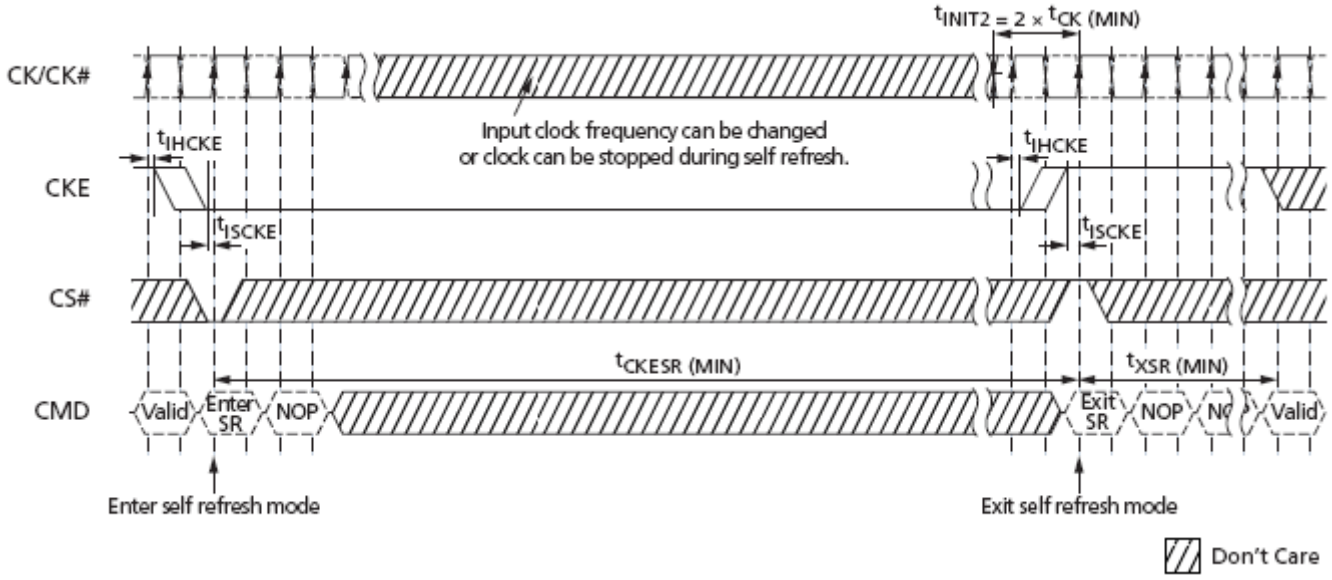
After the device has entered self refresh mode, all external signals other than CKE are“Don’t Care.” For proper self refresh operation, power supply pins (VDD1, VDD2, VDDQ, and VDDCA) must be at valid levels. VDDQ can be turned off during self refresh. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting self refresh, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges . VREFDQ can be at any level between 0 and VDDQ; VREFCA can be at any level between 0 and VDDCA during self refresh.

Before exiting self refresh, VREFDQ and VREFCA must be within specified limits (see AC and DC Logic Input Measurement Levels for Single-Ended Signals . After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during tCKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least tCKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.

Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (tXSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout tXSR, except during self refresh re-entry. NOP commands must be registered on each rising clock edge during tXSR.

Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command or eight per-bank commands) must be issued before issuing a subsequent SELF REFRESH command.

SELF REFRESH Operation



Notes:
1. Input clock frequency can be changed or stopped during self refresh, provided that upon exiting self-refresh, a minimum of two cycles of stable clocks (tINIT2) are provided, and the clock frequency is between the minimum and maximum frequencies for the particular speed grade.
2. The device must be in the all banks idle state prior to entering self refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command can be issued only after tXSR is satisfied. NOPs must be issued during tXSR.

Partial-Array Self Refresh – Bank Masking

Devices in densities of 64Mb–512Mb are comprised of four banks; densities of 1Gb and higher are comprised of eight banks. Each bank can be configured independently whether or not a SELF REFRESH operation will occur in that bank. One 8-bit mode register (accessible via the MRW command) is assigned to program the bank-masking status of each bank up to eight banks. For bank masking bit assignments, see the MR16 PASR Bank Mask (MA[7:0] = 010h) and MR16 Op-Code Bit Definitions tables.

The mask bit to the bank enables or disables a refresh operation of the entire memory space within the bank. If a bank is masked using the bank mask register, a REFRESH operation to the entire bank is blocked and bank data retention is not guaranteed in self refresh mode. To enable a REFRESH operation to a bank, the corresponding bank mask bit must be programmed as “unmasked.” When a bank mask bit is unmasked, the array space being refreshed within that bank is determined by the programmed status of the

segment mask bits.

Partial-Array Self Refresh – Segment Masking

Programming segment mask bits is similar to programming bank mask bits. For densities 1Gb and higher, eight segments are used for masking (see the MR17 PASR Segment Mask (MA[7:0] = 011h) and MR17 PASR Segment Mask Definitions tables). A mode register is used for programming segment mask bits up to eight bits. For densities less than 1Gb, segment masking is not supported.

When the mask bit to an address range (represented as a segment) is programmed as“masked,” a REFRESH operation to that segment is blocked. Conversely, when a segment mask bit to an address range is unmasked, refresh to that segment is enabled.

A segment masking scheme can be used in place of or in combination with a bank masking scheme. Each segment mask bit setting is applied across all banks. For segment masking bit assignments, see the tables noted above.

Bank and Segment Masking Example

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Bank Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0	–	M	–	–	–	–	–	M
Segment 1	0	–	M	–	–	–	–	–	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	–	M	–	–	–	–	–	M
Segment 4	0	–	M	–	–	–	–	–	M
Segment 5	0	–	M	–	–	–	–	–	M
Segment 6	0	–	M	–	–	–	–	–	M
Segment 7	1	M	M	M	M	M	M	M	M

Note: This table provides values for an 8-bank device with REFRESH operations masked to banks 1 and 7, and segments 2 and 7.

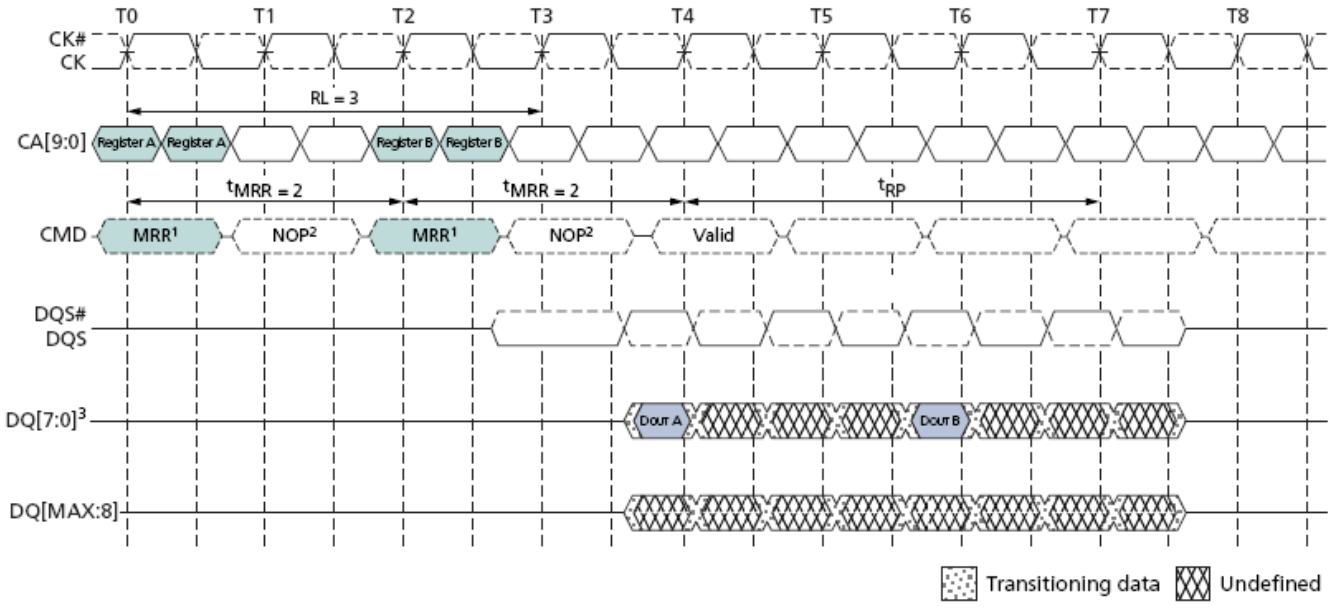
MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register

is selected by CA1f–CA0f and CA9r–CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × tCK + tDQSCK + tDQSQ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined

content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in Data Calibration Pattern Description. All DQS are toggled for the duration of the mode register READ burst. The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (tMRR) is two clock cycles.

MRR Timing – RL = 3, tMRR = 2

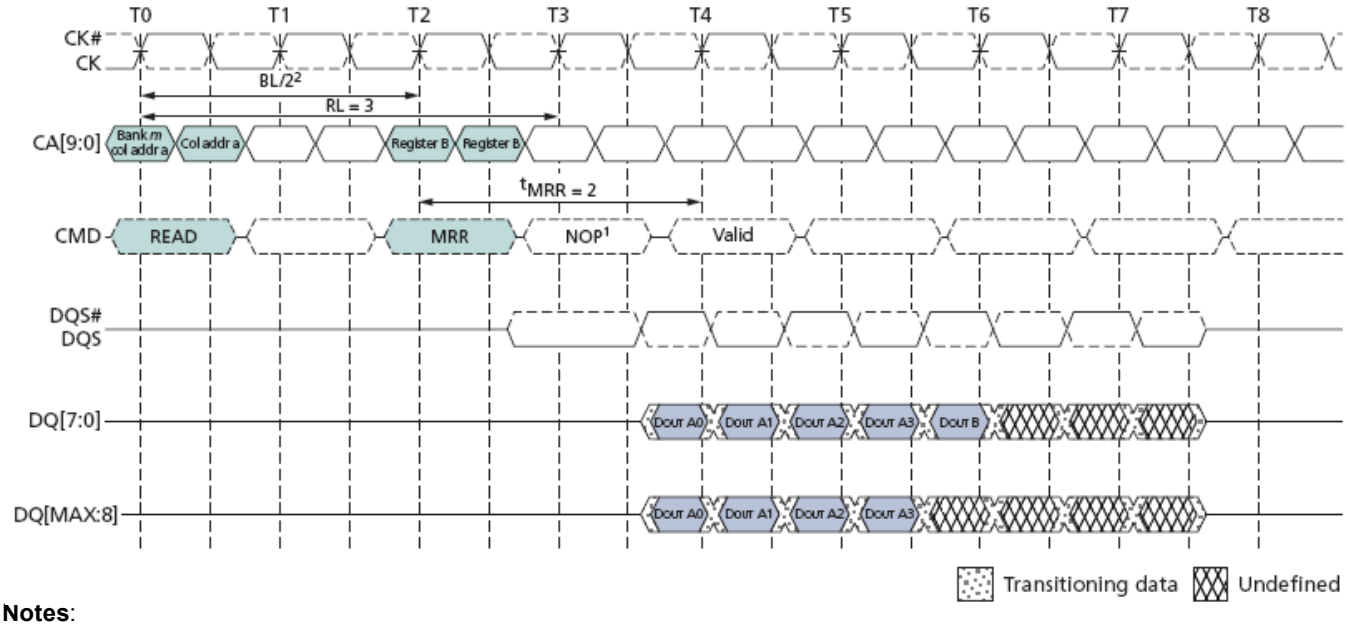


Notes:
1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ Calibration .
2. Only the NOP command is supported during tMRR.
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum MRR to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
5. Minimum MRR to MRW latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

READ bursts and WRITE bursts cannot be truncated by MRR. Following a READ command, the MRR command must not be issued before BL/2 clock cycles have completed.

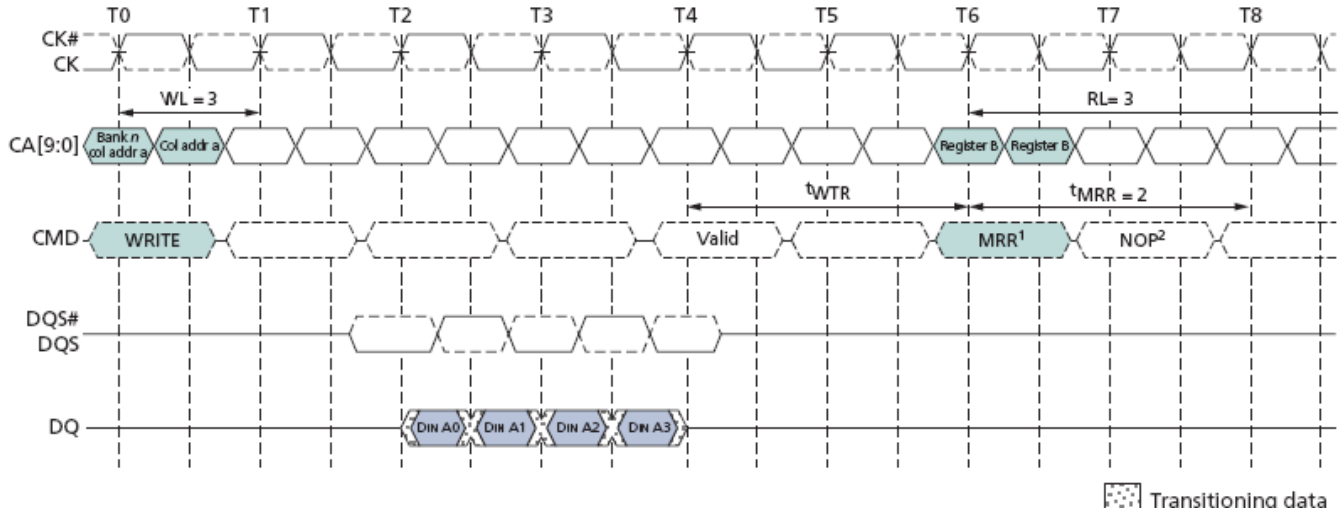
Following a WRITE command, the MRR command must not be issued before WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles have completed. If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for the BL value.

READ to MRR Timing – RL = 3, tMRR = 2



Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Only the NOP command is supported during tMRR.

Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4



Notes:
1. The minimum number of clock cycles from the burst WRITE command to the MRR command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. Only the NOP command is supported during tMRR.

Temperature Sensor

LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements

are being met (see Operating Temperature Range table). Temperature sensor data can be read from MR4 using the mode register read protocol.

Upon exiting self-refresh or power-down, the device temperature status bits will be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges (see table noted above). For example, TCASE could be above 85˚C when MR4[2:0] equals 011b.

To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.

Temperature Sensor Definitions and Operating Conditions

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	C/s	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	Time period between MR4 READs from the system.
Temperature Sensor Interval	^{t}TSI	Max	16	ms	Maximum delay between internal updates of MR4.
System Response Delay	SysRespDelay	Max	System Dependent	ms	Maximum response time from an MR4 READ to the system response.
Device Temperature Margin	TempMargin	Max	2	C	Margin above maximum temperature to support controller response.

LPDDR2 devices accommodate the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:

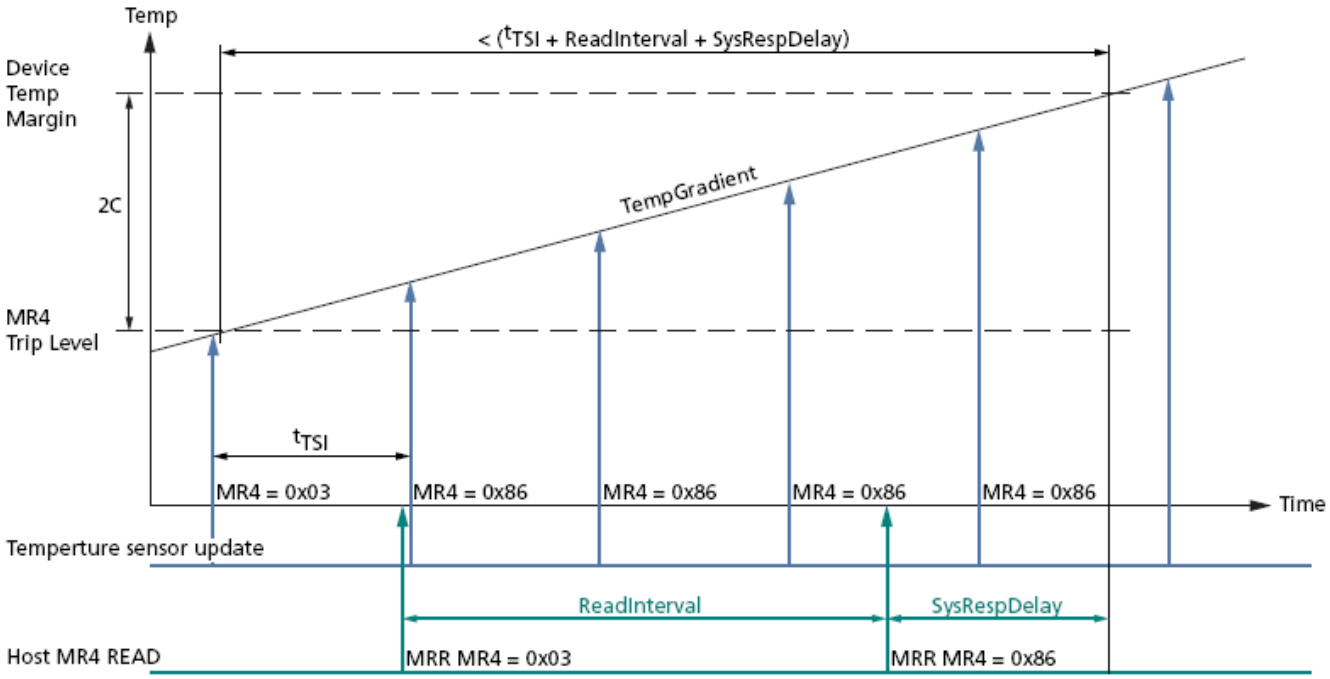
TempGradient × (ReadInterval + tTSI + SysRespDelay) ≤ 2°C

For example, if TempGradient is 10˚C/s and the SysRespDelay is 1ms:

10°C / s × (ReadInterval + 32ms + 1ms) ≤ 2°C

In this case, ReadInterval must not exceed 167ms

Temperature Sensor Timing

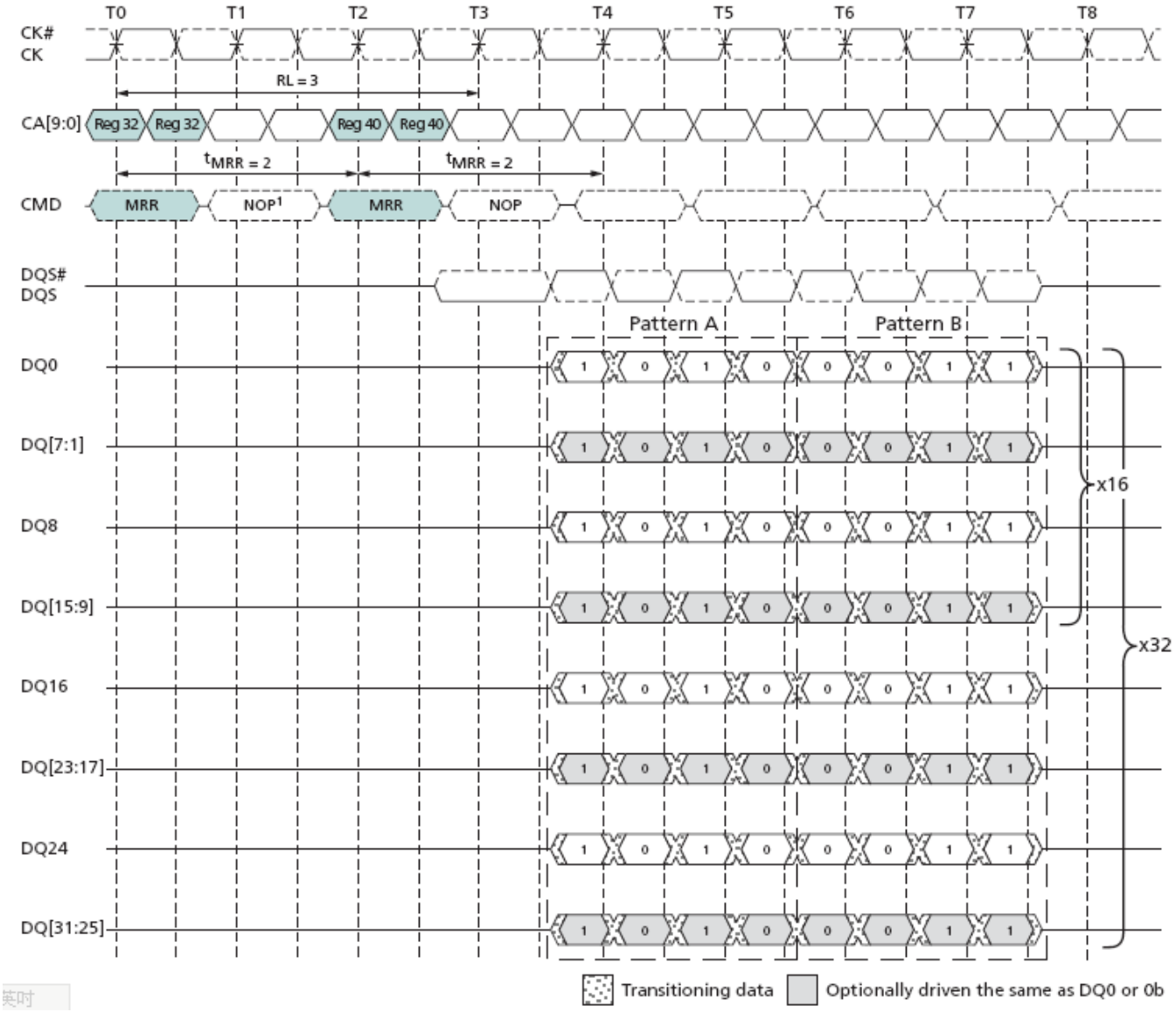


DQ Calibration

Mobile LPDDR2 devices feature a DQ calibration function that outputs one of two predefined system timing calibration patterns. For x16 devices, pattern A (MRR to MRR32), and pattern B (MRR to MRR40), will return the specified pattern on DQ0 and DQ8; x32 devices return the specified pattern on DQ0, DQ8, DQ16, and DQ24.

For x16 devices, DQ[7:1] and DQ[15:9] drive the same information as DQ0 during the MRR burst. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] drive the same information as DQ0 during the MRR burst. MRR DQ calibration commands can occur only in the idle state.

MR32 and MR40 DQ Calibration Timing – RL = 3, tMRR = 2



Note: Only the NOP command is supported during Tmrr

Data Calibration Pattern Description

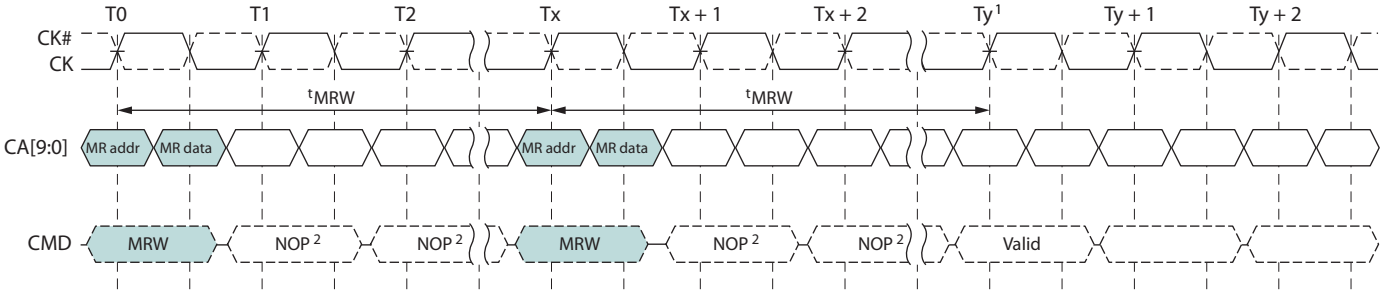
Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Notes
Pattern A	MR32	1	0	1	0	Reads to MR32 return DQ callibration pattern A
Pattern B	MR40	0	0	1	1	Reads to MR32 return DQ callibration pattern B

MODE REGISTER WRITE Command

The MODE REGISTER WRITE (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by

CA1f–CA0f, CA9r–CA4r. The data to be written to the mode register is contained in CA9f–CA2f. The MRW command period is defined by tMRW. MRWs to read-only registers have no impact on the functionality of the device. MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

MODE REGISTER WRITE Timing – RL = 3, tMRW = 5



Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All Banks idle	MRR	Mode Register Reading (All Banks idle)	All Banks idle
	MRW	Mode Register Writing (All Banks idle)	All Banks idle
	MRW (Reset)	Restting (Device Auto-Init)	All Banks idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) idle)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (Reset)	Not Allowed	Not Allowed

Notes:
1. At time Ty, the device is in the idle state.
2. Only the NOP command is supported during tMRW.

MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see RESET Command under Power-Up). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during tINIT4. After MRW RESET, boot timings must be observed until the

device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed.

For MRW RESET timing, see Figure of Voltage Ramp and Initialization Sequence.

MRW ZQ Calibration Commands

The MRW command is used to initiate a ZQ calibration command that calibrates output driver impedance across process, temperature, and voltage. LPDDR2-S4 devices support ZQ calibration. To achieve tighter tolerances, proper ZQ calibration must be performed.

There are four ZQ calibration commands and related timings: tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT is used for initialization calibration; tZQRESET is used for resetting ZQ to the default output impedance; tZQCL is used for long calibration(s); and tZQCS is used for short calibration(s). See the MR10 Calibration (MA[7:0] = 0Ah) table for ZQ calibration command code definitions.

ZQINIT must be performed for LPDDR2 devices. ZQINIT provides an output impedance accuracy of ±15%. After initialization, the ZQ calibration long (ZQCL) can be used to recalibrate the system to an output impedance accuracy of ±15%. A ZQ calibration short (ZQCS) can be used periodically to compensate for temperature and voltage drift in the system.

ZQRESET resets the output impedance calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to ±30% when ZQCS and ZQCL commands are not used.

One ZQCS command can effectively correct at least 1.5% (ZQ correction) of output impedance errors within tZQCS for all speed bins, assuming the maximum sensitivities specified in the tables "output Driver Sensitivity Definition" and "Output Driver Temperature and Voltage Sensitivity" (page 133) are met. The appropriate interval between ZQCS commands can be determined using these tables and system-specific parameters.

LPDDR2 devices are subject to temperature drift rate (Tdriftrate) and voltage drift rate (Vdriftrate) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula.

ZQcorrection / (Tsens × Tdriftrate) + (Vsens × Vdriftrate)

Where Tsens = MAX (dRONdT) and Vsens = MAX (dRONdV) define temperature and voltage

sensitivities.

For example, if Tsens = 0.75%/˚C, Vsens = 0.20%/mV, Tdriftrate = 1˚C/sec, and Vdriftrate =15 mV/sec, then the interval between ZQCS commands is calculated as:

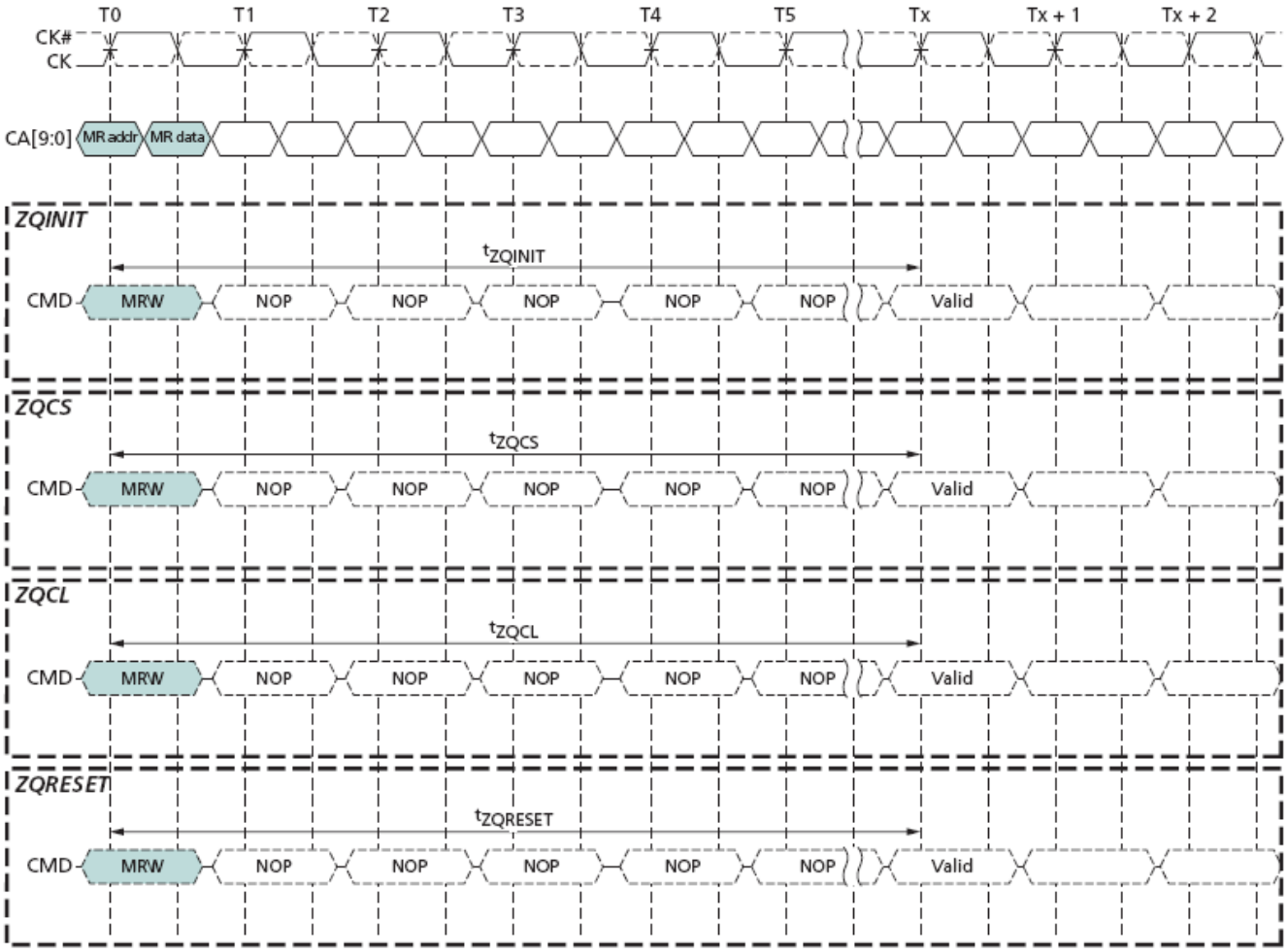
1.5 / (0.75 × 1) + (0.20 × 15) = 0.4s

A ZQ calibration command can only be issued when the device is in the idle state with all banks precharged.

No other activities can be performed on the data bus during calibration periods (tZQINIT, tZQCL, or tZQCS). The quiet time on the data bus helps to accurately calibrate output impedance. There is no required quiet time after the ZQRESET command. If multiple devices share a single ZQ resistor, only one device can be calibrating at any given time. After calibration is complete, the ZQ ball circuitry is disabled to reduce power consumption.

In systems sharing a ZQ resistor between devices, the controller must prevent tZQINIT, tZQCS, and tZQCL overlap between the devices. ZQRESET overlap is acceptable. If the ZQ resistor is absent from the system, ZQ must be connected to VDDCA. In this situation, the device must ignore ZQ calibration commands and the device will use the default calibration settings.

Z(



Notes:
1. Only the NOP command is supported during ZQ calibrations.
2. CKE must be registered HIGH continuously during the calibration period.
3. All devices connected to the DQ bus should be High-Z during the calibration process.

ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm (±1% tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited.

Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS# is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down;

if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

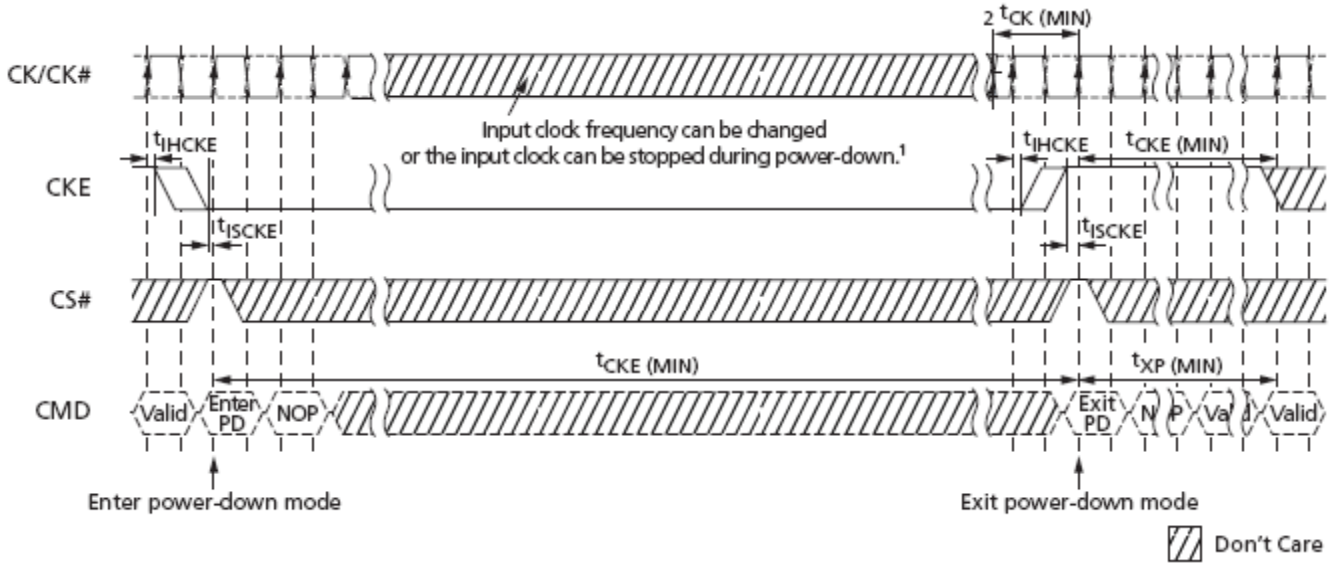
Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until tCKE is satisfied. VREFCA must be maintained at a valid level during power-down.

VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges (see AC and DC Operating Conditions).

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in REFRESH Command.

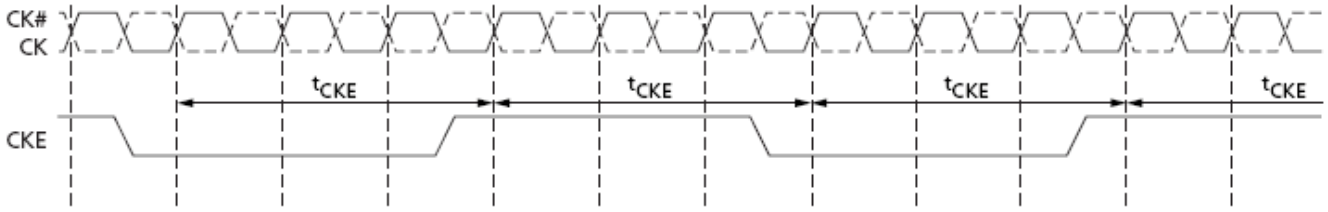
The power-down state is exited when CKE is registered HIGH. The controller must drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing section.

Power-Down Entry and Exit Timing

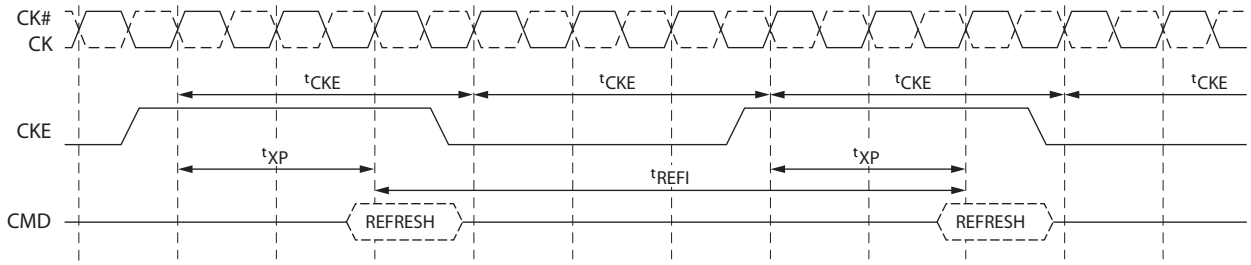


Note: Input clock frequency can be changed or the input clock stopped during power-down, provided that the clock frequency is between the minimum and maximum specified frequencies for the speed grade in use, and that prior to power-down exit, a minimum of two stable clocks complete.

CKE Intensive Environment

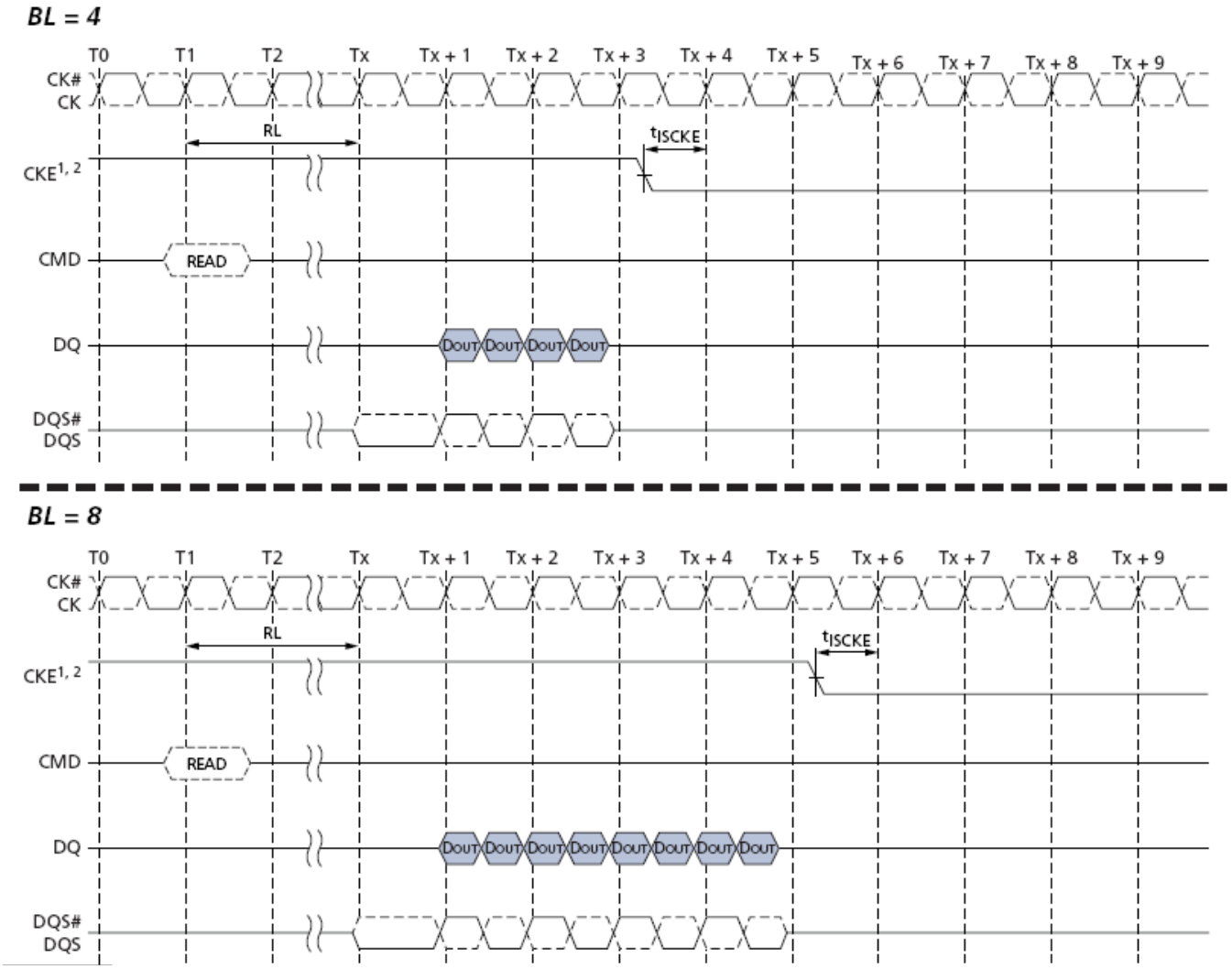


REFRESH-to-REFRESH Timing in CKE Intensive Environments



Note: The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

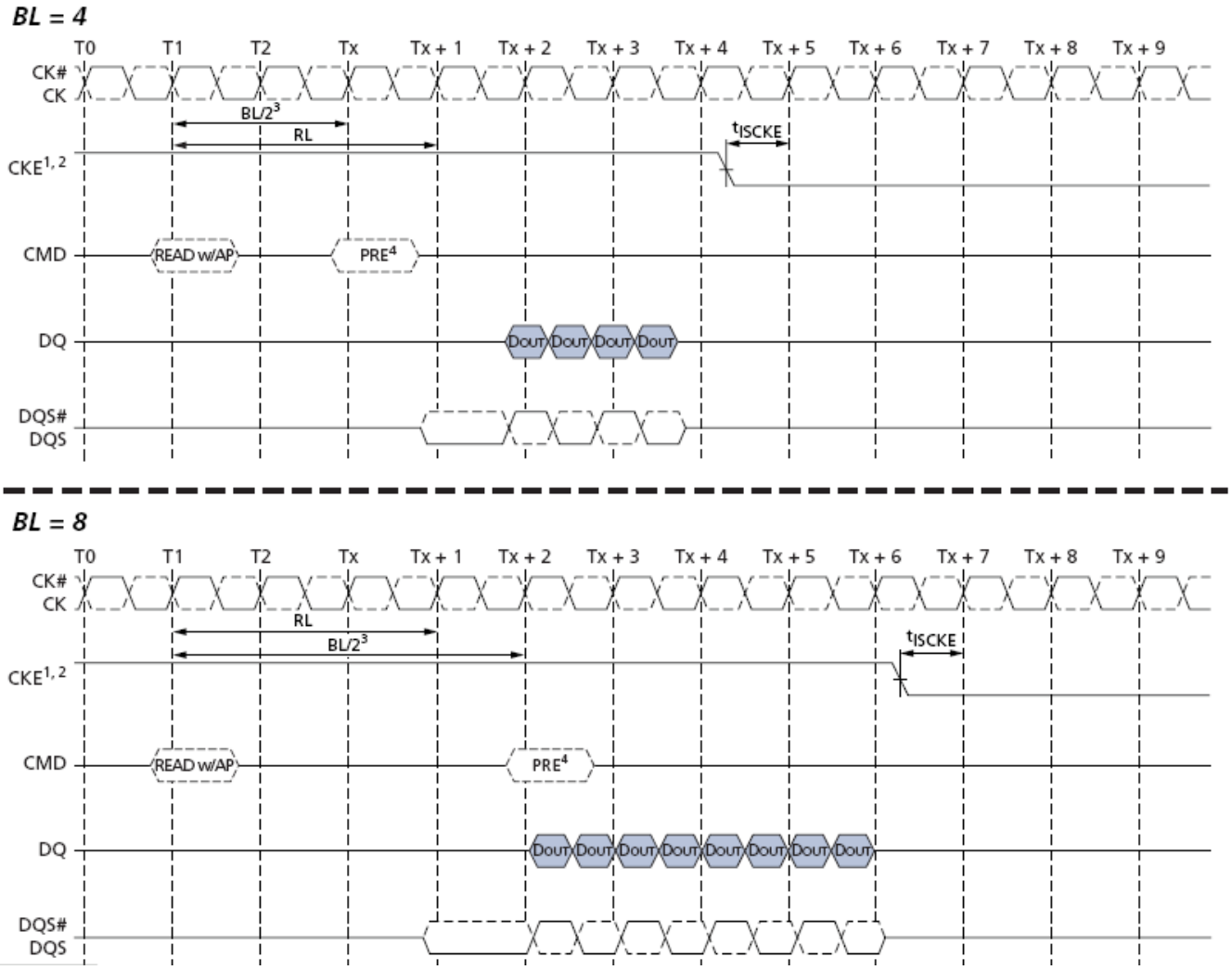
READ to Power-Down Entry



Read to Power-Down entry

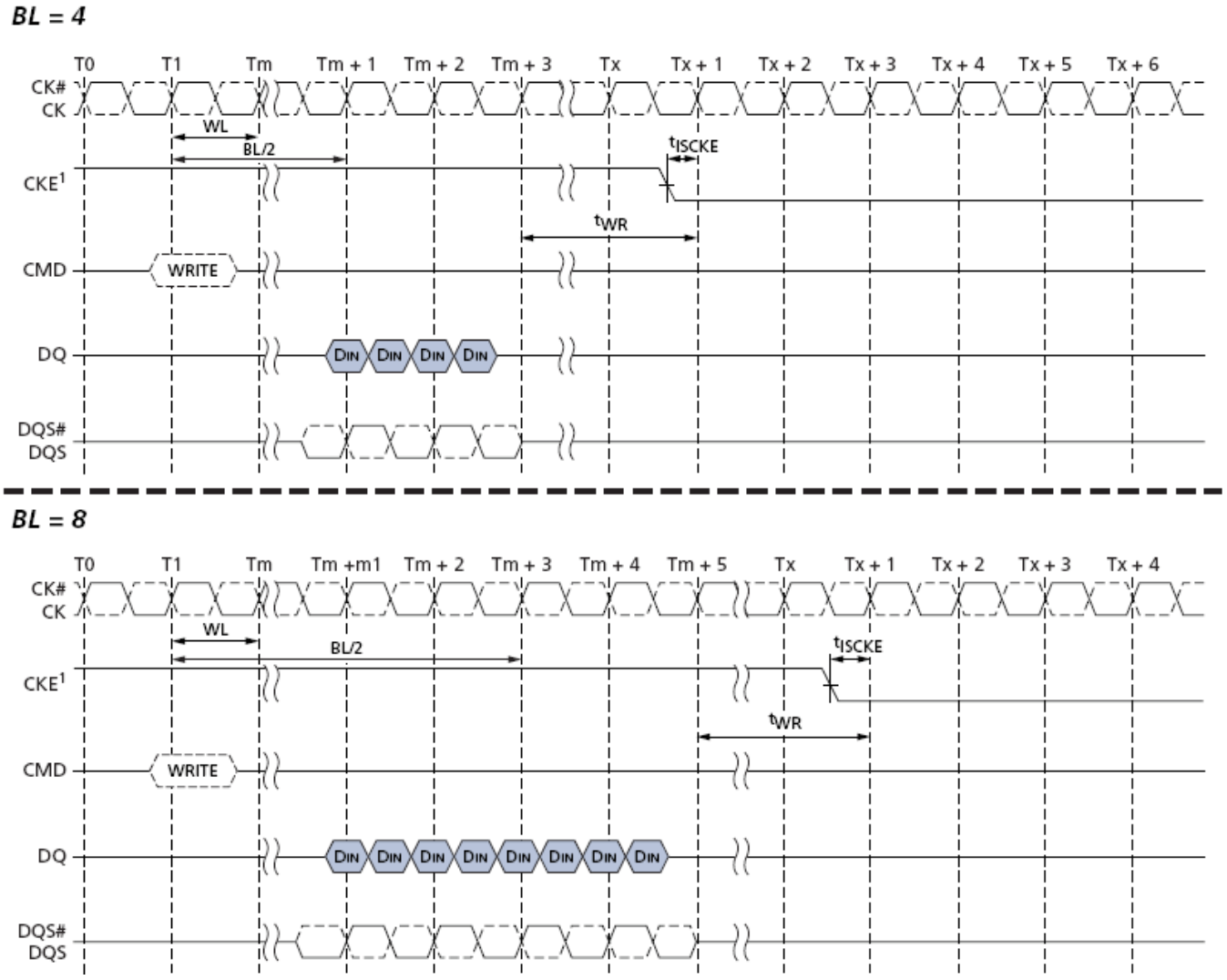
Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at (RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1) clock cycles after the clock on which the READ command is registered

READ with Auto Precharge to Power-Down Entry



Notes:
1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at (RL + RU(tDQSCK/tCK)+ BL/2 + 1) clock cycles after the clock on which the READ command is registered.
3. BL/2 with tRTP = 7.5ns and tRAS (MIN) is satisfied.
4. Start internal PRECHARGE

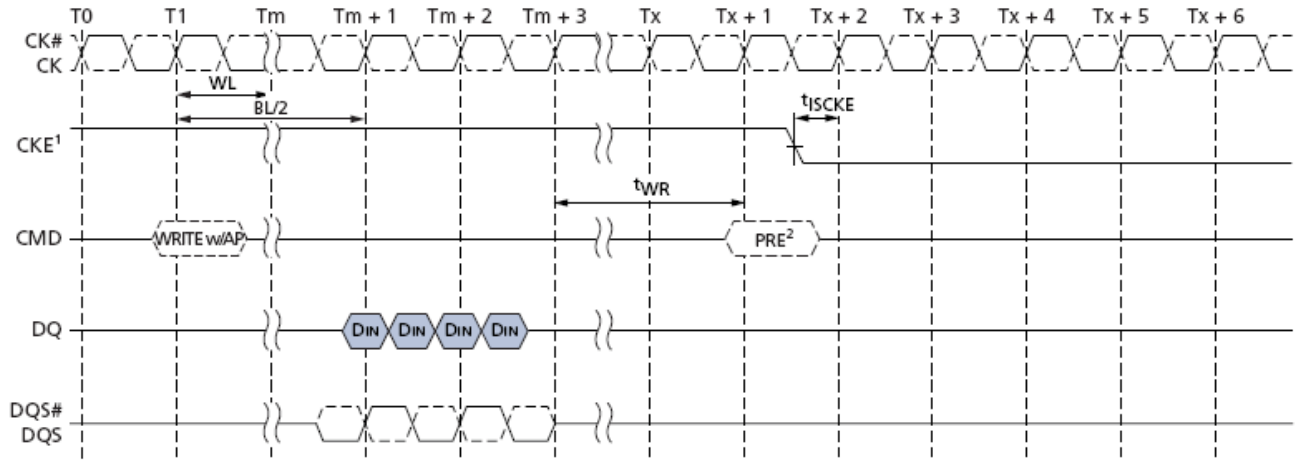
WRITE to Power-Down Entry



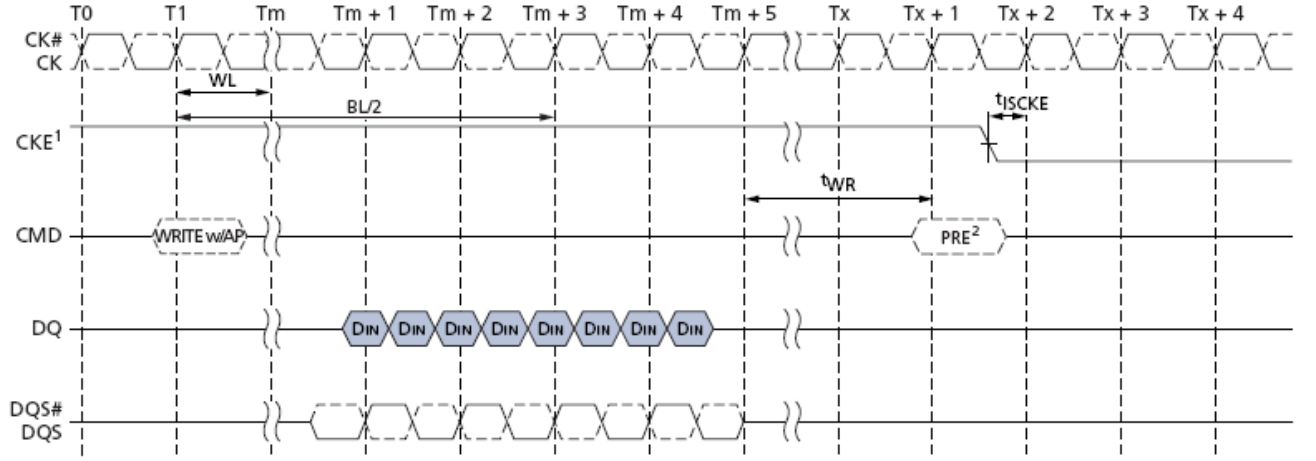
Note: CKE can be registered LOW at (WL + 1 + BL/2 + RU(tWR/tCK)) clock cycles after the clock on which the WRITE command is registered.

WRITE with Auto Precharge to Power-Down Entry

BL = 4

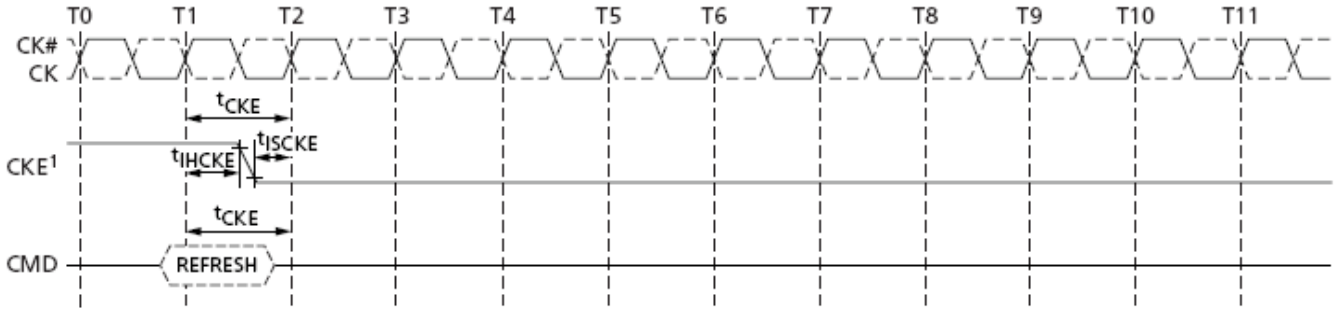


BL = 8



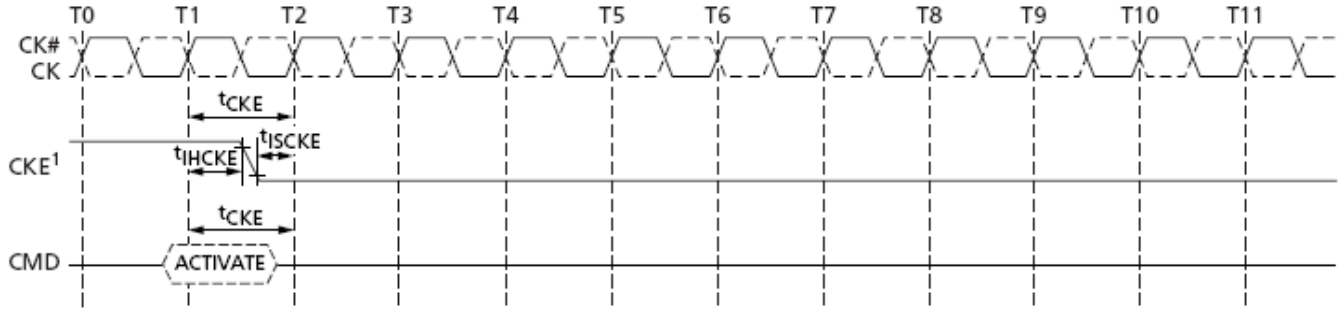
Notes:
1. CKE can be registered LOW at (WL + 1 + BL/2 + RU(tWR/tCK + 1) clock cycles after the WRITE command is registered.
2. Start internal PRECHARGE

REFRESH Command to Power-Down Entry



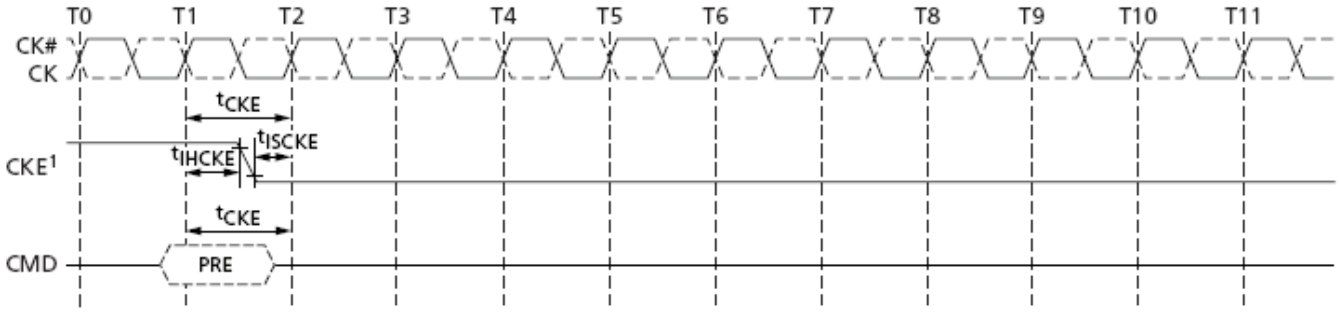
Note: CKE can go LOW tIHCKE after the clock on which the REFRESH command is registered.

ACTIVATE Command to Power-Down Entry



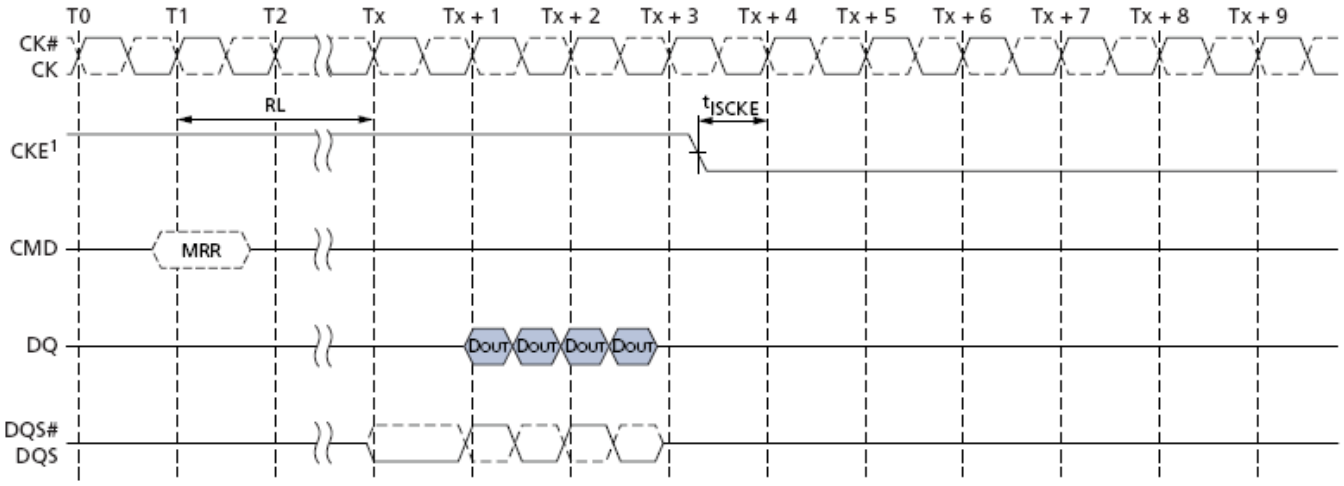
Note: CKE can go LOW at tIHCKE after the clock on which the ACTIVATE command is registered

PRECHARGE Command to Power-Down Entry



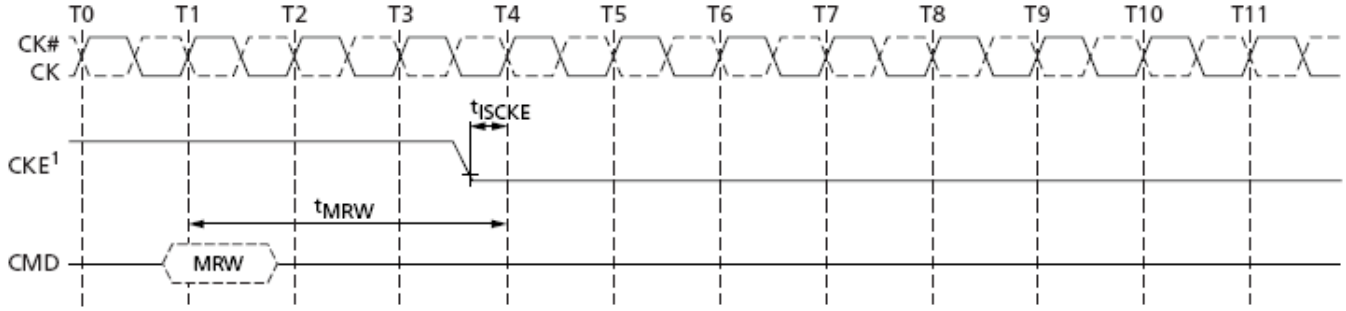
Note: CKE can go LOW tIHCKE after the clock on which the PRECHARGE command is registered.

MRR Command to Power-Down Entry



Note: CKE can be registered LOW at (RL + RU(tDQSCK/tCK)+ BL/2 + 1) clock cycles after the clock on which the MRR command is registered.

MRW Command to Power-Down Entry



Note: CKE can be registered LOW tMRW after the clock on which the MRW command is registered

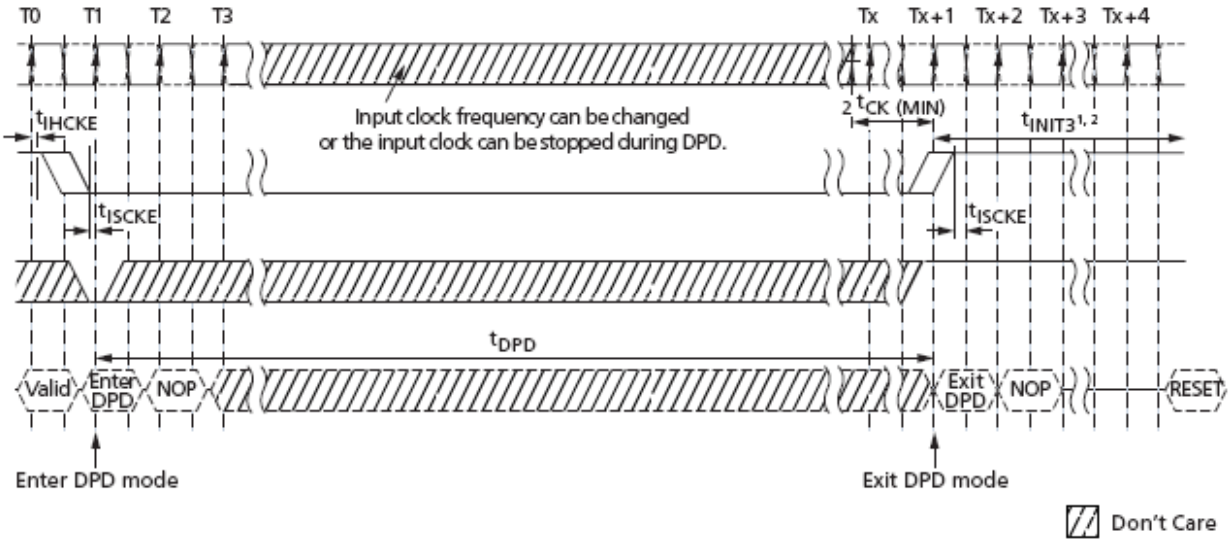
Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress, however, deep power-down IDD specifications will not be applied until those operations complete. The contents of the array will be lost upon entering DPD mode.

In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. VREFDQ can be at any level between 0 and VDDQ, and VREFCA can be at any level between 0 and VDDCA during DPD. All power supplies (including VREF) must be within the specified limits prior to exiting DPD (see AC and DC Operating Conditions).

To exit DPD, CKE must be HIGH, tISCKE must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

Deep Power-Down Entry and Exit Timing



Notes:
1. The initialization sequence can start at any time after Tx + 1.
2. tINIT3 and Tx + 1 refer to timings in the initialization sequence. For details, see Mode Register Definition

Input Clock Frequency Changes and Stop Events

LPDDR2 support Clock frequency changes and clock stop under the conditions detailed in this section

Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, Mobile LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab or REFpb commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,tRCD and tRP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, tCK(MIN) and tCK(MAX) must be met for each clock cycle.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

For clock stop, CK is held LOW and CK# is held HIGH.

NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has two possible encodings: CS# HIGH at the clock rising edge N; and CS# LOW with CA0, CA1, CA2 HIGH at the clock rising edge N.

The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle

Electrical Specifications

Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2,3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T_{STG}	-55	125	°C	5

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. See “Power-Ramp” section in “Power-up, Initialization, and Power-Off” for relationships between power supplies.
3. VREFDQ 0.6 x VDDQ; however, VREFDQ may be VDDQ provided that VREFDQ 300mV.
4. VREFCA 0.6 x VDDCA; however, VREFCA may be VDDCA provided that VREFCA 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

Thermal Resistance

Package	Theta-ja (Airflow = 0m/s)	Theta-jc	Units
134-ball	47.64	7.52	°C/W
168-ball	68.65	6.42	

Input/Output Capacitance

Parameter	Symbol	LPDDR2 1066-466		LPDDR2 400-200		Unit	Notes
		MIN	MAX	MIN	MAX		
Input capacitance, CK and CK#	C_{CK}	1.0	2.0	1.0	2.0	pF	2, 3
Input capacitance delta, CK and CK#	C_{DCK}	0	0.20	0	0.25	pF	2, 3, 4
Input capacitance, all other input-only pins	C_I	1.0	2.0	1.0	2.0	pF	2, 3, 5
Input capacitance delta, all other input-only pins	C_{DI}	–0.40	+0.40	–0.50	+0.50	pF	2, 3, 6
Input/output capacitance, DQ, DM, DQS, DQS#	C_{IO}	1.25	2.5	1.25	2.5	pF	2, 3, 7, 8
Input/output capacitance delta, DQS, DQS#	C_{DDQS}	0	0.25	0	0.30	pF	2, 3, 8, 9
Input/output capacitance delta, DQ, DM	C_{DIO}	–0.5	+0.5	–0.6	+0.6	pF	2, 3, 8, 10

Notes:
1. TC –25˚C to +105˚C; VDDQ = 1.14–1.3V; VDDCA = 1.14–1.3V; VDD1 = 1.7–1.95V; VDD2 = 1.14–1.3V).
2. This parameter applies to die devices only (does not include package capacitance).
3. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to
JEP147 (procedure for measuring input capacitance using a vector network analyzer), with VDD1, VDD2, VDDQ, VSS, VSSCA, and
VSSQ applied; all other pins are left floating.
4. Absolute value of CCK - CCK#.
5. CI applies to CS#, CKE, and CA[9:0].
6. CDI = CI - 0.5 × (CCK + CCK#).
7. DM loading matches DQ and DQS.
8. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).
9. Absolute value of CDQS and CDQS#.
10. CDIO = CIO - 0.5 × (CDQS + CDQS#) in byte-lane.
11. Maximum external load capacitance on ZQ pin: 5pF.

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.3	Core Power2	V
VDDCA	1.14	1.20	1.3	Input Buffer Power	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 VDD1 uses significantly less power than VDD2

Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current For CA, CKE, CS#, CK, CK# Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	I_L	-2	2	uA	2
V_{REF} supply leakage current V_{REFDQ} = VDDQ/2 or V_{REFCA} = VDDCA/2 (All other pins not under test = 0V)	I_{VREF}	-1	1	uA	1

Notes:
1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS/DQS# output leakage specification.

Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Commercial	T_{OPER}	0	85	°C
Industrial		-40	85	
Automotive, A1		-40	85	
Automotive, A2		-40	105	

Notes:
1. Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard. Operation outside the range is not permitted.
2. Some applications require operation of LPDDR2 in the maximum temperature conditons in the Extended Temperature Range between 85°C and 105°C case temperature. For LPDDR2 devices, some derating is neccessary to operate in this range. See MR4 and section on Temperature Sensor.
3. Either the device case temperature rating or the temperature sensor (See “Temperature Sensor”) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature.
4. Operation below 85°C is in the Standard Temperature Range.

AC and DC Input Levels for Single-Ended CA and CS# Signals

Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
V_{IHCA}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2
V_{ILCA}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2
V_{IHCA}(DC)	DC input logic high	Vref + 0.130	VDDCA	Vref + 0.200	VDDCA	V	1
V_{ILCA}(DC)	DC input logic low	VSSCA	Vref - 0.130	VSSCA	Vref - 0.200	V	1
V_{RefCA}(DC)	Reference Voltage for CA and CS# inputs	0.49 * VDDCA	0.51 * VDDCA	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

Notes:
1. For CA and CS# input only pins. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications”
3. The ac peak noise on VRefCA may not allow VRefCA to deviate from VRefCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDCA/2 +/- 12 mV.

AC and DC Input Levels for CKE

Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Notes
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1

Note:
1. See “Overshoot and Undershoot Specifications”

AC and DC Input Levels for Single-Ended Data Signals

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2, 5
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2, 5
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	Vref + 0.200	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	VSSQ	Vref - 0.200	V	1
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

Notes:
1. For DQ input only pins. Vref = VrefDQ(DC).
2. See “Overshoot and Undershoot Specifications”
3. The ac peak noise on VRefDQ may not allow VRefDQ to deviate from VRefDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12 mV).
4. For reference: approx. VDDQ/2 +/- 12 mV.

LPDDR2-S4 Refresh Requirement Parameters

Parameter		Symbol	256Mb	Unit
Number of Banks			4	
Refresh Window Tcase ≤ 85°C		tREFW	32	ms
Refresh Window 85°C < Tcase ≤ 105°C		tREFW	8	ms
Required number of REFRESH commands (min)		R	4096	
Average time between REFRESH commands (for reference only) Tcase ≤ 85°C"	REFab	tREFI	7.8	us
	REFpb	tREFIpb	Not permitted	
Refresh Cycle time		tRFCab	90	ns
Per Bank Refresh Cycle time		tRFCpb	N/A	ns
Burst Refresh Window = (4 x 8 x tRFCab)		tREFBW	2.88	us

AC TIMINGS

LPDDR2 AC Timing Table (1,2)

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
Max. Frequency		~		533	466	400	333	266	233	200	166	133	100	MHz
Clock Timing														
Average Clock Period	t_{CK}(avg)	min				2.5	3	3.75	4.3	5	6	7.5	10	ns
		max		100										
Average high pulse width	t_{CH}(avg)	min		0.45										t_{CK}(avg)
		max		0.55										
Average low pulse width	t_{CL}(avg)	min		0.45										t_{CK}(avg)
		max		0.55										
Absolute Clock Period	t_{CK}(abs)	min		t_{CK}(avg)min + t_{JIT}(per),min										ps
Absolute clock HIGH pulse width (with allowed jitter)	t_{CH}(abs), allowed	min		0.43										t_{CK}(avg)
		max		0.57										t_{CK}(avg)
Absolute clock LOW pulse width (with allowed jitter)	t_{CL}(abs), allowed	min		0.43										t_{CK}(avg)
		max		0.57										t_{CK}(avg)
Clock Period Jitter (with allowed jitter)	t_{JIT}(per), allowed	min		-90	-95	-100	-110	-120	-130	-140	-150	-180	-250	ps
		max		90	95	100	110	120	130	140	150	180	250	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t_{JIT}(cc), allowed	max		180	190	200	220	240	260	280	300	360	500	ps
Duty cycle Jitter (with allowed jitter)	t_{JIT}(duty), allowed	min		min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) * t_{CK}(avg)										ps
		max		max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) * t_{CK}(avg)										ps
Cumulative error across 2 cycles	t_{ERR}(2per), allowed	min		-132	-140	-147	-162	-177	-191	-206	-221	-265	-368	ps
		max		132	140	147	162	177	191	206	221	265	368	
Cumulative error across 3 cycles	t_{ERR}(3per), allowed	min		-157	-166	-175	-192	-210	-227	-245	-262	-314	-437	ps
		max		157	166	175	192	210	227	245	262	314	437	
Cumulative error across 4 cycles	t_{ERR}(4per), allowed	min		-175	-185	-194	-214	-233	-253	-272	-291	-350	-486	ps
		max		175	185	194	214	233	253	272	291	350	486	
Cumulative error across 5 cycles	t_{ERR}(5per), allowed	min		-188	-199	-209	-230	-251	-272	-293	-314	-377	-524	ps
		max		188	199	209	230	251	272	293	314	377	524	
Cumulative error across 6 cycles	t_{ERR}(6per), allowed	min		-200	-211	-222	-244	-266	-288	-311	-333	-399	-555	ps
		max		200	211	222	244	266	288	311	333	399	555	
Cumulative error across 7 cycles	t_{ERR}(7per), allowed	min		-209	-221	-232	-256	-279	-302	-325	-348	-418	-581	ps
		max		209	221	232	256	279	302	325	348	418	581	

LPDDR2 AC Timing Table (1,2)

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
Cumulative error across 8 cycles	t_{ERR}(8per), allowed	min		-217	-229	-214	-266	-290	-314	-338	-362	-435	-604	ps
		max		217	229	214	266	290	314	338	362	435	604	
Cumulative error across 9 cycles	t_{ERR}(9per), allowed	min		-224	-237	-249	-274	-299	-324	-349	-374	-449	-624	ps
		max		224	237	249	274	299	324	349	374	449	624	
Cumulative error across 10 cycles	t_{ERR}(10per), allowed	min		-231	-244	-257	-282	-308	-334	-359	-385	-462	-641	ps
		max		231	244	257	282	308	334	359	385	462	641	
Cumulative error across 11 cycles	t_{ERR}(11per), allowed	min		-237	-250	-263	-289	-316	-342	-368	-395	-474	-658	ps
		max		237	250	263	289	316	342	368	395	474	658	
Cumulative error across 12 cycles	t_{ERR}(12per), allowed	min		-242	-256	-269	-296	-323	-350	-377	-403	-484	-672	ps
		max		242	256	269	296	323	350	377	403	484	672	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	t_{ERR}(nper), allowed	min		t_{ERR}(nper),allowed,min = (1 + 0.68ln(n)) * t_{JIT}(per),allowed,min										ps
		max		t_{ERR}(nper),allowed,max = (1 + 0.68ln(n)) * t_{JIT}(per),allowed,max										

LPDDR2 AC Timing Table (1,2)

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
ZQ Calibration Parameters														
Initialization Calibration Time	t_{ZQINIT}	min		1										us
Long Calibration Time	t_{ZQCL}	min	6	360										ns
Short Calibration Time	t_{ZQCS}	min	6	90										ns
Calibration Reset Time	$t_{ZQRESET}$	min	3	50										ns
Read Parameters (3)														
DQS output access time from CK/CK#	t_{DQSCK}	min		2500										ps
		max		5500										
DQSCK Delta Short(4)	$t_{DQSCKDS}$	max		330	380	450	540	670	770	900	1080	1350	1800	ps
DQSCK Delta Medium(5)	$t_{DQSCKDM}$	max		680	780	900	1050	1350	1550	1800	1900	2000	2100	ps
DQSCK Delta Long(6)	$t_{DQSCKDL}$	max		920	1050	1200	1400	1800	2100	2400	-	-	-	ps
DQS - DQ skew	t_{DQSQ}	max		200	220	240	280	340	370	400	500	600	700	ps
Data hold skew factor	t_{QHS}	max		230	260	280	340	400	450	480	600	750	1000	ps
DQS Output High Pulse Width	t_{QSH}	min		t_{CH}(abs) - 0.05										t_{CK}(avg)
DQS Output Low Pulse Width	t_{QSL}	min		t_{CL}(abs) - 0.05										t_{CK}(avg)
Data Half Period	t_{QHP}	min		min(t_{QSH}, t_{QSL})										t_{CK}(avg)
DQ / DQS output hold time from DQS	t_{QH}	min		t_{QHP} - t_{QHS}										ps
Read preamble(8)	t_{RPRE}	min		0.9										t_{CK}(avg)
Read postamble(9)	t_{RPST}	min		t_{CL}(abs) - 0.05										t_{CK}(avg)
DQS low-Z from clock(7)	$t_{LZ(DQS)}$	min		$t_{DQSCK(MIN)}$ - 300										ps
DQ low-Z from clock(7)	$t_{LZ(DQ)}$	min		$t_{DQSCK(MIN)}$ - (1.4 * $t_{QHS(MAX)}$)										ps
DQS high-Z from clock(7)	$t_{HZ(DQS)}$	max		$t_{DQSCK(MAX)}$ - 100										ps
DQ high-Z from clock(7)	$t_{HZ(DQ)}$	max		$t_{DQSCK(MAX)}$ + (1.4 * $t_{DQSQ(MAX)}$)										ps

LPDDR2 AC Timing Table (1,2)

Paramete	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
Write Parameters (3)														
DQ and DM input hold time (Vref based)	t_{DH}	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input setup time (Vref based)	t_{DS}	min		210	235	270	350	430	450	480	600	750	1000	ps
DQ and DM input pulse width	t_{DIPW}	min		0.35										t_{CK}(avg)
Write command to 1st DQS latching transition	t_{DQSS}	min		0.75										t_{CK}(avg)
		max		1.25										
DQS input high-level width	t_{DQSH}	min		0.4										t_{CK}(avg)
DQS input low-level width	t_{DQSL}	min		0.4										t_{CK}(avg)
DQS falling edge to CK setup time	t_{DSS}	min		0.2										t_{CK}(avg)
DQS falling edge hold time from CK	t_{DSH}	min		0.2										t_{CK}(avg)
Write postamble	t_{WPST}	min		0.4										t_{CK}(avg)
Write preamble	t_{WPRE}	min		0.35										t_{CK}(avg)

LPDDR2 AC Timing Table [1,2]

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
CKE Input Parameters														
CKE min. pulse width (high and low pulse width)	t_{CKE}	min	3	3										t_{CK}(avg)
CKE input setup time	t_{ISCKE}(10)	min		0.25										t_{CK}(avg)
CKE input hold time	t_{IHCKE}(11)	min		0.25										t_{CK}(avg)
Command Address Input Parameters [3]														
Address and control input setup time (Vref based)	t_{IS} [12]	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input hold time (Vref based)	t_{IH} [12]	min		220	250	290	370	460	520	600	740	900	1150	ps
Address and control input pulse width	t_{IPW}	min		0.40										t_{CK}(avg)
Boot Parameters (10 MHz - 55 MHz) [13,14,15]														
Clock Cycle Time	t_{CKb}	max	-	100										ns
		min		81										
CKE Input Setup Time	t_{ISCKEb}	min	-	2.5										ns
CKE Input Hold Time	t_{IHCKEb}	min	-	2.5										ns
Address & Control Input Setup Time	t_{ISb}	min	-	1150										ps
Address & Control Input Hold Time	t_{IHb}	min	-	1150										ps
DQS Output Data Access Time from CK/CK#	t_{DQSCKb}	min	-	2.0										ns
		max		10.0										
Data Strobe Edge to Ouput Data Edge t_{DQSQb} - 1.2	t_{DQSQb}	max	-	1.2										ns
Data Hold Skew Factor	t_{QHSb}	max	-	1.2										ns
Mode Register Parameters														
MODE REGISTER Write command period	t_{MRW}	min	5	5										t_{CK}(avg)
Mode Register Read command period	t_{MRR}	min	2	2										t_{CK}(avg)

LPDDR2 AC Timing Table (1,2)

Parameter	Symbol	min max	min t_{CK}	LPDDR2										Unit
				1066	933	800	667	533	466	400	333	266	200	
LPDDR2 SDRAM Core Parameters (16)														
Read Latency	RL	min	3	8	7	6	5	4		3	3			t_{CK}(avg)
Write Latency	WL	min	1	4	4	3	2	2		1	1			t_{CK}(avg)
ACTIVE to ACTIVE command period (18)	t_{RC}	min		t_{RAS} + t_{RPab} (with all-bank Precharge) t_{RAS} + t_{RPpb} (with per-bank Precharge)										ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	t_{CKESR}	min	3	15						15				ns
Self refresh exit to next valid command delay	t_{XSR}	min	2	t_{RFCab} + 10										ns
Exit power down to next valid command delay	t_{XP}	min	2	7.5						7.5				ns
LPDDR2-S4 CAS to CAS delay	t_{CCD}	min	2	2						2				t_{CK}(avg)
Internal Read to Precharge command delay	t_{RTP}	min	2	7.5						7.5				ns
RAS to CAS Delay(19)	t_{RCD}	Fast (min)	3	15						15				ns
		Typ (min)	3	18						18				ns
Row Precharge Time(19) (single bank)	t_{RPpb}	Fast (min)	3	15						15				ns
		Typ (min)	3	18						18				ns
Row Precharge Time(19) (all banks)	t_{RPab} 4-bank	Fast (min)	3	15						15				ns
		Typ (min)	3	18						18				ns
Row Active Time	t_{RAS}	min	3	42						42				ns
		max	-	70						70				us
Write Recovery Time	t_{WR}	min	3	15						15				ns
Internal Write to Read Command Delay	t_{WTR}	min	2	7.5						10				ns
Active bank A to Active bank B	t_{RRD}	min	2	10						10				ns
Four Bank Activate Window	t_{FAW}	min	8	50						50	60			ns
Minimum Deep Power Down Time	t_{DPD}	min		500						500				us

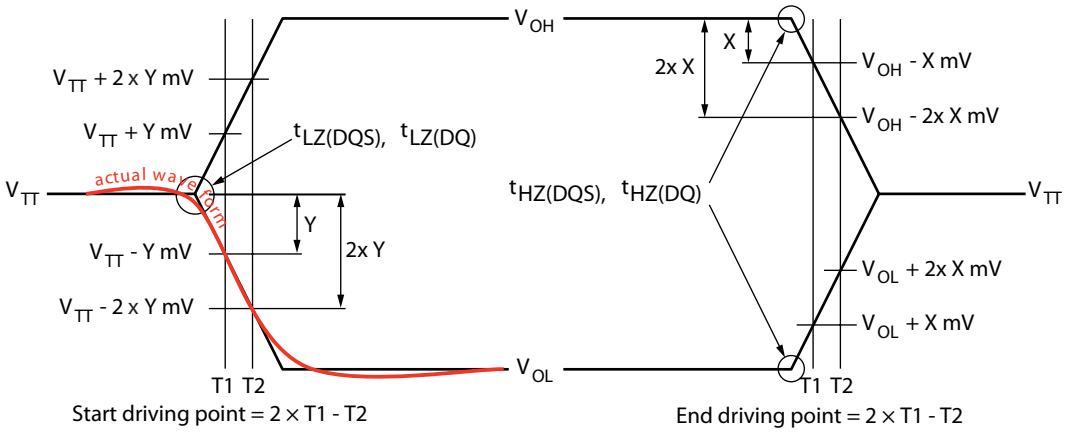
Table 103 — LPDDR2 AC Timing Table

Parameter	Symbol	min max	min t_{CK}	LPDDR2									Unit
				1066	933	800	667	533	466	400	333	266	200	
LPDDR2 Temperature De-Rating[17]														
t_{DQSCK} De-Rating	t_{DQSCK} (Derated)	max		5620	6000									ps
Core Timings Temperature De-Rating	t_{RCD} (Derated)	min		t_{RCD} + 1.875										ns
	t_{RC} (Derated)	min		t_{RC} + 1.875										ns
	t_{RAS} (Derated)	min		t_{RAS} + 1.875										ns
	t_{RP} (Derated)	min		t_{RP} + 1.875										ns
	t_{RRD} (Derated)	min		t_{RRD} + 1.875										ns

Notes:
1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to VREF.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
7. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS, DQS#.

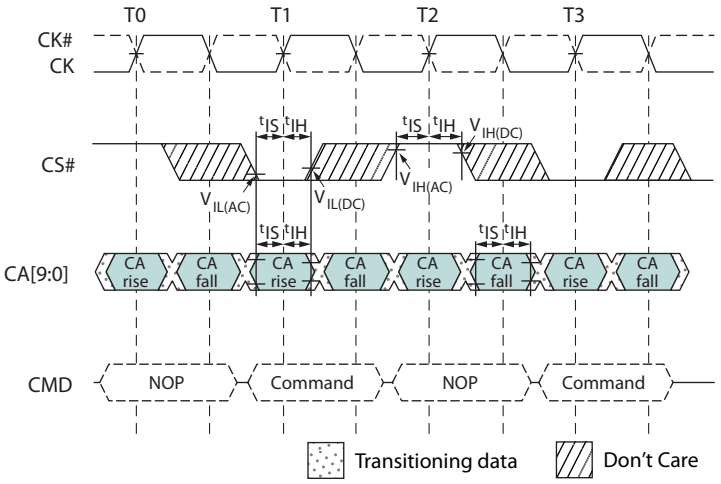
Output Transition Timing

(Note #7)



8. Measured from the point when DQS, DQS# begins driving the signal to the point when DQS, DQS# begins driving the first rising strobe edge.
9. Measured from the last falling strobe edge of DQS, DQS# to the point when DQS, DQS# finishes driving the signal.
10. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK, CK# crossing.
11. CKE input hold time is measured from CK, CK# crossing to CKE reaching a HIGH/LOW voltage level.
12. Input set-up/hold time for signal (CA[9:0], CS#).
13. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
14. The LPDDR device will set some mode register default values upon receiving a RESET (MRW) command as specified in — Mode Register Definition‖.
15. The output skew parameters are measured with default output impedance settings using the reference load.
16. The minimum tCK column applies only when tCK is greater than 6ns.
17. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 opcode.
18. Use even addressing whenever possible to optimize for long-life.
19. The parts support the parameter values corresponding to Typical. For parts that support Fast values, contact ISSI.

Command Input Setup and Hold Timing



Notes:
1. The setup and hold timing shown applies to all commands.
2. Setup and hold conditions also apply to the CKE pin. For timing diagrams related to the CKE pin, see Power-Down .

CA and CS# Setup, Hold, and Derating

The For all input signals (CA and CS#), the total required setup time (tIS) and hold time (tIH) is calculated by adding the data sheet tIS (base) and tIH (base) values to the ΔtIS and ΔtIH derating values, respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) typical slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. The setup (tIS) typical slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the typical slew rate line between the shaded VREF(DC)-to-(AC) region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded VREF(DC)-to-AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value.

The hold (tIH) typical slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). The hold (tIH) typical slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the typical slew rate line between the shaded DC-to-VREF(DC) region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between the shaded DC-to-VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value.

For a valid transition, the input signal must remain above or below VIH/VIL(AC) for a specified time, tVAC. For slow slew rates the total setup time could be a negative value (that is, a valid input signal will not have reached VIH/VIL(AC) at the time of the rising clock transition). A valid input signal is still required to complete the transition and reach VIH/VIL(AC).

For slew rates between the values listed, the derating values are obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

CA and CS# Setup and Hold Base Values (> 400 MHz, 1 V/ns slew rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
^{t}IS (base)	0	30	70	150	240	300	$V_{IH}/V_{IL(AC)} = V_{REF(DC)} \pm 220mV$
^{t}IH (base)	90	120	160	240	330	390	$V_{IH}/V_{IL(DC)} = V_{REF(DC)} \pm 130mV$

Note: AC/DC referenced for 1 V/ns CA and CS# slew rate and 2 V/ns differential CK, CK# slew rate.

Derating Values for AC/DC-based tIS/tIH (AC220) - tIS, tIH derating in [ps], AC/DC-based

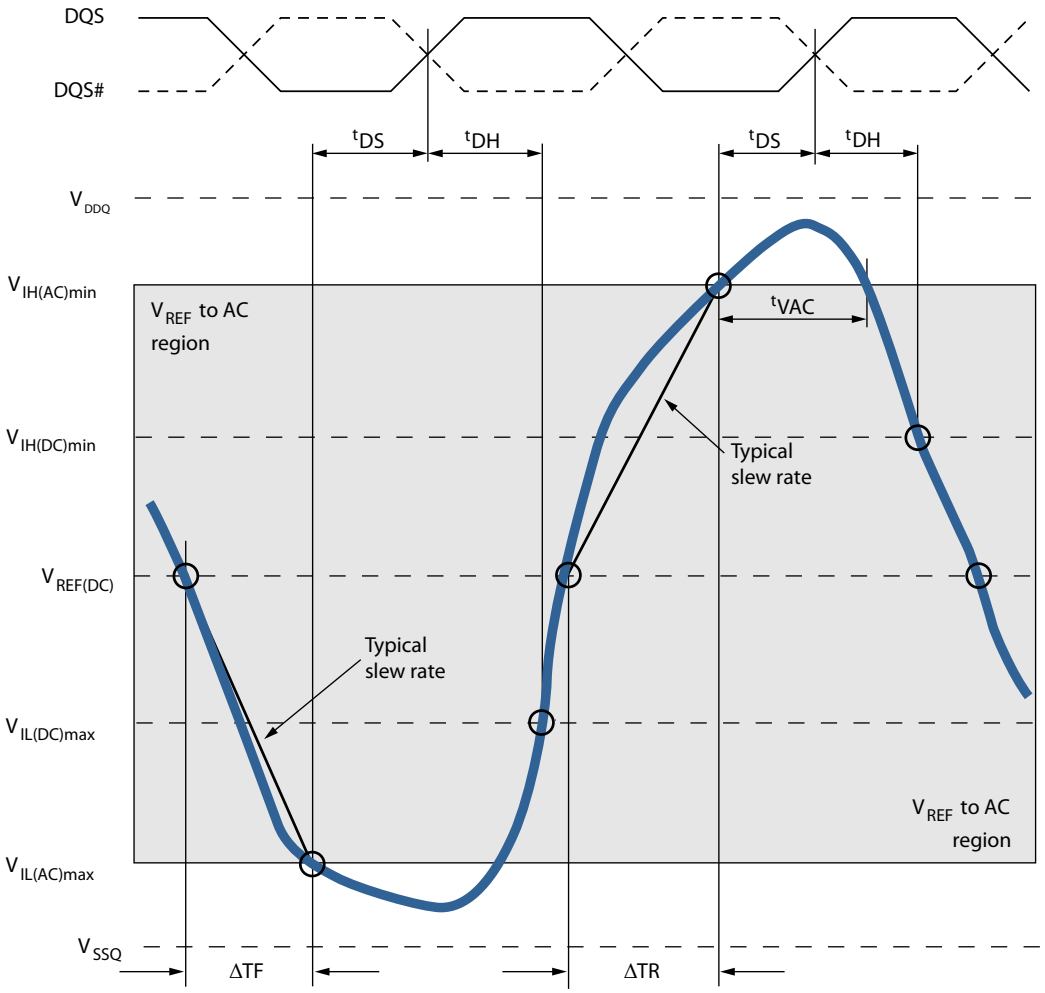
		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS# slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: Shaded cells are not supported.

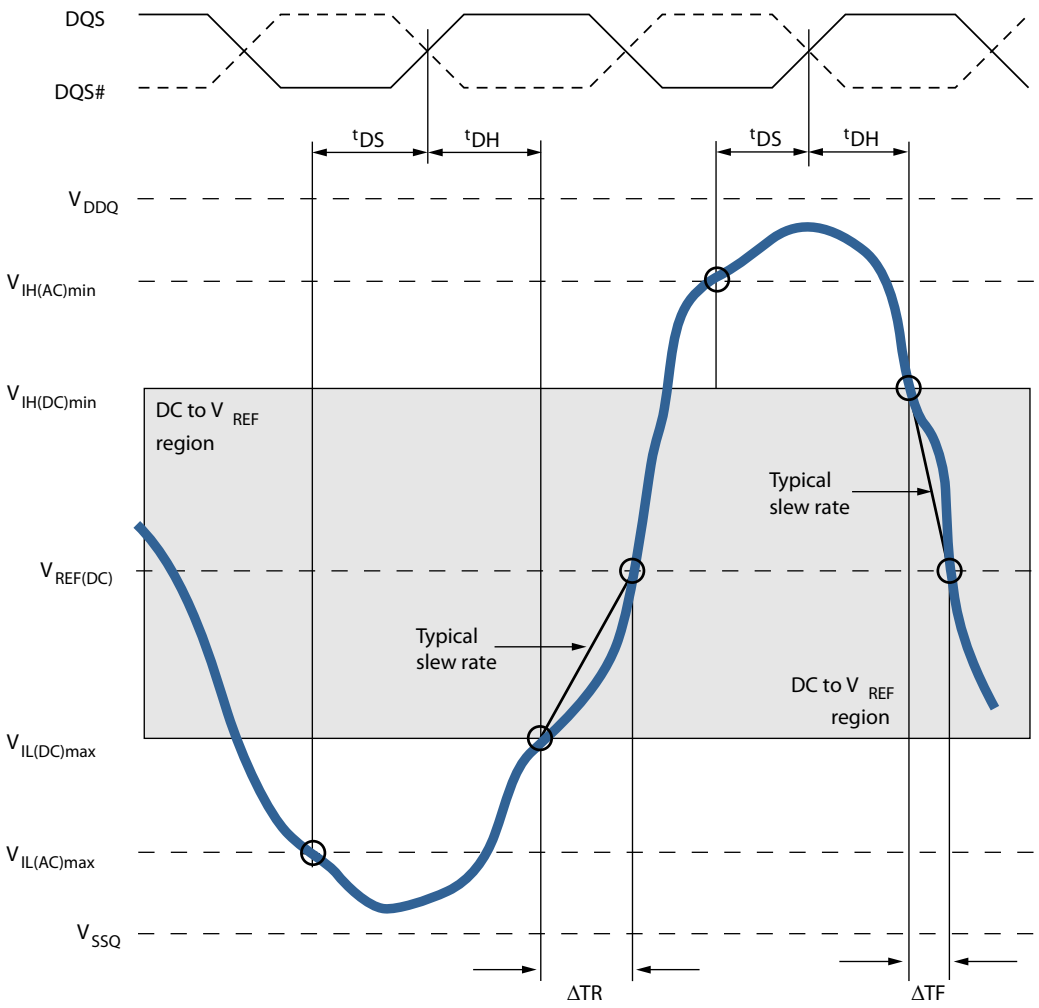
Required Time for Valid Transition with tVAC Above VIH(AC) and Below VIL(AC)

Slew Rate (V/ns)	tVAC at 300mV (ps)		tVAC at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–

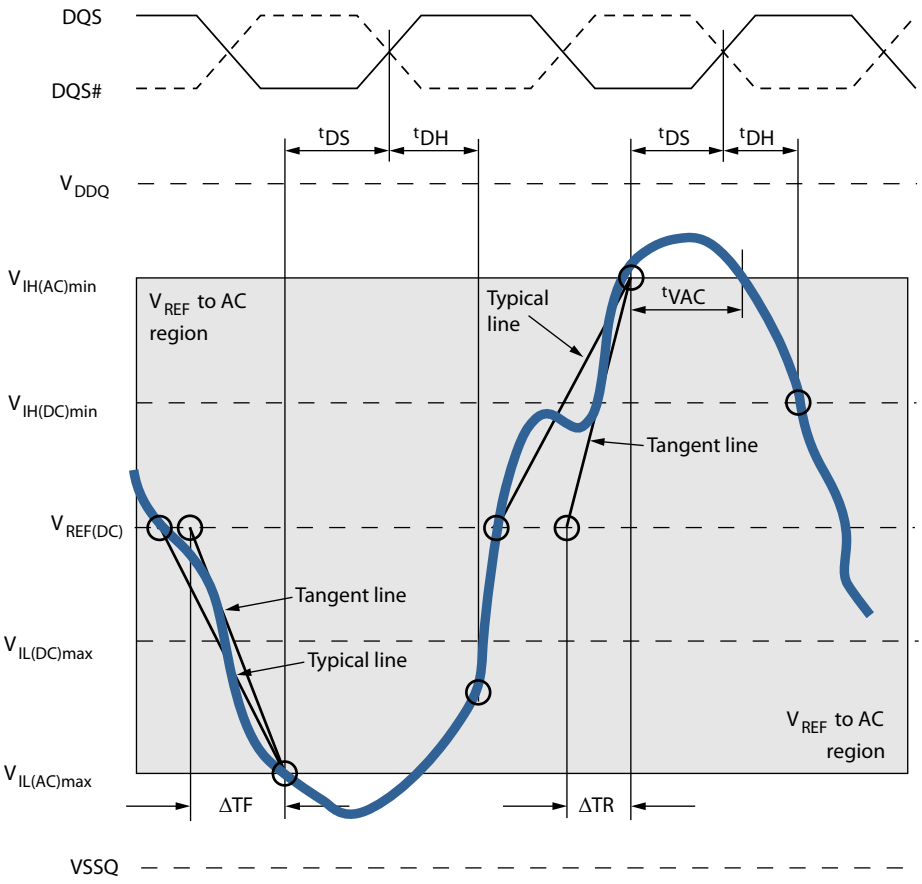
Typical Slew Rate and tVAC: tIS for CA and CS# Relative to Clock



Typical Slew Rate – tIH for CA and CS# Relative to Clock



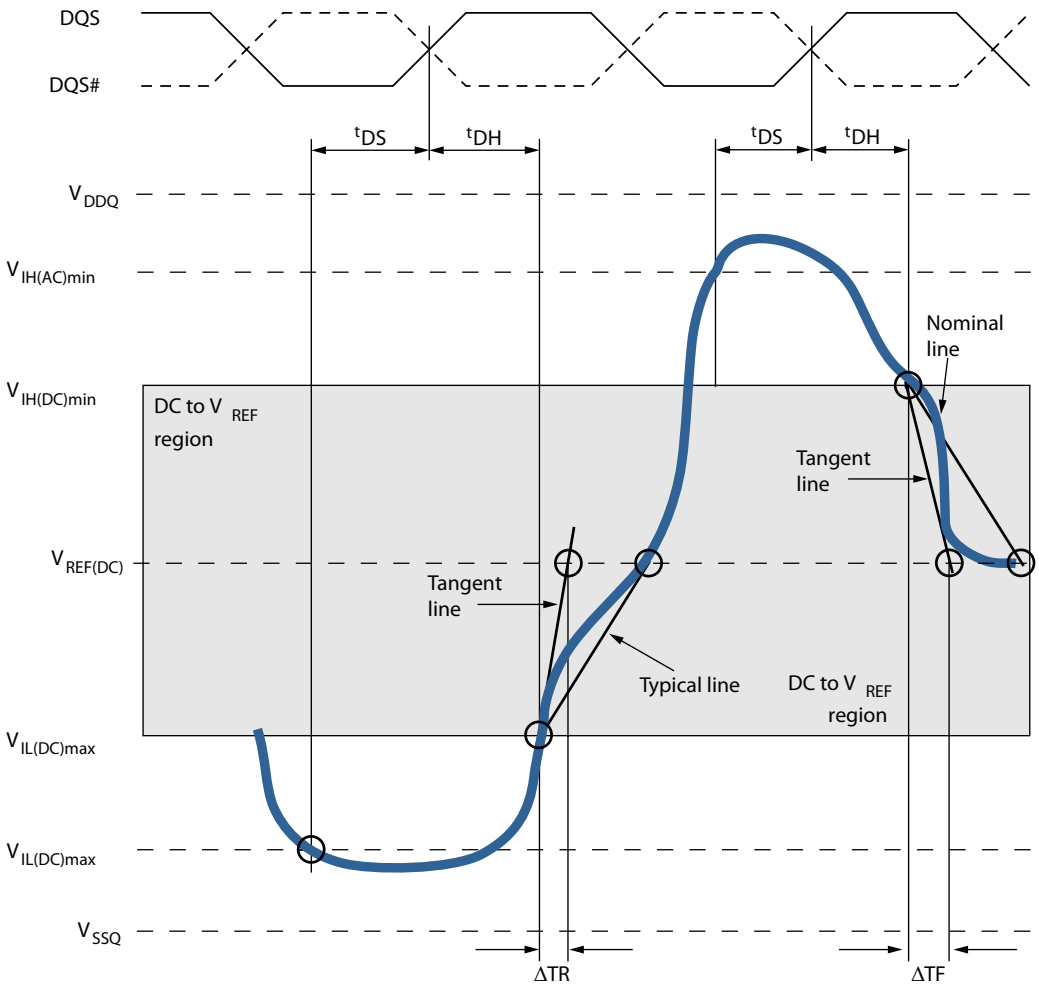
Tangent Line: tIS for CA and CS# Relative to Clock



$$\text{Setup slew rate falling signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(AC)max}]}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{\text{tangent line } [V_{IH(AC)min} - V_{REF(DC)}]}{\Delta TR}$$

Tangent Line: tIH for CA and CS# Relative to Clock



Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (tDS) and hold time (tDH) by adding the data sheet tDS(base) and tDH(base) values to the ΔtDS and ΔtDH derating values, respectively . Example: tDS = tDS(base) + ΔtDS.

The typical tDS slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. The typical tDS slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) max .

If the actual signal is consistently earlier than the typical slew rate , the area shaded gray between the VREF(DC) region and the AC region, use the typical slew rate for the derating value. If the actual signal is later than the typical slew rate line anywhere between the shaded VREF(DC) region and the AC region, the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value .

The typical tDH slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). The typical tDH slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC)

If the actual signal is consistently later than the typical slew rate line between the shaded DC-level-to-VREF(DC) region, use the typical slew rate for the derating value. If the actual signal is earlier than the typical slew rate line anywhere between shaded DC to- VREF(DC) region, the slew rate of a tangent line to the actual signal from the DC level to the VREF(DC) level is used for the derating value .

For a valid transition, the input signal must remain above or below VIH/VIL(AC) for the specified time, tVAC . The total setup time for slow slew rates could be negative (that is, a valid input signal may not have reached VIH/VIL(AC) at the time of the rising clock transition). A valid input

signal is still required to complete the transition and reach VIH/VIL(AC).

For slew rates between the values listed in the tables on the following page, the derating values can be obtained using linear interpolation. Slew rate values are not typically subject to production testing. They are verified by design and characterization.

Data Setup and Hold Base Values (>400 MHz, 1 V/ns slew rate)

Parameter	Data Rate						Reference
	1066	933	800	667	533	466	
^{t}DS (base)	-10	15	50	130	210	230	$V_{IH}/V_{IL(AC)} = V_{REF(DC)}$ ±220mV
^{t}DH (base)	80	105	140	220	300	320	$V_{IH}/V_{IL(DC)} = V_{REF(DC)}$ ±130mV

Note: AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate.

Derating Values for AC/DC-based tDS/tDH (AC220) - tDS, tDH derating in [ps], AC/DC-based

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: Shaded cells are not supported.

Derating Values for AC/DC-based tDS/tDH (AC300) - tDS, tDH derating in [ps], AC/DC-based

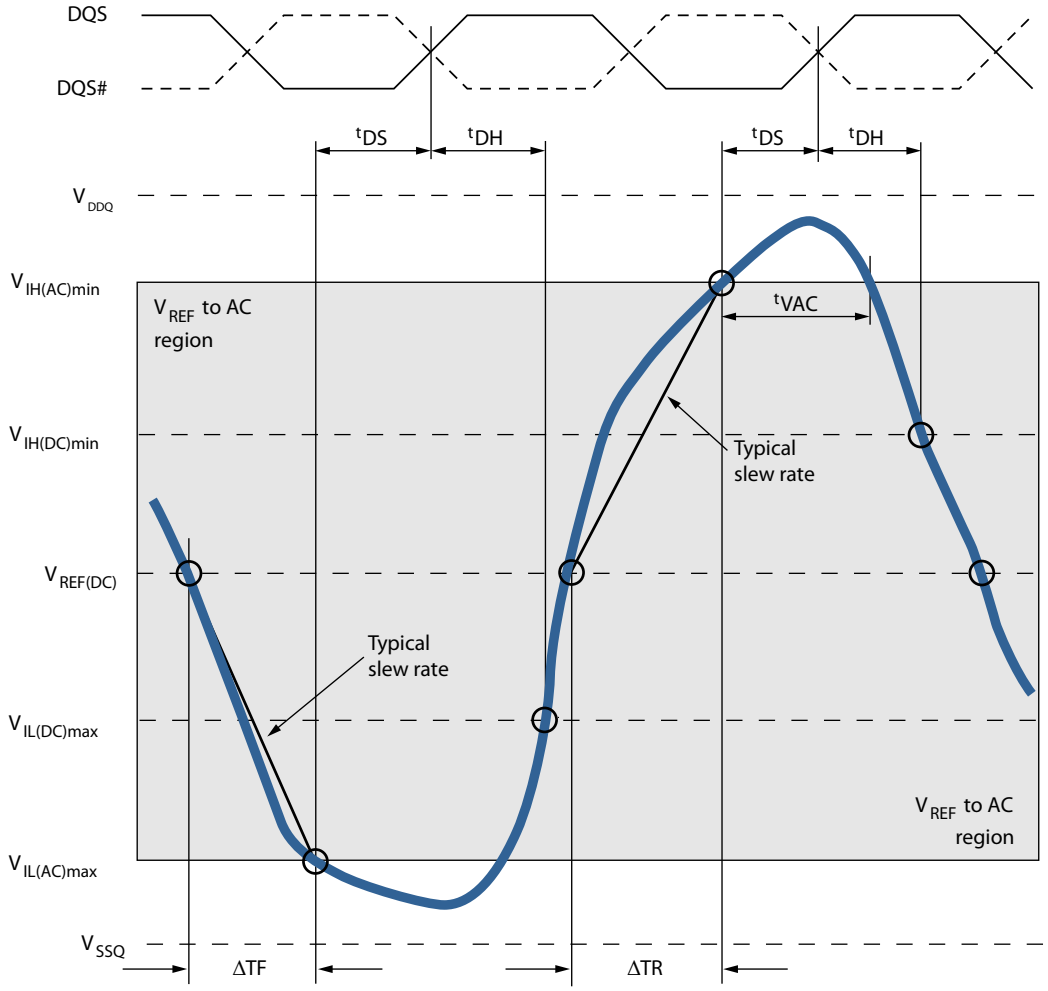
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4												4	-35	-40	-11	-8

Note: Shaded cells are not supported.

Required tVAC Above VIH(AC) or Below VIL(AC) for Valid Transition

Slew Rate (V/ns)	tVAC at 300mV (ps)		tVAC at 220mV (ps)	
	Min	Max	Min	Max
>2.0	75	–	175	–
2.0	57	–	170	–
1.5	50	–	167	–
1.0	38	–	163	–
0.9	34	–	162	–
0.8	29	–	161	–
0.7	22	–	159	–
0.6	13	–	155	–
0.5	0	–	150	–
<0.5	0	–	150	–

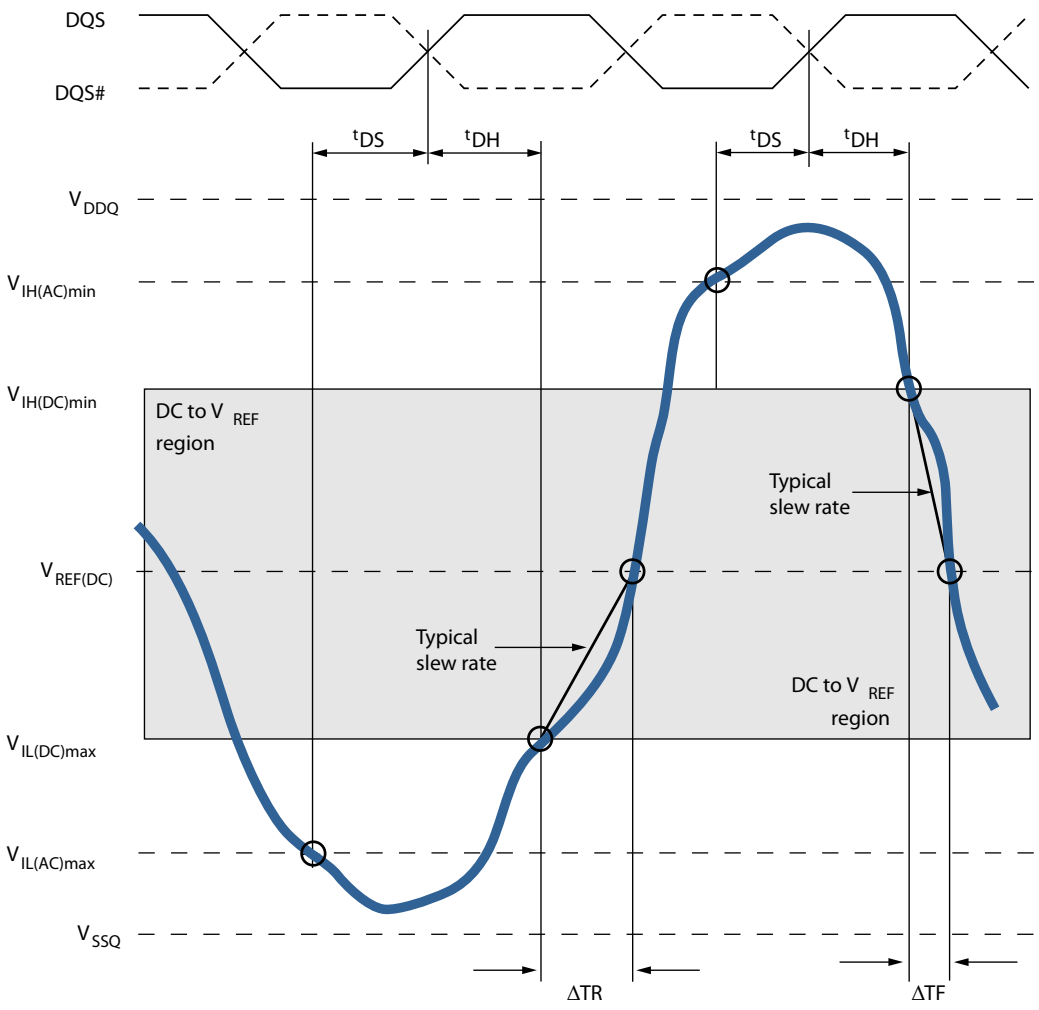
Typical Slew Rate and tVAC – tDS for DQ Relative to Strobe



$$\text{Setup slew rate falling signal} = \frac{V_{REF(DC)} - V_{IL(AC)max}}{\Delta TF}$$

$$\text{Setup slew rate rising signal} = \frac{V_{IH(AC)min} - V_{REF(DC)}}{\Delta TR}$$

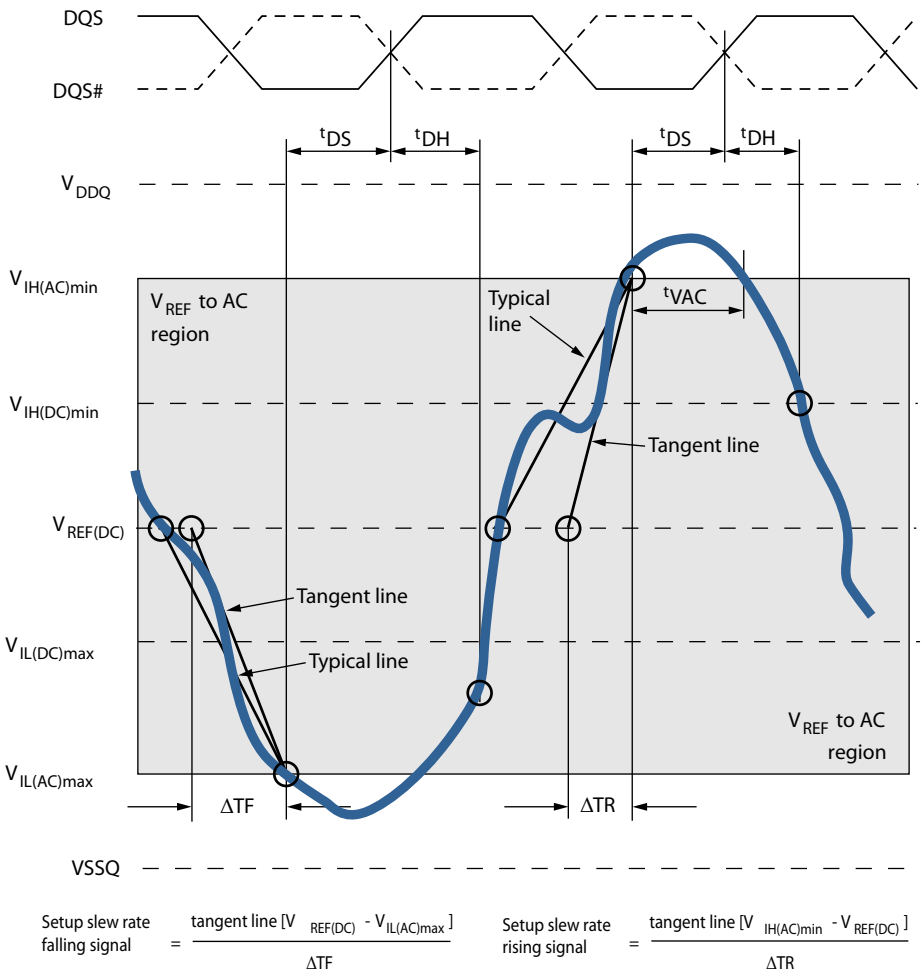
Typical Slew Rate: tDH for DQ Relative to Strobe



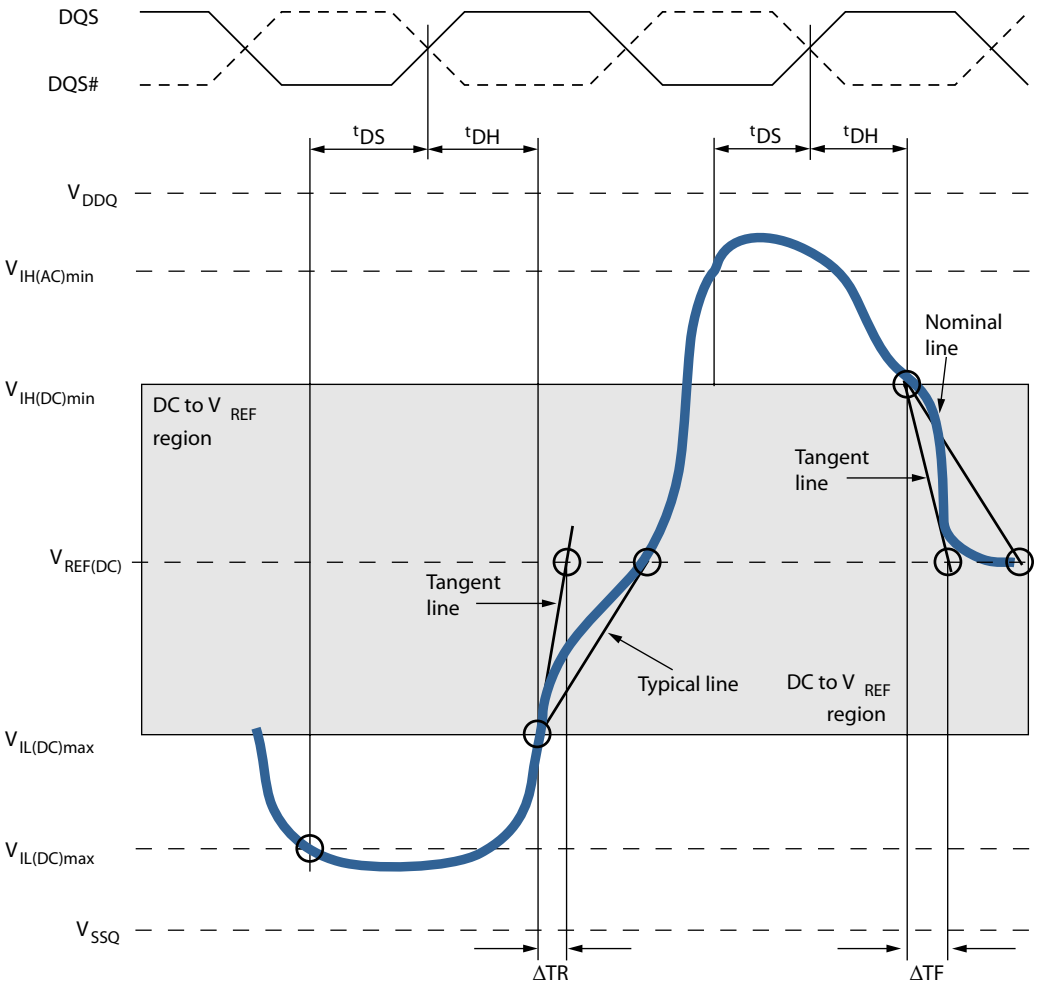
$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)min} - V_{REF(DC)}}{\Delta TF}$$

$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)max}}{\Delta TR}$$

Tangent Line: tDS for DQ with Respect to Strobe



Tangent Line: tDH for DQ with Respect to Strobe



IDD Specifications and Conditions

The following definitions and conditions are used in the IDD measurement tables unless stated otherwise:

- LOW: VIN ≤ VIL(DC)max
- HIGH: VIN ≥ VIH(DC)min
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See Tables bellow

Switching for CA Input Signal

	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising	CK Rising/ CK#Falling	CK Falling/ CK# Rising
Cycle	N		N + 1		N + 2		N + 3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:
1. CS# must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus

Switching for IDD4R

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N +1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	LHLLHLH	L
Rising	H	L	N + 2	Read_Rising	HLH	LHLLHLH	H
Falling	H	L	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

Switching for IDD4W

Clock	CKE	CS#	Clock Cycle Number	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	LLH	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N +1	NOP	LLL	LLLLLLL	H
Falling	H	H	N + 1	NOP	HLH	LHLLHLH	L
Rising	H	L	N + 2	Write_Rising	LLH	LHLLHLH	H
Falling	H	L	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N + 3	NOP	LLL	HHHHHHH	H
Falling	H	H	N + 3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The noted pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current (SDRAM): $^{t}CK = {}^{t}CKmin$; $^{t}RC = {}^{t}RCmin$; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	I_{DD01}	V_{DD1}	
	I_{DD02}	V_{DD2}	
	$I_{DD0,in}$	V_{DDCA} , V_{DDQ}	4
Idle power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I_{DD2P1}	V_{DD1}	
	I_{DD2P2}	V_{DD2}	
	$I_{DD2P,in}$	V_{DDCA} , V_{DDQ}	4
Idle power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDCA} , V_{DDQ}	4
Idle non-power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDCA} , V_{DDQ}	4
Idle non-power-down standby current with clock stopped: CK = LOW; CK# = HIGH; CKE is HIGH; CS# is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDCA} , V_{DDQ}	4
Active power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDCA} , V_{DDQ}	4
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDCA} , V_{DDQ}	4
Active non-power-down standby current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDCA} , V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS# is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDCA} , V_{DDQ}	4
Operating burst READ current: $^{t}CK = {}^{t}CKmin$; CS# is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer	I_{DD4R1}	V_{DD1}	
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: $^{t}CK = {}^{t}CKmin$; CS# is HIGH between valid commands; One bank is active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDCA} , V_{DDQ}	4
All-bank REFRESH burst current: $^{t}CK = {}^{t}CKmin$; CKE is HIGH between valid commands; $^{t}RC = {}^{t}RFCabmin$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	$I_{DD5,in}$	V_{DDCA} , V_{DDQ}	4

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: ^{t}CK = ^{t}CKmin; CKE is HIGH between valid commands; ^{t}RC = ^{t}REFI; CA bus inputs are switching; Data bus inputs are stable	I_{DD5AB1}	V_{DD1}	
	I_{DD5AB2}	V_{DD2}	
	$I_{DD5AB,in}$	V_{DDCA} , V_{DDQ}	4
Self refresh current (–25˚C to +85˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate	I_{DD61}	V_{DD1}	6
	I_{DD62}	V_{DD2}	6
	$I_{DD6,in}$	V_{DDCA} , V_{DDQ}	4, 6
Self refresh current (+85˚C to +105˚C): CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD6ET1}	V_{DD1}	6, 7
	I_{DD6ET2}	V_{DD2}	6, 7
	$I_{DD6ET,in}$	V_{DDCA} , V_{DDQ}	4, 6, 7
Deep power-down current: CK = LOW, CK# = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD81}	V_{DD1}	7
	I_{DD82}	V_{DD2}	7
	$I_{DD8,in}$	V_{DDCA} , V_{DDQ}	4, 7

Notes:
1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the summation of VDDQ and VDDCA.
5. Guaranteed by design with output reference load and RON = 40 ohm.
6. This is the general definition that applies to full-array SELF REFRESH).
7. IDD6ET and IDD8 are typical values, are sampled only, and are not tested.

IDD SPECIFICATIONS

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD01}	V_{DD1}	25	25	25	mA
I_{DD02}	V_{DD2}	40	40	40	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD2P1}	V_{DD1}	200	200	200	µA
I_{DD2P2}	V_{DD2}	300	300	300	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD2PS1}	V_{DD1}	200	200	200	µA
I_{DD2PS2}	V_{DD2}	300	300	300	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD2N1}	V_{DD1}	1	1	1	mA
I_{DD2N2}	V_{DD2}	30	30	30	mA
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	5	5	5	
I_{DD2NS1}	V_{DD1}	1	1	1	mA
I_{DD2NS2}	V_{DD2}	5	5	5	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	5	5	5	
I_{DD3P1}	V_{DD1}	1.5	1.5	1.5	mA
I_{DD3P2}	V_{DD2}	2.5	2.5	2.5	mA
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	100	100	100	µA
I_{DD3PS1}	V_{DD1}	1.5	1.5	1.5	mA
I_{DD3PS2}	V_{DD2}	2.5	2.5	2.5	mA
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	100	100	100	µA
I_{DD3N1}	V_{DD1}	4	4	4	mA
I_{DD3N2}	V_{DD2}	30	30	30	mA
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	5	5	5	
I_{DD3NS1}	V_{DD1}	4	4	4	mA
I_{DD3NS2}	V_{DD2}	10	10	10	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	5	5	5	
I_{DD4R1}	V_{DD1}	4	4	4	mA
I_{DD4R2}	V_{DD2}	180	160	150	
$I_{DD4R,in}$	V_{DDCA}	6	6	6	
I_{DD4W1}	V_{DD1}	4	4	4	mA
I_{DD4W2}	V_{DD2}	180	160	150	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	20	20	20	
I_{DD51}	V_{DD1}	30	30	30	mA
I_{DD52}	V_{DD2}	40	40	40	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	6	6	6	

IDD SPECIFICATIONS (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade			Unit
		-18	-25	-3	
I_{DD5AB1}	V_{DD1}	3	3	3	mA
I_{DD5AB2}	V_{DD2}	35	35	35	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	6	6	6	
I_{DD61}	V_{DD1}	750	750	750	µA
I_{DD62}	V_{DD2}	700	700	700	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	50	50	50	
I_{DD6ET1}	V_{DD1}	1000	1000	1000	µA
I_{DD6ET2}	V_{DD2}	950	950	950	
$I_{DD6ET,in}$	V_{DDCA} + V_{DDQ}	80	80	80	
I_{DD81}	V_{DD1}	20	20	20	µA
I_{DD82}	V_{DD2}	150	150	150	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	15	15	15	

IDD6 Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

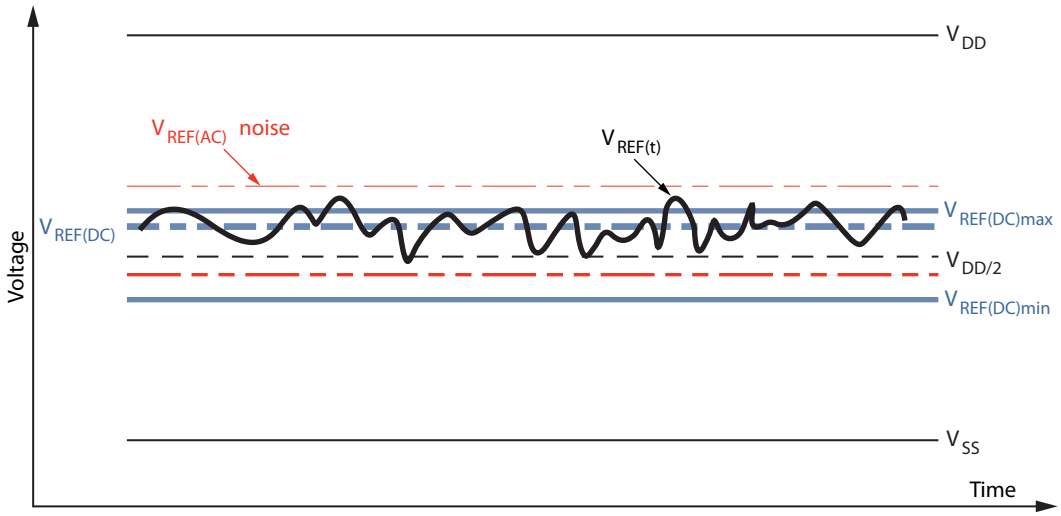
PASR	Supply	-40°C to +85°C	+85°C to +105°C	Unit
Full array	V_{DD1}	750	1000	µA
	V_{DD2}	700	950	
	V_{DDi}	50	80	
1/2 array	V_{DD1}	650	900	
	V_{DD2}	550	850	
	V_{DDi}	50	80	
1/4 array	V_{DD1}	600	700	
	V_{DD2}	500	600	
	V_{DDi}	50	80	
1/8 array	V_{DD1}	500	550	
	V_{DD2}	450	480	
	V_{DDi}	50	80	

VREF Tolerances

The DC tolerance limits and AC noise limits for the reference voltages VREFCA and VREFDQ are illustrated below. This figure shows a valid reference voltage VREF(t) as a function of time. VDD is used in place of VDDCA for VREFCA, and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (for example, 1 second) and is specified as a fraction of the linear average of VDDQ or VDDCA, also over a very long period of time (for example, 1 second). This average must meet the MIN/MAX requirements in Table of Single-Ended AC and DC Input Levels for CA and CS# Inputs. Additionally, VREF(t) can temporarily deviate from VREF(DC)

by no more than ±1% VDD. VREF(t) cannot track noise on VDDQ or VDDCA if doing so would force VREF outside these specifications.

VREF DC Tolerance and VREF AC Noise Limits



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC), and VIL(DC) are dependent on VREF.

VREF DC variations affect the absolute voltage a signal must reach to achieve a valid HIGH or LOW, as well as the time from which setup and hold times are measured. When VREF is outside the specified levels, devices will function correctly with appropriate timing deratings as long as:

• VREF is maintained between 0.44 x VDDQ (or VDDCA) and 0.56 x VDDQ (or VDDCA), and

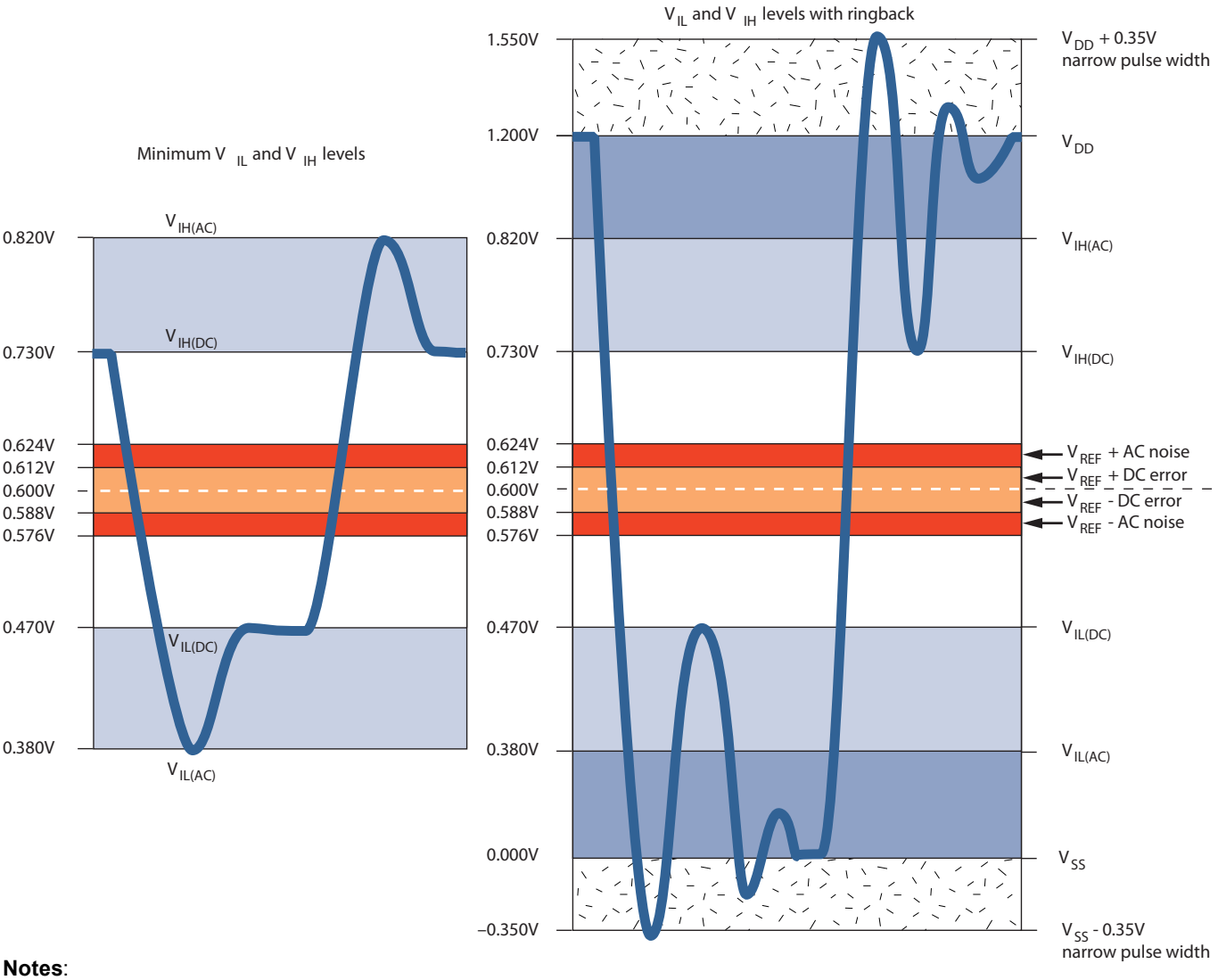
• the controller achieves the required single-ended AC and DC input levels from instantaneous VREF .

System timing and voltage budgets must account for VREF deviations outside this range.

The setup/hold specification and derating values must include time and voltage associated with VREF AC noise. Timing and voltage effects due to AC noise on VREF up to the specified limit (±1% VDD) are included in LPDDR2 timings and their associated deratings.

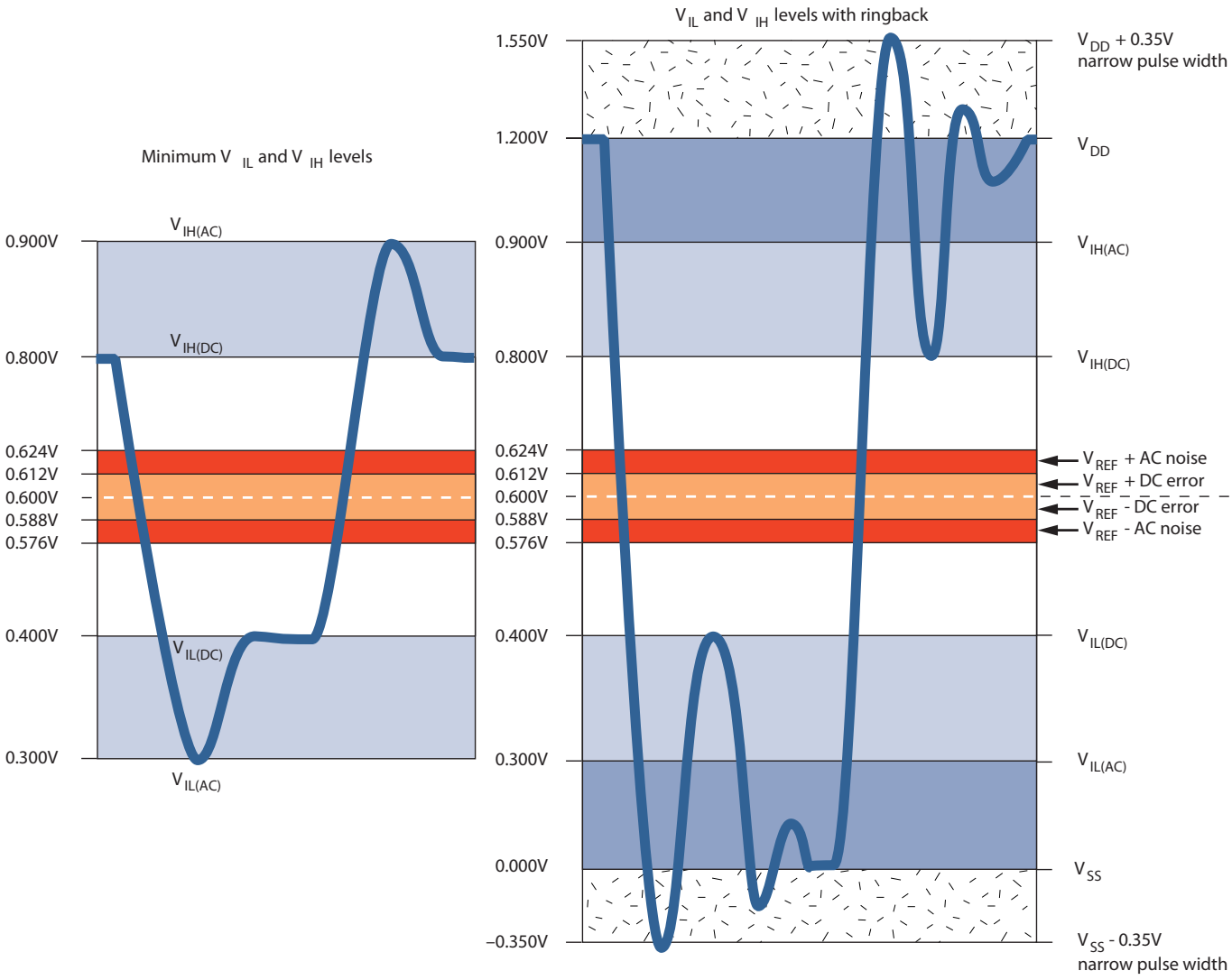
Input Signal

LPDDR2 466-1066 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, CK#, and CS# VDD stands for VDDCA. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
3. For CA[9:0], CK, CK#, and CS# VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.

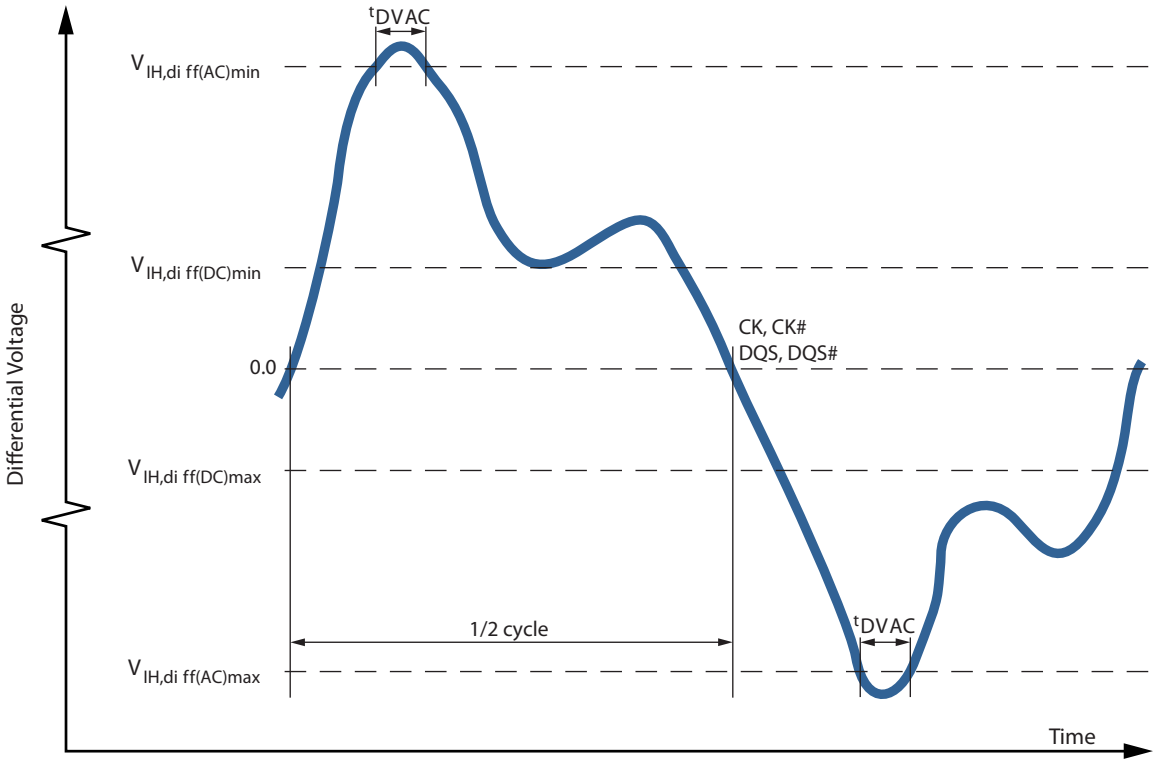
LPDDR2-200 to LPDDR2-400 Input Signal



Notes:
1. Numbers reflect typical values.
2. For CA[9:0], CK, CK#, and CS# VDD stands for VDDCA. For DQ, DM, DQS, and DQS#, VDD stands for VDDQ.
3. For CA[9:0], CK, CK#, and CS# VSS stands for VSSCA. For DQ, DM, DQS, and DQS#, VSS stands for VSSQ.

AC and DC Logic Input Measurement Levels for Differential Signals

Differential AC Swing Time and tDVAC



Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{IH,diff(AC)}$	Differential input HIGH AC	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	$2 \times (V_{IH(AC)} - V_{REF})$	Note 1	V	2
$V_{IL,diff(AC)}$	Differential input LOW AC	Note 1	$2 \times (V_{REF} - V_{IL(AC)})$	Note 1	$2 \times (V_{REF} - V_{IL(AC)})$	V	2
$V_{IH,diff(DC)}$	Differential input HIGH	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	$2 \times (V_{IH(DC)} - V_{REF})$	Note 1	V	3
$V_{IL,diff(DC)}$	Differential input LOW	Note 1	$2 \times (V_{REF} - V_{IL(DC)})$	Note 1	$2 \times (V_{REF} - V_{IL(DC)})$	V	3

Notes:
1. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# must be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals and must comply with the specified limitations for overshoot and undershoot.
2. For CK and CK#, use VIH/VIL(AC) of CA and VREFCA; for DQS and DQS#, use VIH/VIL(AC) of DQ and VREFDQ. If a reduced
AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. Used to define a differential signal slew rate.

CK/CK# and DQS/DQS# Time Requirements Before Ringback (tDVAC)

Slew Rate (V/ns)	$^{t}DVAC$ (ps) at $V_{IH}/V_{ILdiff(AC)}$ = 440mV	$^{t}DVAC$ (ps) at $V_{IH}/V_{ILdiff(AC)}$ = 600mV
	Min	Min
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

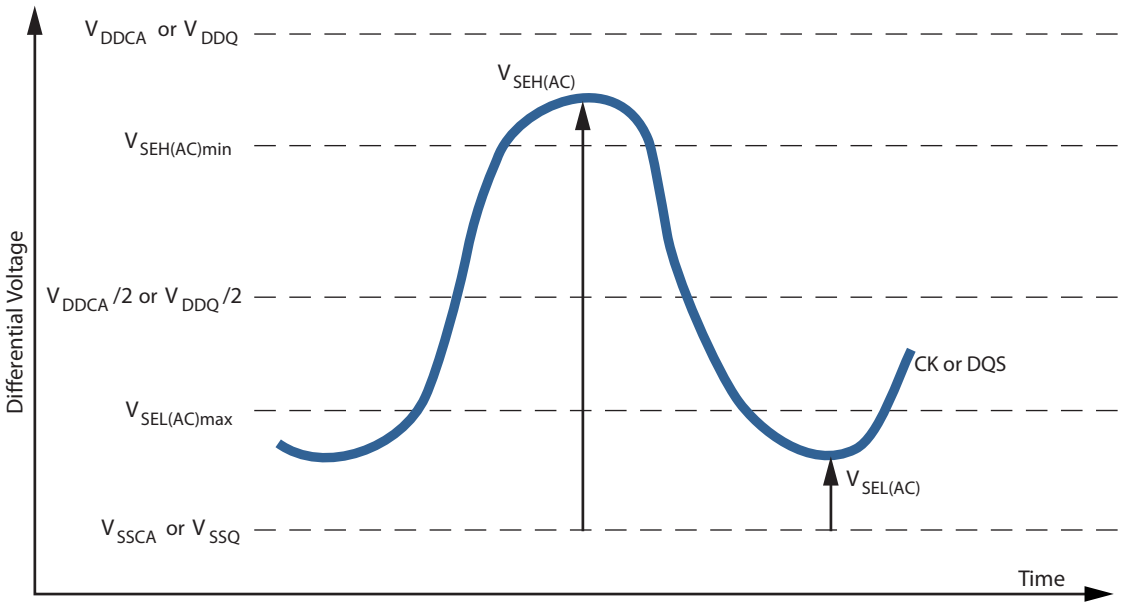
Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, CK#, DQS, and DQS#) must also comply with certain requirements for single-ended signals.

CK and CK# must meet VSEH(AC)min/VSEL(AC)max in every half cycle. DQS, DQS# must meet VSEH(AC)min/VSEL(AC)max in every half cycle preceding and following a valid transition.

The applicable AC levels for CA and DQ differ by speed bin.

Single-Ended Requirements for Differential Signals



Note that while CA and DQ signal requirements are referenced to VREF, the single-ended components of differential signals also have a requirement with respect to VDDQ/2 for DQS, and VDDCA/2 for CK.

The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach VSEL(AC)max or VSEH(AC)min has no bearing on timing. This requirement does, however, add a restriction on the common mode characteristics of these signals.

Single-Ended Levels for CK, CK#, DQS, DQS#

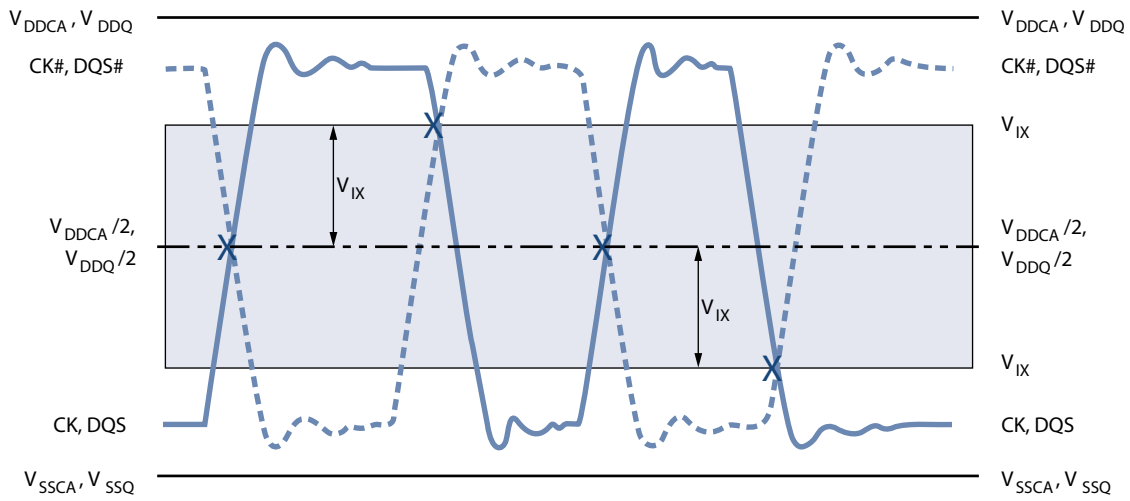
Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Notes
		Min	Max	Min	Max		
$V_{SEH(AC)}$	Single-ended HIGH level for strobes	(V_{DDQ}/2) + 0.220	Note 1	(V_{DDQ}/2) + 0.300	Note 1	V	2, 3
	Single-ended HIGH level for CK, CK#	(V_{DDCA}/2) + 0.220	Note 1	(V_{DDCA}/2) + 0.300	Note 1	V	2, 3
$V_{SEL(AC)}$	Single-ended LOW level for strobes	Note 1	(V_{DDQ}/2) - 0.220	Note 1	(V_{DDQ}/2) + 0.300	V	2, 3
	Single-ended LOW level for CK, CK#	Note 1	(V_{DDCA}/2) - 0.220	Note 1	(V_{DDCA}/2) + 0.300	V	2, 3

Notes:
1. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# must be within the respective limits (VIH(DC)max, VIL(DC)min) for single-ended signals and must comply with the specified limitations for overshoot and undershoot.
2. For CK and CK#, use VIH/VIL(AC) of CA and VREFCA; for DQS and DQS#, use VIH/VIL(AC) of DQ and VREFDQ. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced voltage level also applies.
3. Used to define a differential signal slew rate.

Differential Input Crosspoint Voltage

To ensure tight setup and hold times as well as output skew parameters with respect to clock and strobe, each crosspoint voltage of differential input signals (CK, CK#, DQS, and DQS#) must meet the specifications in the table "Single-Ended Levels" (page 124). The differential input crosspoint voltage (VIX) is measured from the actual crosspoint of the true signal and complement to the mid-level between VDD and VSS.

VIX Definition



Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Notes
		Min	Max		
$V_{IXCA(AC)}$	Differential input crosspoint voltage relative to $V_{DDCA}/2$ for CK and CK#	–120	120	mV	1, 2
$V_{IXDQ(AC)}$	Differential input crosspoint voltage relative to $V_{DDQ}/2$ for DQS and DQ#	–120	120	mV	1, 2

Notes:
1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and it is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK and CK#, VREF = VREFCA(DC). For DQS and DQS#, VREF = VREFDQ(DC).

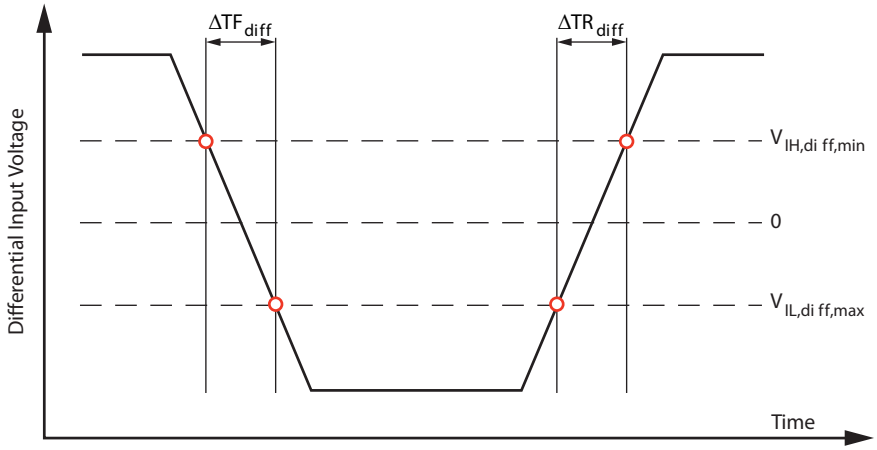
Input Slew Rate

Differential Input Slew Rate Definition

Description	Measured [1]		Defined by
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$[V_{IH,diff,min} - V_{IL,diff,max}] / \Delta TF_{diff}$

Note: The differential signals (CK/CK# and DQS/DQS#) must be linear between these thresholds.

Differential Input Slew Rate Definition for CK, CK#, DQS, and DQS#



Output Characteristics and Operating Conditions

Single-Ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Notes
$V_{OH(AC)}$	AC output HIGH measurement level (for output slew rate)		V_{REF} + 0.12	V	
$V_{OL(AC)}$	AC output LOW measurement level (for output slew rate)		V_{REF} - 0.12	V	
$V_{OH(DC)}$	DC output HIGH measurement level (for I-V curve linearity)		0.9 x V_{DDQ}	V	1
$V_{OL(DC)}$	DC output LOW measurement level (for I-V curve linearity)		0.1 x V_{DDQ}	V	2
I_{OZ}	Output leakage current (DQ, DM, DQS, DQS#); DQ, DQS, DQS# are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}	MIN	–5	µA	
		MAX	+5	µA	
MMpupd	Delta output impedance between pull-up and pull-down for DQ/DM	MIN	–15	%	
		MAX	+15	%	

Notes:
1. IOH = –0.1mA.
2. IOL = 0.1mA.

Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit
$V_{OHdiff(AC)}$	AC differential output HIGH measurement level (for output SR)	+ 0.2 x V_{DDQ}	V
$V_{OLdiff(AC)}$	AC differential output LOW measurement level (for output SR)	- 0.2 x V_{DDQ}	V

Single-Ended Output Slew Rate

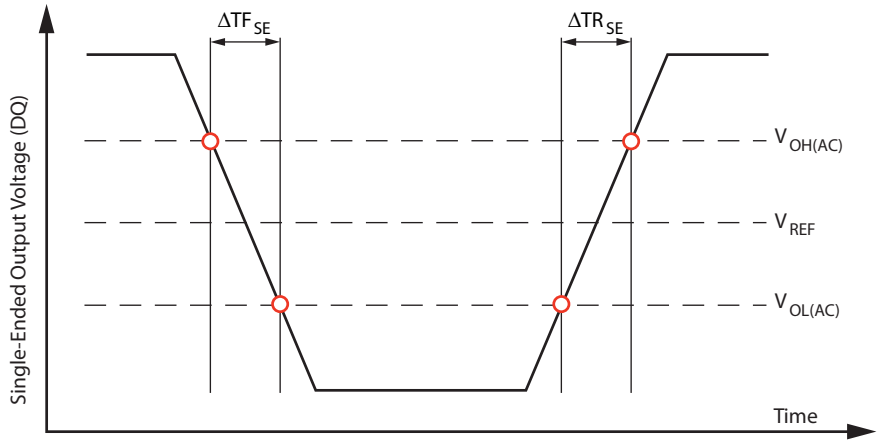
With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single-ended signals.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{SE}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{SE}$

Note: Output slew rate is verified by design and characterization and may not be subject to production testing.

Single-Ended Output Slew Rate Definition



Single-Ended Output Slew Rate

Parameter	Symbol	Value		Unit
		Min	Max	
Single-ended output slew rate (output impedance = 40 Ω ±30%)	SRQ_{SE}	1.5	3.5	V/ns
Single-ended output slew rate (output impedance = 60 Ω ±30%)	SRQ_{SE}	1.0	2.5	V/ns
Output slew-rate-matching ratio (pull-up to pull-down)		0.7	1.4	–

Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = singleended signals
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

Differential Output Slew Rate

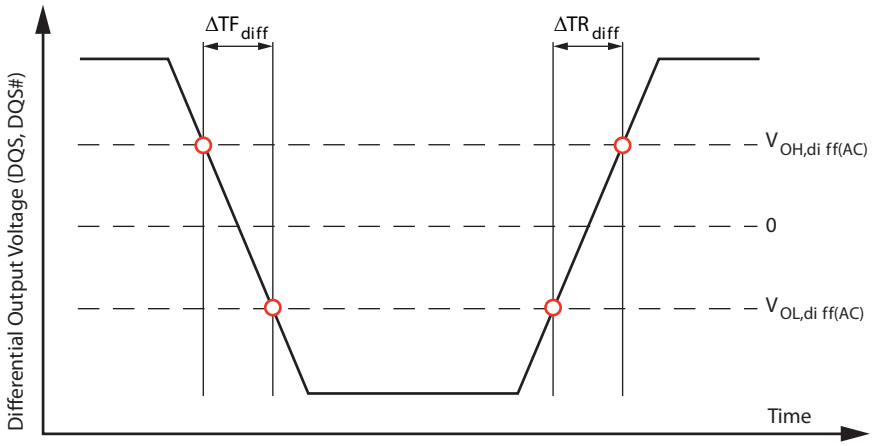
With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL,diff(AC) and VOH,diff(AC) for differential signals.

Differential Output Slew Rate Definition

Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate (output impedance = 40 Ω ±30%)	SRQ_{diff}	3.0	7.0	V/ns

Note: Output slew rate is verified by design and characterization and may not be subject to production testing.

Differential Output Slew Rate Definition



Parameter	Symbol	Value		Unit
		Min	Max	
Differential output slew rate (output impedance = 40 Ω ±30%)	SRQ_{diff}	3.0	7.0	V/ns
Differential output slew rate (output impedance = 60 Ω ±30%)	SRQ_{diff}	2.0	5.0	V/ns

Notes:
1. Definitions: SR = slew rate; Q = output (similar to DQ = data-in, data-out); SE = singleended signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

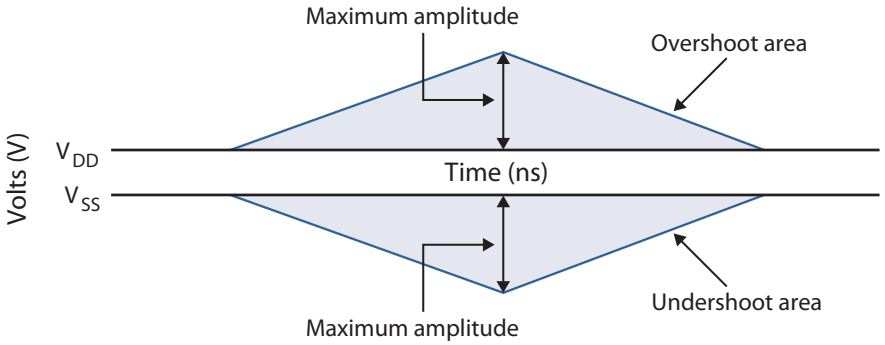
AC Overshoot/Undershoot Specification

Applies for CA[9:0], CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM

Parameter	1066	933	800	667	533	400	333	Unit
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	0.35	0.35	0.35	0.35	V
Maximum area above V_{DD} [1]	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns
Maximum area below V_{SS} [2]	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V/ns

Notes:
1. VDD stands for VDDCA for CA[9:0], CK, CK#, CS#, and CKE. VDD stands for VDDQ for DQ, DM, DQS, and DQS#.
2. VSS stands for VSSCA for CA[9:0], CK, CK#, CS#, and CKE. VSS stands for VSSQ for DQ, DM, DQS, and DQS#.

Overshoot and Undershoot Definition

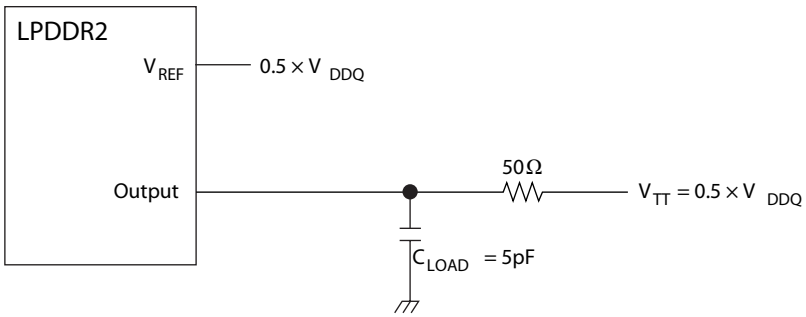


Notes:
1. VDD stands for VDDCA for CA[9:0], CK, CK#, CS#, and CKE. VDD stands for VDDQ for DQ, DM, DQS, and DQS#.
2. VSS stands for VSSCA for CA[9:0], CK, CK#, CS#, and CKE. VSS stands for VSSQ for DQ, DM, DQS, and DQS#.

HSUL_12 Driver Output Timing Reference Load

The timing reference loads are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally with one or more coaxial transmission lines terminated at the tester electronics.

HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note: All output timing parameter values (tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc.) are reported with respect to this reference load. This reference load is also used to report slew rate.

Output Driver Impedance

The output driver impedance is selected by a mode register during initialization. The selected value is able to maintain the tight tolerances specified if proper ZQ calibration is performed. Output specifications refer to the default output driver unless specifically

stated otherwise. A functional representation of the output buffer is shown in bellow. The output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:

RONPU = (VDDQ – VOUT) / ABS(IOUT)

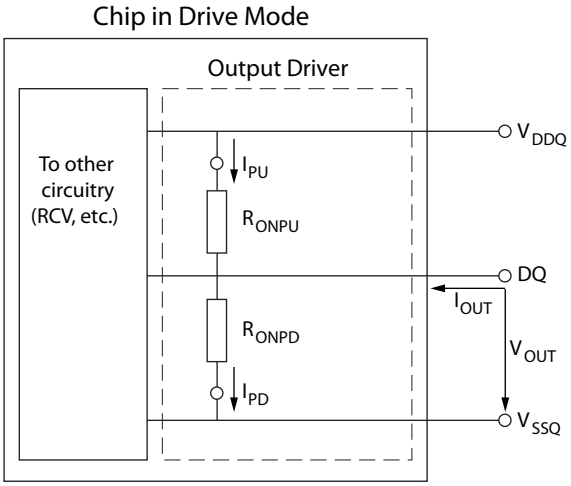
When RONPD is turned off.

RONPD = VOUT / ABS(IOUT)

When RONPU is turned off.

Output Driver

Chip in drive mode



Output Driver Impedance Characteristics with ZQ Calibration

Output driver impedance is defined by the value of the external reference resistor RZQ. Typical RZQ is 240 ohms.

Output Driver DC Electrical Characteristics with ZQ Calibration

R_{ONnom}	Resistor	V_{OUT}	Min	Typ	Max	Unit	Notes
34.3Ω	R_{ON34PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
	R_{ON34PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/7$	
40.0Ω	R_{ON40PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
	R_{ON40PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/6$	
48.0Ω	R_{ON48PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
	R_{ON48PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/5$	
60.0Ω	R_{ON60PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
	R_{ON60PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/4$	
80.0Ω	R_{ON80PD}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
	R_{ON80PU}	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/3$	
120.0Ω	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.85	1.00	1.15	$R_{ZQ}/2$	
Mismatch between pull-up and pull-down	MM_{PUPD}		–15.00		+15.00	%	5

Notes:
1. Applies across entire operating temperature range after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration, with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration.
4. Pull-down and pull-up output driver impedances should be calibrated at 0.5 x VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down, MMPUPD:
Measure RONPU and RONPD, both at 0.5 × VDDQ:
MMPUPD =((RONPU – RONPD) / RON,nom) × 100
For example, with MMPUPD (MAX) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen

Output Driver Sensitivity Definition

Symbol	Parameter	Min	Max	Unit
R_{ONPD}	R_{ON} temperature sensitivity	0.00	0.75	%/°C
R_{ONPU}	R_{ON} voltage sensitivity	0.00	0.20	%/mV

Notes:
1. ΔT = T - T (at calibration). ΔV = V - V (at calibration).
2. dRONdT and dRONdV are not subject to production testing; they are verified by design and characterization.

Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
R_{ONPD}	R_{ON} temperature sensitivity	0.00	0.75	%/°C
R_{ONPU}	R_{ON} voltage sensitivity	0.00	0.20	%/mV

Output Impedance Characteristics Without ZQ Calibration

Output driver impedance is defined by design and characterization as the default setting.

Output Driver DC Electrical Characteristics Without ZQ Calibration

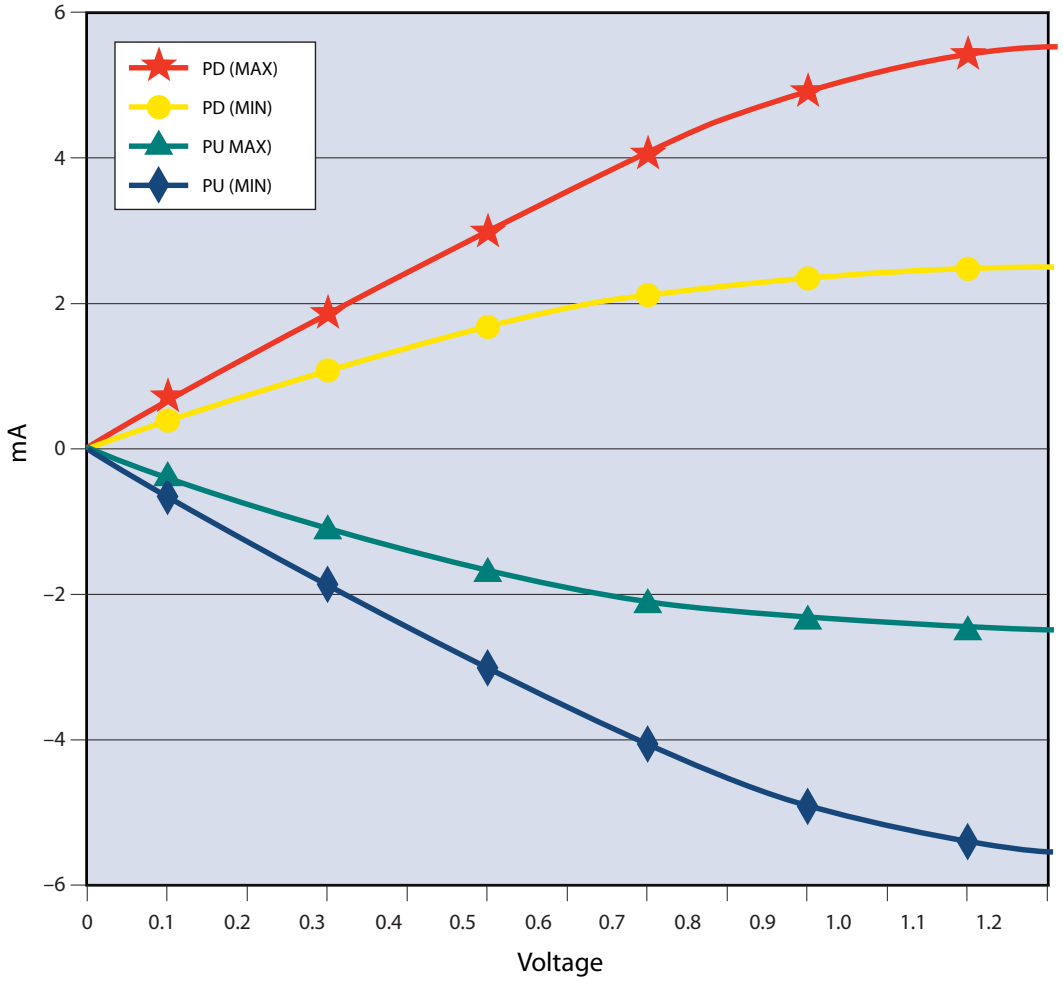
RON $_{nom}$	Resistor	V_{OUT}	Min	Typ	Max	Unit
34.3Ω	R_{ON34PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
	R_{ON34PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/7$
40.0Ω	R_{ON40PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
	R_{ON40PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/6$
48.0Ω	R_{ON48PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
	R_{ON48PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/5$
60.0Ω	R_{ON60PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
	R_{ON60PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/4$
80.0Ω	R_{ON80PD}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$
	R_{ON80PU}	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/3$
120.0Ω	$R_{ON120PD}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$
	$R_{ON120PU}$	$0.5 \times V_{DDQ}$	0.70	1.00	1.30	$R_{ZQ}/2$

Notes:
1. Applies across entire operating temperature range, without calibration.
2. RZQ = 240Ω

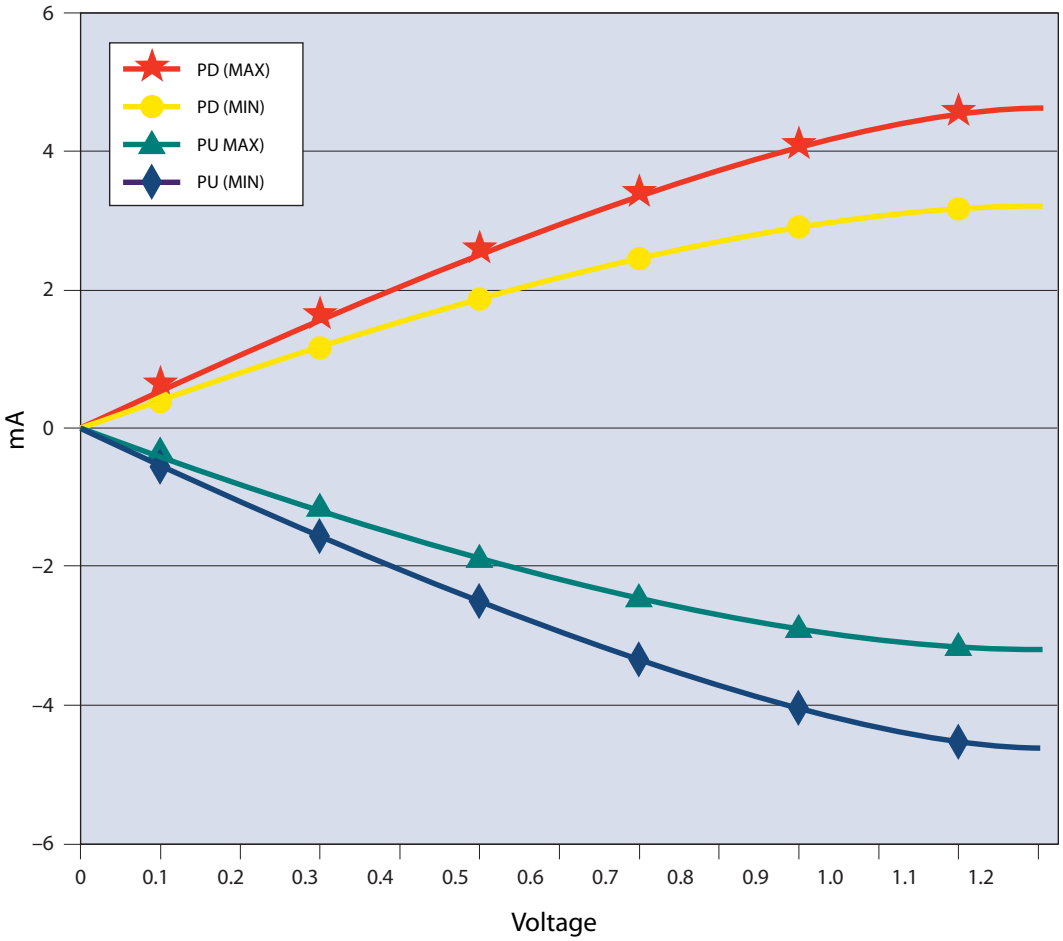
I-V Curves

	$R_{ON} = 240\Omega$ (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current (mA) / R_{ON} (ohms)				Current (mA) / R_{ON} (ohms)			
	Default Value after ZQRESET		With Calibration		Default Value after ZQRESET		With Calibration	
Voltage (V)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)	Min (mA)	Max (mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	–0.19	–0.32	–0.21	–0.26
0.10	0.38	0.64	0.40	0.53	–0.38	–0.64	–0.40	–0.53
0.15	0.56	0.94	0.60	0.78	–0.56	–0.94	–0.60	–0.78
0.20	0.74	1.26	0.79	1.04	–0.74	–1.26	–0.79	–1.04
0.25	0.92	1.57	0.98	1.29	–0.92	–1.57	–0.98	–1.29
0.30	1.08	1.86	1.17	1.53	–1.08	–1.86	–1.17	–1.53
0.35	1.25	2.17	1.35	1.79	–1.25	–2.17	–1.35	–1.79
0.40	1.40	2.46	1.52	2.03	–1.40	–2.46	–1.52	–2.03
0.45	1.54	2.74	1.69	2.26	–1.54	–2.74	–1.69	–2.26
0.50	1.68	3.02	1.86	2.49	–1.68	–3.02	–1.86	–2.49
0.55	1.81	3.30	2.02	2.72	–1.81	–3.30	–2.02	–2.72
0.60	1.92	3.57	2.17	2.94	–1.92	–3.57	–2.17	–2.94
0.65	2.02	3.83	2.32	3.15	–2.02	–3.83	–2.32	–3.15
0.70	2.11	4.08	2.46	3.36	–2.11	–4.08	–2.46	–3.36
0.75	2.19	4.31	2.58	3.55	–2.19	–4.31	–2.58	–3.55
0.80	2.25	4.54	2.70	3.74	–2.25	–4.54	–2.70	–3.74
0.85	2.30	4.74	2.81	3.91	–2.30	–4.74	–2.81	–3.91
0.90	2.34	4.92	2.89	4.05	–2.34	–4.92	–2.89	–4.05
0.95	2.37	5.08	2.97	4.23	–2.37	–5.08	–2.97	–4.23
1.00	2.41	5.20	3.04	4.33	–2.41	–5.20	–3.04	–4.33
1.05	2.43	5.31	3.09	4.44	–2.43	–5.31	–3.09	–4.44
1.10	2.46	5.41	3.14	4.52	–2.46	–5.41	–3.14	–4.52
1.15	2.48	5.48	3.19	4.59	–2.48	–5.48	–3.19	–4.59
1.20	2.50	5.55	3.23	4.65	–2.50	–5.55	–3.23	–4.65

Output Impedance = 240 Ohms, I-V Curves After ZQRESET



Output Impedance = 240 Ohms, I-V Curves After Calibration



Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Definitions and Calculations

Symbol	Description	Calculation	Notes
^{t}CK(avg) and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit ^{t}CK(avg) represents the actual clock average ^{t}CK(avg)of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. ^{t}CK(avg)can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$t_{CK(avg)} = \left(\sum_{j=1}^{N} t_{CK_j}\right)/N$ Where N = 200	
^{t}CK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
^{t}CH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$t_{CH(avg)} = \left(\sum_{j=1}^{N} t_{CH_j}\right)/(N \times t_{CK(avg)})$ Where N = 200	
^{t}CL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$t_{CL(avg)} = \left(\sum_{j=1}^{N} t_{CL_j}\right)/(N \times t_{CK(avg)})$ Where N = 200	
^{t}JIT(per)	The single-period jitter defined as the largest deviation of any signal ^{t}CK from ^{t}CK(avg).	$t_{JIT(per)} = \text{min/max of} \left(t_{CK_i} - t_{CK(avg)}\right)$ Where i = 1 to 200	1
^{t}JIT(per),act	The actual clock jitter for a given system.		
^{t}JIT(per), allowed	The specified clock period jitter allowance.		
^{t}JIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. ^{t}JIT(cc) defines the cycle-to-cycle jitter.	$t_{JIT(cc)} = \text{max of} \left(t_{CK_{i+1}} - t_{CK_i}\right)$	1
^{t}ERR(nper)	The cumulative error across n multiple consecutive cycles from ^{t}CK(avg).	$t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j}\right) - (n \times t_{CK(avg)})$	1
^{t}ERR(nper),act	The actual cumulative error over n cycles for a given system.		
^{t}ERR(nper), allowed	The specified cumulative error allowance over n cycles.		
^{t}ERR(nper),min	The minimum ^{t}ERR(nper).	$t_{ERR(nper),min} = (1 + 0.68LN(n)) \times t_{JIT(per),min}$	2

Symbol	Description	Calculation	Notes
^{t}ERR(nper),max	The maximum ^{t}ERR(nper).	^{t}ERR(nper),max = (1 + 0.68LN(n)) × ^{t}JIT(per),max	2
^{t}JIT(duty)	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	^{t}JIT(duty),min = MIN((^{t}CH(abs),min – ^{t}CH(avg),min), (^{t}CL(abs),min – ^{t}CL(avg),min)) × ^{t}CK(avg) ^{t}JIT(duty),max = MAX((^{t}CH(abs),max – ^{t}CH(avg),max), (^{t}CL(abs),max – ^{t}CL(avg),max)) × ^{t}CK(avg)	

Notes:
1. Not subject to production testing.
2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

tCK(abs), tCH(abs), and tCL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

tCK(abs), tCH(abs), and tCL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min ^{2}/^{t}CK(avg)min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min ^{2}/^{t}CK(avg)min	^{t}CK(avg)

Notes:
1. tCK(avg),min is expressed in ps for this table.
2. tJIT(duty),min is a negative value

Clock Period Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (tJIT(per)) in excess of the values found in the AC Timing section. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized

and verified to support tnPARAM = RU[tPARAM/tCK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks or tCK(avg), may need to be increased based on the values for each core timing parameter.

Cycle Time Derating for Core Timing Parameters

For a given number of clocks (tnPARAM), when tCK(avg) and tERR(tnPARAM) exceed tERR(tnPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{t_{PARAM} + t_{ERR}(t_{nPARAM),act} - t_{ERR}(t_{nPARAM),allowed}}{t_{nPARAM}} - t_{CK(avg)}\right), 0\right\}$$

Conduct cycle time derating analysis for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (tnPARAM), clock cycle derating should be specified with tJIT(per). For a given number of clocks (tnPARAM), when tCK(avg) and (tERR(tnPARAM),act) exceed the supported cumulative tERR(tnPARAM),allowed, if the equation below results in a positive value for a core timing parameter (tCORE), the required clock cycle derating (in clocks) will be that positive value.

$$\text{ClockCycleDerating} = RU\left\{\frac{t_{PARAM} + t_{ERR}(t_{nPARAM),act} - t_{ERR}(t_{nPARAM),allowed}}{t_{CK(avg)}}\right\} - t_{nPARAM}$$

Conduct cycle-time derating analysis for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb) are measured from a command/address signal (CKE, CS, or CA[9:0]) transition edge to its respective clock signal (CK/CK#) crossing. The specification values are not affected by the tJIT(per) applied, as the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

tRPRE

When the device is operated with input clock jitter, tRPRE must be derated by the tJIT(per),act,max of the input clock that exceeds tJIT(per),allowed,max. Output deratings are relative to the input clock.

$$t_{RPRE(min,derated)} = 0.9 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}} \right)$$

For example, if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500ps, tJIT(per),act,min = –172ps, and JIT(per),act,max = +193ps, then tRPRE,min, derated = 0.9 - (tJIT(per), act,max - tJIT(per), allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500 = 0.8628 tCK(avg).

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal transition (DMn or DQm, where: n = 0, 1, 2, or 3; and m = DQ[31:0]), and specified timings must be met with respect to that clock edge. Therefore, they are not affected by tJIT(per).

tQSH, tQSL

These parameters are affected by duty cycle jitter, represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min. tQSH(abs)min = tCH(abs)min - 0.05 tQSL(abs)min = tCL(abs)min - 0.05. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = min [(tQSH(abs)min × tCK(avg)min - tDQSQmax - tQHSmax), (tQSL(abs)min × tCK(avg)min - tDQSQmax - tQHSmax)]. This minimum data-valid window must be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter, represented by tCL(abs). Therefore, tRPST(abs)min can be specified by tCL(abs)min. tRPST(abs)min = tCL(abs)min - 0.05 = tQSL(abs)min.

Clock Jitter Effects on WRITE Timing Parameters

tDS, tDH

These parameters are measured from a data signal (DMn or DQm, where n = 0, 1, 2, 3; and m = DQ[31:0]) transition edge to its respective data strobe signal (DQSn, DQSn#: n = 0,1,2,3) crossing. The specification values are not affected by the amount of tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDSS, tDSH

These parameters are measured from a data strobe signal crossing (DQSx, DQSx#) to its clock signal crossing (CK/CK#). The specification values are not affected by the amount of tJIT(per)) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

tDQSS

This parameter is measured from the clock signal (CK, CK#) crossing to the first latching data strobe signal (DQSx, DQSx#) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual tJIT(per),act of the input clock in excess of tJIT(per),allowed.

$$t_{DQSS(min,derated)} = 0.75 - \left(\frac{t_{JIT(per),act,min} - t_{JIT(per),allowed,min}}{t_{CK(avg)}}\right)$$

$$t_{DQSS(max,derated)} = 1.25 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}}\right)$$

For example, if the measured jitter into an LPDDR2-800 device has tCK(avg) = 2500ps, tJIT(per),act,min = -172ps, and tJIT(per),act,max = +193ps, then:

tDQSS,(min,derated) = 0.75 - (tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = 0.7788 tCK(avg), and tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg).

ORDERING INFORMATION

Commercial Range: T_C = 0°C to +85°C

Clock	Speed Grade	Order Part No.	Organization	Package
333 MHz	-3	IS43LD16160B-3BL	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-3BL	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
400 MHz	-25	IS43LD16160B-25BL	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-25BL	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
533 MHz	-18	IS43LD16160B-18BL	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-18BL	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free

Industrial Range: T_C = -40°C to +85°C

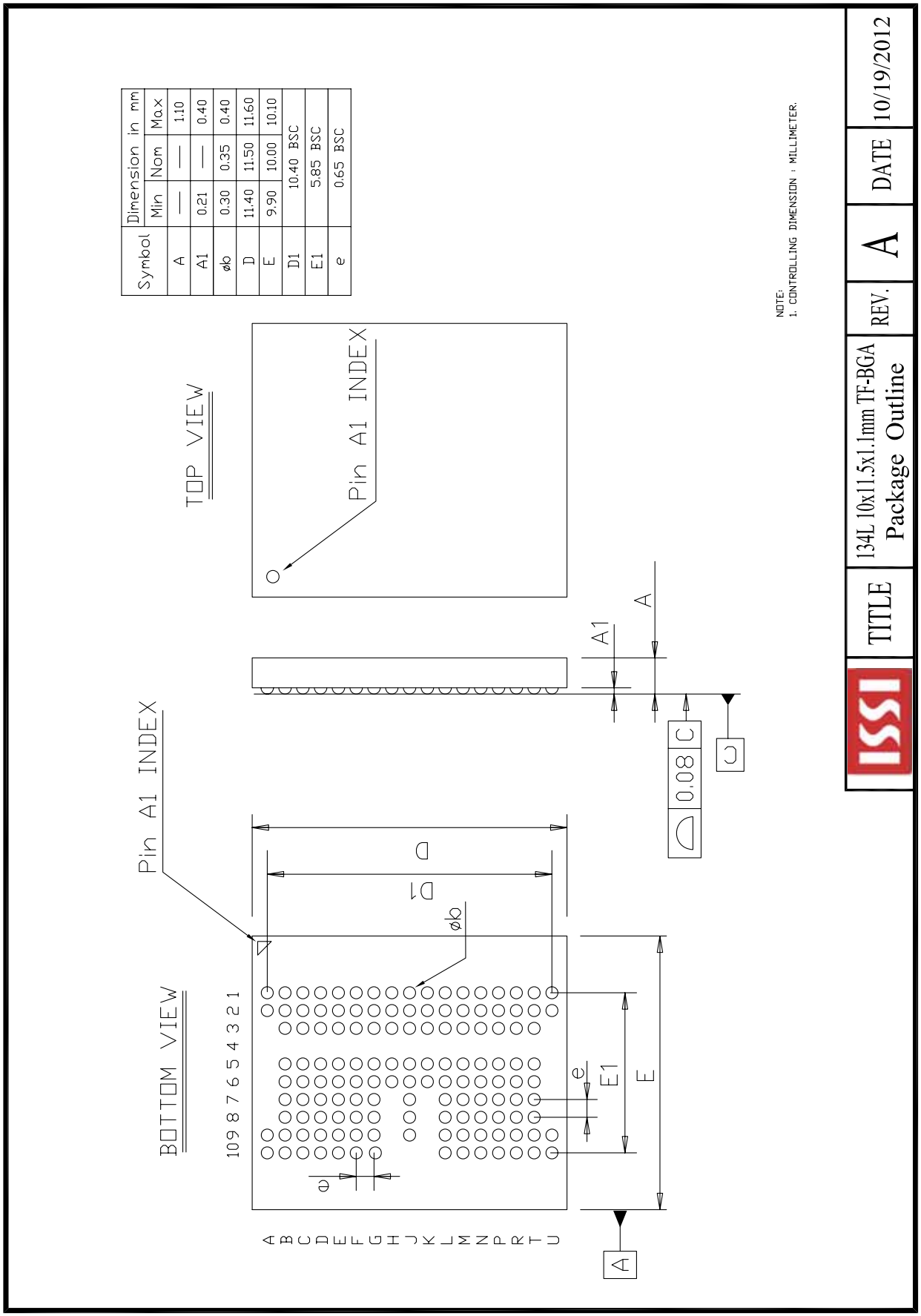
Clock	Speed Grade	Order Part No.	Organization	Package
333 MHz	-3	IS43LD16160B-3BLI	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-3BLI	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
400 MHz	-25	IS43LD16160B-25BLI	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-25BLI	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
533 MHz	-18	IS43LD16160B-18BLI	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS43LD32800B-18BLI	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free

Automotive, A1 Range: T_C = -40°C to +85°C

Clock	Speed Grade	Order Part No.	Organization	Package
333 MHz	-3	IS46LD16160B-3BLA1	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-3BLA1	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-3BPLA1	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free
400 MHz	-25	IS46LD16160B-25BLA1	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-25BLA1	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-25BPLA1	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free
533 MHz	-18	IS46LD16160B-18BLA1	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-18BLA1	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-18BPLA1	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free

Automotive, A2 Range: T_C = -40°C to +105°C

Clock	Speed Grade	Order Part No.	Organization	Package
333 MHz	-3	IS46LD16160B-3BLA2	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-3BLA2	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-3BPLA2	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free
400 MHz	-25	IS46LD16160B-25BLA2	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-25BLA2	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-25BPLA2	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free
533 MHz	-18	IS46LD16160B-18BLA2	16Mb x 16, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-18BLA2	8Mb x 32, LPDDR2-S4	134 ball FBGA, lead free
		IS46LD32800B-18BPLA2	8Mb x 32, LPDDR2-S4	168 ball PoP FBGA, lead free


Symbol
Dimension in mm
Min
Nom
Max
A — — 1.10
A1 0.21 — 0.40
øb 0.30 0.35 0.40
D 11.40 11.50 11.60
E 9.90 10.00 10.10
D1 10.40 BSC
E1 5.85 BSC
e 0.65 BSC
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
TOP VIEW
Pin A1 INDEX
A1
A
0.08 C
C
Pin A1 INDEX
BOTTOM VIEW
1 2 3 4 5 6 7 8 9 10
A B C D E F G H J K L M N P R T U
D
D1
øb
e
E1
E
A
TITLE
134L 10x11.5x1.1mm TF-BGA
Package Outline
REV.
A
DATE
10/19/2012