IS61LP6436A
IS61LP6432A

Long-term Support
World Class Quality

64K x 32, 64K x 36 SYNCHRONOUS PIPELINED STATIC RAM

MAY 2017

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP package
- Power-down snooze mode
- Power Supply:
  +3.3V V_{DD}
  +3.3V or 2.5V V_{DDQ} (I/O)
- Lead-free available

DESCRIPTION

The *ISSI* IS61LP6432A/36A is a high-speed synchronous static RAM designed to provide a burstable, high-performance memory for high speed networking and communication applications. The IS61LP6432A is organized as 64K words by 32 bits and the IS61LP6436A is organized as 64K words by 36 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

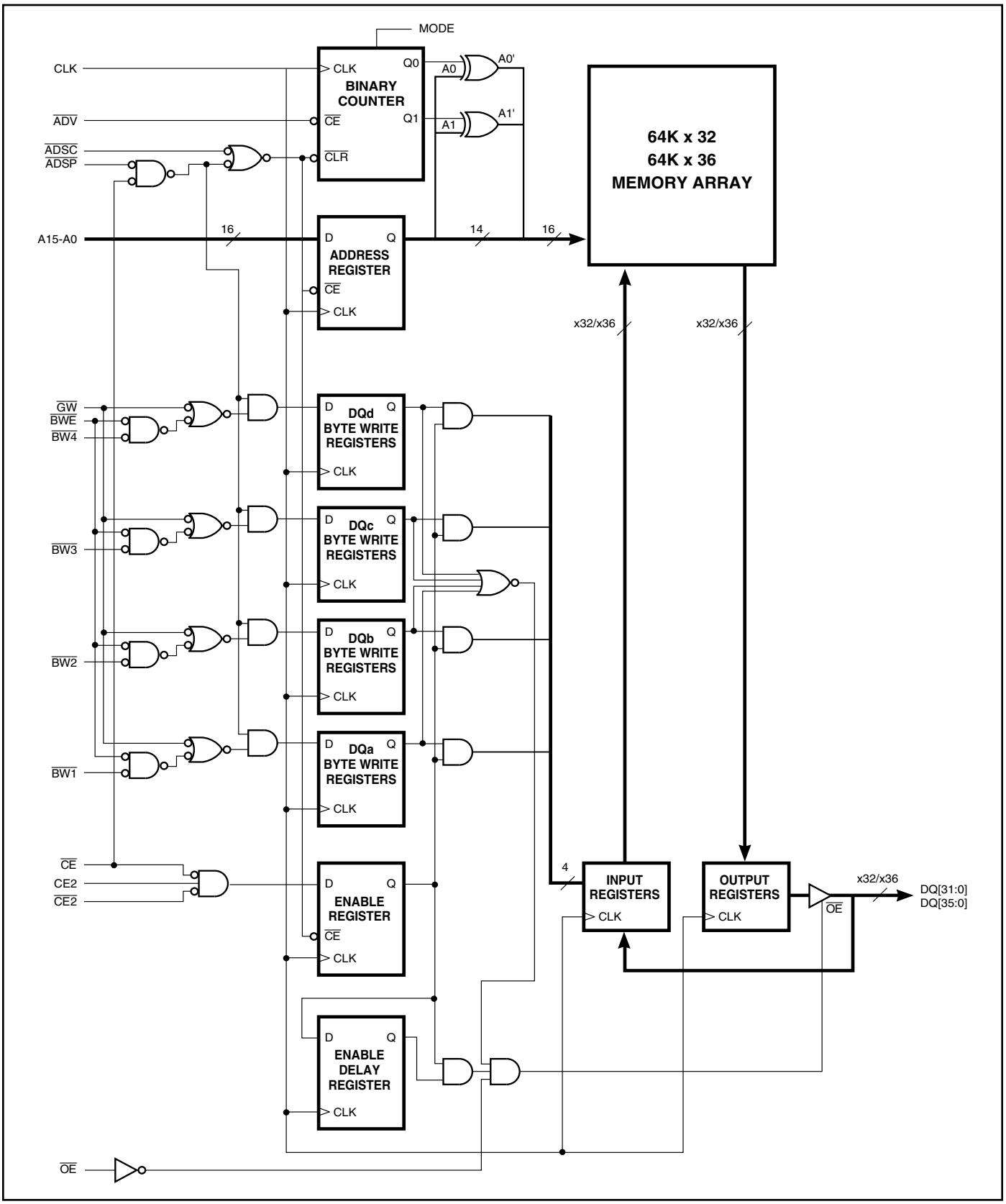
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

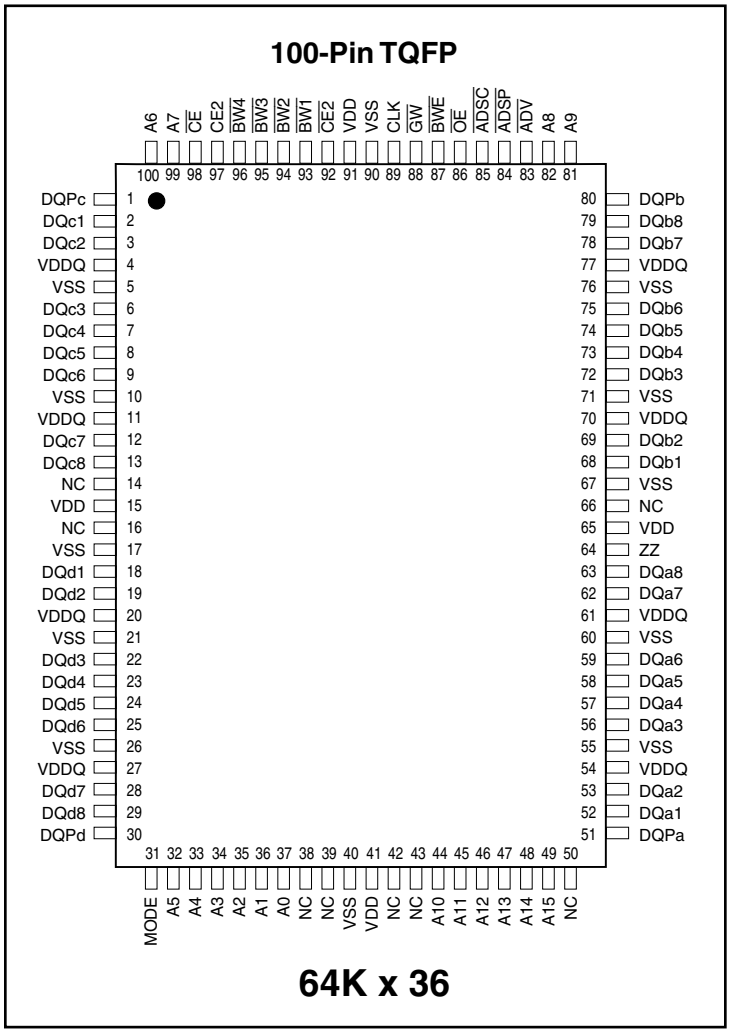
FAST ACCESS TIME

Symbol	Parameter	-166	-133	Units
t_{KQ}	Clock Access Time	3.5	4	ns
t_{KC}	Cycle Time	6	7.5	ns
	Frequency	166	133	MHz

BLOCK DIAGRAM



PIN CONFIGURATION

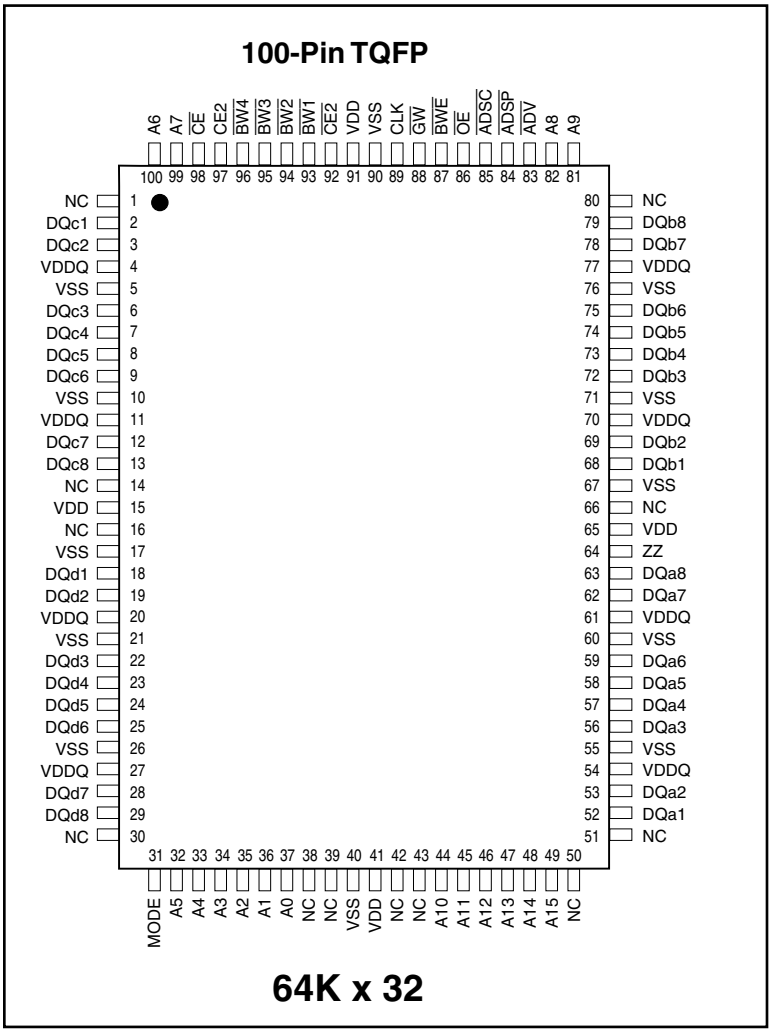


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A15	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
Vss	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION



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MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
Vss	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

TRUTH TABLE[1-8]

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa}$-d) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

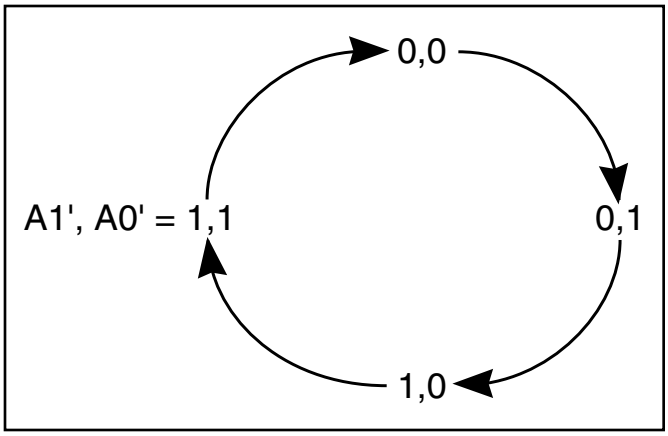
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = Vss)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to Vss for I/O Pins	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to Vss for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to Vss	–0.5 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V ± 5% 2.5V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%	3.3V ± 5% 2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			2.5V (I/O)		3.3V (I/O)		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = 1.0 mA (2.5V)	2.0	—	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	–0.3	0.8	V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$(1)	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{DDQ}$, $\overline{OE} = V_I$	–5	5	–5	5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

				-166	-133	
Symbol	Parameter	Test Conditions		Max.	Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, V_{DD} = Max. Cycle Time ≥ t_{KC} min.	Com. Ind.	190 200	180 190	mA mA
I_{SB1}	Standby Current	Device Deselected, V_{DD} = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.	Com. Ind.	70 80	70 80	mA mA
I_{ZZ}	Power-down Mode Current	ZZ = V_{DD} Clock Running All Inputs ≤ V_{SS} + 0.2V or ≥ V_{DD} – 0.2V	Com. Ind.	35 40	35 40	mA mA

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to Vss, or tied to V_{DD}.
2. The MODE pin should be tied to V_{DD} or Vss. It exhibits ±10 µA maximum leakage current when tied to ≤ Vss + 0.2V or ≥ V_{DD} – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

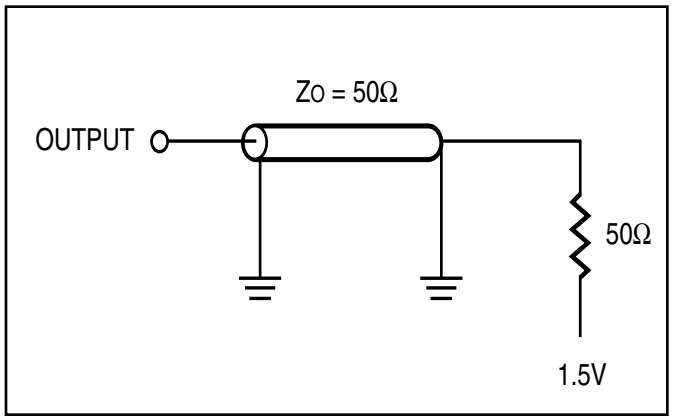


Figure 1

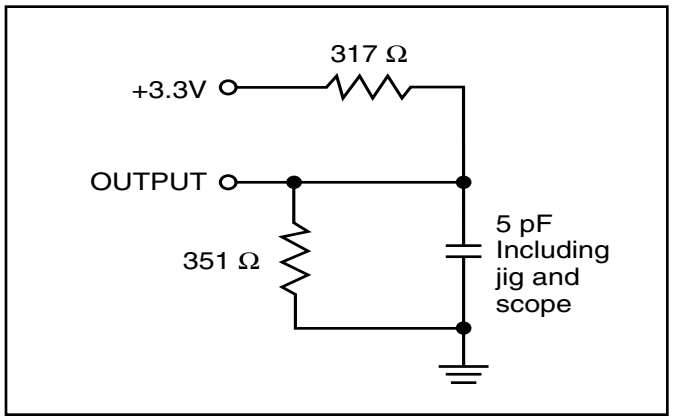


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

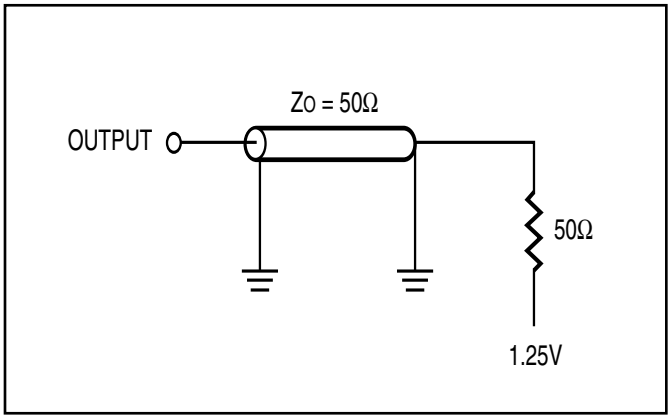


Figure 3

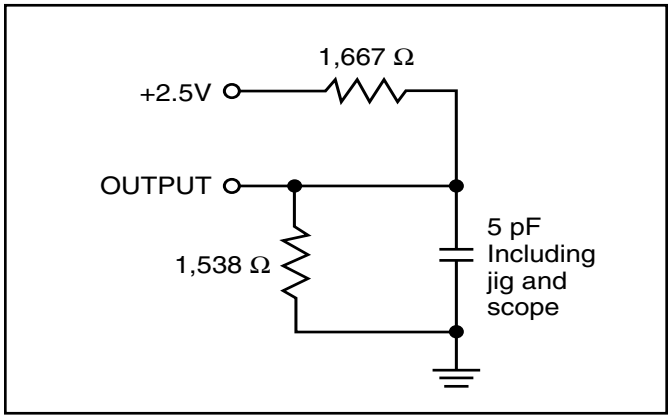


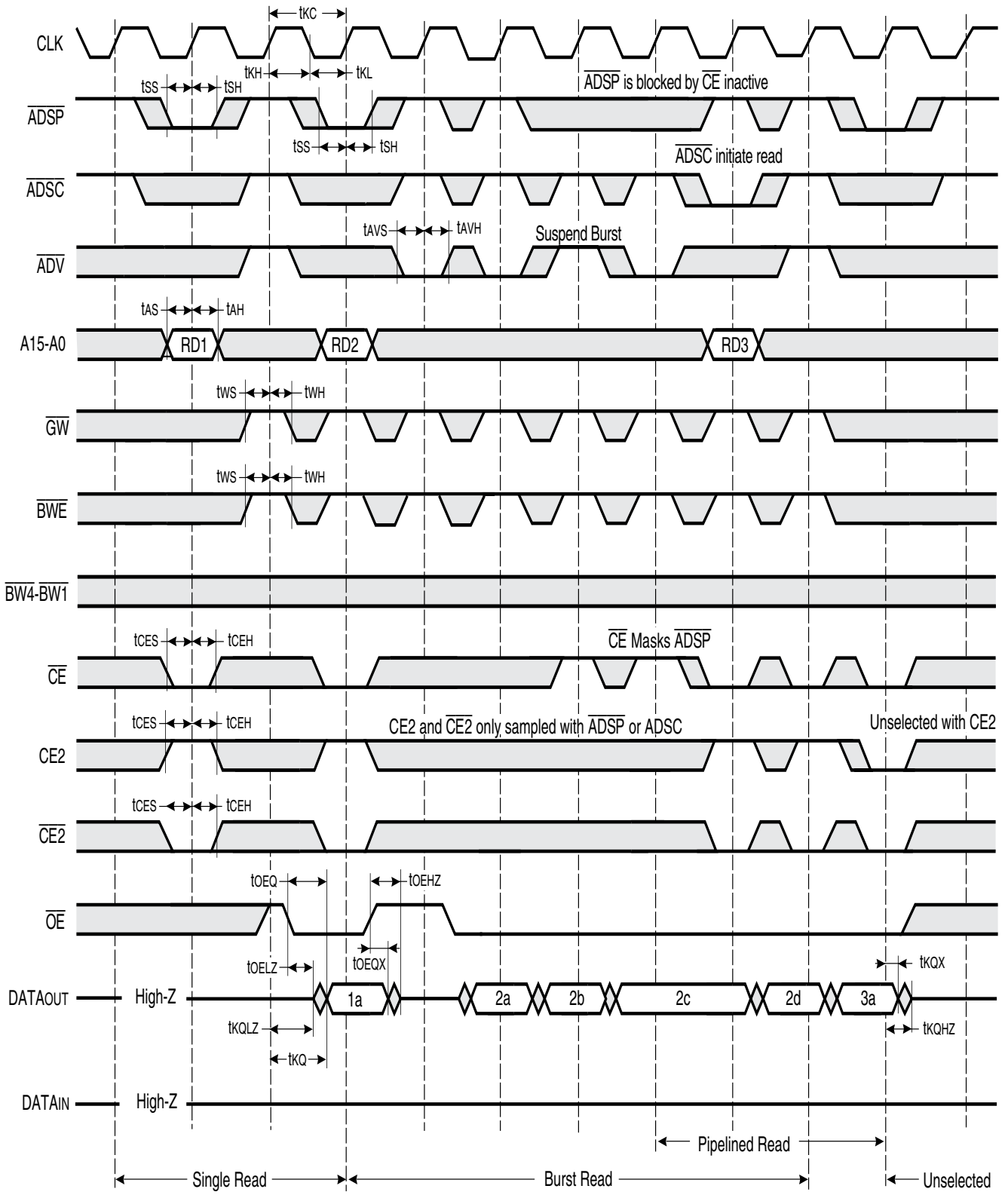
Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_{MAX}[3]	Clock Frequency	—	166	—	133	MHz
t_{KC}[3]	Cycle Time	6	—	7.5	—	ns
t_{KH}	Clock High Time	2.4	—	2.8	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.8	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	4	ns
t_{KQX}[1]	Clock High to Output Invalid	3	—	3	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.5	—	3.8	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	4.5	2	5	ns
t_{AS}[3]	Address Setup Time	2.1	—	2.1	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}[3]	Write Setup Time	1.5	—	1.5	—	ns
t_{CES}[3]	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}[3]	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}[3]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[3]	Address Status Hold Time	0.5	—	0.5	—	ns
t_{WH}[3]	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}[3]	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}[3]	Address Advance Hold Time	0.5	—	0.5	—	ns

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

READ/WRITE CYCLE TIMING

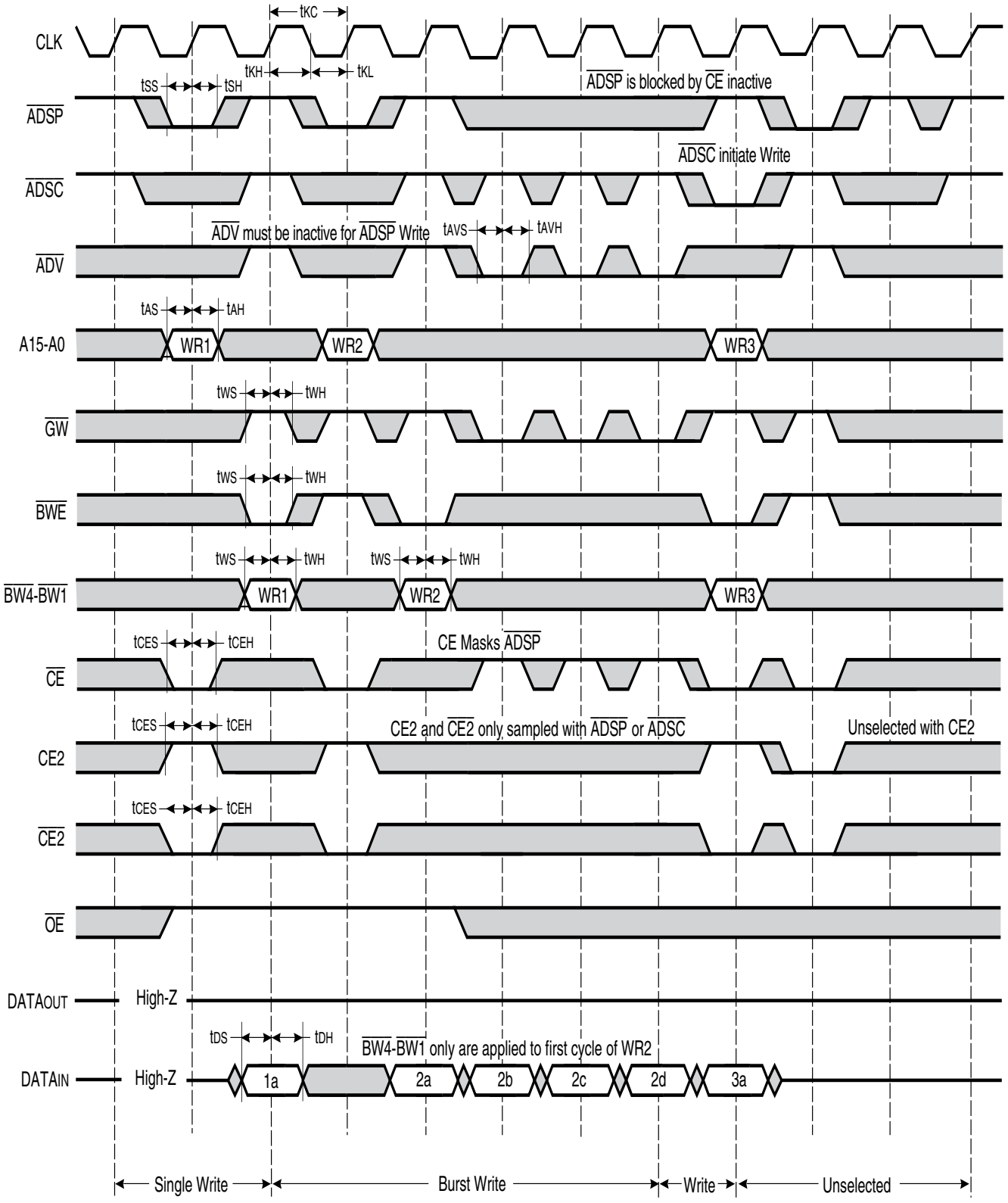


WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{KC}[1]	Cycle Time	6	—	7.5	—	ns
t_{KH}[1]	Clock High Time	2.4	—	2.8	—	ns
t_{KL}[1]	Clock Low Time	2.4	—	2.8	—	ns
t_{AS}[1]	Address Setup Time	2.1	—	2.1	—	ns
t_{SS}[1]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}[1]	Write Setup Time	1.5	—	1.5	—	ns
t_{DS}[1]	Data In Setup Time	1.5	—	1.5	—	ns
t_{CES}[1]	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AVS}[1]	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}[1]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[1]	Address Status Hold Time	0.5	—	0.5	—	ns
t_{DH}[1]	Data In Hold Time	1.0	—	1.0	—	ns
t_{WH}[1]	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}[1]	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{AVH}[1]	Address Advance Hold Time	0.5	—	0.5	—	ns

Note:
1. Tested with load in Figure 1.

WRITE CYCLE TIMING

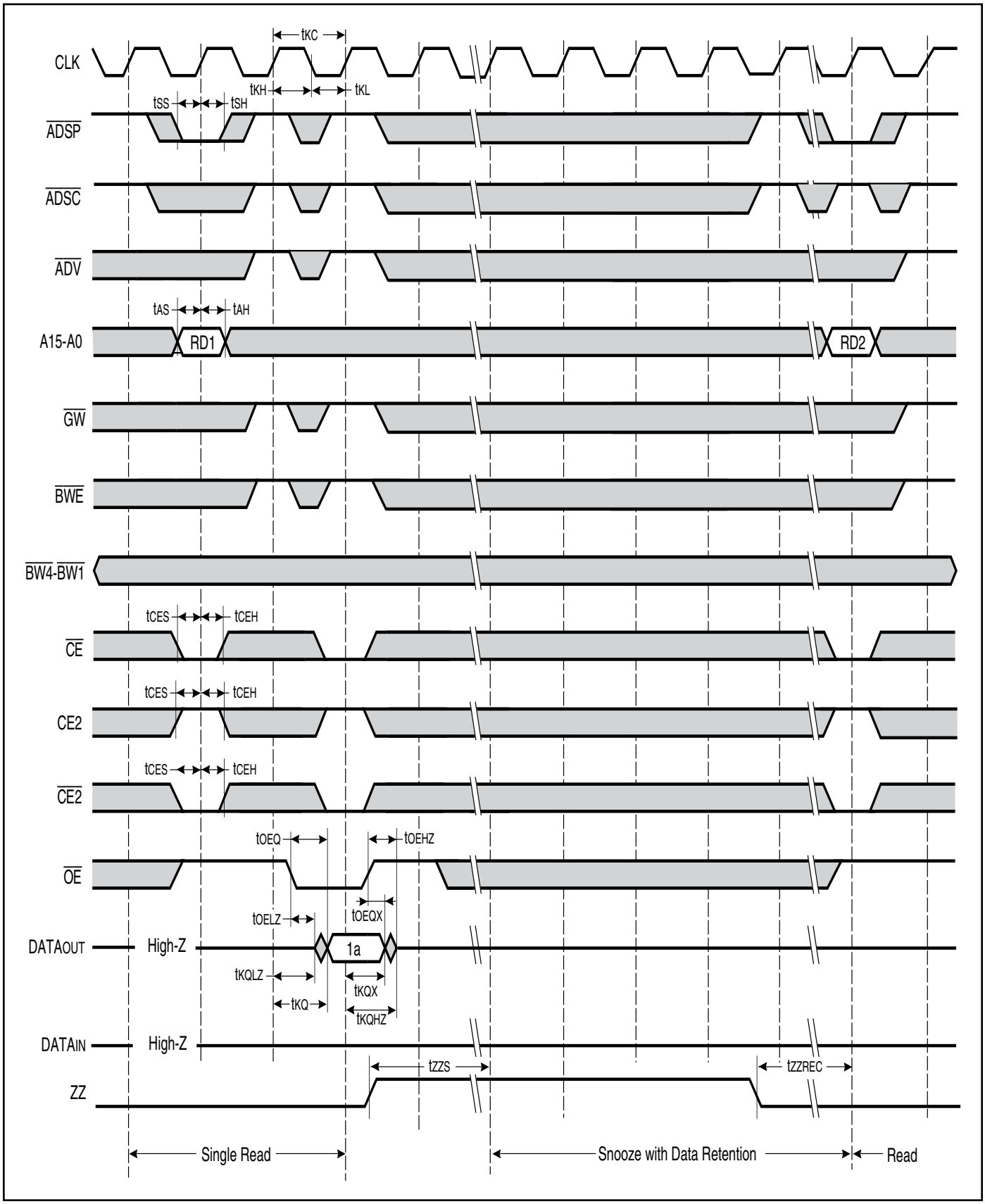


SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-133		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{KC}[3]	Cycle Time	6	—	7.5	—	ns
t_{KH}[3]	Clock High Time	2.4	—	2.8	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.8	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	4	ns
t_{KQX}[1]	Clock High to Output Invalid	1.5	—	1.5	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.5	—	3.9	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	4.5	2	5.0	ns
t_{AS}[3]	Address Setup Time	2.1	—	2.1	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{CES}[3]	Chip Enable Setup Time	1.5	—	1.5	—	ns
t_{AH}[3]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[3]	Address Status Hold Time	0.5	—	0.5	—	ns
t_{CEH}[3]	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{ZZS}	ZZ Standby	2	—	2	—	cyc
t_{ZZREC}	ZZ Recovery	2	—	2	—	cyc

Notes:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION: IS61LP6432A

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
133 MHz	IS61LP6432A-133TQLI	TQFP, Lead-free

ORDERING INFORMATION: IS61LP6436A

Industrial Range: –40°C to +85°C

Speed	Order Part Number	Package
166 MHz	IS61LP6436A-166TQLI	TQFP, Lead-free
133 MHz	IS61LP6436A-133TQLI	TQFP, Lead-free