

IS61WV10248EDBLL IS64WV10248EDBLL



1M x 8 HIGH-SPEED ASYNCHRONOUS CMOS STATIC RAM WITH ECC

APRIL 2020

FEATURES

- High-speed access times: 8, 10, 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with \overline{CE} and \overline{OE} options
- \overline{CE} power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Packages available:
 - 48-ball miniBGA (6mm x 8mm)
 - 44-pin TSOP (Type II)
- Industrial and Automotive Temperature Support
- Lead-free available

DESCRIPTION

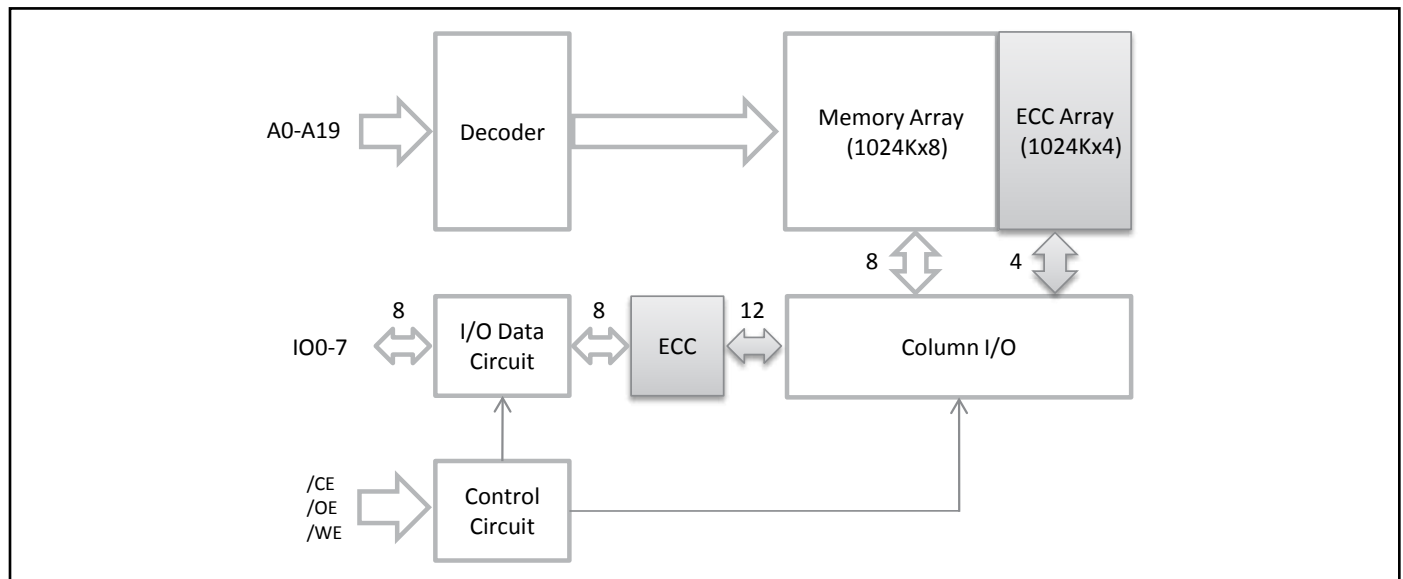
The *ISSI* IS61/64WV10248EDBLL are very high-speed, low power, 1M-word by 8-bit CMOS static RAM. The IS61/64WV10248EDBLL are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

The IS61/64WV10248EDBLL operate from a single power supply and all inputs are TTL-compatible.

The IS61/64WV10248EDBLL are available in 48 ball mini BGA (6mm x 8mm) and 44-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM



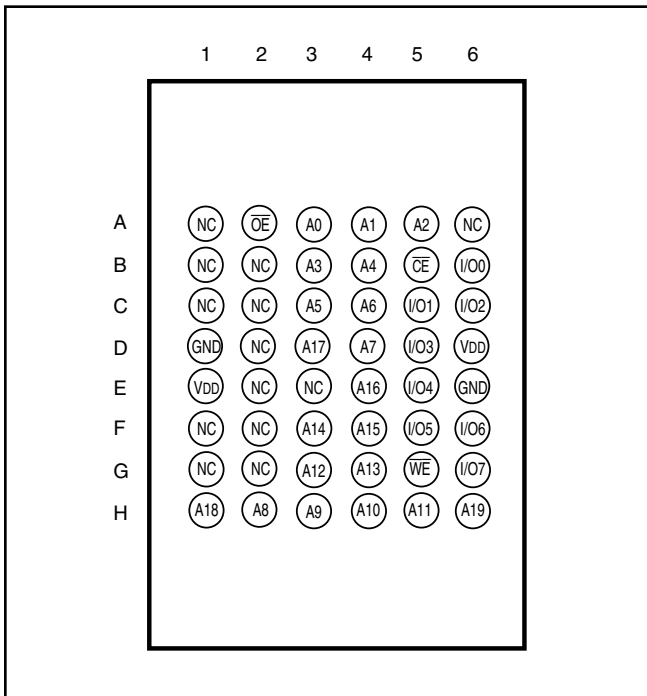
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Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

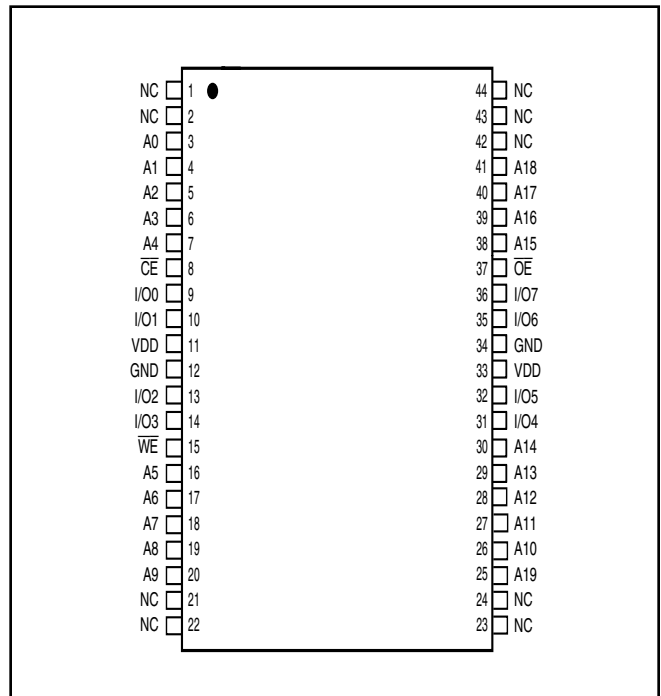
- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION

48-pin Mini BGA (B) (6mm x 8mm)



44-pin TSOP (Type II)



PIN DESCRIPTIONS

| | |
|-----------------|---------------------|
| A0-A19 | Address Inputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| I/O0-I/O7 | Data Input / Output |
| VDD | Power |
| GND | Ground |
| NC | No Connection |

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | I/O Operation | V _{DD} Current |
|------------------------------|-----------------|-----------------|-----------------|------------------|-------------------------------------|
| Not Selected (Power-down) | X | H | X | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | High-Z | I _{CC} |
| Read | H | L | L | D _{OUT} | I _{CC} |
| Write | L | L | X | D _{IN} | I _{CC} |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|-------------------------------|------|
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | V _{DD} Relates to GND | -0.3 to 4.0 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{I/O} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

OPERATING RANGE (V_{DD})¹

| Range | Ambient Temperature | IS61WV10248EDBLL V _{DD} (8, 10ns) | IS64WV10248EDBLL V _{DD} (10ns) |
|-----------------|---------------------|---|--|
| Industrial | -40°C to +85°C | 2.4V-3.6V | — |
| Automotive (A1) | -40°C to +85°C | — | 2.4V-3.6V |
| Automotive (A3) | -40°C to +125°C | — | 2.4V-3.6V |

Note:

1. Contact SRAM@issi.com for 1.8V option

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC with hamming code for each byte
- Detect and correct one bit error per byte
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{DD} = Min., I _{OH} = -1.0 mA | 1.8 | — | V |
| V _{OL} | Output LOW Voltage | V _{DD} = Min., I _{OL} = 1.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled | -1 | 1 | μA |

Note:

- V_{IL} (min.) = -0.3V DC; V_{IL} (min.) = -2.0V AC (pulse width ≤ 2 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width ≤ 2 ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

| Parameter | Unit (2.4V-3.6V) |
|---|-------------------------------|
| Input Pulse Level | 0.4V to V _{DD} -0.3V |
| Input Rise and Fall Times | 1.5ns |
| Input and Output Timing and Reference Level (V _{Ref}) | V _{DD} /2 |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

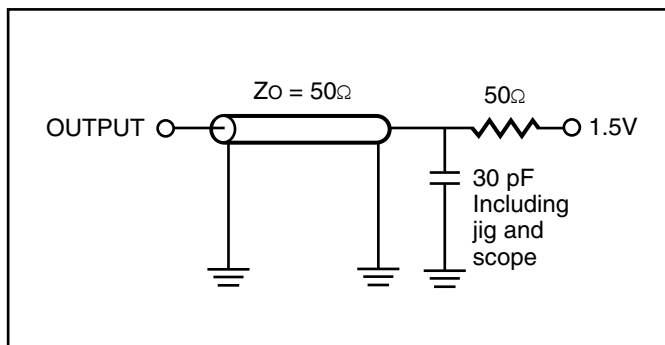


Figure 1.

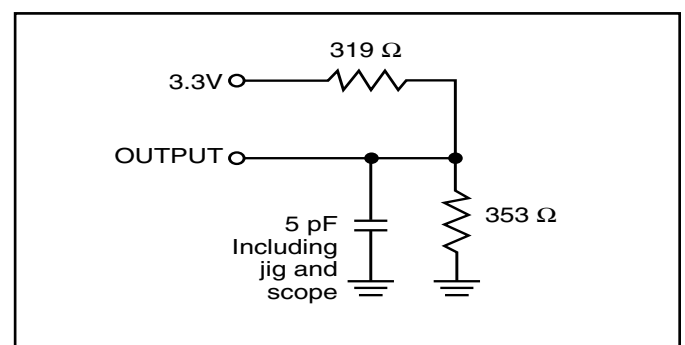


Figure 2.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | | -8 | | -10 | | -20 | | Unit |
|------------------|--|--|---------------------|------|------|------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| I _{CC} | V _{DD} Dynamic Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} | Com. | — | 50 | — | 45 | — | 35 | mA |
| | | | Ind. | — | 60 | — | 55 | — | 45 | |
| | | | Auto. | — | — | — | 65 | — | 60 | |
| | | | typ. ⁽²⁾ | | | 15 | | | | |
| I _{CC1} | Operating Supply Current | V _{DD} = Max., I _{OUT} = 0 mA, f = 0 | Com. | — | 20 | — | 20 | — | 20 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 25 | |
| | | | Auto. | — | — | — | 50 | — | 50 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0 | Com. | — | 20 | — | 20 | — | 20 | mA |
| | | | Ind. | — | 25 | — | 25 | — | 25 | |
| | | | Auto. | — | — | — | 45 | — | 45 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Com. | — | 10 | — | 10 | — | 10 | mA |
| | | | Ind. | — | 15 | — | 15 | — | 15 | |
| | | | Auto. | — | — | — | 35 | — | 35 | |
| | | | typ. ⁽²⁾ | | | 2 | | | | |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|---------------------------------|----------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 8 | — | 10 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 5.5 | — | 6.5 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | — | 3 | — | 4 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 3 | 0 | 4 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | 3 | — | ns |
| t _{PU} | Power Up Time | 0 | — | 0 | — | ns |
| t _{PD} | Power Down Time | — | 8 | — | 10 | ns |

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

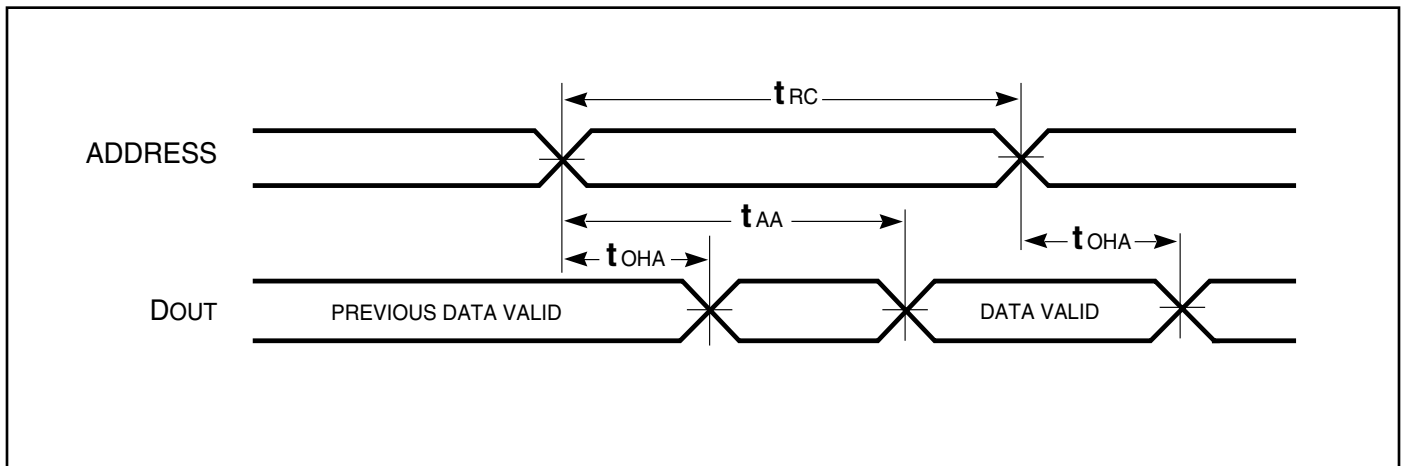
| Symbol | Parameter | -20 ns | | Unit |
|---------------------------------|----------------------------------|--------|------|------|
| | | Min. | Max. | |
| t _{RC} | Read Cycle Time | 20 | — | ns |
| t _{AA} | Address Access Time | — | 20 | ns |
| t _{OHA} | Output Hold Time | 2.5 | — | ns |
| t _{ACE} | \overline{CE} Access Time | — | 20 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 8 | ns |
| t _{HZOE⁽²⁾} | \overline{OE} to High-Z Output | 0 | 8 | ns |
| t _{LZOE⁽²⁾} | \overline{OE} to Low-Z Output | 0 | — | ns |
| t _{HZCE⁽²⁾} | \overline{CE} to High-Z Output | 0 | 8 | ns |
| t _{LZCE⁽²⁾} | \overline{CE} to Low-Z Output | 3 | — | ns |
| t _{PU} | Power Up Time | 0 | — | ns |
| t _{PD} | Power Down Time | — | 20 | ns |

Notes:

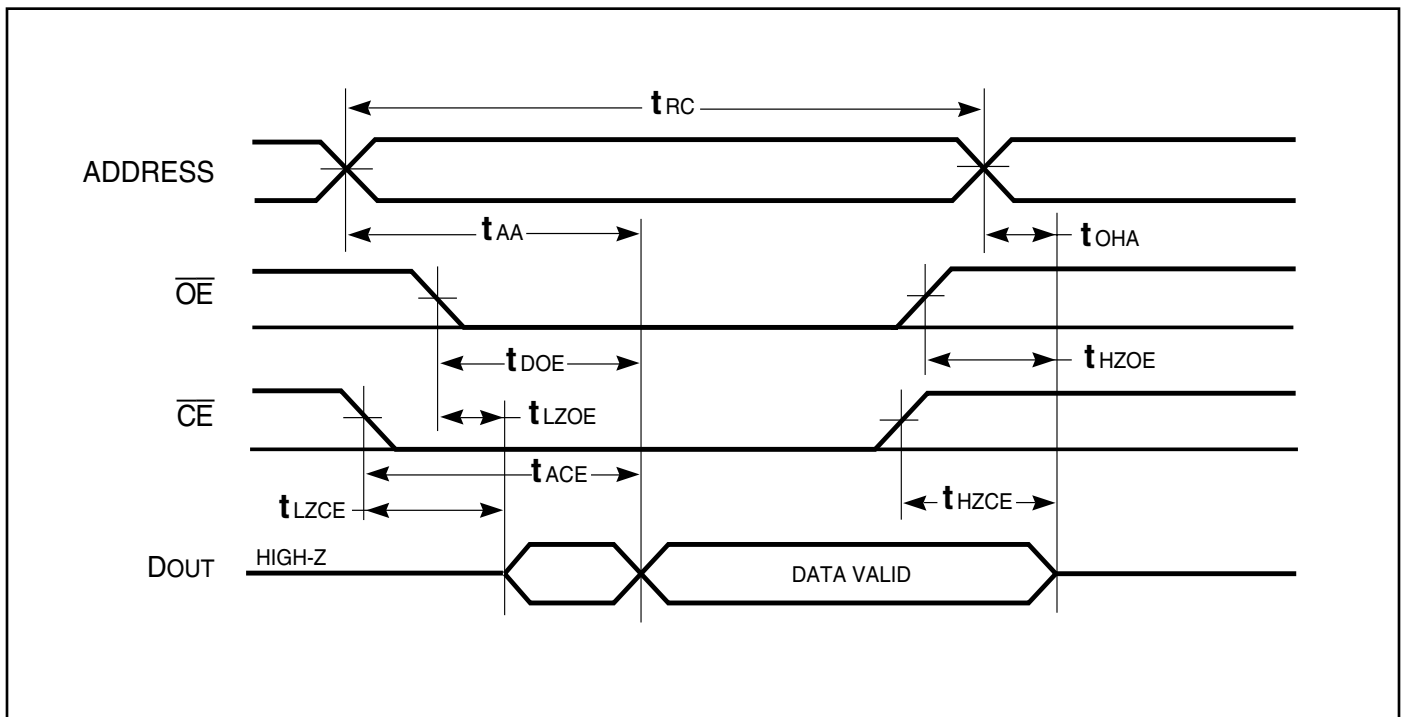
1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)



READ CYCLE NO. 2^(1,3) (\overline{CE} and \overline{OE} Controlled)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | Unit |
|----------------------------------|---|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 6.5 | — | 8 | — | ns |
| t _{AW} | Address Setup Time to Write End | 6.5 | — | 8 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 6.5 | — | 8 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 8.0 | — | 10 | — | ns |
| t _{SD} | Data Setup to Write End | 5 | — | 6 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | ns |
| t _{HZWE} ⁽²⁾ | \overline{WE} LOW to High-Z Output | — | 3.5 | — | 5 | ns |
| t _{LZWE} ⁽²⁾ | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | ns |

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

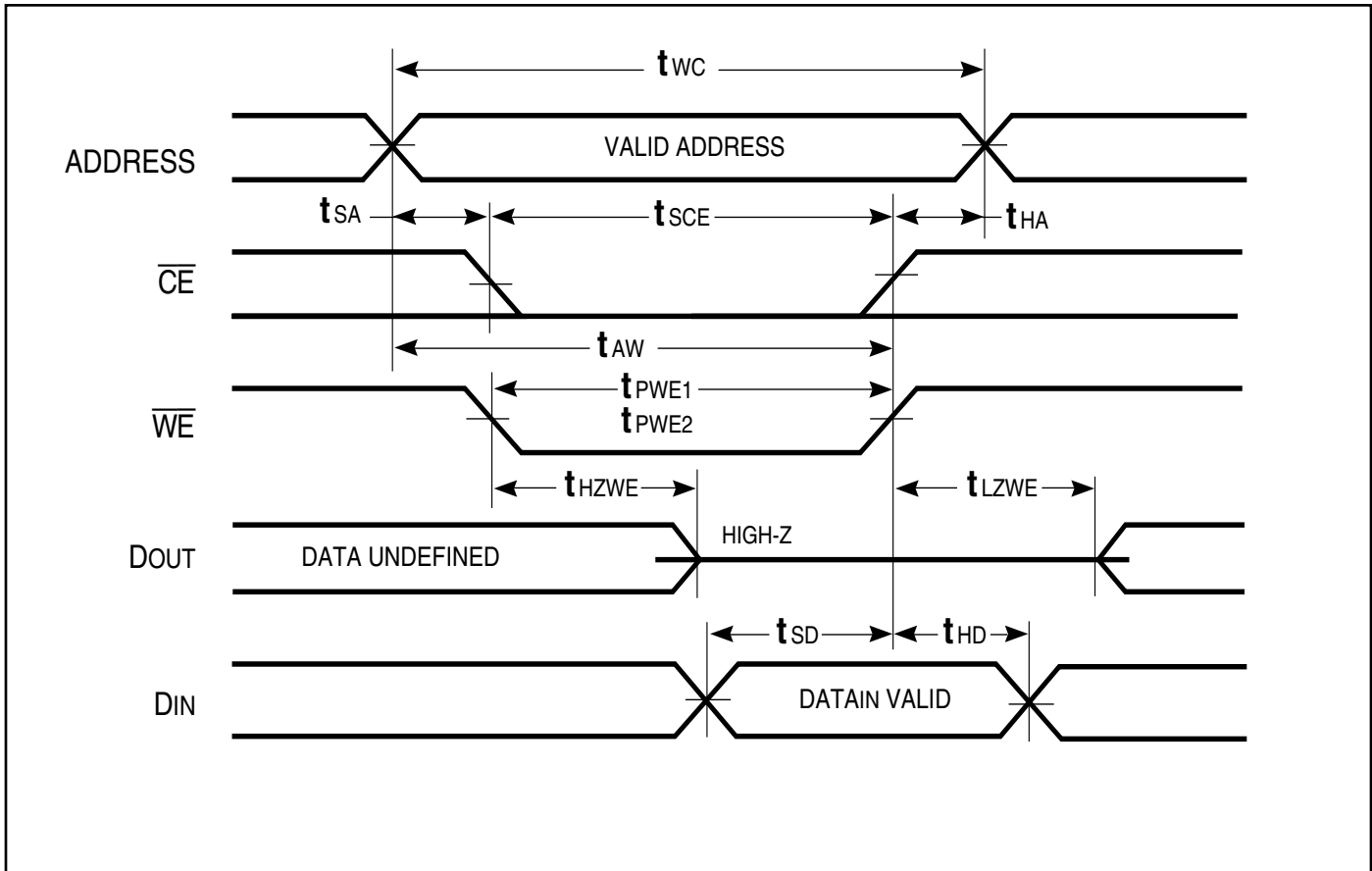
| Symbol | Parameter | -20 ns | | Unit |
|---------------------------------|---|--------|------|------|
| | | Min. | Max. | |
| t _{WC} | Write Cycle Time | 20 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 12 | — | ns |
| t _{AW} | Address Setup Time to Write End | 12 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | ns |
| t _{PWE1} | \overline{WE} Pulse Width (\overline{OE} = HIGH) | 12 | — | ns |
| t _{PWE2} | \overline{WE} Pulse Width (\overline{OE} = LOW) | 17 | — | ns |
| t _{SD} | Data Setup to Write End | 9 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 9 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 3 | — | ns |

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

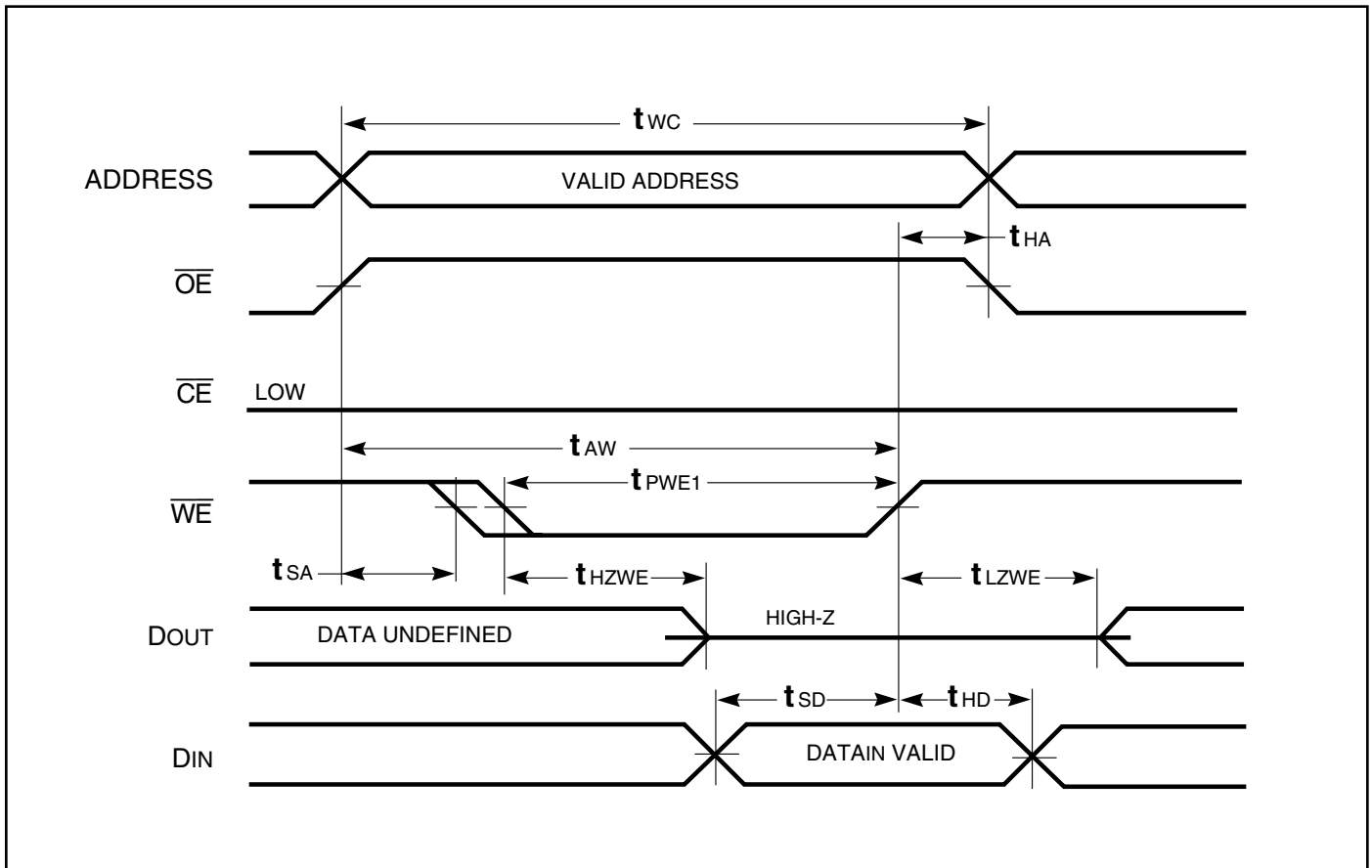
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) (\overline{CE} Controlled, \overline{OE} = HIGH or LOW)



AC WAVEFORMS

WRITE CYCLE NO. 2^(1,2) (\overline{WE} Controlled: \overline{OE} is HIGH During Write Cycle)

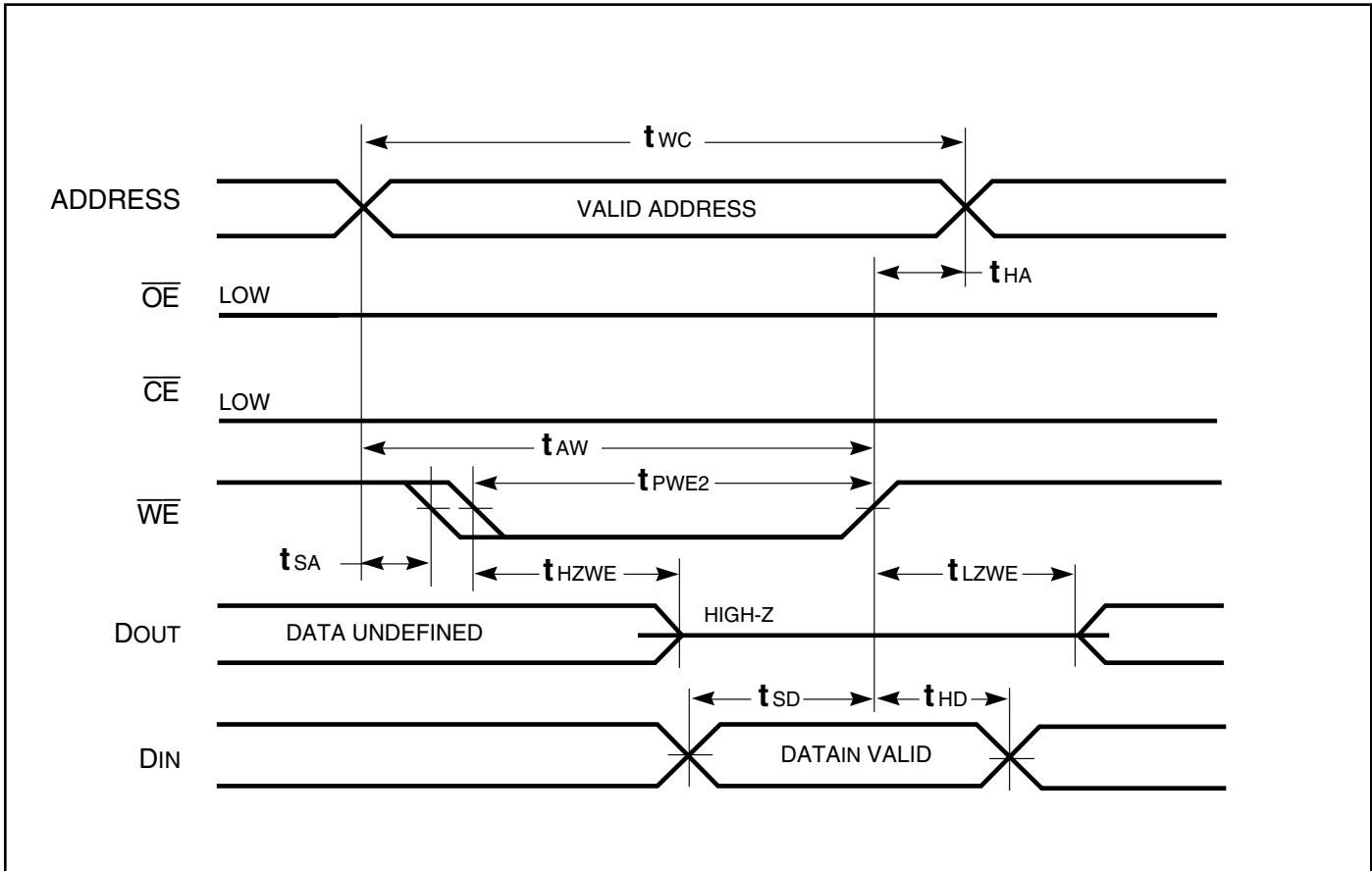


Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

AC WAVEFORMS

WRITE CYCLE NO. 3 (\overline{WE} Controlled: \overline{OE} is LOW During Write Cycle)

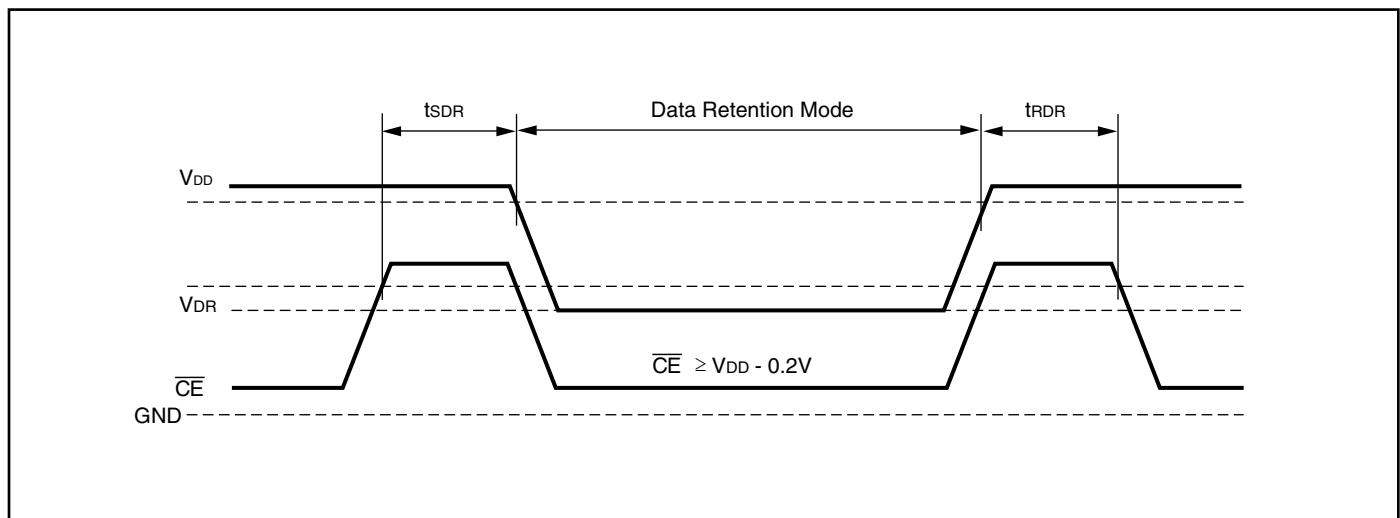


DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol | Parameter | Test Condition | Options | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|----------------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | | 2.0 | — | 3.6 | V |
| I _{DR} | Data Retention Current | V _{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com. Ind. Auto. | — | 2 | 10 15 35 | mA |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | — | — | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | — | — | ns |

Note 1: Typical values are measured at V_{DD} = V_{DR}(min), T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

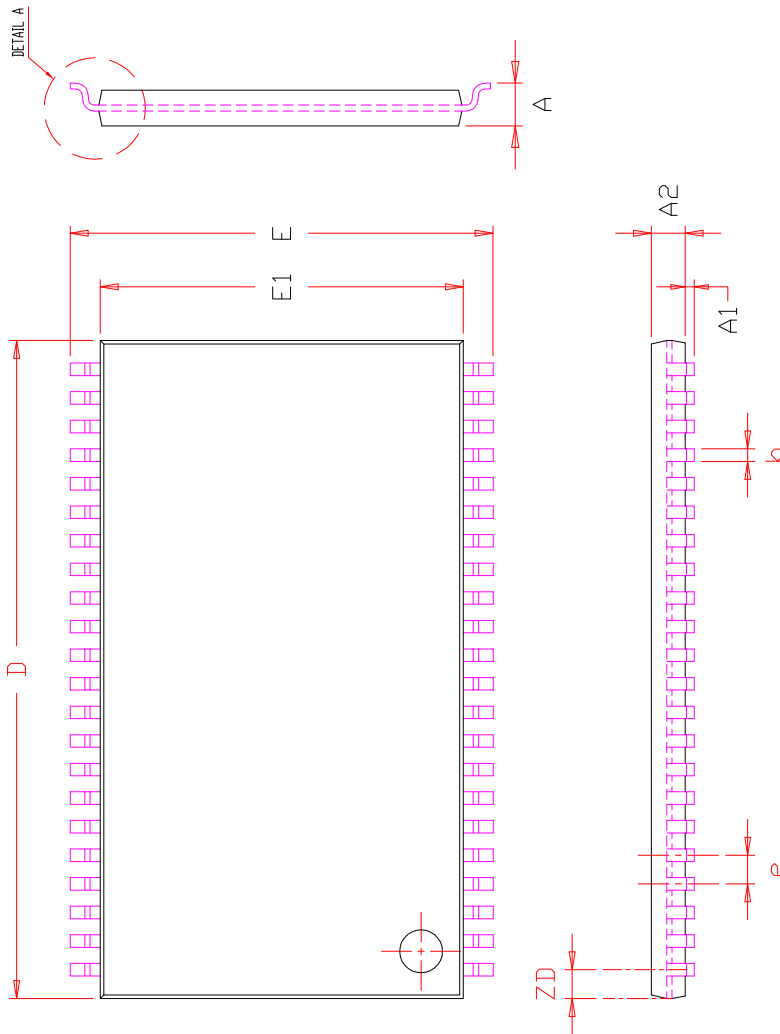
Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|------------|------------------------|------------------------------------|
| 8 | IS61WV10248EDBLL-8BLI | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS61WV10248EDBLL-8TLI | TSOP (Type II), Lead-free |
| 10 | IS61WV10248EDBLL-10BI | 48 mini BGA (6mm x 8mm) |
| | IS61WV10248EDBLL-10BLI | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS61WV10248EDBLL-10TI | TSOP (Type II) |
| | IS61WV10248EDBLL-10TLI | TSOP (Type II), Lead-free |

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

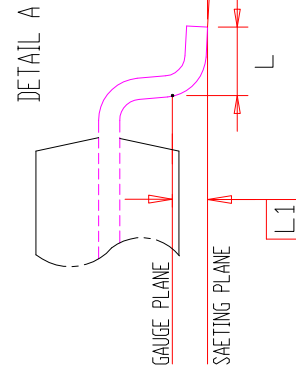
| Speed (ns) | Order Part No. | Package |
|------------|--------------------------|---|
| 10 | IS64WV10248EDBLL-10BA3 | 48 mini BGA (6mm x 8mm) |
| | IS64WV10248EDBLL-10BLA3 | 48 mini BGA (6mm x 8mm), Lead-free |
| | IS64WV10248EDBLL-10CTA3 | TSOP (Type II), Copper Leadframe |
| | IS64WV10248EDBLL-10CTLA3 | TSOP (Type II), Lead-free, Copper Leadframe |



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|-----------------|------------|-------|-------------------|------------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | | 0.45 | 0.012 | | 0.018 |
| D | 18.28 | 18.41 | 18.54 | 0.720 | 0.725 | 0.730 |
| E | 11.56 | 11.76 | 11.96 | 0.455 | 0.463 | 0.471 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 | 0.400 | 0.405 |
| e | | 0.80 BSC. | | | 0.031 BSC. | |
| L | 0.40 | | 0.69 | 0.016 | | 0.027 |
| L1 | | 0.25 BSC. | | | 0.010 BSC. | |
| ZD | | 0.805 REF. | | | 0.032 REF. | |
| ⊕ | 0 | | 8° | 0 | | 8° |

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.



| | | | | | | |
|--|-------|--------------------------------------|------|---|------|------------|
| | TITLE | 44L 400mil TSOP-2 Package Outline | REV. | F | DATE | 06/04/2008 |
| | | | | | | |