IS62/65WV2568DALL
IS62/65WV2568DBLL

256K x 8 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

JULY 2017

FEATURES

- High-speed access time: 35ns, 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.8V ± 10% Vcc (IS62/65WV2568DALL)
  - 2.5V–3.6V Vcc (IS62/65WV2568DBLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Lead-free available

DESCRIPTION

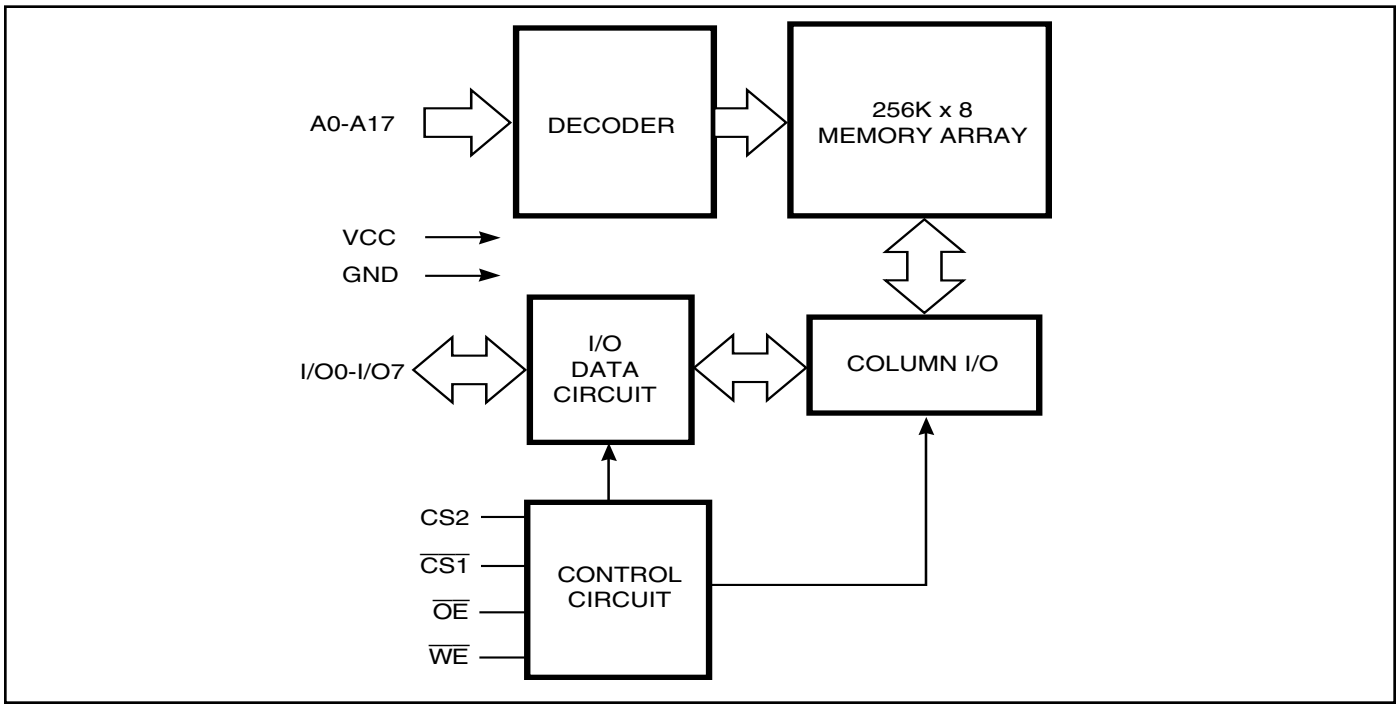
The *ISSI* IS62/65WV2568DALL and IS62/65WV2568DBLL are high-speed, 2M bit static RAMs organized as 256K words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) , the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62/65WV2568DALL and IS62/65WV2568DBLL are packaged in the JEDEC standard 32-pin TSOP (TYPE I), sTSOP (TYPE I), and 36-pin mini BGA.

FUNCTIONAL BLOCK DIAGRAM

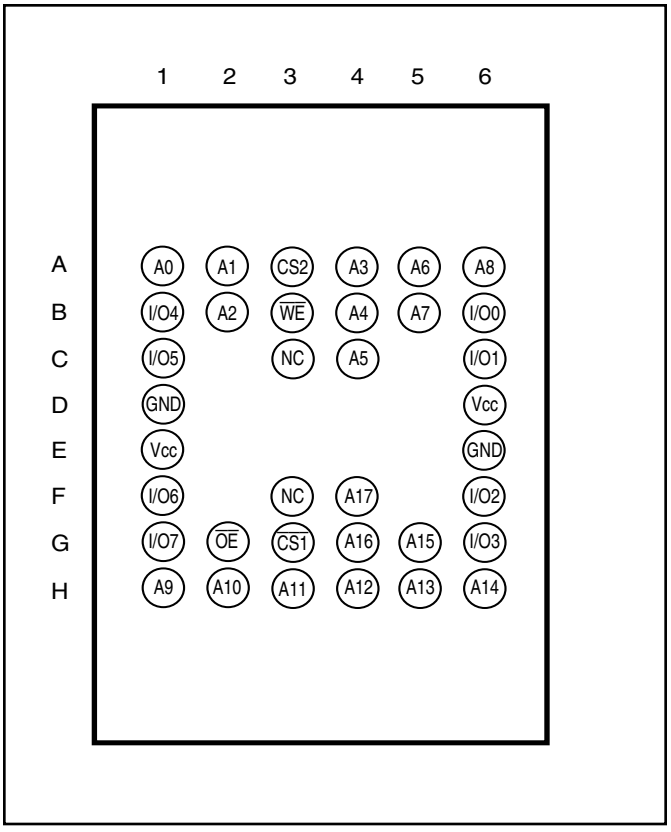


PIN DESCRIPTIONS

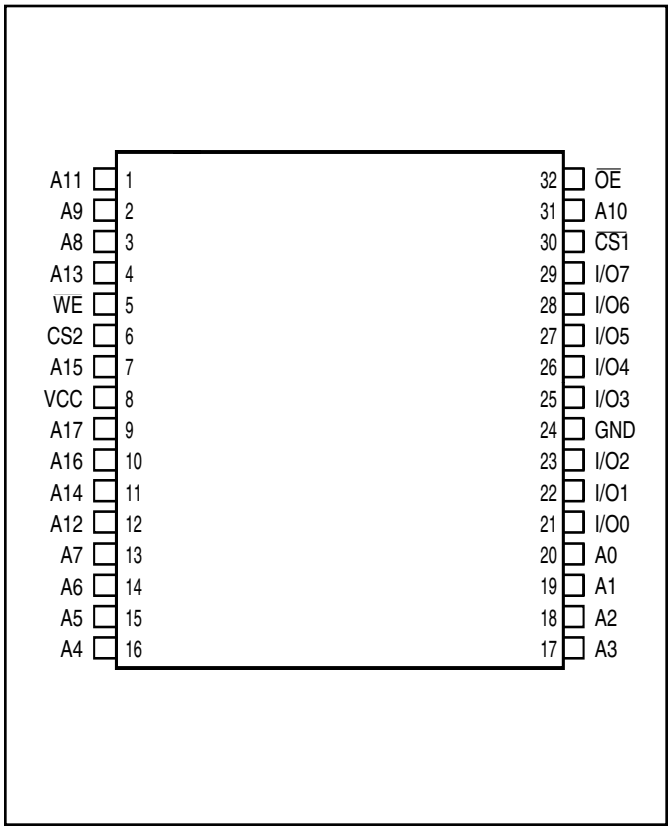
A0-A17	Address Inputs
$\overline{CS1}$	Chip Enable 1 Input
CS2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

PIN CONFIGURATION

36-pin mini BGA (B) (6mm x 8mm)



32-pin TSOP (TYPE I), sTSOP (TYPE I)



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to Vcc+0.3	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (Vcc)

Range	Ambient Temperature	IS62/65WV2568DALL	IS62/65WV2568DBLL
Commercial	0°C to +70°C	1.8V ± 10%	2.5V - 3.6V
Industrial	–40°C to +85°C	1.8V ± 10%	2.5V - 3.6V
Automotive (A3)	–40°C to +125°C	1.8V ± 10%	2.5V - 3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Vcc	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.8V ± 10%	1.4	—	V
		I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.8V ± 10%	—	0.2	V
		I_{OL} = 1.0 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage		1.8V ± 10%	1.4	V_{CC} + 0.2	V
			2.5-3.6V	2.2	V_{CC} + 0.3	V
V_{IL}(1)	Input LOW Voltage		1.8V ± 10%	–0.2	0.4	V
			2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled		–1	1	µA

Notes:
For IS62/65WV2568DALL:
V_{IL} (min.) = -1.0V AC (pluse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{CC} + 1.0V AC; (pluse width < 10ns). Not 100% tested.

For IS62/65WV2568DBLL:
V_{IL} (min.) = -2.0V AC (pluse width < 10ns). Not 100% tested.
V_{IH} (max.) = V_{CC} + 2.0V AC; (pluse width < 10ns). Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	62WV2568DALL (Unit)	62WV2568DBLL (Unit)
Input Pulse Level	0.4V to Vcc-0.2V	0.4V to Vcc-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.8V ± 10%	2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V_{REF}	0.9V	1.5V
V_{TM}	1.8V	2.8V

AC TEST LOADS

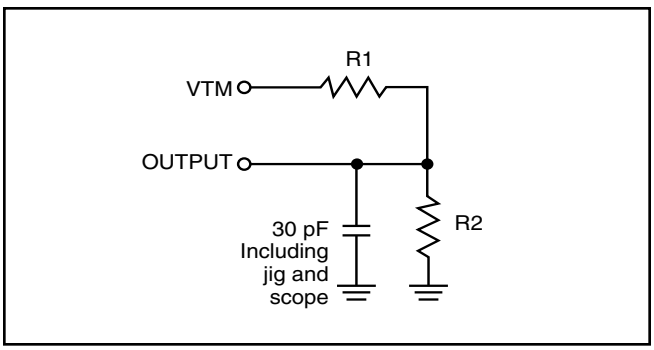


Figure 1

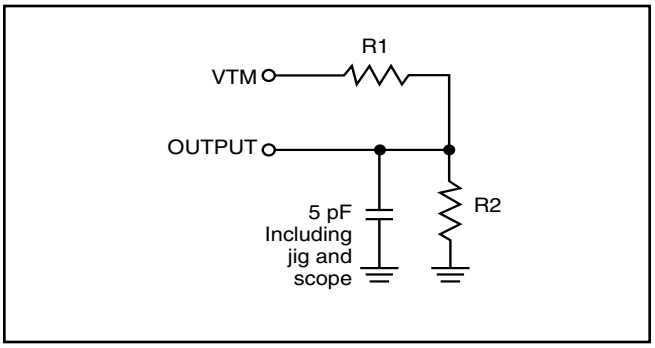


Figure 2

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 35ns	Max. 45ns	Max. 55ns	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	15	12	10	mA
			Ind.	20	15	12	
			Auto.	25	20	15	
			typ.[2]	10	8	6	
I_{SB1}	TTL Standby Current (TTL Inputs)	CS2 = VIL f = 0Hz	Com.	0.1	0.1	0.1	mA
			Ind.	0.2	0.2	0.2	
			Auto.	0.3	0.3	0.3	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	(1) 0V ≤ CS2 ≤ 0.2V OR	Com.	7	7	7	µA
			Ind.	10	10	10	
		(2) $\overline{CS1}$ ≥ VDD - 0.2V,	Auto.	–	30	30	
		CS2 ≥ VDD - 0.2V f= 0Hz	typ.[2]		3		

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{CC} = 3.0V, Ta = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

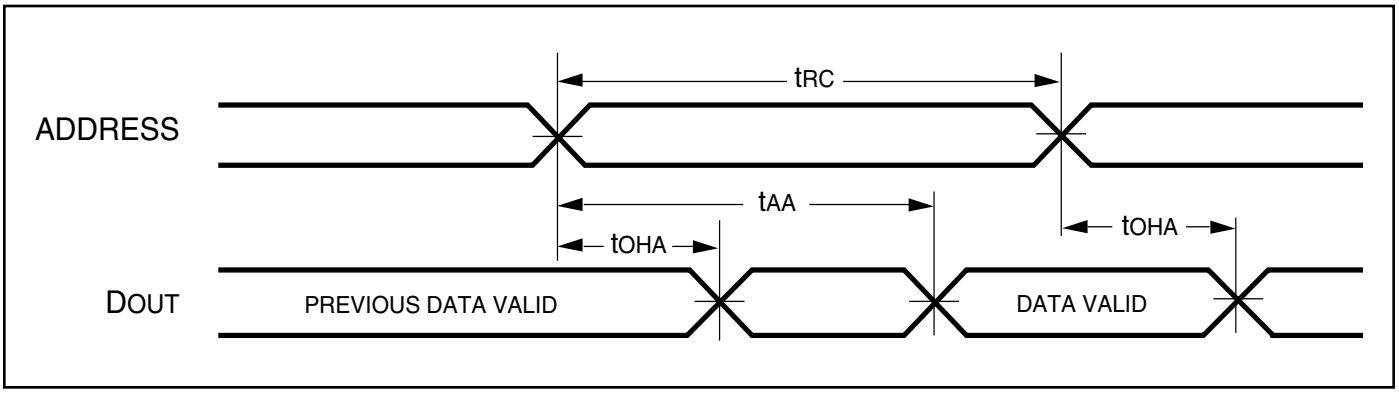
		35ns		45ns		55ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	35	—	45	—	55	ns
t_{DOE}	$\overline{OE}$ Access Time	—	15	—	20	—	25	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	10	—	15	—	20	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	10	0	15	0	20	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	10	—	ns

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

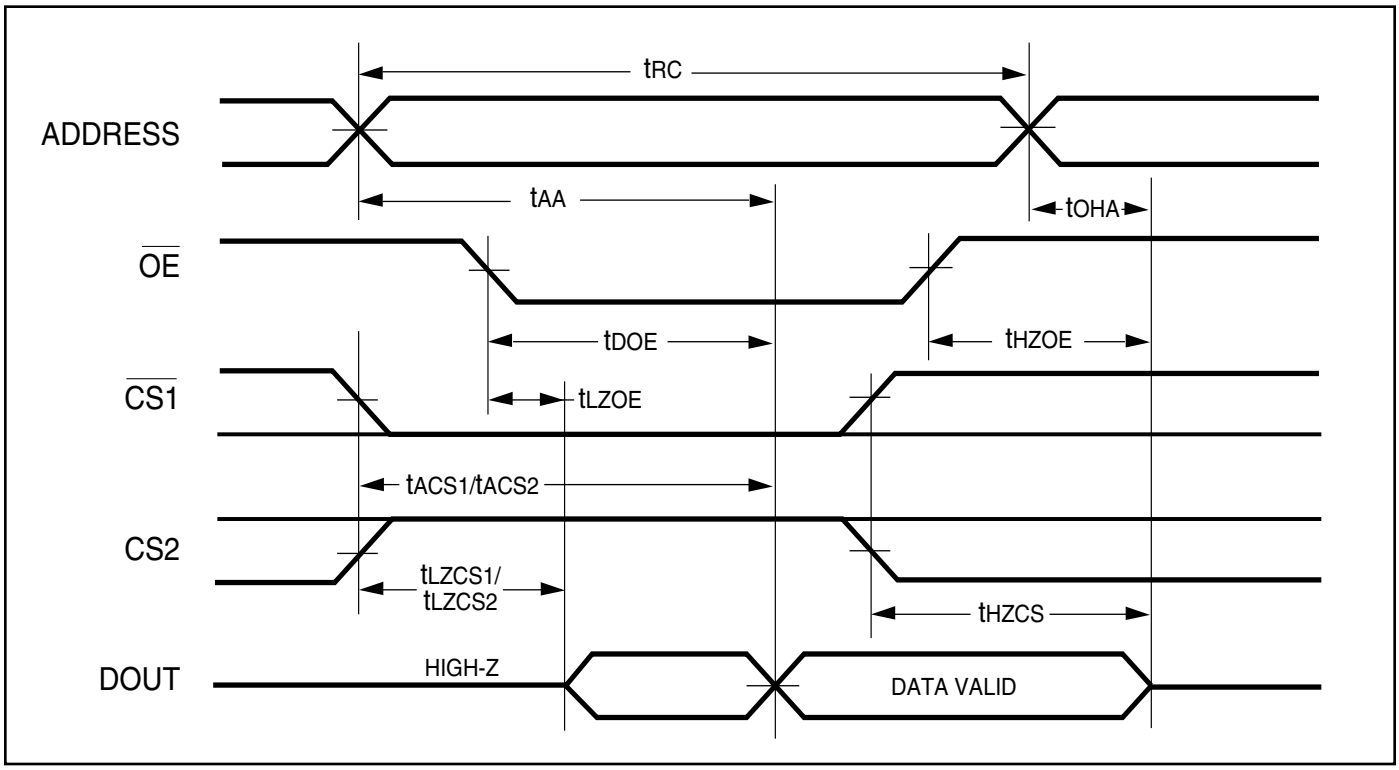
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$= V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW and CS2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

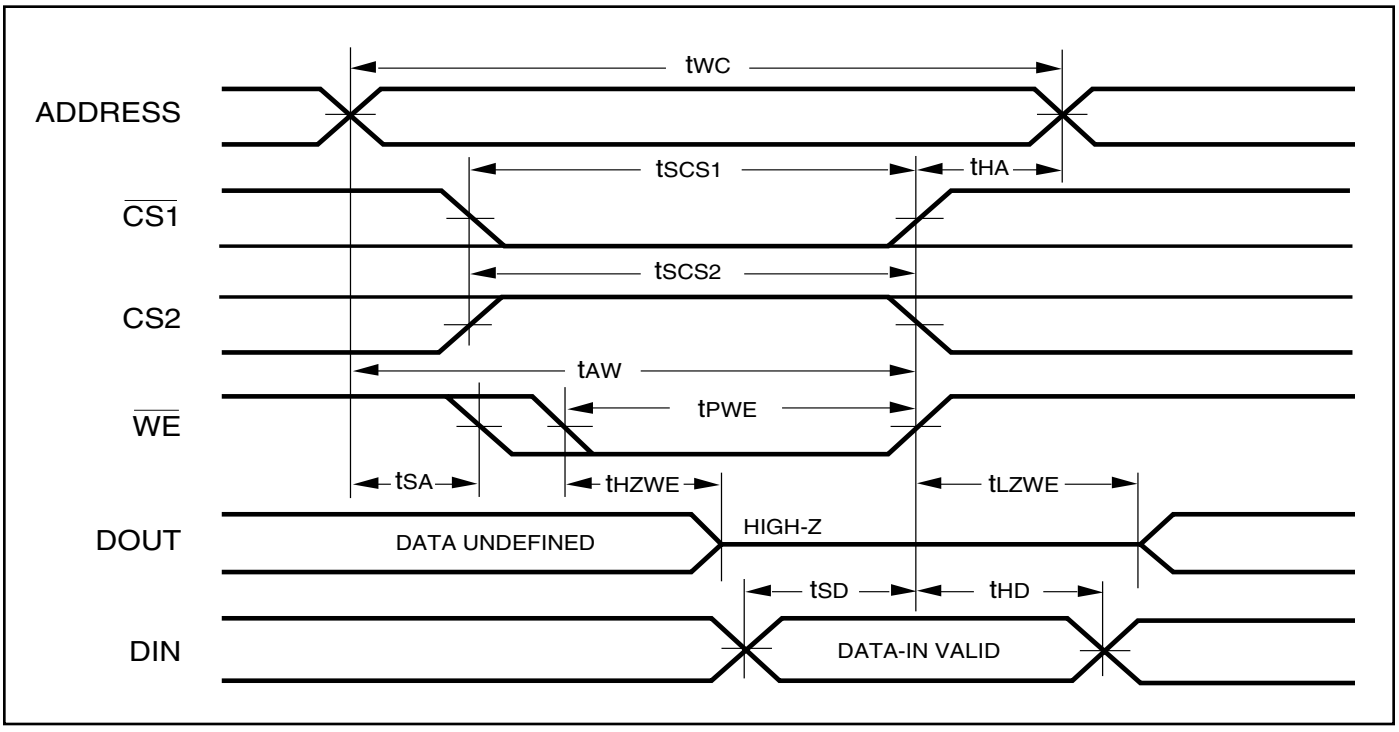
		35ns		45ns		55ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	25	—	35	—	45	—	ns
t_{AW}	Address Setup Time to Write End	25	—	35	—	45	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Addrress Setup Time	0	—	0	—	0	—	ns
t_{PWE}	$\overline{WE}$ Pulse Width	30	—	35	—	40	—	ns
t_{SD}	Data Setup to Write End	15	—	20	—	25	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

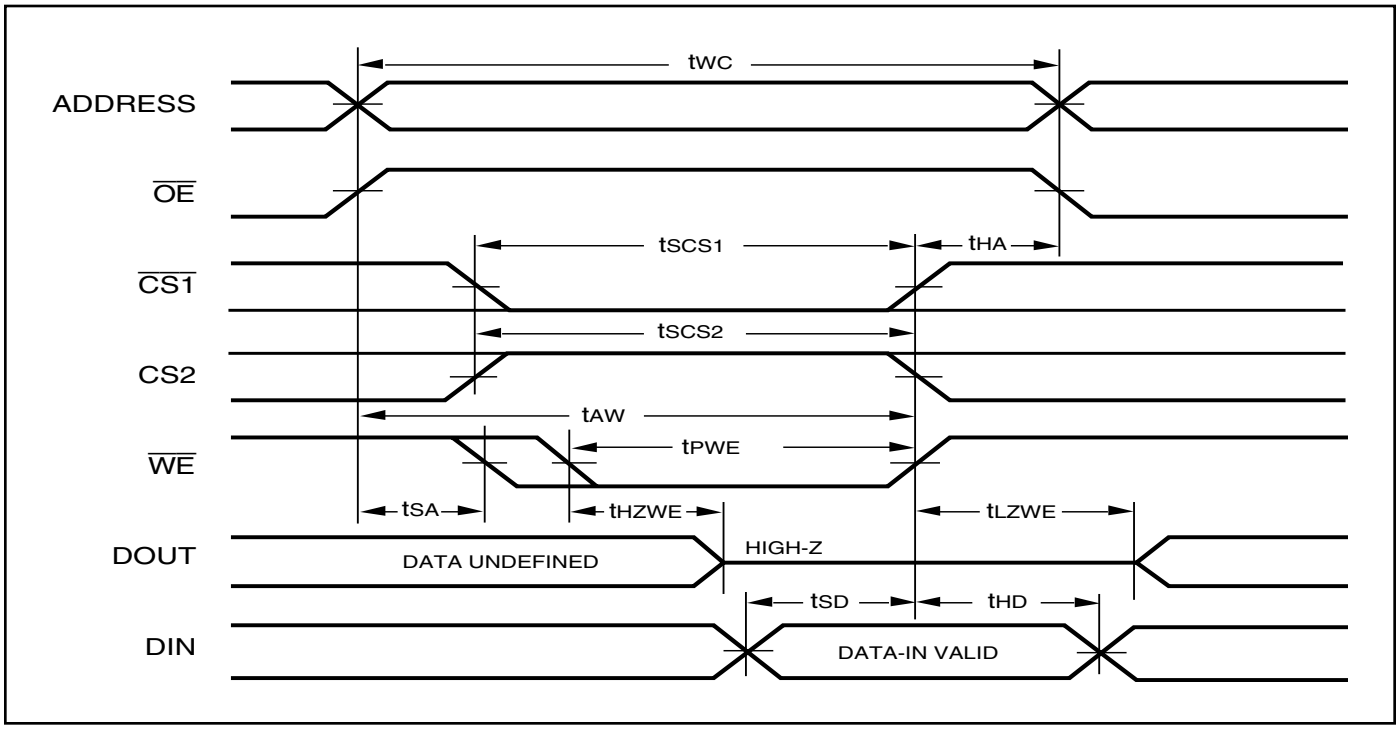
AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{CS1}$/CS2 Controlled, $\overline{OE}$ = HIGH or LOW)

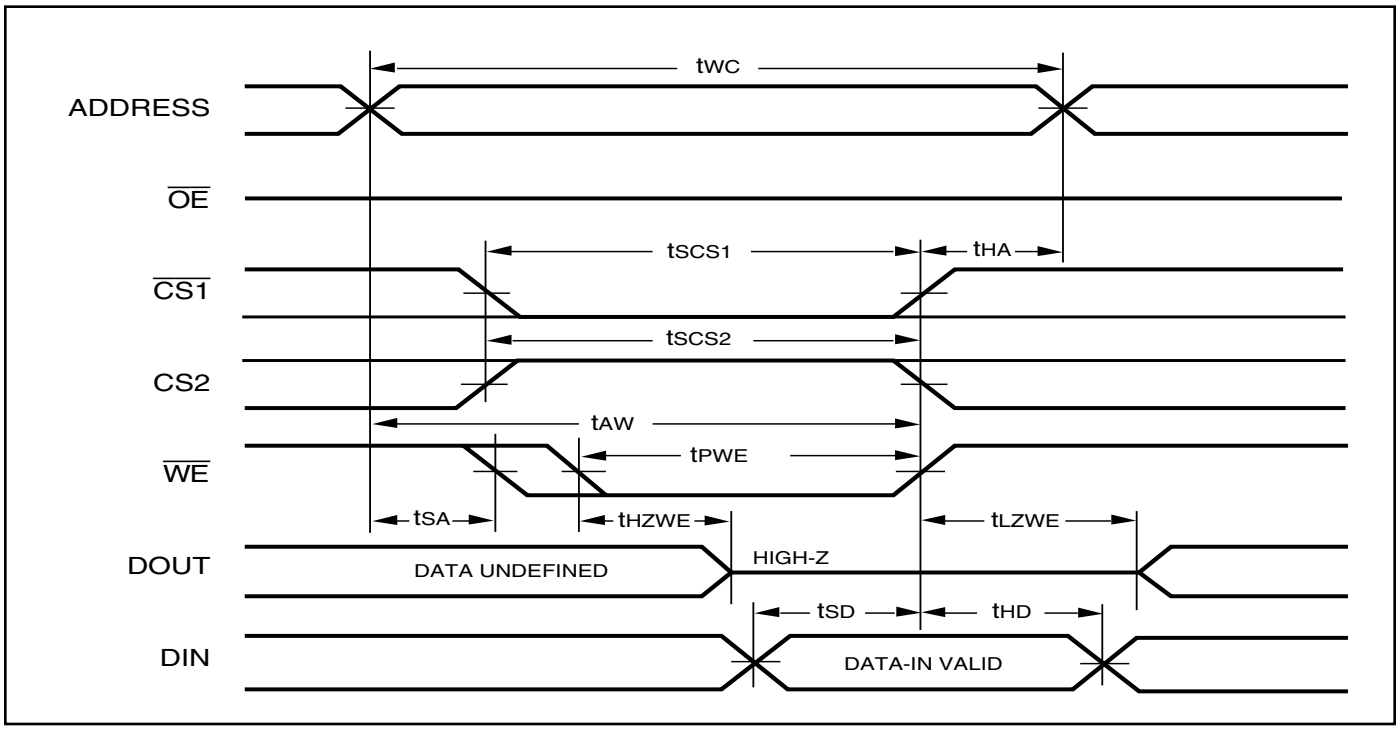


AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

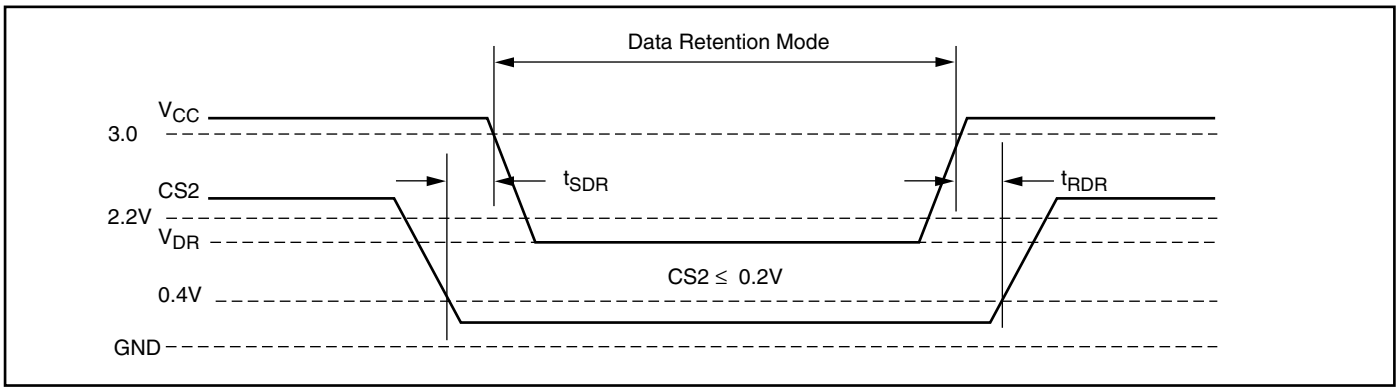


DATA RETENTION SWITCHING CHARACTERISTICS

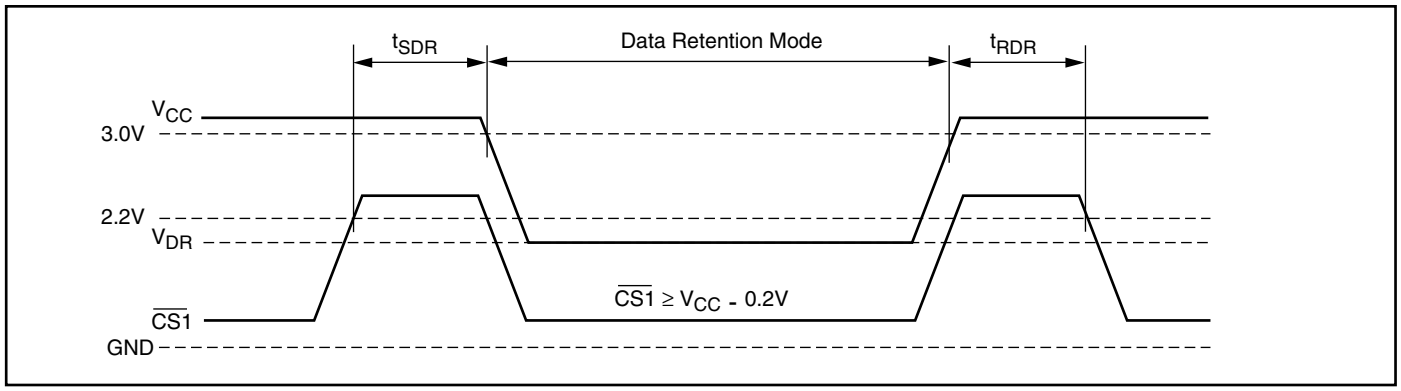
Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	Vcc for Data Retention	See Data Retention Waveform		1.5	3.6	V
I_{DR}	Data Retention Current	(1) 0V ≤ CS2 ≤ 0.2V, or	Com.	—	7	µA
		(2) CS1 ≥ V_{DD} - 0.2V, CS2 ≥ Vdd - 0.2V	Ind.	—	10	
			Auto.	—	20	
			typ.(1)	—	2	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:
1. Typical values are measured at Vcc = V_{DR}(min), T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM (CS2 Controlled)



DATA RETENTION WAVEFORM ($\overline{CS1}$ Controlled)



Note: CS2 must satisy either CS2 ≥ V_{CC} -0.2V or CS2 ≤ 0.2V

ORDERING INFORMATION

IS62WV2568DALL (1.8 ± 10%)
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV2568DALL-55TI	TSOP, TYPE I
55	IS62WV2568DALL-55TLI	TSOP, TYPE I, Lead-free
55	IS62WV2568DALL-55BI	mini BGA (6mm x 8mm)
55	IS62WV2568DALL-55BLI	mini BGA (6mm x 8mm), Lead-free
55	IS62WV2568DALL-55HI	sTSOP, TYPE I
55	IS62WV2568DALL-55HLI	sTSOP, TYPE I, Lead-free

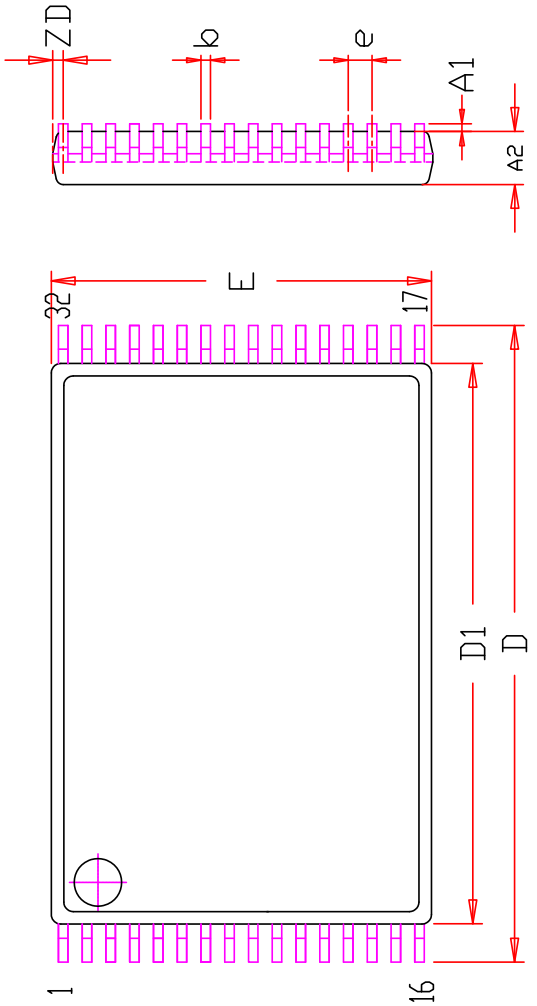
IS62WV2568DBLL (2.5V - 3.6V)
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
35	IS62WV2568DBLL-35HLI	sTSOP, TYPE I
35	IS62WV2568DBLL-35TLI	TSOP, TYPE I, Lead-free
45	IS62WV2568DBLL-45TI	TSOP, TYPE I
45	IS62WV2568DBLL-45TLI	TSOP, TYPE I, Lead-free
45	IS62WV2568DBLL-45BI	mini BGA (6mm x 8mm)
45	IS62WV2568DBLL-45BLI	mini BGA (6mm x 8mm), Lead-free
45	IS62WV2568DBLL-45HI	sTSOP, TYPE I
45	IS62WV2568DBLL-45HLI	sTSOP, TYPE I, Lead-free

IS65WV2568DBLL (2.5V - 3.6V)
Automotive Range (A3): –40°C to +125°C

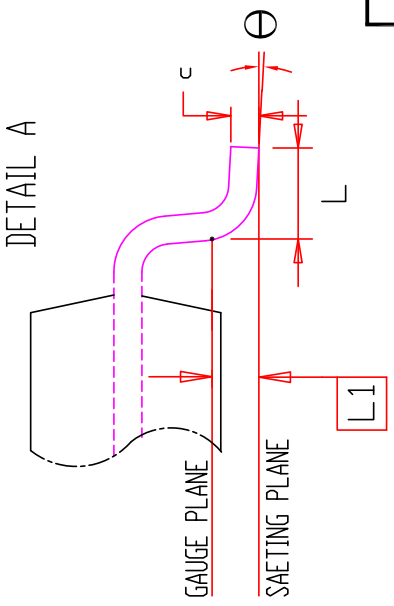
Speed (ns)	Order Part No.	Package
45	IS65WV2568DBLL-45TLA3	TSOP, TYPE I, Lead-free
45	IS65WV2568DBLL-45HLA3	sTSOP, TYPE I, Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95	—	1.25	0.037	—	0.049
A1	0.05	—	0.15	0.002	—	0.008
A2	0.90	—	1.05	0.035	—	0.041
b	0.16	—	0.27	0.006	—	0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°
c	0.10	—	0.21	0.004	—	0.008



NOTE :

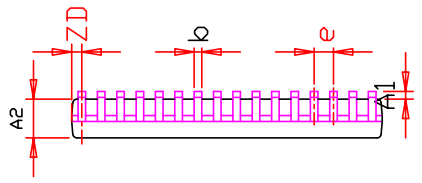
1. Controlling Dimension : mm
2. Dimension D1 and E do not include mold protrusion.
3. Dimension b does not include dambar protrusion/intrusion.
4. Reference Document : JEDEC MO-183
5. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

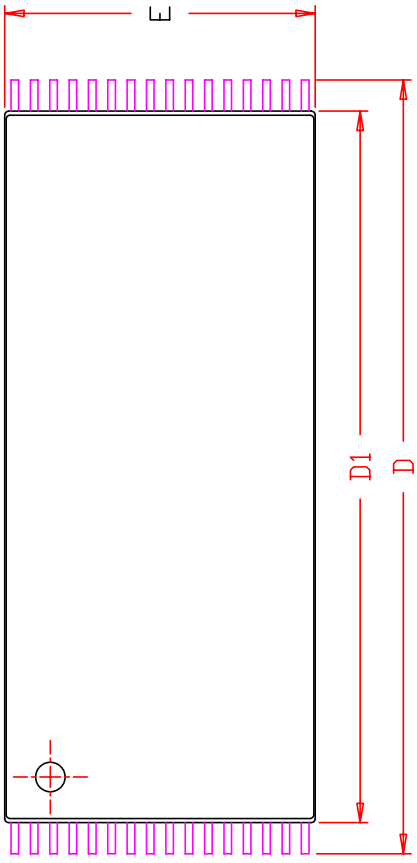


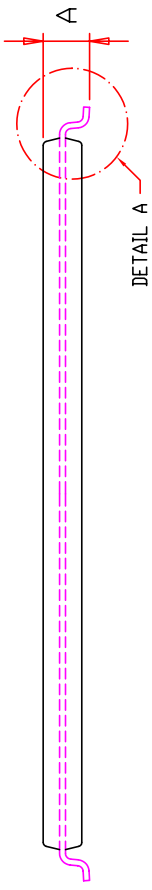
CASE 2

	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	F	DATE	06/21/2017

SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00	—	1.20
A1	0.05	—	0.20
A2	0.95	1.00	1.05
b	0.17	—	0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e		0.50 BSC.	
L	0.40	—	0.70
L1		0.25 BSC.	
ZD		0.25 REF.	
θ	0	5°	8°

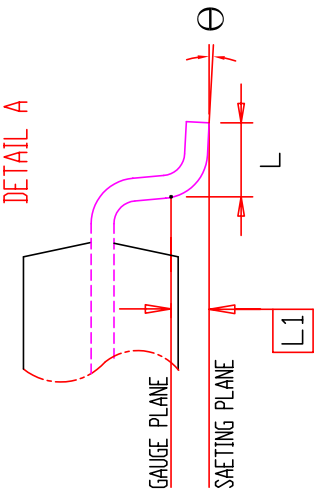






NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.



ISSI®	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	E	DATE	06/08/2006