

## 128K x 8 HIGH-SPEED CMOS STATIC RAM

JUNE 2021

### FEATURES

#### HIGH SPEED: (IS63/64WV1288DALL/DBLL)

- High-speed access time: 8, 10, 12, 20 ns
- Low Active Power: 135 mW (typical)
- Low Standby Power: 12  $\mu$ W (typical)  
CMOS standby

#### LOW POWER: (IS63/64WV1288DALS/DBLS)

- High-speed access time: 25, 35 ns
- Low Active Power: 55 mW (typical)
- Low Standby Power: 12  $\mu$ W (typical)  
CMOS standby
- Single power supply
  - $V_{DD}$  1.65V to 2.2V (IS63WV1288DAxx)
  - $V_{DD}$  2.4V to 3.6V (IS63/64WV1288DBxx)
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- $\overline{CE}$  power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Lead-free available

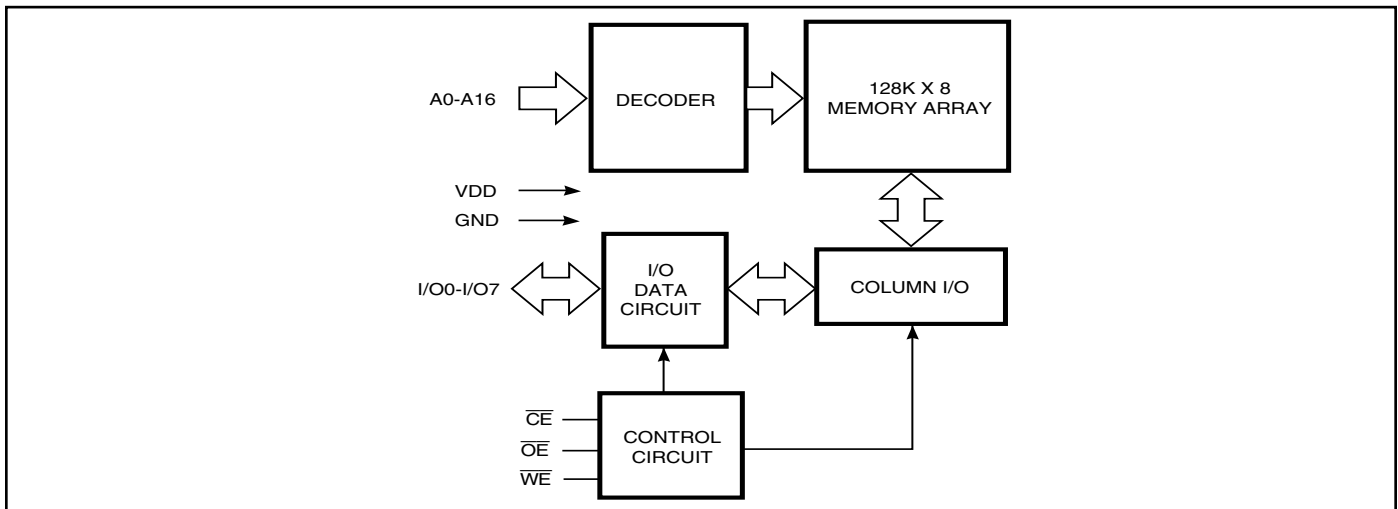
### DESCRIPTION

The *ISSI* IS63/64WV1288Dxxx is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM. The IS63/64WV1288DBLL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 25  $\mu$ W (typical) with CMOS input levels.

The IS63/64WV1288DBLL operates from a single  $V_{DD}$  power supply. The IS63/64WV1288Dxxx is available in 32-pin TSOP (Type II), 32-pin sTSOP (Type I), 48-Ball miniBGA (6mm x 8mm) and 32-pin SOJ (300-mil) packages.

### FUNCTIONAL BLOCK DIAGRAM



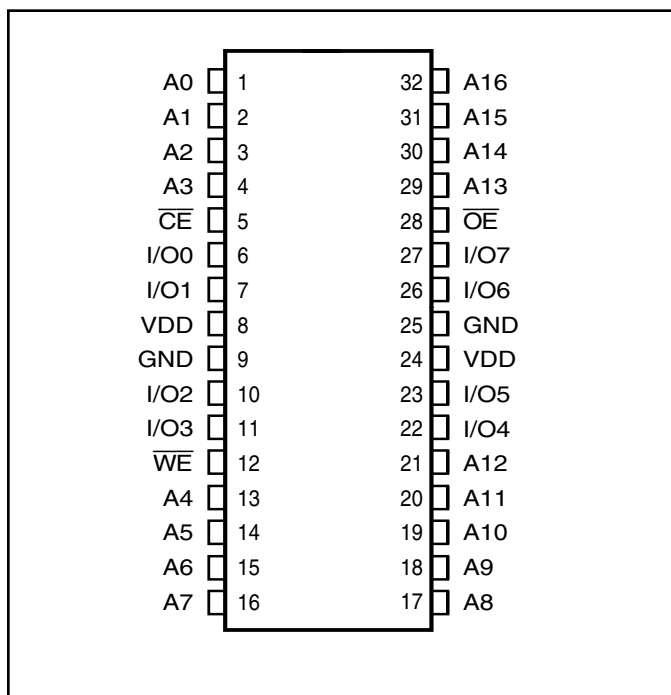
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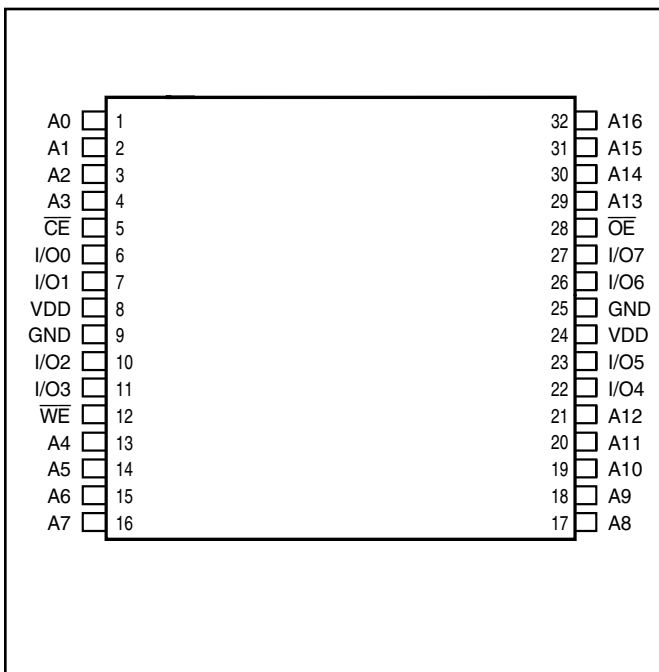
### PIN CONFIGURATION

#### 32-Pin SOJ



### PIN CONFIGURATION

#### 32-Pin TSOP (Type II) (T) 32-Pin sTSOP (Type I) (H)

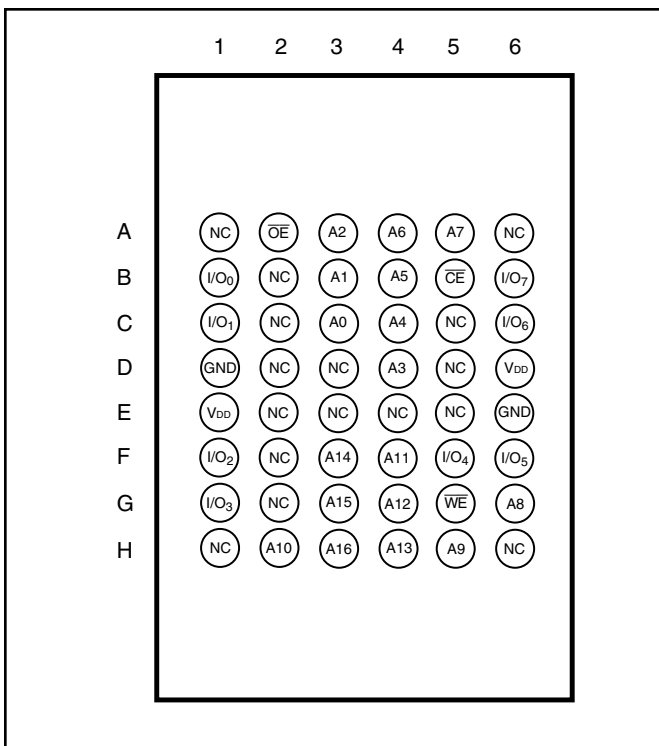


### PIN DESCRIPTIONS

|           |                     |
|-----------|---------------------|
| A0-A16    | Address Inputs      |
| CE        | Chip Enable Input   |
| OE        | Output Enable Input |
| WE        | Write Enable Input  |
| I/O0-I/O7 | Bidirectional Ports |
| VDD       | Power               |
| GND       | Ground              |

### PIN CONFIGURATION

#### 48-mini BGA (B) (6 mm x 8 mm)



## TRUTH TABLE

| Mode                         | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | I/O Operation    | V <sub>DD</sub> Current             |
|------------------------------|-----------------|-----------------|-----------------|------------------|-------------------------------------|
| Not Selected<br>(Power-down) | X               | H               | X               | High-Z           | I <sub>SB1</sub> , I <sub>SB2</sub> |
| Output Disabled              | H               | L               | H               | High-Z           | I <sub>CC1</sub> , I <sub>CC2</sub> |
| Read                         | H               | L               | L               | D <sub>OUT</sub> | I <sub>CC1</sub> , I <sub>CC2</sub> |
| Write                        | L               | L               | X               | D <sub>IN</sub>  | I <sub>CC1</sub> , I <sub>CC2</sub> |

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Parameter                            | Value                        | Unit |
|-------------------|--------------------------------------|------------------------------|------|
| V <sub>TERM</sub> | Terminal Voltage with Respect to GND | -0.5 to V <sub>DD</sub> +0.5 | V    |
| T <sub>STG</sub>  | Storage Temperature                  | -65 to +150                  | °C   |
| P <sub>T</sub>    | Power Dissipation                    | 1.5                          | W    |
| V <sub>DD</sub>   | V <sub>DD</sub> Related to GND       | -0.2 to +3.9                 | V    |

### Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## AC TEST CONDITIONS

| Parameter  | Unit<br>(2.4V-3.6V)     | Unit<br>(3.3V ± 5%)       | Unit<br>(1.65V-2.2V)    |
|--|-------------------------|---------------------------|-------------------------|
| Input Pulse Level  | 0.4V to $V_{DD} - 0.3V$ | 0.4V to $V_{DD} - 0.3V$   | 0.4V to $V_{DD} - 0.3V$ |
| Input Rise and Fall Times                                    | 1V/ ns                  | 1V/ ns                    | 1V/ ns                  |
| Input and Output Timing<br>and Reference Level ( $V_{Ref}$ ) | $V_{DD} / 2$            | $\frac{V_{DD}}{2} + 0.05$ | 0.9V                    |
| Output Load  | See Figures 1 and 2     | See Figures 1 and 2       | See Figures 1 and 2     |
| R1 ( $\Omega$ )  | 1909                    | 317                       | 13500                   |
| R2 ( $\Omega$ )  | 1105                    | 351                       | 10800                   |
| $V_{TM}$ (V)   | 3.0V                    | 3.3V                      | 1.8V                    |

## AC TEST LOADS

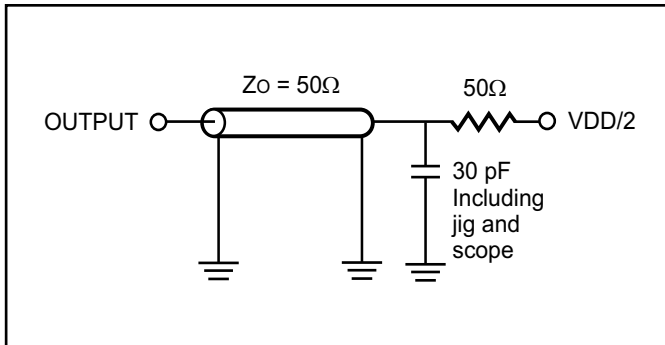


Figure 1.

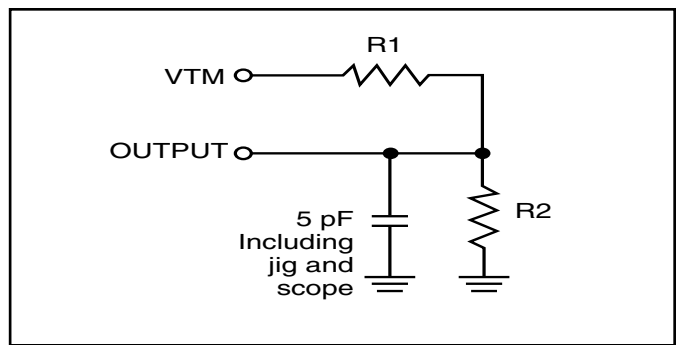


Figure 2.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 3.3V \pm 5\%$

| Symbol   | Parameter                        | Test Conditions                                   | Min. | Max.           | Unit          |
|----------|----------------------------------|---|------|----------------|---------------|
| $V_{OH}$ | Output HIGH Voltage              | $V_{DD} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$  | 2.4  | —              | V             |
| $V_{OL}$ | Output LOW Voltage               | $V_{DD} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$   | —    | 0.4            | V             |
| $V_{IH}$ | Input HIGH Voltage               |   | 2    | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input LOW Voltage <sup>(1)</sup> |   | -0.3 | 0.8            | V             |
| $I_{LI}$ | Input Leakage                    | $GND \leq V_{IN} \leq V_{DD}$                     | -1   | 1              | $\mu\text{A}$ |
| $I_{LO}$ | Output Leakage                   | $GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled | -1   | 1              | $\mu\text{A}$ |

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 2.4V-3.6V$

| Symbol   | Parameter                        | Test Conditions                                   | Min. | Max.           | Unit          |
|----------|----------------------------------|---|------|----------------|---------------|
| $V_{OH}$ | Output HIGH Voltage              | $V_{DD} = \text{Min.}, I_{OH} = -1.0 \text{ mA}$  | 1.8  | —              | V             |
| $V_{OL}$ | Output LOW Voltage               | $V_{DD} = \text{Min.}, I_{OL} = 1.0 \text{ mA}$   | —    | 0.4            | V             |
| $V_{IH}$ | Input HIGH Voltage               |   | 2.0  | $V_{DD} + 0.3$ | V             |
| $V_{IL}$ | Input LOW Voltage <sup>(1)</sup> |   | -0.3 | 0.8            | V             |
| $I_{LI}$ | Input Leakage                    | $GND \leq V_{IN} \leq V_{DD}$                     | -1   | 1              | $\mu\text{A}$ |
| $I_{LO}$ | Output Leakage                   | $GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled | -1   | 1              | $\mu\text{A}$ |

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

$V_{DD} = 1.65V-2.2V$

| Symbol         | Parameter           | Test Conditions                                   | $V_{DD}$  | Min. | Max.           | Unit          |
|----------------|---------------------|---|-----------|------|----------------|---------------|
| $V_{OH}$       | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$                        | 1.65-2.2V | 1.4  | —              | V             |
| $V_{OL}$       | Output LOW Voltage  | $I_{OL} = 0.1 \text{ mA}$                         | 1.65-2.2V | —    | 0.2            | V             |
| $V_{IH}$       | Input HIGH Voltage  |   | 1.65-2.2V | 1.4  | $V_{DD} + 0.2$ | V             |
| $V_{IL}^{(1)}$ | Input LOW Voltage   |   | 1.65-2.2V | -0.2 | 0.4            | V             |
| $I_{LI}$       | Input Leakage       | $GND \leq V_{IN} \leq V_{DD}$                     |           | -1   | 1              | $\mu\text{A}$ |
| $I_{LO}$       | Output Leakage      | $GND \leq V_{OUT} \leq V_{DD}$ , Outputs Disabled |           | -1   | 1              | $\mu\text{A}$ |

**Note:**

- $V_{IL} (\text{min.}) = -0.3V \text{ DC}; V_{IL} (\text{min.}) = -2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.  
 $V_{IH} (\text{max.}) = V_{DD} + 0.3V \text{ DC}; V_{IH} (\text{max.}) = V_{DD} + 2.0V \text{ AC}$  (pulse width < 10 ns). Not 100% tested.

## HIGH SPEED (IS63WV1288DALL/DBLL)

### OPERATING RANGE (V<sub>DD</sub>) (IS63WV1288DALL)

| Range      | Ambient Temperature | V <sub>DD</sub> | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C        | 1.65V-2.2V      | 20ns  |
| Industrial | -40°C to +85°C      | 1.65V-2.2V      | 20ns  |
| Automotive | -40°C to +125°C     | 1.65V-2.2V      | 20ns  |

### OPERATING RANGE (V<sub>DD</sub>) (IS63WV1288DBLL)<sup>(1)</sup>

| Range      | Ambient Temperature | V <sub>DD</sub> (8 ns) <sup>1</sup> | V <sub>DD</sub> (10 ns) <sup>1</sup> |
|------------|---------------------|-------------------------------------|--------------------------------------|
| Commercial | 0°C to +70°C        | 3.3V ± 5%                           | 2.4V-3.6V                            |
| Industrial | -40°C to +85°C      | 3.3V ± 5%                           | 2.4V-3.6V                            |

**Note:**

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

### OPERATING RANGE (V<sub>DD</sub>) (IS64WV1288DBLL)<sup>(2)</sup>

| Range      | Ambient Temperature | V <sub>DD</sub> (8 ns) <sup>2</sup> | V <sub>DD</sub> (10 ns) <sup>2</sup> |
|------------|---------------------|-------------------------------------|--------------------------------------|
| Automotive | -40°C to +125°C     | 3.3V ± 5%                           | 2.4V-3.6V                            |

**Note:**

- When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

## POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol           | Parameter  | Test Conditions  |                      | -8   |      | -10  |      | -12  |      | -20  |      | Unit |
|------------------|--|--|----------------------|------|------|------|------|------|------|------|------|------|
|                  |  |  |                      | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |
| I <sub>CC</sub>  | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub><br>CE = V <sub>IL</sub><br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V, or<br>V <sub>IN</sub> ≤ 0.4V | Com.                 | —    | 65   | —    | 50   | —    | 45   | —    | 40   | mA   |
|                  |  |  | Ind.                 | —    | 70   | —    | 55   | —    | 50   | —    | 45   |      |
|                  |  |  | Auto. <sup>(3)</sup> | —    | —    | —    | 65   | —    | 55   | —    | 50   |      |
|                  |  |  | typ. <sup>(2)</sup>  |      |      | 45   |      | 45   |      |      |      |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = Max.,<br>CE ≥ V <sub>DD</sub> - 0.2V,<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0                                   | Com.                 | —    | 40   | —    | 40   | —    | 40   | —    | 40   | μA   |
|                  |  |  | Ind.                 | —    | 55   | —    | 55   | —    | 55   | —    | 55   |      |
|                  |  |  | Auto.                | —    | —    | —    | 90   | —    | 90   | —    | 90   |      |
|                  |  |  | typ. <sup>(2)</sup>  |      |      | 4    |      | 4    |      |      |      |      |

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.
- For Automotive grade at 15ns, typ. I<sub>CC</sub> = 38mA, not 100% tested.

## LOW POWER (IS63WV1288DALS/DBLS)

### OPERATING RANGE (V<sub>DD</sub>) (IS63WV1288DALS)

| Range      | Ambient Temperature | V <sub>DD</sub> | Speed |
|------------|---------------------|-----------------|-------|
| Commercial | 0°C to +70°C        | 1.65V-2.2V      | 45ns  |
| Industrial | -40°C to +85°C      | 1.65V-2.2V      | 45ns  |
| Automotive | -40°C to +125°C     | 1.65V-2.2V      | 55ns  |

### OPERATING RANGE (V<sub>DD</sub>) (IS63WV1288DBLS)

| Range      | Ambient Temperature | V <sub>DD</sub> (35 ns) |
|------------|---------------------|-------------------------|
| Commercial | 0°C to +70°C        | 2.4V-3.6V               |
| Industrial | -40°C to +85°C      | 2.4V-3.6V               |

### OPERATING RANGE (V<sub>DD</sub>) (IS64WV1288DBLS)

| Range      | Ambient Temperature | V <sub>DD</sub> (35 ns) |
|------------|---------------------|-------------------------|
| Automotive | -40°C to +125°C     | 2.4V-3.6V               |

## POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol           | Parameter  | Test Conditions  |                     | -25  |      | -35  |      | -45  |      | Unit |
|------------------|--|--|---------------------|------|------|------|------|------|------|------|
|                  |  |  |                     | Min. | Max. | Min. | Max. | Min. | Max. |      |
| I <sub>CC</sub>  | V <sub>DD</sub> Dynamic Operating Supply Current | V <sub>DD</sub> = Max.,<br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub><br>$\overline{CE} = V_{IL}$<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3V, or<br>V <sub>IN</sub> ≤ 0.4V | Com.                | —    | 15   | —    | 15   | —    | 12   | mA   |
|                  |  |  | Ind.                | —    | 20   | —    | 20   | —    | 18   |      |
|                  |  |  | Auto.               | —    | 30   | —    | 30   | —    | 25   |      |
|                  |  |  | typ. <sup>(2)</sup> | 18   |      |      |      |      |      |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>DD</sub> = Max.,<br>$\overline{CE} \geq V_{DD} - 0.2V$ ,<br>V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0                               | Com.                | —    | 40   | —    | 40   | —    | 40   | μA   |
|                  |  |  | Ind.                | —    | 50   | —    | 50   | —    | 50   |      |
|                  |  |  | Auto.               | —    | 75   | —    | 75   | —    | 75   |      |
|                  |  |  | typ. <sup>(2)</sup> | 4    |      |      |      |      |      |      |

#### Note:

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

## CAPACITANCE<sup>(1,2)</sup>

| Symbol           | Parameter                | Conditions            | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 6    | pF   |
| C <sub>I/O</sub> | Input/Output Capacitance | V <sub>OUT</sub> = 0V | 8    | pF   |

#### Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>DD</sub> = 3.3V.

### READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol                           | Parameter             | -8 ns |      | -10 ns |      | -12 ns |      | Unit |
|----------------------------------|-----------------------|-------|------|--------|------|--------|------|------|
|                                  |                       | Min.  | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>RC</sub>                  | Read Cycle Time       | 8     | —    | 10     | —    | 12     | —    | ns   |
| t <sub>AA</sub>                  | Address Access Time   | —     | 8    | —      | 10   | —      | 12   | ns   |
| t <sub>OHA</sub>                 | Output Hold Time      | 2     | —    | 2      | —    | 2      | —    | ns   |
| t <sub>ACE</sub>                 | CE Access Time        | —     | 8    | —      | 10   | —      | 12   | ns   |
| t <sub>DOE</sub>                 | OE Access Time        | —     | 4    | —      | 5    | —      | 6    | ns   |
| t <sub>LZOE</sub> <sup>(2)</sup> | OE to Low-Z Output    | 0     | —    | 0      | —    | 0      | —    | ns   |
| t <sub>HZOE</sub> <sup>(2)</sup> | OE to High-Z Output   | 0     | 4    | 0      | 5    | 0      | 6    | ns   |
| t <sub>LZCE</sub> <sup>(2)</sup> | CE to Low-Z Output    | 3     | —    | 3      | —    | 3      | —    | ns   |
| t <sub>HZCE</sub> <sup>(2)</sup> | CE to High-Z Output   | 0     | 4    | 0      | 5    | 0      | 6    | ns   |
| t <sub>PU</sub>                  | CE to Power Up Time   | 0     | —    | 0      | —    | 0      | —    | ns   |
| t <sub>PD</sub>                  | CE to Power Down Time | —     | 8    | —      | 10   | —      | 12   | ns   |

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V loading specified in Figure 1.
2. Tested with the loading specified in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

### READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol                           | Parameter           | -20 ns |      | -25 ns |      | -35 ns |      | -45 ns |      | Unit |
|----------------------------------|---------------------|--------|------|--------|------|--------|------|--------|------|------|
|                                  |                     | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>RC</sub>                  | Read Cycle Time     | 20     | —    | 25     | —    | 35     | —    | 45     | —    | ns   |
| t <sub>AA</sub>                  | Address Access Time | —      | 20   | —      | 25   | —      | 35   | —      | 45   | ns   |
| t <sub>OHA</sub>                 | Output Hold Time    | 2.5    | —    | 6      | —    | 8      | —    | 10     | —    | ns   |
| t <sub>ACE</sub>                 | CE Access Time      | —      | 20   | —      | 25   | —      | 35   | —      | 45   | ns   |
| t <sub>DOE</sub>                 | OE Access Time      | —      | 8    | —      | 12   | —      | 15   | —      | 20   | ns   |
| t <sub>HZOE</sub> <sup>(2)</sup> | OE to High-Z Output | 0      | 8    | 0      | 8    | 0      | 10   | 0      | 15   | ns   |
| t <sub>LZOE</sub> <sup>(2)</sup> | OE to Low-Z Output  | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| t <sub>HZCE</sub> <sup>(2)</sup> | CE to High-Z Output | 0      | 8    | 0      | 8    | 0      | 10   | 0      | 15   | ns   |
| t <sub>LZCE</sub> <sup>(2)</sup> | CE to Low-Z Output  | 3      | —    | 10     | —    | 10     | —    | 10     | —    | ns   |

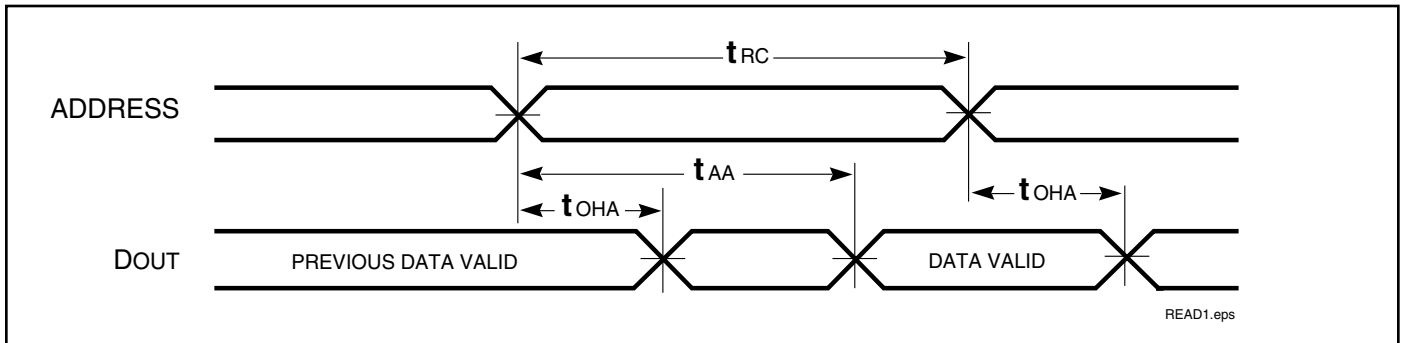
**Notes:**

1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

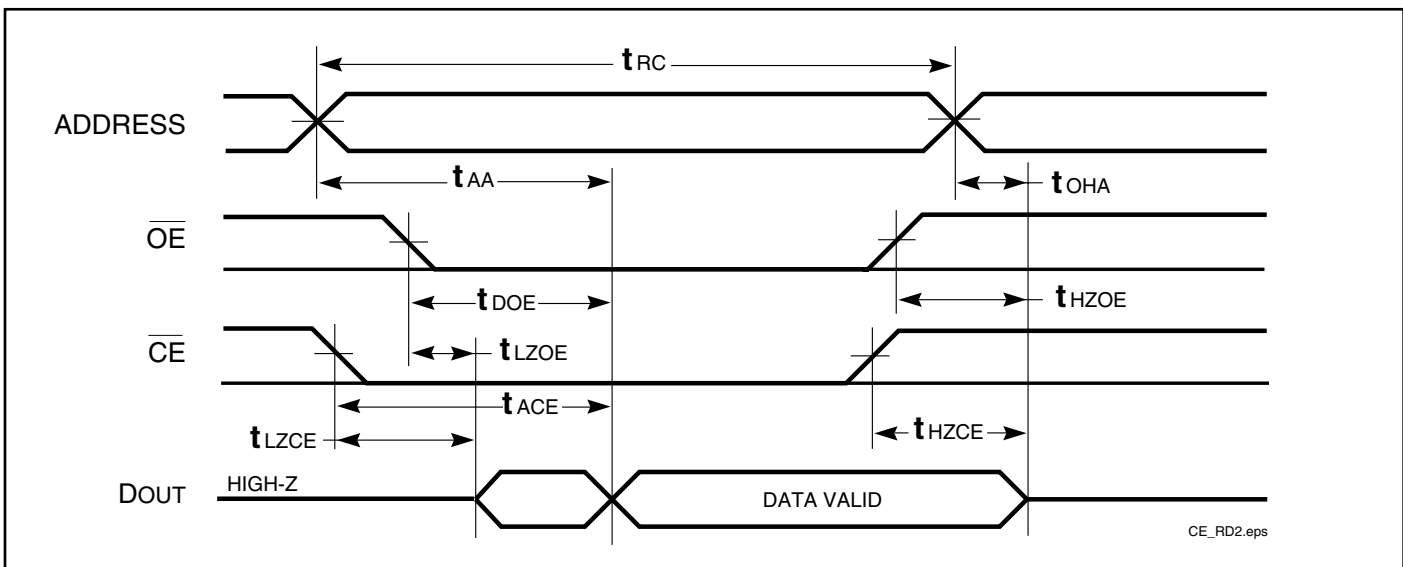


## AC WAVEFORMS

### READ CYCLE NO. 1<sup>(1,2)</sup>



### READ CYCLE NO. 2<sup>(1,3)</sup>



**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range)

| Symbol                                      | Parameter   | -8 ns |      | -10 ns |      | -12 ns |      | Unit |
|---|---|-------|------|--------|------|--------|------|------|
|   |   | Min.  | Max. | Min.   | Max. | Min.   | Max. |      |
| t <sub>wc</sub>                             | Write Cycle Time                                    | 8     | —    | 10     | —    | 12     | —    | ns   |
| t <sub>sce</sub>                            | $\overline{CE}$ to Write End                        | 7     | —    | 7      | —    | 8      | —    | ns   |
| t <sub>aw</sub>                             | Address Setup Time to Write End                     | 8     | —    | 8      | —    | 8      | —    | ns   |
| t <sub>ha</sub>                             | Address Hold from Write End                         | 0     | —    | 0      | —    | 0      | —    | ns   |
| t <sub>sa</sub>                             | Address Setup Time                                  | 0     | —    | 0      | —    | 0      | —    | ns   |
| t <sub>pwe<sub>1</sub></sub> <sup>(1)</sup> | $\overline{WE}$ Pulse Width ( $\overline{OE}$ High) | 7     | —    | 7      | —    | 8      | —    | ns   |
| t <sub>pwe<sub>2</sub></sub> <sup>(2)</sup> | $\overline{WE}$ Pulse Width ( $\overline{OE}$ Low)  | 8     | —    | 10     | —    | 12     | —    | ns   |
| t <sub>sd</sub>                             | Data Setup to Write End                             | 5     | —    | 5      | —    | 6      | —    | ns   |
| t <sub>hd</sub>                             | Data Hold from Write End                            | 0     | —    | 0      | —    | 0      | —    | ns   |
| t <sub>hzwe</sub> <sup>(2)</sup>            | $\overline{WE}$ LOW to High-Z Output                | —     | 4    | —      | 5    | —      | 6    | ns   |
| t <sub>lzwe</sub> <sup>(2)</sup>            | $\overline{WE}$ HIGH to Low-Z Output                | 3     | —    | 3      | —    | 3      | —    | ns   |

**Notes:**

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

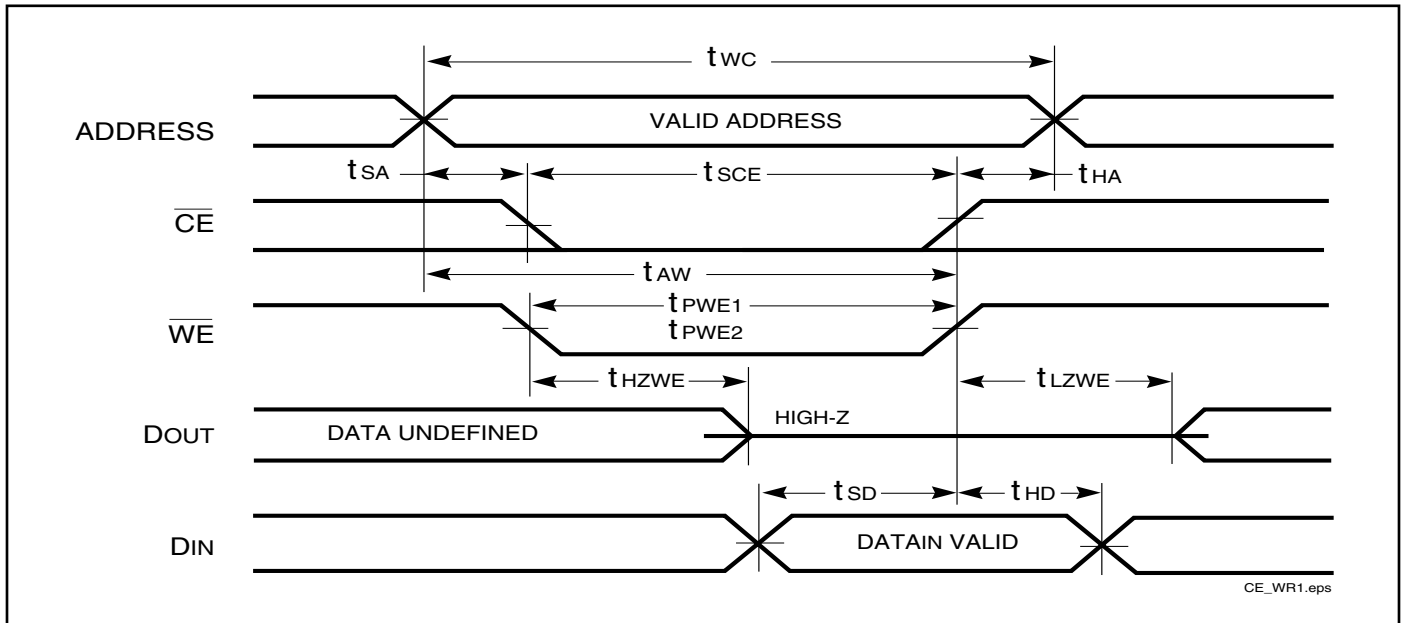
| Symbol                           | Parameter   | -20 ns |      | -25 ns |      | -35 ns |      | -45ns |      | Unit |
|----------------------------------|---|--------|------|--------|------|--------|------|-------|------|------|
|                                  |   | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.  | Max. |      |
| t <sub>wc</sub>                  | Write Cycle Time                                      | 20     | —    | 25     | —    | 35     | —    | 45    | —    | ns   |
| t <sub>sce</sub>                 | $\overline{CE}$ to Write End                          | 12     | —    | 18     | —    | 25     | —    | 35    | —    | ns   |
| t <sub>aw</sub>                  | Address Setup Time to Write End                       | 12     | —    | 15     | —    | 25     | —    | 35    | —    | ns   |
| t <sub>ha</sub>                  | Address Hold from Write End                           | 0      | —    | 0      | —    | 0      | —    | 0     | —    | ns   |
| t <sub>sa</sub>                  | Address Setup Time                                    | 0      | —    | 0      | —    | 0      | —    | 0     | —    | ns   |
| t <sub>pwe1</sub>                | $\overline{WE}$ Pulse Width ( $\overline{OE}$ = HIGH) | 12     | —    | 18     | —    | 30     | —    | 35    | —    | ns   |
| t <sub>pwe2</sub>                | $\overline{WE}$ Pulse Width ( $\overline{OE}$ = LOW)  | 17     | —    | 20     | —    | 30     | —    | 35    | —    | ns   |
| t <sub>sd</sub>                  | Data Setup to Write End                               | 9      | —    | 12     | —    | 15     | —    | 20    | —    | ns   |
| t <sub>hd</sub>                  | Data Hold from Write End                              | 0      | —    | 0      | —    | 0      | —    | 0     | —    | ns   |
| t <sub>hzwe</sub> <sup>(3)</sup> | $\overline{WE}$ LOW to High-Z Output                  | —      | 9    | —      | 12   | —      | 20   | —     | 20   | ns   |
| t <sub>lzwe</sub> <sup>(3)</sup> | $\overline{WE}$ HIGH to Low-Z Output                  | 3      | —    | 5      | —    | 5      | —    | 5     | —    | ns   |

**Notes:**

1. Test conditions assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

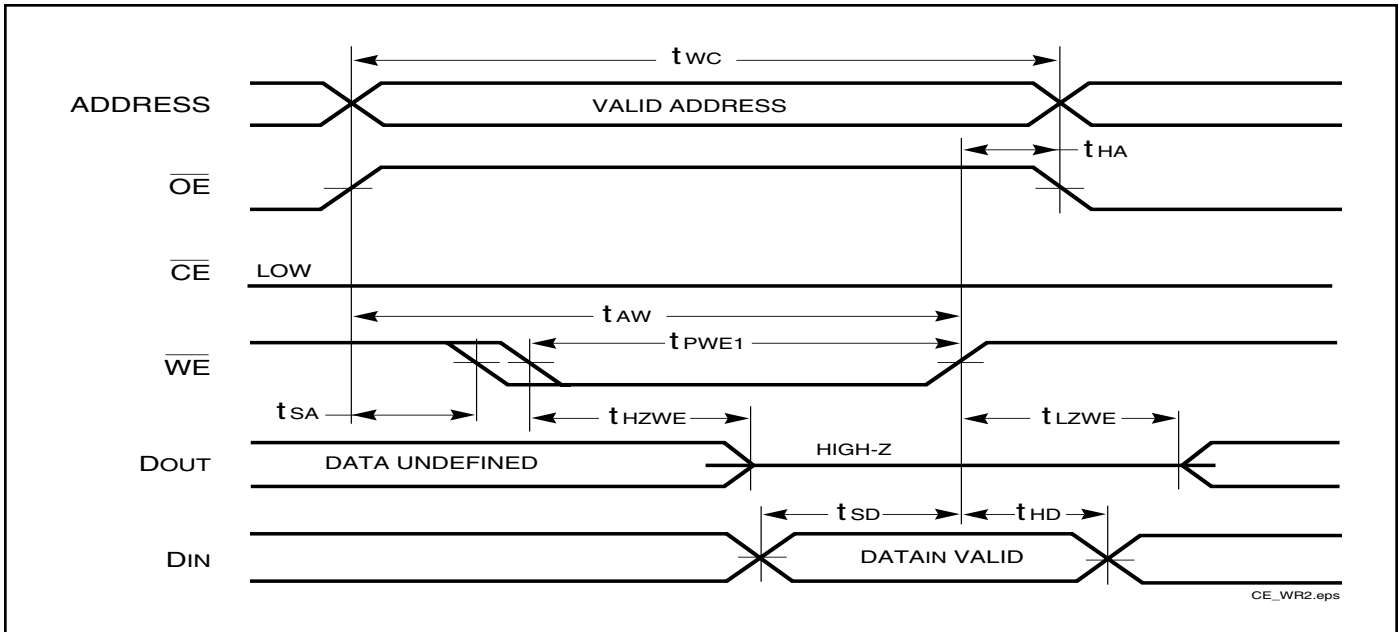
## AC WAVEFORMS

### WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

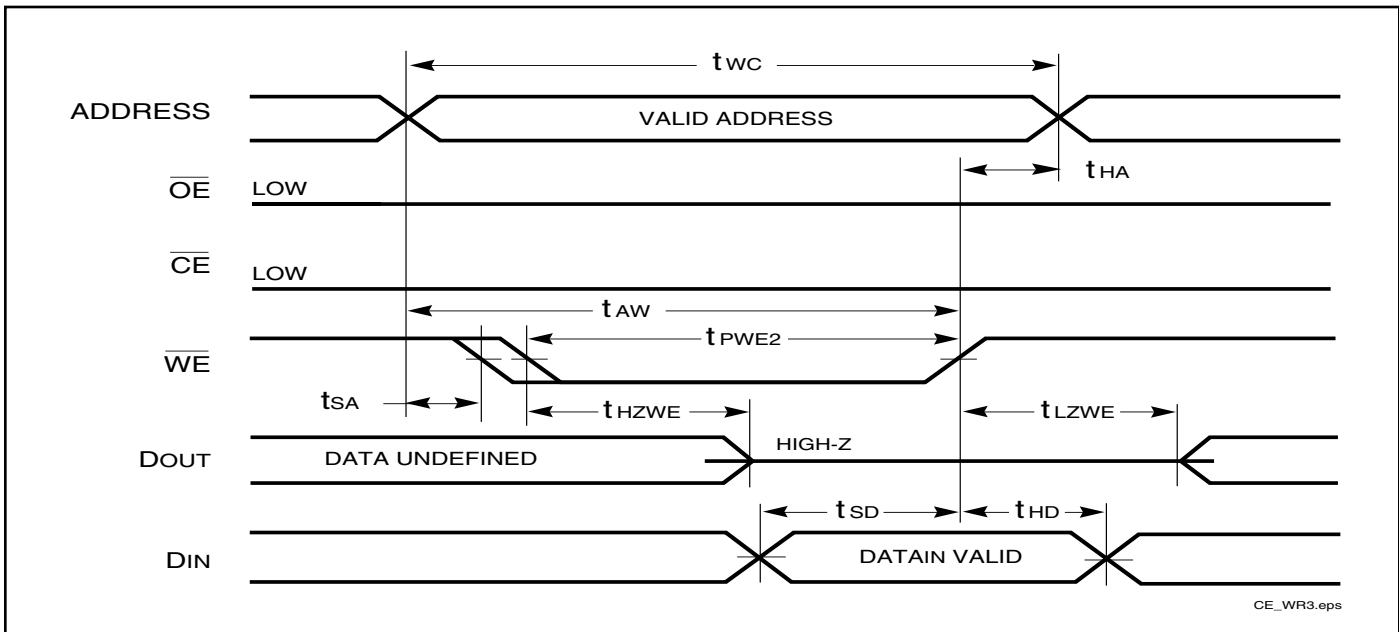


## AC WAVEFORMS

### WRITE CYCLE NO. 2<sup>(1)</sup> ( $\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)



### WRITE CYCLE NO. 3 ( $\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



#### Notes:

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} > V_{IH}$ .

## HIGH SPEED (IS63/4WV1288DALL/DBLL)

### DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol           | Parameter                          | Test Condition   | Options               | Min.            | Typ. <sup>(1)</sup> | Max.           | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|----------------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                                |                       | 2.0             | —                   | 3.6            | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com.<br>Ind.<br>Auto. | —               | 4                   | 40<br>55<br>90 | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                                |                       | 0               | —                   | —              | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                                |                       | t <sub>RC</sub> | —                   | —              | ns   |

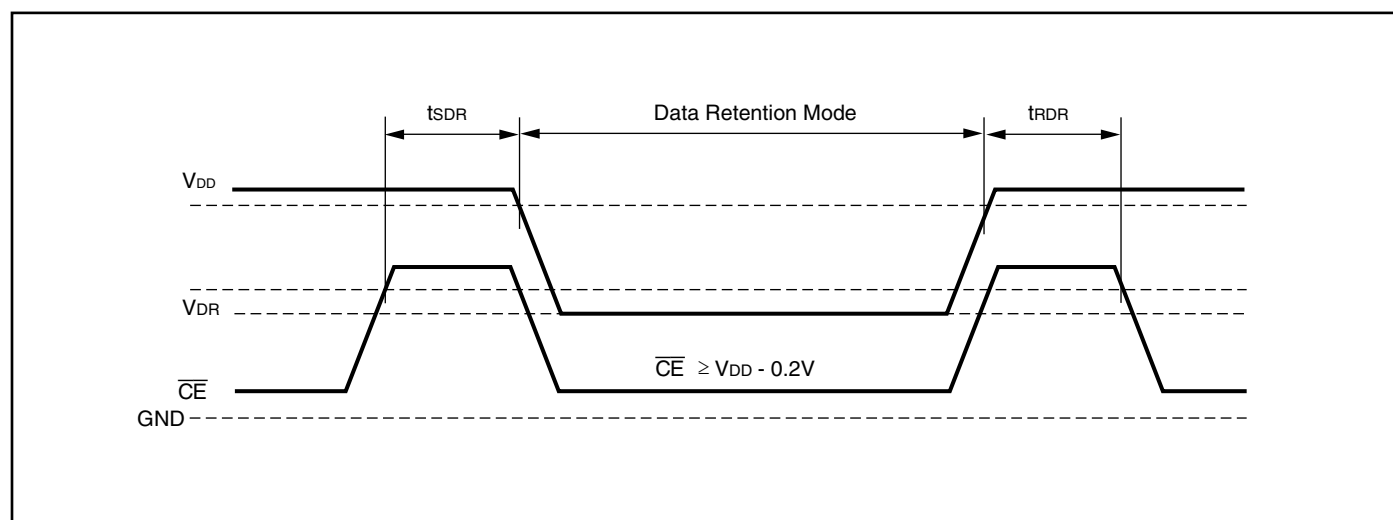
**Note 1:** Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol           | Parameter                          | Test Condition   | Options               | Min.            | Typ. <sup>(1)</sup> | Max.           | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|----------------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                                |                       | 1.2             | —                   | 3.6            | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com.<br>Ind.<br>Auto. | —               | 4                   | 40<br>55<br>90 | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                                |                       | 0               | —                   | —              | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                                |                       | t <sub>RC</sub> | —                   | —              | ns   |

**Note 1:** Typical values are measured at V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CE}$ Controlled)



## LOW POWER (IS63/4WV1288DALS/DBLS)

### DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

| Symbol           | Parameter                          | Test Condition   | Options               | Min.            | Typ. <sup>(1)</sup> | Max.           | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|----------------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                                |                       | 2.0             | —                   | 3.6            | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com.<br>Ind.<br>Auto. | —               | 4                   | 40<br>50<br>75 | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                                |                       | 0               | —                   | —              | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                                |                       | t <sub>RC</sub> | —                   | —              | ns   |

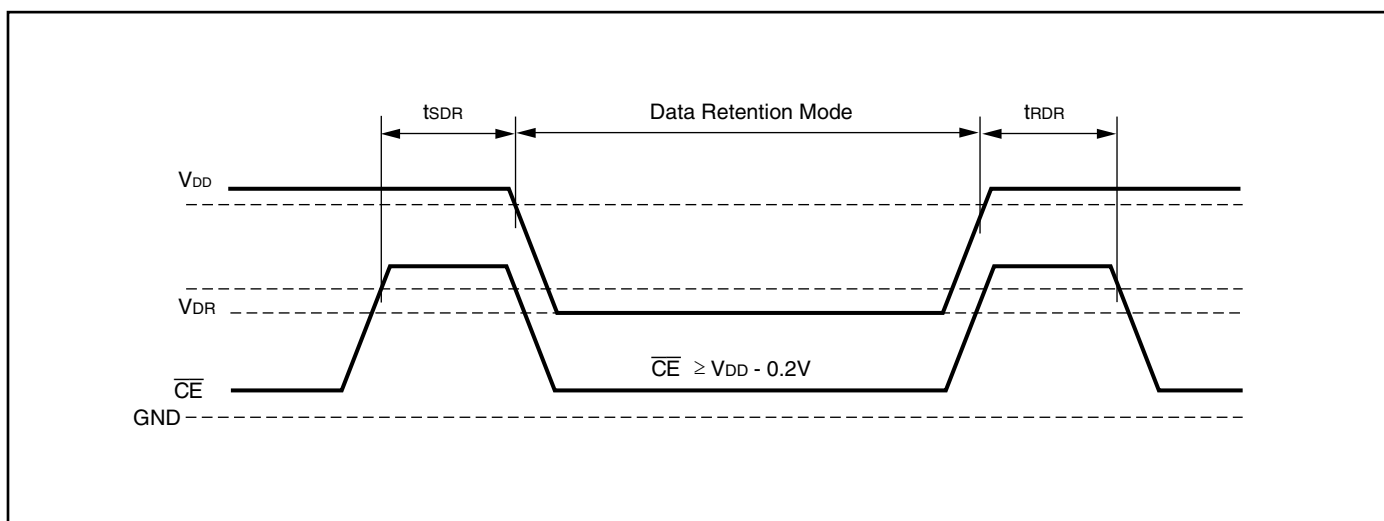
**Note 1:** Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION SWITCHING CHARACTERISTICS (1.65V-2.2V)

| Symbol           | Parameter                          | Test Condition   | Options               | Min.            | Typ. <sup>(1)</sup> | Max.           | Unit |
|------------------|------------------------------------|--|-----------------------|-----------------|---------------------|----------------|------|
| V <sub>DR</sub>  | V <sub>DD</sub> for Data Retention | See Data Retention Waveform                                |                       | 1.2             | —                   | 3.6            | V    |
| I <sub>DR</sub>  | Data Retention Current             | V <sub>DD</sub> = 1.2V, $\overline{CE} \geq V_{DD} - 0.2V$ | Com.<br>Ind.<br>Auto. | —               | 4                   | 40<br>50<br>75 | μA   |
| t <sub>SDR</sub> | Data Retention Setup Time          | See Data Retention Waveform                                |                       | 0               | —                   | —              | ns   |
| t <sub>RDR</sub> | Recovery Time                      | See Data Retention Waveform                                |                       | t <sub>RC</sub> | —                   | —              | ns   |

**Note 1:** Typical values are measured at V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 25°C and not 100% tested.

### DATA RETENTION WAVEFORM ( $\overline{CE}$ Controlled)



## ORDERING INFORMATION

### Industrial Range: $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

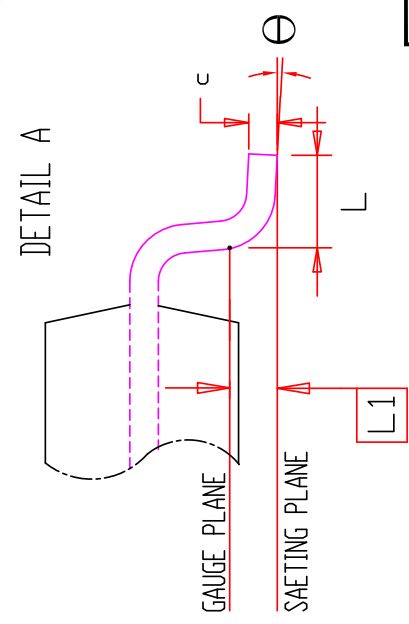
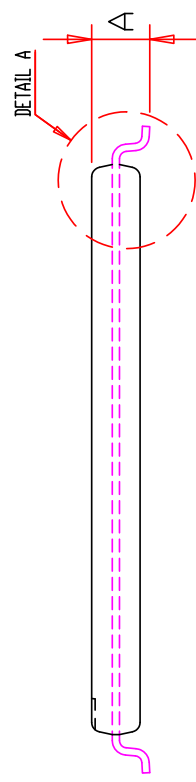
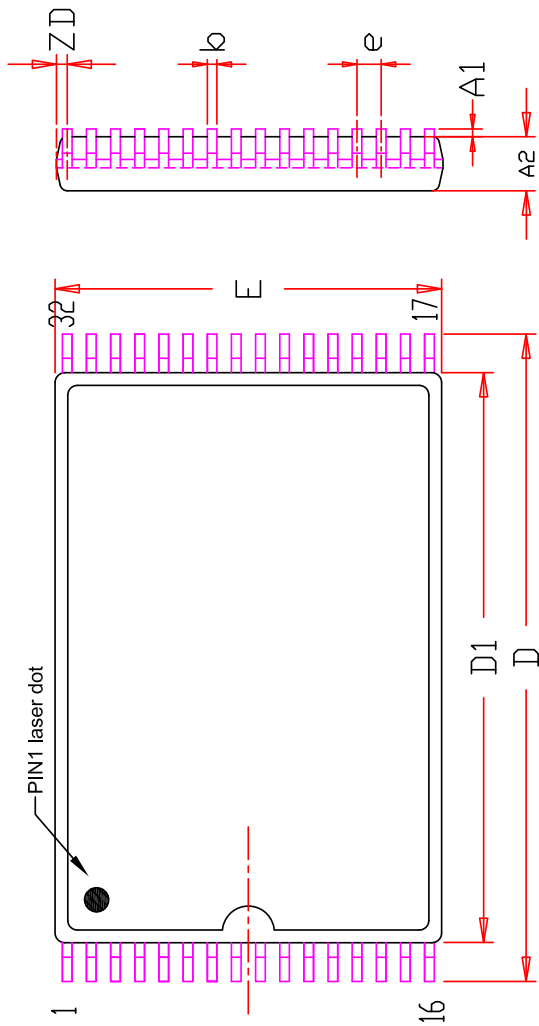
| Speed (ns) | Order Part No.       | Package                                 |
|------------|----------------------|---|
| 8          | IS63WV1288DBLL-8TLI  | 32-pin TSOP (Type II), Lead-free        |
|            | IS63WV1288DBLL-8HLI  | sTSOP (Type I) (8mm x13.4mm), Lead-free |
|            | IS63WV1288DBLL-8JLI  | 32-pin SOJ (300-mil), Lead-free         |
| 10         | IS63WV1288DBLL-10TLI | 32-pin TSOP (Type II), Lead-free        |
|            | IS63WV1288DBLL-10HLI | sTSOP (Type I) (8mm x13.4mm), Lead-free |
|            | IS63WV1288DBLL-10JLI | 32-pin SOJ (300-mil), Lead-free         |

### Automotive Range (A3): $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

| Speed (ns) | Order Part No.         | Package   |
|------------|------------------------|---|
| 10(8*)     | IS64WV1288DBLL-10CTLA3 | 32-pin TSOP (Type II), Copper Lead frame, Lead-free |
|            | IS64WV1288DBLL-10HLA3  | sTSOP (Type I) (8mm x13.4mm), Lead-free             |

**Note:**

1. Speed = 8ns for  $V_{DD} = 3.3V + 5\%$ . Speed = 10ns for  $V_{DD} = 2.4V-3.6V$ .



| SYMBOL | DIMENSION IN MM |       |       | DIMENSION IN INCH |       |       |
|--------|-----------------|-------|-------|-------------------|-------|-------|
|        | MIN             | NOM   | MAX   | MIN               | NOM   | MAX   |
| A      | 0.95            |       | 1.25  | 0.037             |       | 0.049 |
| A1     | 0.05            |       | 0.15  | 0.002             |       | 0.008 |
| A2     | 0.90            |       | 1.05  | 0.035             |       | 0.041 |
| b      | 0.16            |       | 0.27  | 0.006             |       | 0.011 |
| D      | 13.10           | 13.40 | 13.70 | 0.516             | 0.528 | 0.539 |
| D1     | 11.70           | 11.80 | 11.90 | 0.461             | 0.465 | 0.469 |
| E      | 7.90            | 8.00  | 8.10  | 0.311             | 0.315 | 0.319 |
| e      | 0.50 BSC.       |       |       | 0.020 BSC.        |       |       |
| L      | 0.30            | 0.50  | 0.70  | 0.012             | 0.020 | 0.028 |
| L1     | 0.25 BSC.       |       |       | 0.010 BSC.        |       |       |
| ZD     | 0.25 REF.       |       |       | 0.010 REF.        |       |       |
| Theta  | 0               | 3°    | 5°    | 0                 | 3°    | 5°    |
| c      | 0.10            |       | 0.21  | 0.004             |       | 0.008 |

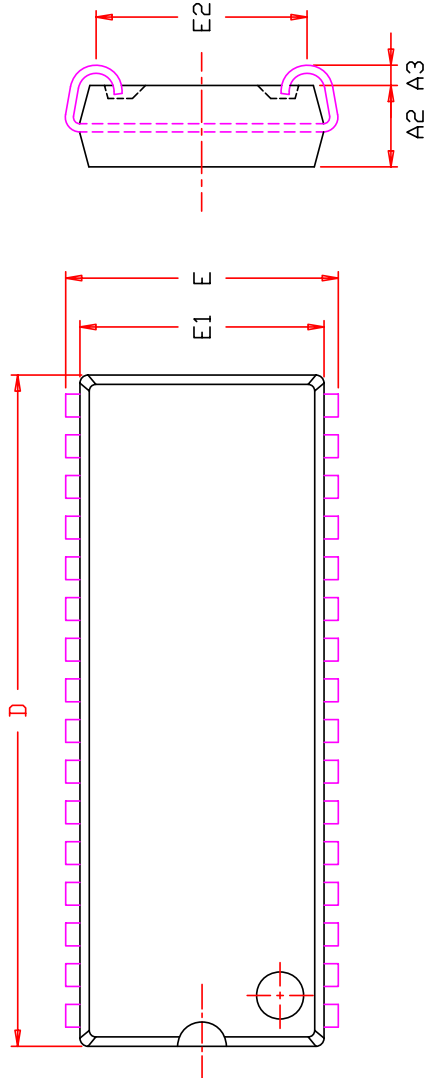
**NOTE :**

1. Controlling Dimension : mm
2. Dimension D1 and E do not include mold protrusion.
3. Dimension b does not include dambar protrusion/intrusion.
4. Reference Document : JEDEC MO-183
5. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

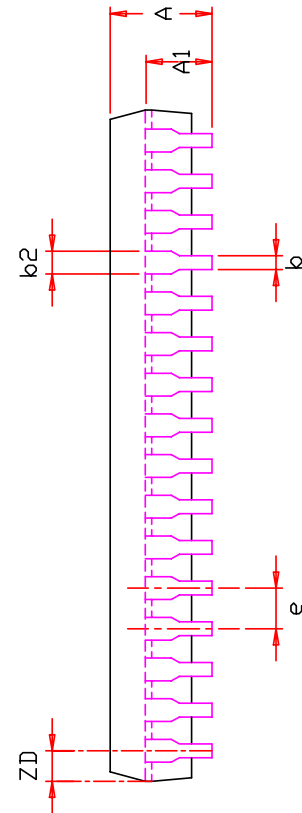
**CASE 1**

|  |  |      |            |
|--|--|------|------------|
|  | TITLE                                  | REV. | DATE       |
|  | 32L 8x13.4mm TSOP-1<br>Package Outline | F    | 06/21/2017 |





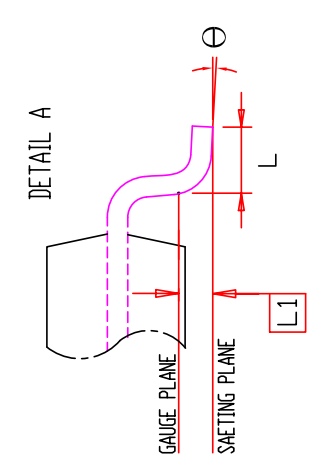
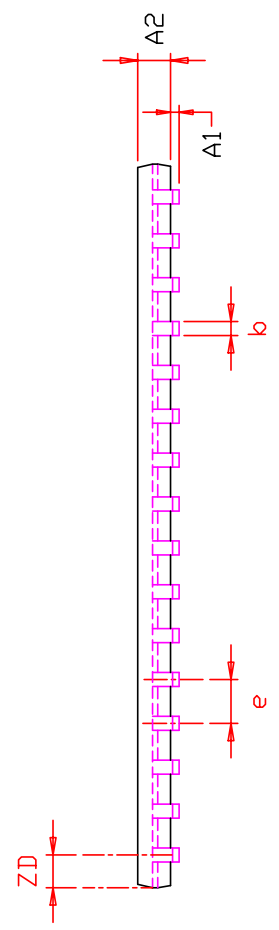
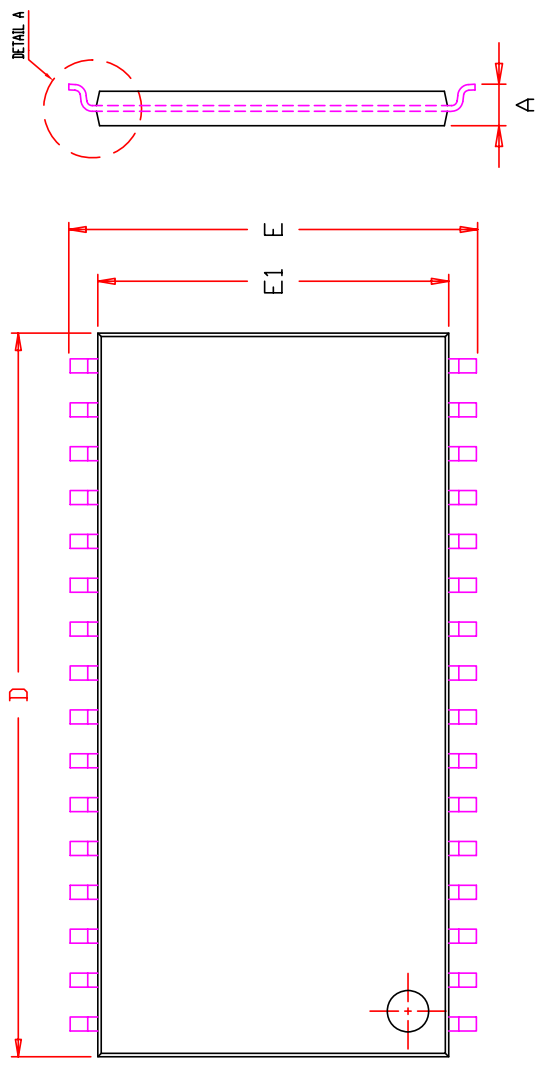
| SYMBOL | DIMENSION IN MM |      |       | DIMENSION IN INCH |       |       |
|--------|-----------------|------|-------|-------------------|-------|-------|
|        | MIN.            | NOM. | MAX.  | MIN.              | NOM.  | MAX.  |
| A      | 3.05            |      | 3.76  | 0.120             |       | 0.148 |
| A1     | 2.08            |      | 2.41  | 0.082             |       | 0.095 |
| A2     | 2.41            | 2.54 | 2.67  | 0.095             | 0.100 | 0.105 |
| A3     | 0.64            |      | 1.09  | 0.025             |       | 0.043 |
| b      | 0.41            |      | 0.51  | 0.016             |       | 0.020 |
| b2     | 0.66            |      | 0.81  | 0.026             |       | 0.032 |
| D      | 20.82           |      | 21.09 | 0.820             |       | 0.830 |
| E      | 8.38            | 8.51 | 8.64  | 0.330             | 0.335 | 0.340 |
| E1     | 7.49            | 7.62 | 7.75  | 0.295             | 0.300 | 0.305 |
| E2     | 6.48            |      | 6.99  | 0.255             |       | 0.275 |
| e      | 1.27            | BSC. |       | 0.050             | BSC.  |       |
| ZD     | 0.95            | REF. |       | 0.037             | REF.  |       |



**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

|      |       |                                   |      |   |      |            |
|------|-------|-----------------------------------|------|---|------|------------|
| ISSI | TITLE | 32L 300mil SOJ<br>Package Outline | REV. | C | DATE | 08/14/2009 |
|      |       |                                   |      |   |      |            |



| SYMBOL | DIMENSION IN MM |       |       | DIMENSION IN INCH |       |       |
|--------|-----------------|-------|-------|-------------------|-------|-------|
|        | MIN.            | NOM.  | MAX.  | MIN.              | NOM.  | MAX.  |
| A      | 1.00            |       | 1.20  | 0.039             |       | 0.047 |
| A1     | 0.05            |       | 0.15  | 0.002             |       | 0.006 |
| A2     | 0.95            | 1.00  | 1.05  | 0.037             | 0.039 | 0.041 |
| b      | 0.30            |       | 0.52  | 0.012             |       | 0.020 |
| D      | 20.82           | 20.95 | 21.08 | 0.820             | 0.825 | 0.830 |
| E      | 11.56           | 11.76 | 11.96 | 0.455             | 0.463 | 0.471 |
| E1     | 10.03           | 10.16 | 10.29 | 0.395             | 0.400 | 0.405 |
| e      | 1.27 BSC.       |       |       | 0.050 BSC.        |       |       |
| L      | 0.40            | 0.50  | 0.60  | 0.016             | 0.020 | 0.024 |
| L1     | 0.25 BSC.       |       |       | 0.010 BSC.        |       |       |
| ZD     | 0.95 REF.       |       |       | 0.037 REF.        |       |       |
| θ      | 0               |       | 8°    | 0                 |       | 8°    |

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

|  |                                      |      |            |
|--|--------------------------------------|------|------------|
|  | TITLE                                | REV. | DATE       |
|  | 32L 400mil TSOP-2<br>Package Outline | E    | 06/23/2009 |