

IS65C256AL IS62C256AL



32K x 8 LOW POWER CMOS STATIC RAM

FEBRUARY 2020

FEATURES

- Access time: 25 ns, 45 ns
- Low active power: 200 mW (typical)
- Low standby power
 - 150 μ W (typical) CMOS standby
 - 15 mW (typical) operating
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- Lead-free available
- Industrial and Automotive temperatures available

DESCRIPTION

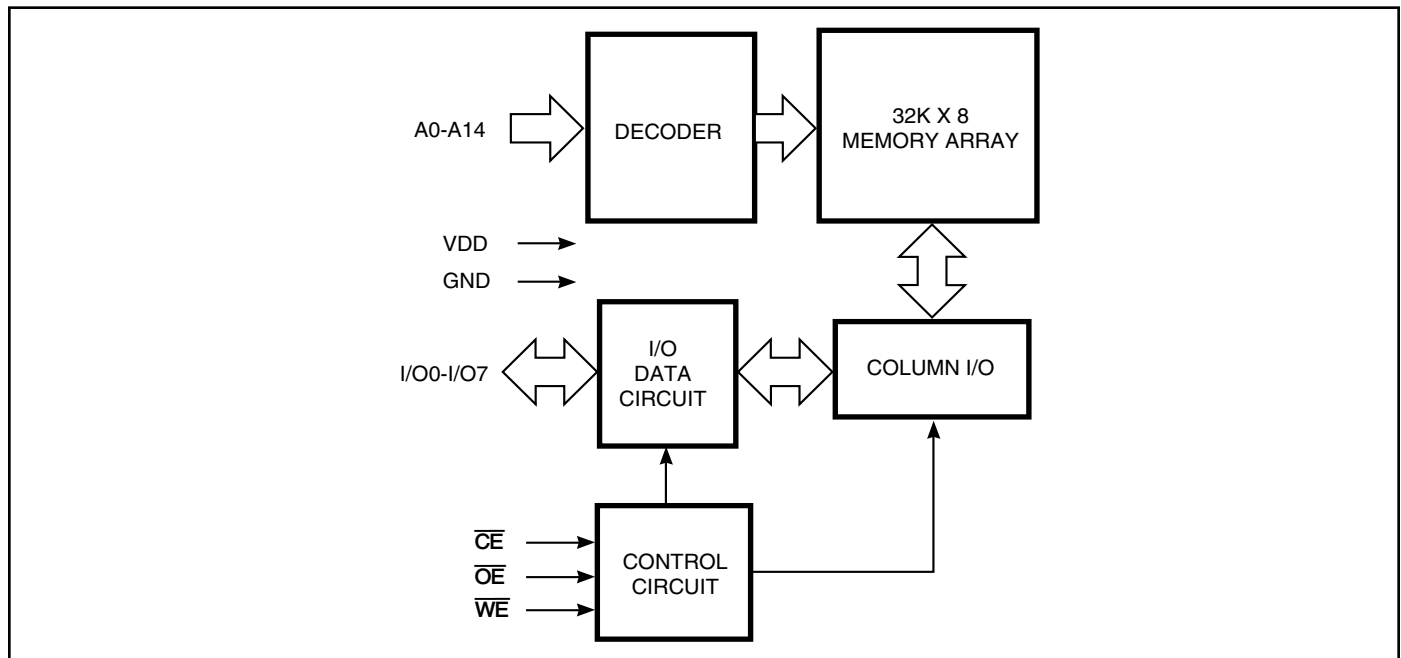
The *ISSI* IS62C256AL/IS65C256AL is a low power, 32,768 word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance, low power CMOS technology.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 150 μ W (typical) at CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Select (\overline{CE}) input and an active LOW Output Enable (\overline{OE}) input. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS62C256AL/IS65C256AL is pin compatible with other 32Kx8 SRAMs in plastic SOP or TSOP (Type I) package.

FUNCTIONAL BLOCK DIAGRAM

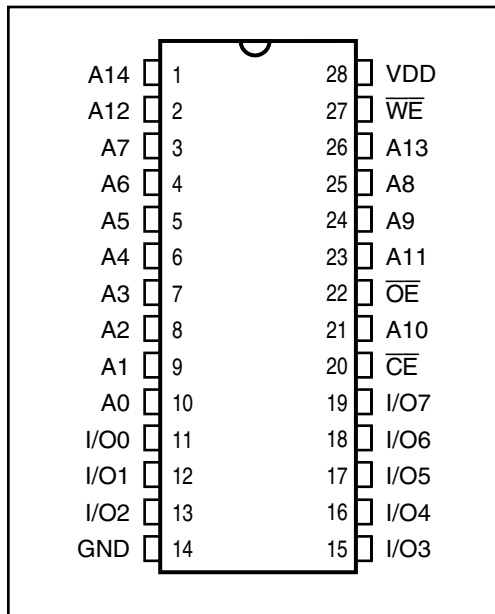


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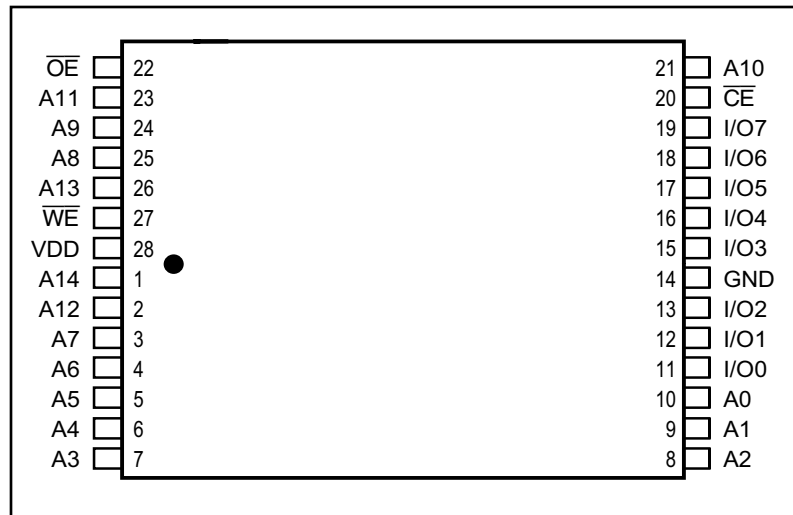
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- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

PIN CONFIGURATION
28-Pin SOP



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
CE	Chip Select Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
VDD	Power
GND	Ground

TRUTH TABLE

Mode	WE	CE	OE	I/O Operation	VDD Current
Not Selected (Power-down)	X	H	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
PT	Power Dissipation	0.5	W
IOUT	DC Output Current (LOW)	20	mA

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Part No.	Range	Ambient Temperature	V _{DD}
IS62C256AL	Commercial	0°C to +70°C	5V ± 10%
IS62C256AL	Industrial	-40°C to +85°C	5V ± 10%
IS65C256AL	Automotive	-40°C to +125°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -1.0 mA	2.4	—	V	
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 2.1 mA	—	0.4	V	
V _{IH}	Input HIGH Voltage		2.2	V _{DD} + 0.5	V	
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V	
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-10	10	
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	Com.	-1	1	μA
			Ind.	-2	2	
			Auto.	-10	10	

Note: 1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-25 ns		-45 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC1}	V _{DD} Operating Supply Current	V _{DD} = Max., \overline{CE} = V _{IL} I _{OUT} = 0 mA, f = 0	Com.	—	15	—	15	mA
			Ind.	—	20	—	20	
			Auto.	—	25	—	25	
I _{CC2}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., \overline{CE} = V _{IL} I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	25	—	20	mA
			Ind.	—	30	—	25	
			Auto.	—	35	—	30	
			typ. ⁽²⁾	15	12			
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	100	—	100	μA
			Ind.	—	120	—	120	
			Auto.	—	150	—	150	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	15	—	15	μA
			Ind.	—	20	—	20	
			Auto.	—	50	—	50	
			typ. ⁽²⁾	5	5			

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 5.0V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	10	pF

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-25 ns		-45 ns		Unit
		Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	25	—	45	—	ns
t _{AA}	Address Access Time	—	25	—	45	ns
t _{OHA}	Output Hold Time	2	—	2	—	ns
t _{ACS}	CE Access Time	—	25	—	45	ns
t _{DOE}	OE Access Time	—	13	—	25	ns
t _{LZOE⁽²⁾}	OE to Low-Z Output	0	—	0	—	ns
t _{HZOE⁽²⁾}	OE to High-Z Output	0	12	0	20	ns
t _{LZCS⁽²⁾}	CE to Low-Z Output	3	—	3	—	ns
t _{HZCS⁽²⁾}	CE to High-Z Output	0	12	0	20	ns
t _{PU⁽³⁾}	CE to Power-Up	0	—	0	—	ns
t _{PD⁽³⁾}	CE to Power-Down	—	20	—	30	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

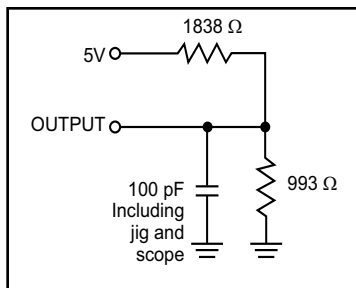


Figure 1.

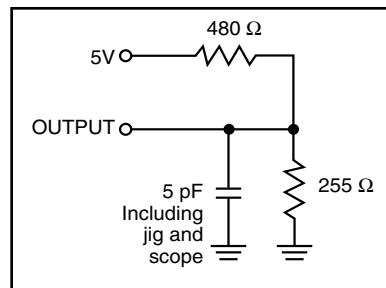
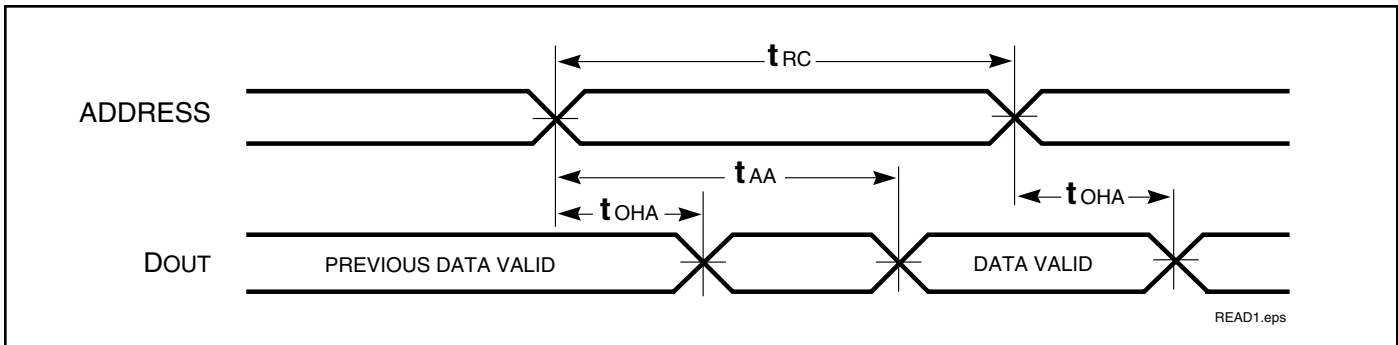


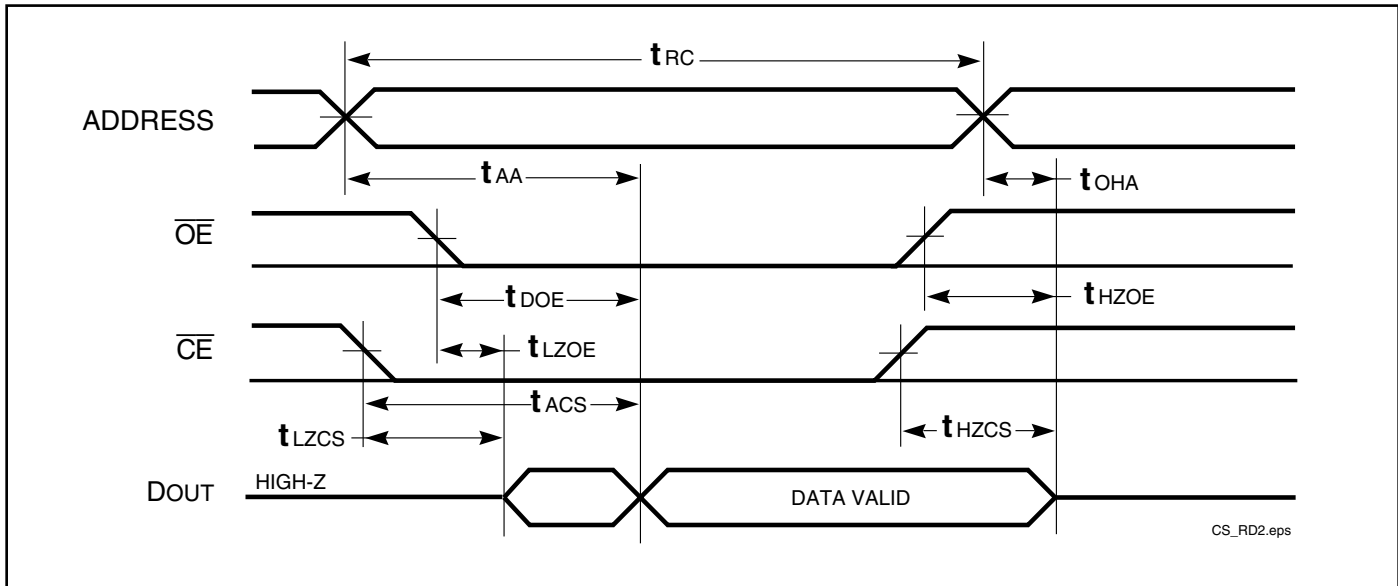
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
3. Address is valid prior to or coincident with \overline{CE} LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

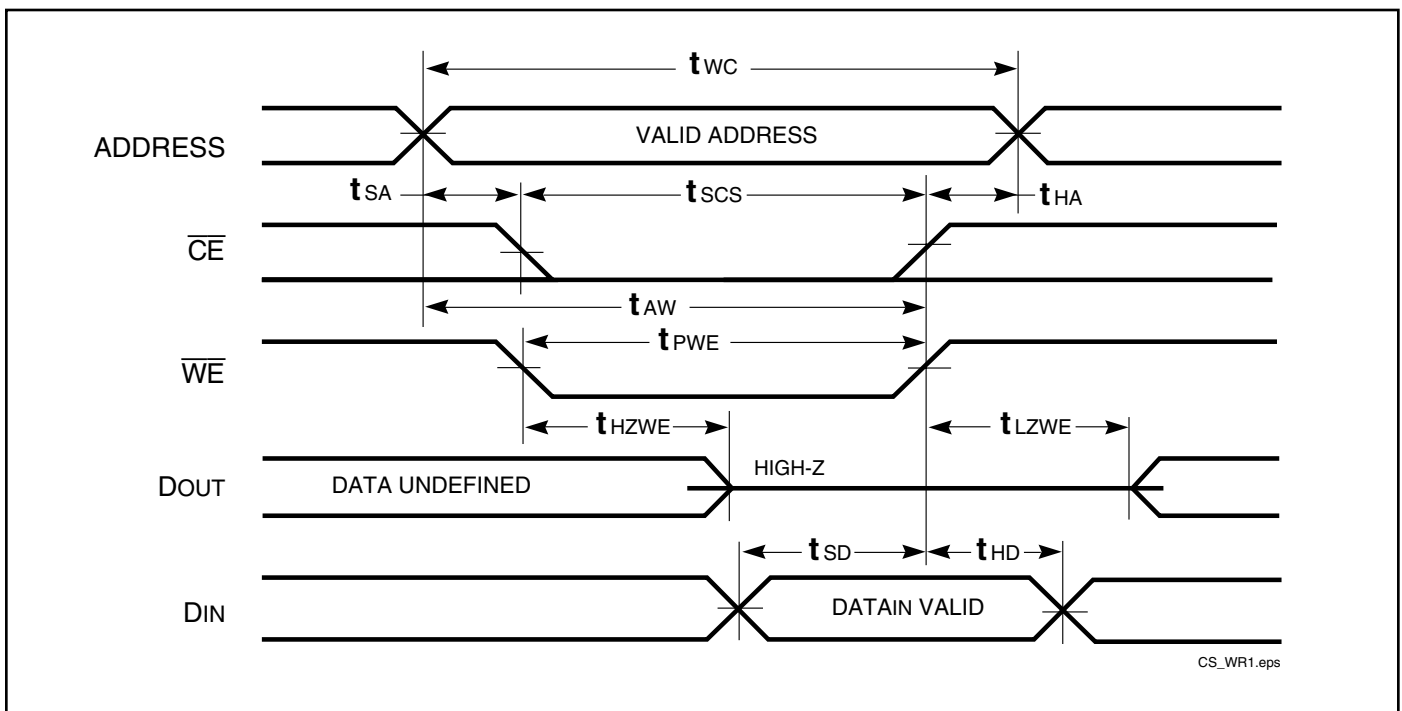
Symbol	Parameter	-25 ns		-45 ns		Unit
		Min.	Max.	Min.	Max.	
t _{wc}	Write Cycle Time	25	—	45	—	ns
t _{scs}	\overline{CE} to Write End	15	—	35	—	ns
t _{aw}	Address Setup Time to Write End	15	—	25	—	ns
t _{ha}	Address Hold from Write End	0	—	0	—	ns
t _{sa}	Address Setup Time	0	—	0	—	ns
t _{pwe⁽⁴⁾}	\overline{WE} Pulse Width	15	—	25	—	ns
t _{sd}	Data Setup to Write End	12	—	20	—	ns </td
t _{hd}	Data Hold from Write End	0	—	0	—	ns
t _{hzwe⁽²⁾}	\overline{WE} LOW to High-Z Output	—	8	—	20	ns
t _{lzwe⁽²⁾}	\overline{WE} HIGH to Low-Z Output	0	—	0	—	ns

Notes:

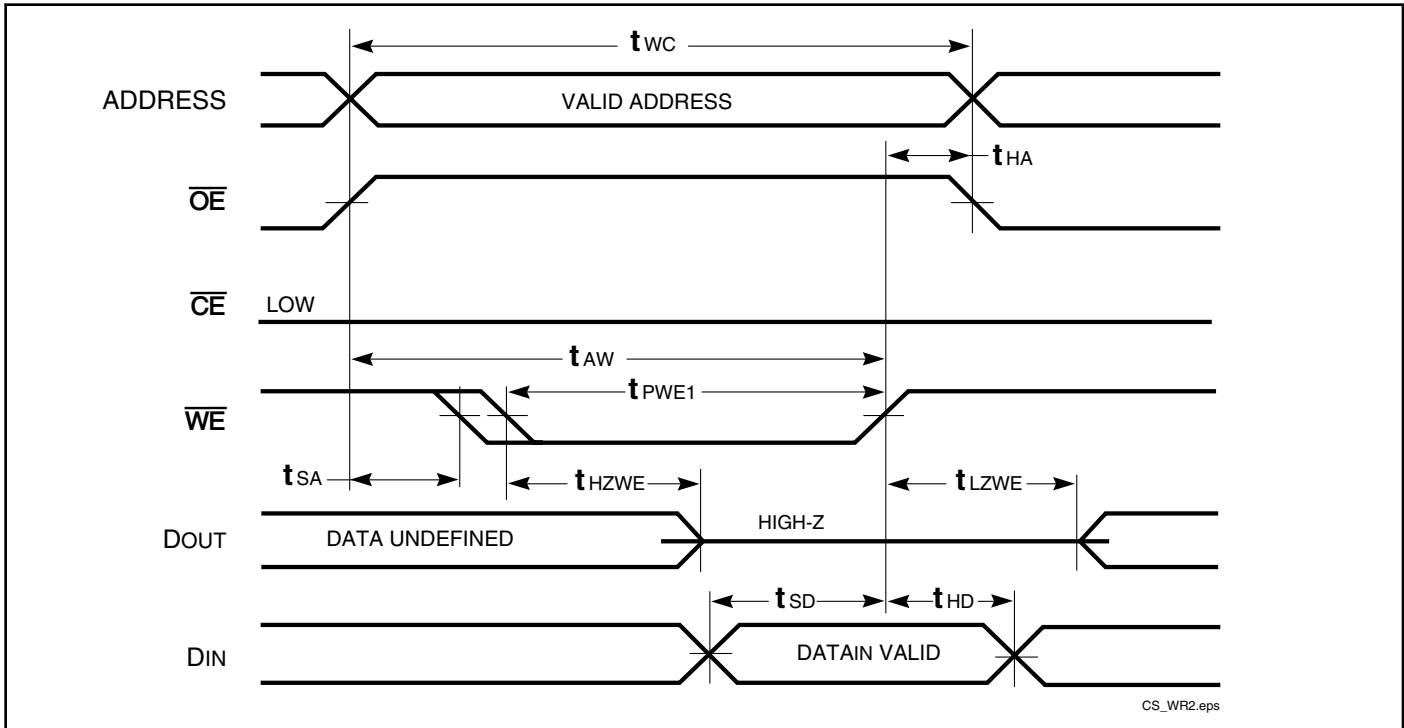
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with \overline{OE} HIGH.

AC WAVEFORMS

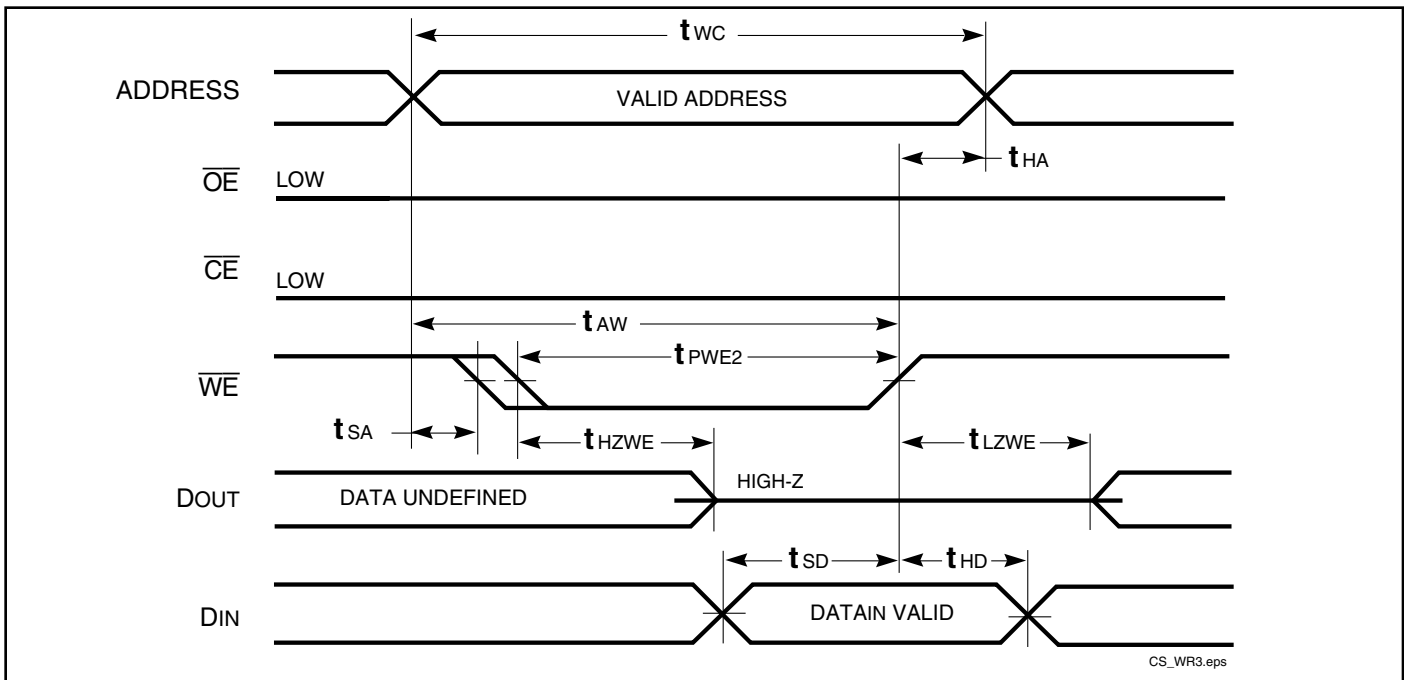
WRITE CYCLE NO. 1 (\overline{CE} Controlled, \overline{OE} is HIGH or LOW) ⁽¹⁾



WRITE CYCLE NO. 2 (\overline{OE} is HIGH During Write Cycle) ^(1,2)



WRITE CYCLE NO. 3 (\overline{OE} is LOW During Write Cycle) ⁽¹⁾



Notes:

1. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

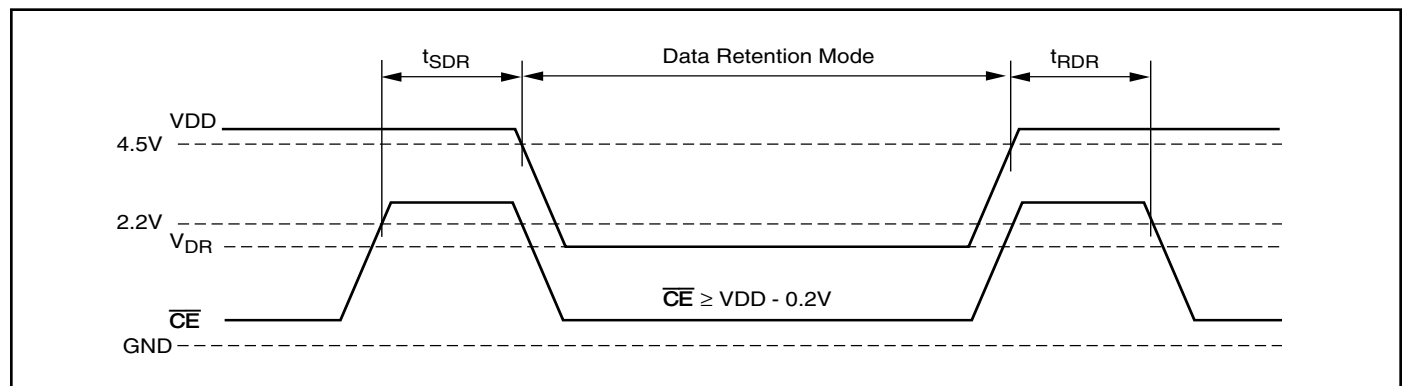
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0		5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V, \overline{CE} \geq V_{DD} - 0.2V$	Com.	—	15	μA
		$V_{IN} \geq V_{DD} - 0.2V, \text{ or } V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	20	
			Auto.	—	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0			ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}			ns

Note:

1. Typical Values are measured at $V_{DD} = 5V, T_A = 25^\circ C$ and not 100% tested.

DATA RETENTION WAVEFORM (\overline{CE} Controlled)



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62C256AL-45TL	TSOP, Lead-free
	IS62C256AL-45UL	Plastic SOP, Lead-free

ORDERING INFORMATION

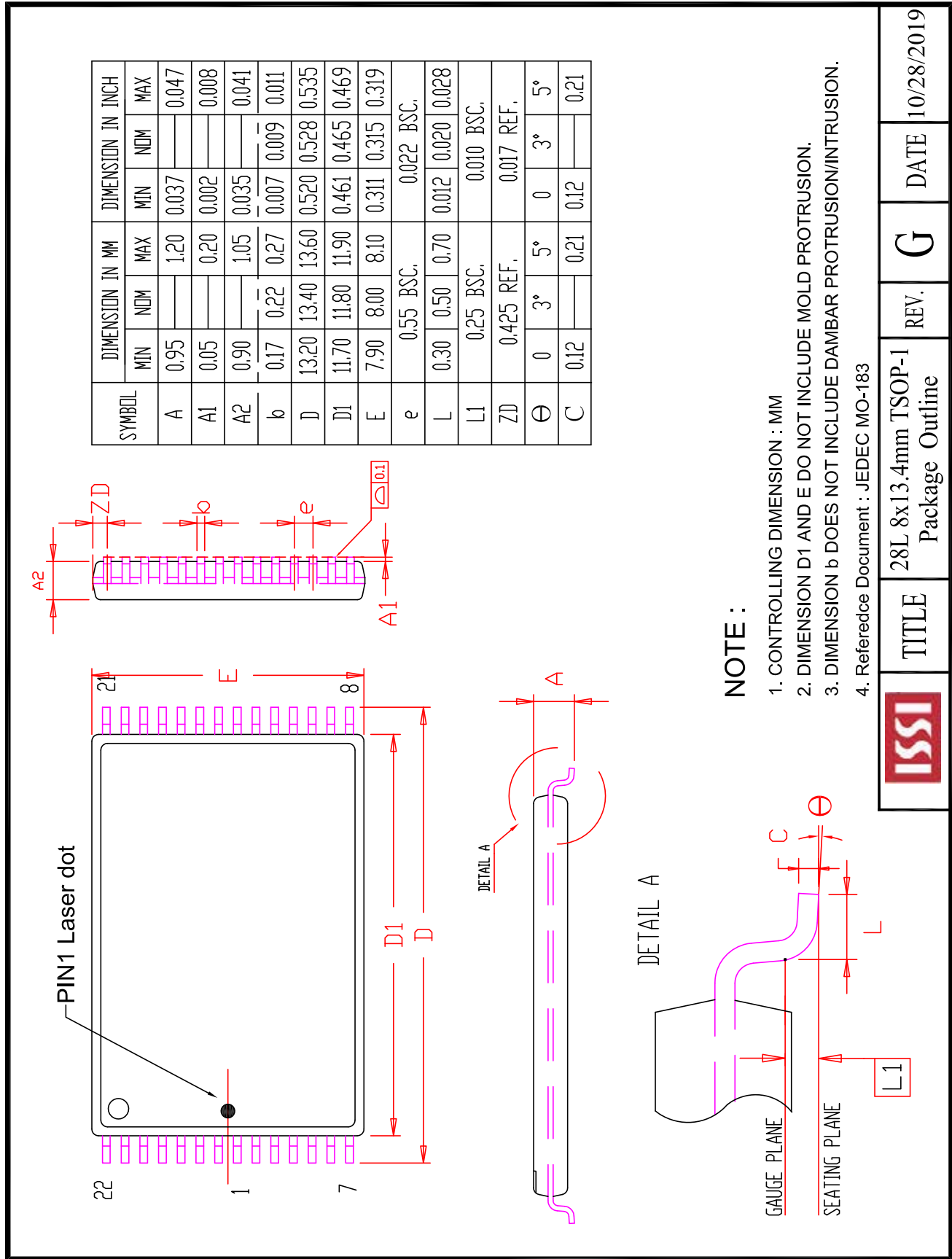
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
25	IS62C256AL-25ULI	Plastic SOP, Lead-free
45	IS62C256AL-45TLI	TSOP, Lead-free
	IS62C256AL-45ULI	Plastic SOP, Lead-free

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Speed (ns)	Order Part No.	Package
25	IS65C256AL-25TLA3	TSOP, Lead-free
	IS65C256AL-25ULA3	Plastic SOP, Lead-free
45	IS65C256AL-45TLA3	TSOP, Lead-free
	IS65C256AL-45ULA3	Plastic SOP, Lead-free



NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

	TITLE	28L 8x13.4mm TSOP-1 Package Outline	REV.	G	DATE	10/28/2019
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