JANUARY 2015

1Mx16 LOW VOLTAGE, ULTRA LOW POWER & LOW POWER CMOS STATIC RAM

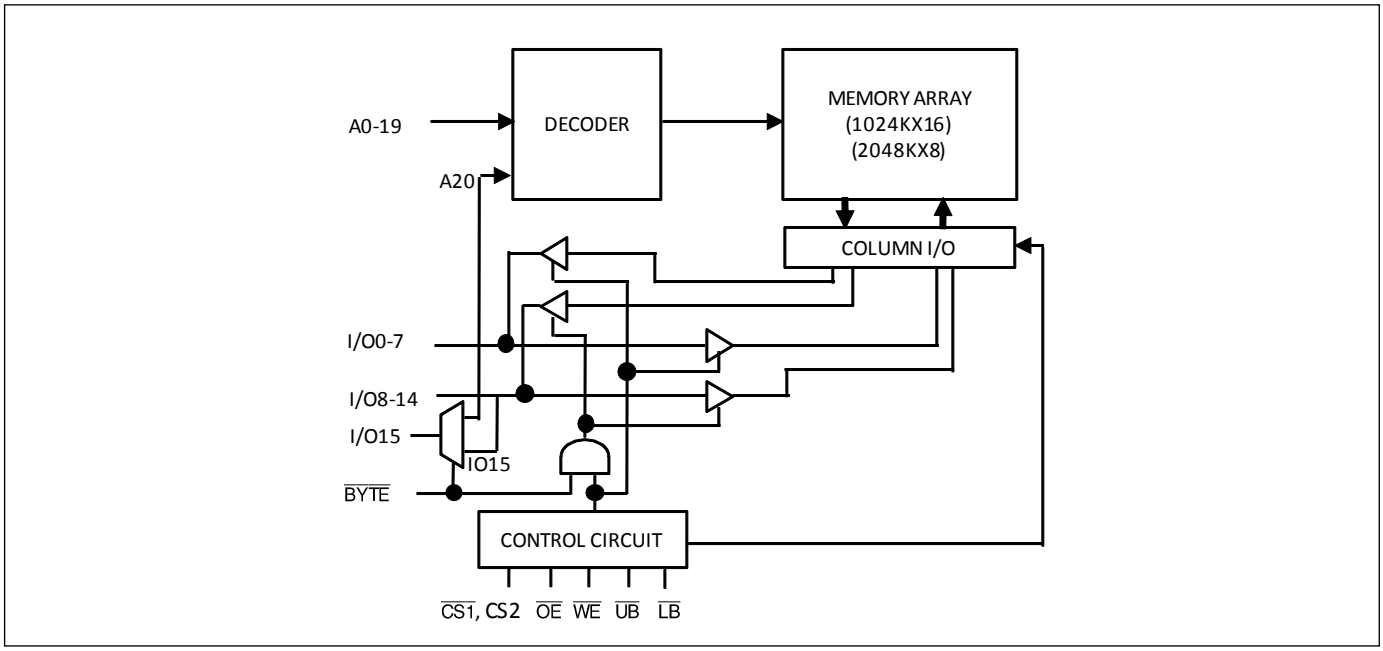
KEY FEATURES

- High-speed access time: 45ns, 55ns.
- CMOS low power operation
  - 25 µA (typical) CMOS standby
- CMOS for optimum speed and power and TTL compatible interface levels
- Single power supply
  - 1.65V~1.98V V_{DD} (IS62/65WV102416DALL)
  - 2.2V~3.6V V_{DD} (IS62/65WV102416DBLL)
- Fully static operation: no clock or refresh required
- Industrial and Automotive temperature support

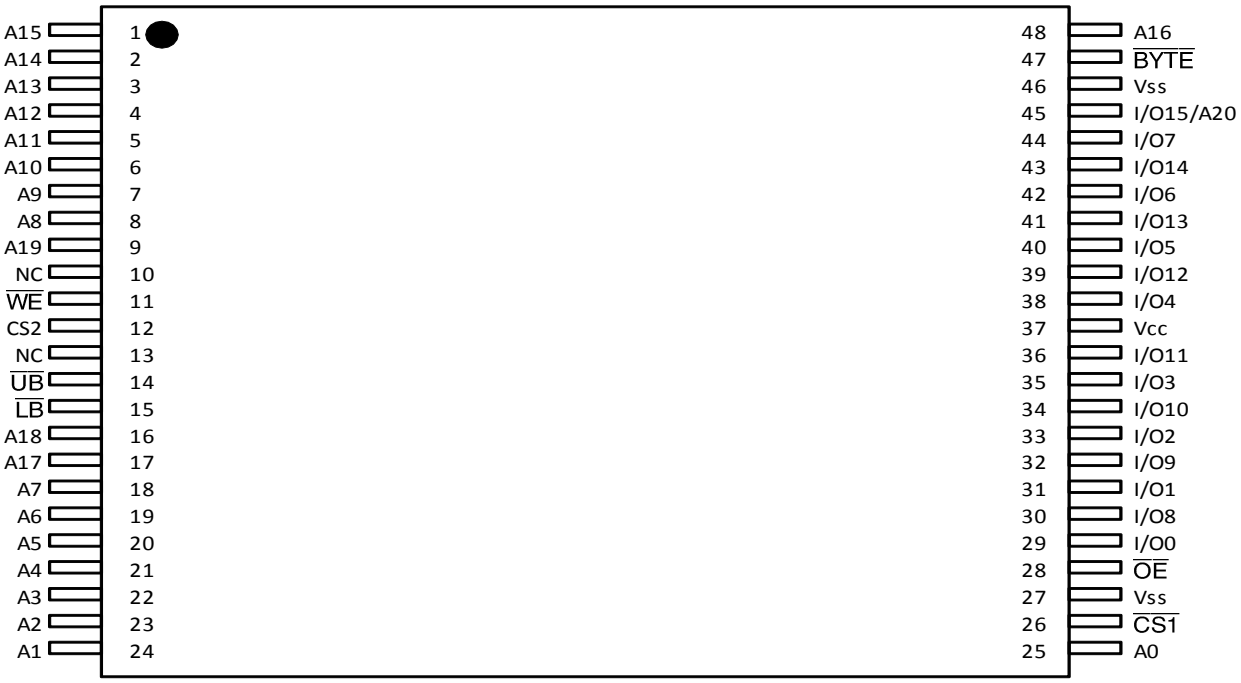
DESCRIPTION

The *ISSI* IS62/65WV102416DALL, IS62/65WV102416DBLL are ULTRA LOW POWER CMOS 16Mbit static RAMs organized as 1M words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices. The IS62WV102416DALL/DBLL and IS65WV102416DALL/DBLL are packaged in 48-Pin TSOP (TYPE I).

BLOCK DIAGRAM



48-PIN TSOP-I



PIN DESCRIPTIONS

A0-A19	Address Inputs
I/O0-I/O14	Data Inputs/Outputs, I/O8 to I/O14 pins are not used in x8 Mode.
I/O15/A20	I/O15, when used in a x16 Mode. A20 when used in a x8 Mode,
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7). This pin is not used in x8 Mode.
$\overline{UB}$	Upper-byte Control (I/O8-I/O15). This pin is not used in x8 Mode.
$\overline{BYTE}$	$\overline{BYTE}$ pin must be tied to either V_{DD} to use the device as a 1024Kx16 SRAM or GND to use as 2048Kx8 SRAM. In x8 mode, Pin 45 becomes A20, while $\overline{UB}$, $\overline{LB}$ and I/O8 to I/O14 pins are not used.
NC	No Connection
VDD	Power
Vss	Ground

*For x8/x16 switchable configuration BGA option, please contact sram@issi.com

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected ($\overline{CS1}$ HIGH or CS2 LOW or both $\overline{UB}$ and $\overline{LB}$ are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be either ISB1 or ISB2 depending on the input level. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input LOW. The input and output pins(I/O0-15) are in data input mode. Output buffers are closed during this time even if $\overline{OE}$ is LOW. $\overline{UB}$ and $\overline{LB}$ enables a byte write feature. By enabling $\overline{LB}$ LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with $\overline{UB}$ being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input HIGH. When $\overline{OE}$ is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. $\overline{UB}$ and $\overline{LB}$ enables a byte read feature. By enabling $\overline{LB}$ LOW, data from memory appears on I/O0-7. And with $\overline{UB}$ being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling $\overline{OE}$ HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

TRUTH TABLE

Mode	$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	VDD Current
Not Selected	H	X	X	X	X	X	High-Z	High-Z	ISB1,ISB2
	X	L	X	X	X	X	High-Z	High-Z	
	X	X	X	X	H	H	High-Z	High-Z	
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	ICC
	L	H	H	H	X	L	High-Z	High-Z	
Read	L	H	H	L	L	H	DOUT	High-Z	ICC
	L	H	H	L	H	L	High-Z	DOUT	
	L	H	H	L	L	L	DOUT	DOUT	
Write	L	H	L	X	L	H	DIN	High-Z	ICC
	L	H	L	X	H	L	High-Z	DIN	
	L	H	L	X	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tBIAS	Temperature Under Bias	–55 to +125	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.9(V_{DD}+0.3V)	V
tStg	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE(1)

Range	Device Marking	Ambient Temperature	VDD (min)	VDD (typ)	VDD (max)
Commercial	IS62WV102416DALL	0°C to +70°C	1.65V	1.8V	1.98V
Industrial	IS62WV102416DALL	-40°C to +85°C	1.65V	1.8V	1.98V
Automotive	IS65WV102416DALL	-40°C to +125°C	1.65V	1.8V	1.98V
Commercial	IS62WV102416DBLL	0°C to +70°C	2.2V	3.3V	3.6V
Industrial	IS62WV102416DBLL	-40°C to +85°C	2.2V	3.3V	3.6V
Automotive	IS65WV102416DBLL	-40°C to +125°C	2.2V	3.3V	3.6V

Note:
1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	10	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		10	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	43.8	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	7.7	°C/W

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

ELECTRICAL CHARACTERISTICS

IS62(5)WV102416DALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	—	0.2	V
V_{IH}(1)	Input HIGH Voltage		1.4	V_{DD} + 0.2	V
V_{IL}(1)	Input LOW Voltage		–0.2	0.4	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. V_{ILL}(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV102416DBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{DD} < 2.7, I_{OH} = -0.1 mA	2.0	—	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OH} = -1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	2.2 ≤ V_{DD} < 2.7, I_{OL} = 0.1 mA	—	0.4	V
		2.7 ≤ V_{DD} ≤ 3.6, I_{OL} = 2.1 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage	2.2 ≤ V_{DD} < 2.7	1.8	V_{DD} + 0.3	V
		2.7 ≤ V_{DD} ≤ 3.6	2.2	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage	2.2 ≤ V_{DD} < 2.7	–0.3	0.6	V
		2.7 ≤ V_{DD} ≤ 3.6	–0.3	0.8	V
I_{LI}	Input Leakage	GND < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. V_{ILL}(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

IS62(5)WV102416DALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT}=0mA, f=f_{MAX}	Com.	6	12	mA
			Ind.	-	12	
			Auto.	-	12	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT} = 0mA, f=0Hz	Com.	3	6	mA
			Ind.	-	6	
			Auto.	-	6	
ISB1	CMOS Standby Current (CMOS Inputs)	$V_{DD}=V_{DD}(max)$, (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1}$ ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V or (3) $\overline{LB}$ and $\overline{UB}$ ≥ V_{DD}- 0.2V $\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	25	50	µA
			Ind.	-	65	µA
			Auto.	-	165	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

IS62(5)WV102416DBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	Typ.	Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT}=0mA, f=f_{MAX}	Com.	6	12	mA
			Ind.	-	12	
			Auto.	-	12	
ICC1	V_{DD} Static Operating Supply Current	$V_{DD}=V_{DD}(max)$, I_{OUT} = 0mA, f=0Hz	Com.	3	6	mA
			Ind.	-	6	
			Auto.	-	6	
ISB1	CMOS Standby Current (CMOS Inputs)	$V_{DD}=V_{DD}(max)$, (1) 0V ≤ CS2 ≤ 0.2V or (2) $\overline{CS1}$ ≥ V_{DD} - 0.2V, CS2 ≥ V_{DD} - 0.2V or (3) $\overline{LB}$ and $\overline{UB}$ ≥ V_{DD}- 0.2V $\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	25	50	µA
			Ind.	-	65	µA
			Auto.	-	165	µA

Note:
Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = VDD(typ), TA = 25°C

AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	45	-	55	-	ns	1,5
Address Access Time	tAA	-	45	-	55	ns	1
Output Hold Time	tOHA	8	-	8	-	ns	1
$\overline{CS1}$, CS2 Access Time	tACS1/tACS2	-	45	-	55	ns	1
$\overline{OE}$ Access Time	tDOE	-	22	-	25	ns	1
$\overline{OE}$ to High-Z Output	tHZOE	-	18	-	18	ns	2
$\overline{OE}$ to Low-Z Output	tLZOE	5	-	5	-	ns	2
$\overline{CS1}$, CS2 to High-Z Output	tHZCS//tHZCS2	-	18	-	18	ns	2
$\overline{CS1}$, CS2 to Low-Z Output	tLZCS/tLZCS2	10	-	10	-	ns	2
$\overline{LB}$, $\overline{UB}$ Access Time	tBA	-	45	-	55	ns	1
$\overline{LB}$, $\overline{UB}$ to High-Z Output	tHZB	-	18	-	18	ns	2
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	tLZB	10	-	10	-	ns	2

WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	45ns		55ns		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	45	-	55	-	ns	1,3,5
$\overline{CS1}$,CS2 to Write End	tSCS1/tSCS2	35	-	40	-	ns	1,3
Address Setup Time to Write End	tAW	35	-	40	-	ns	1,3
Address Hold from Write End	tHA	0	-	0	-	ns	1,3
Address Setup Time	tSA	0	-	0	-	ns	1,3
$\overline{LB}$, /$\overline{UB}$ Valid to End of Write	tPWB	35	-	40	-	ns	1,3
$\overline{WE}$ Pulse Width	tPWE	35	-	40	-	ns	1,3,4
Data Setup to Write End	tSD	28	-	28	-	ns	1,3
Data Hold from Write End	tHD	0	-	0	-	ns	1,3
$\overline{WE}$ LOW to High-Z Output	tHZWE	-	18	-	18	ns	2,3
$\overline{WE}$ HIGH to Low-Z Output	tLZWE	10	-	10	-	ns	2,3

Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS1}$=LOW, CS2=HIGH, ($\overline{UB}$ or $\overline{LB}$)=LOW, and $\overline{WE}$=LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE is LOW.
5. Address inputs must meet V_{IH} and V_{IL} SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Symbol	Conditions	Units
Input Rise Time	T_R	1.0	V/ns
Input Fall Time	T_F	1.0	V/ns
Output Timing Reference Level	V_{REF}	½ V_{TM}	V
Output Load Conditions	Refer to Figure 1 and 2		

OUTPUT LOAD CONDITIONS FIGURES

Figure1

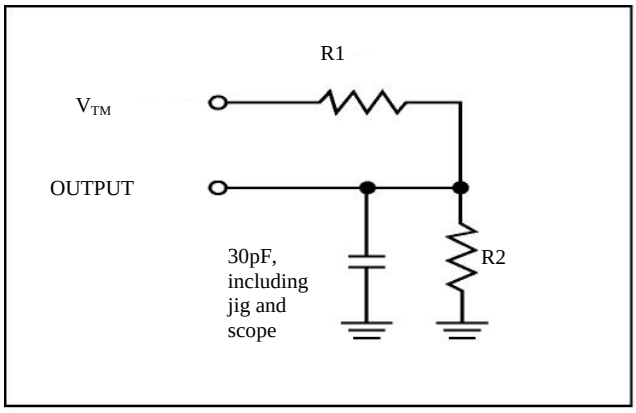
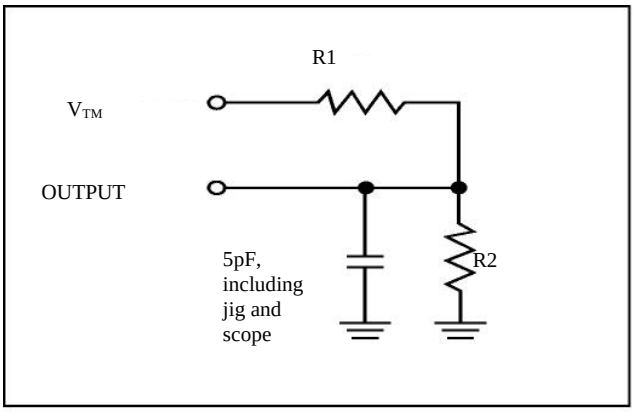


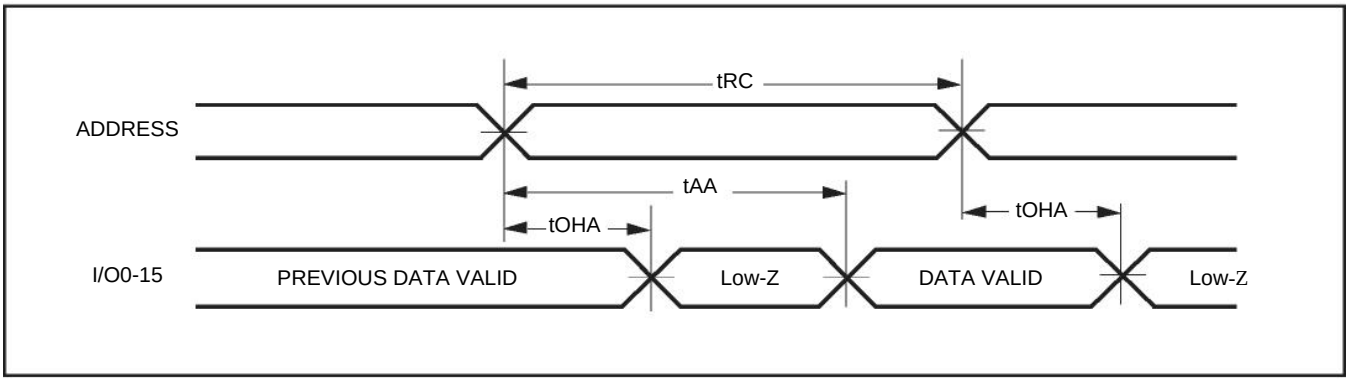
Figure2



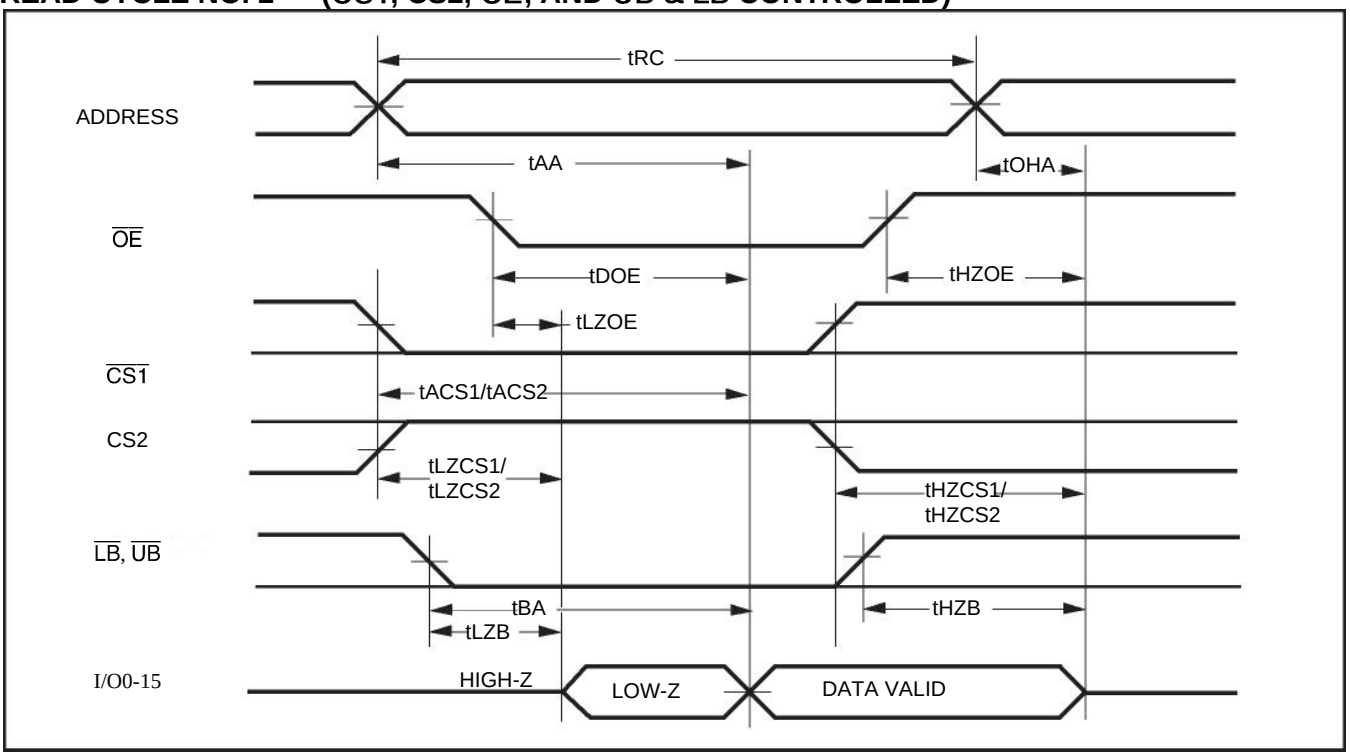
Parameters	V_{DD}=1.65~1.98V	V_{DD}=2.2~2.7V	V_{DD}=2.7~3.6V
R1	13500Ω	16667Ω	1103Ω
R2	10800Ω	15385Ω	1554Ω
V_{TM}	VDD	VDD	VDD

TIMING DIAGRAM

READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED) ($\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})

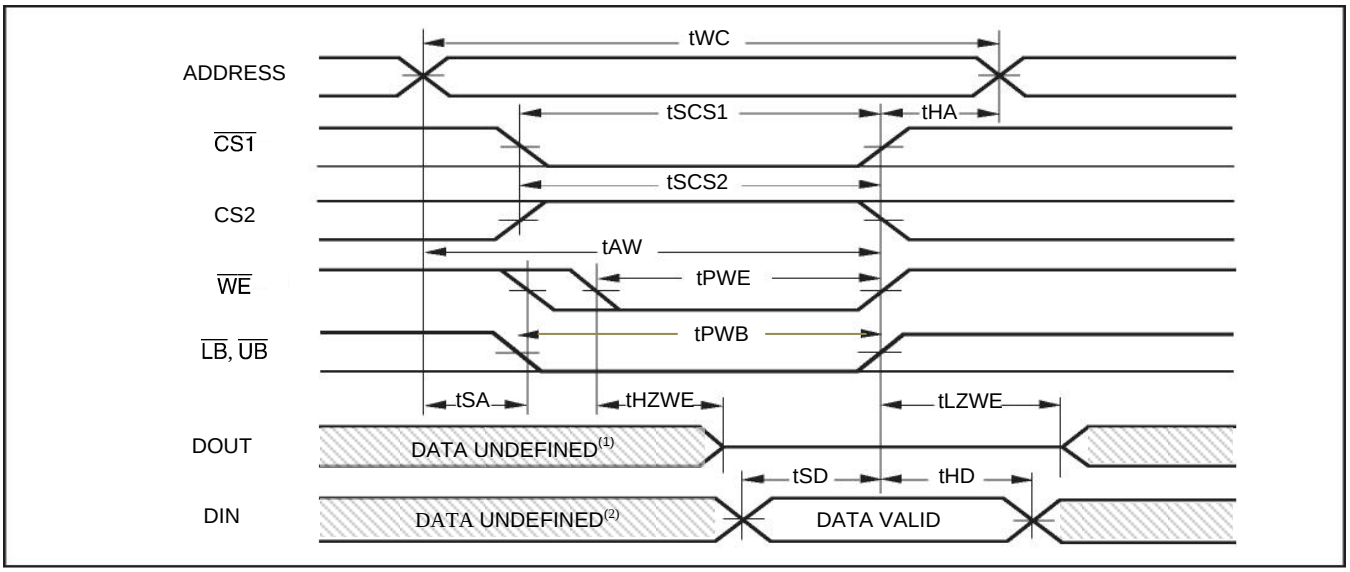


READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$ & $\overline{LB}$ CONTROLLED)



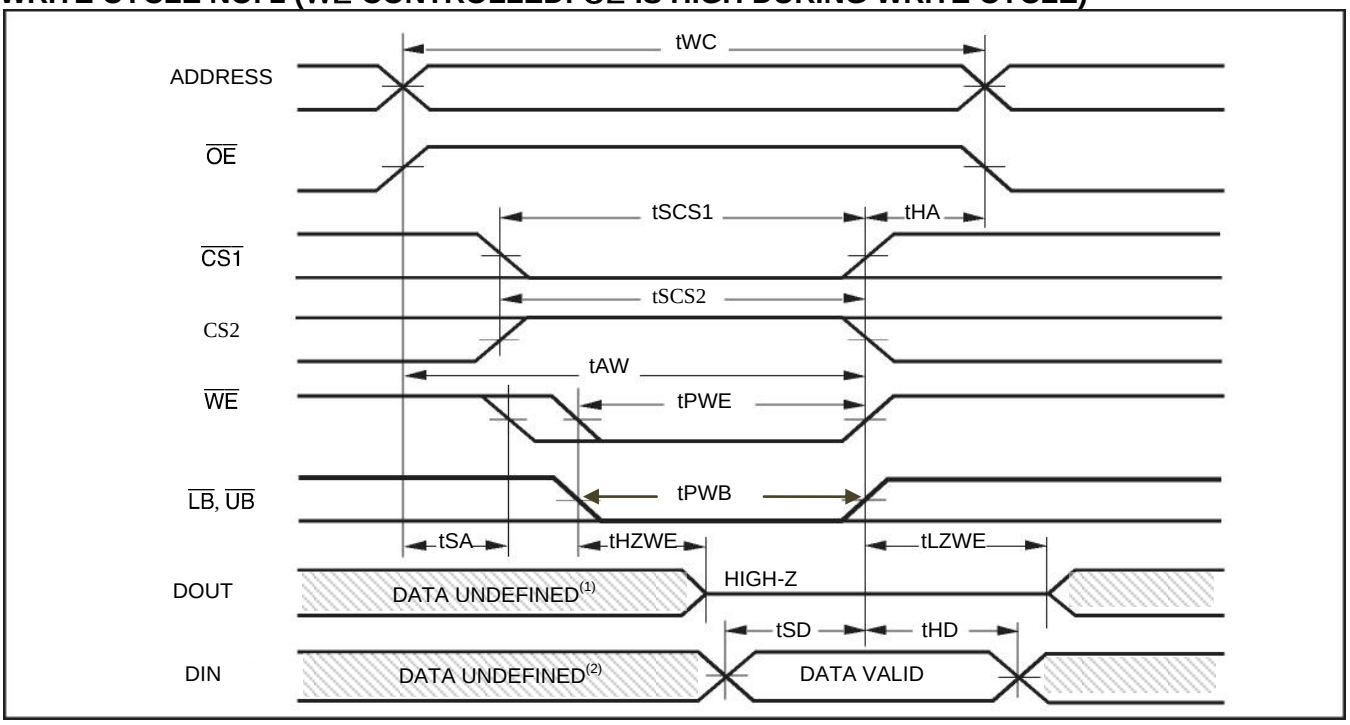
Notes:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$=VIL.CS2=$\overline{WE}$=VIH.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE NO. 1 ($\overline{CS1}$ CONTROLLED, $\overline{OE}$ = HIGH OR LOW)



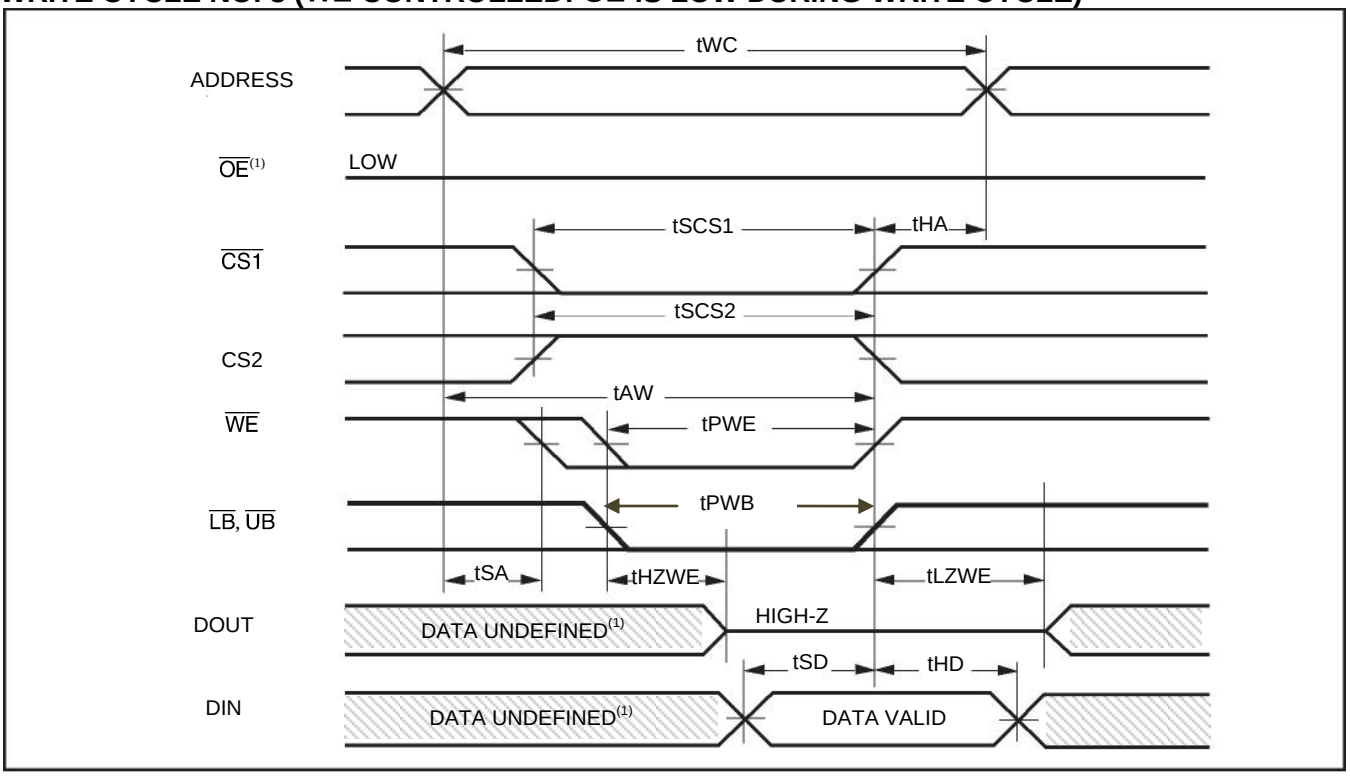
Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after $\overline{OE}$ goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

WRITE CYCLE NO. 2 ($\overline{WE}$ CONTROLLED: $\overline{OE}$ IS HIGH DURING WRITE CYCLE)



Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after $\overline{OE}$ goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

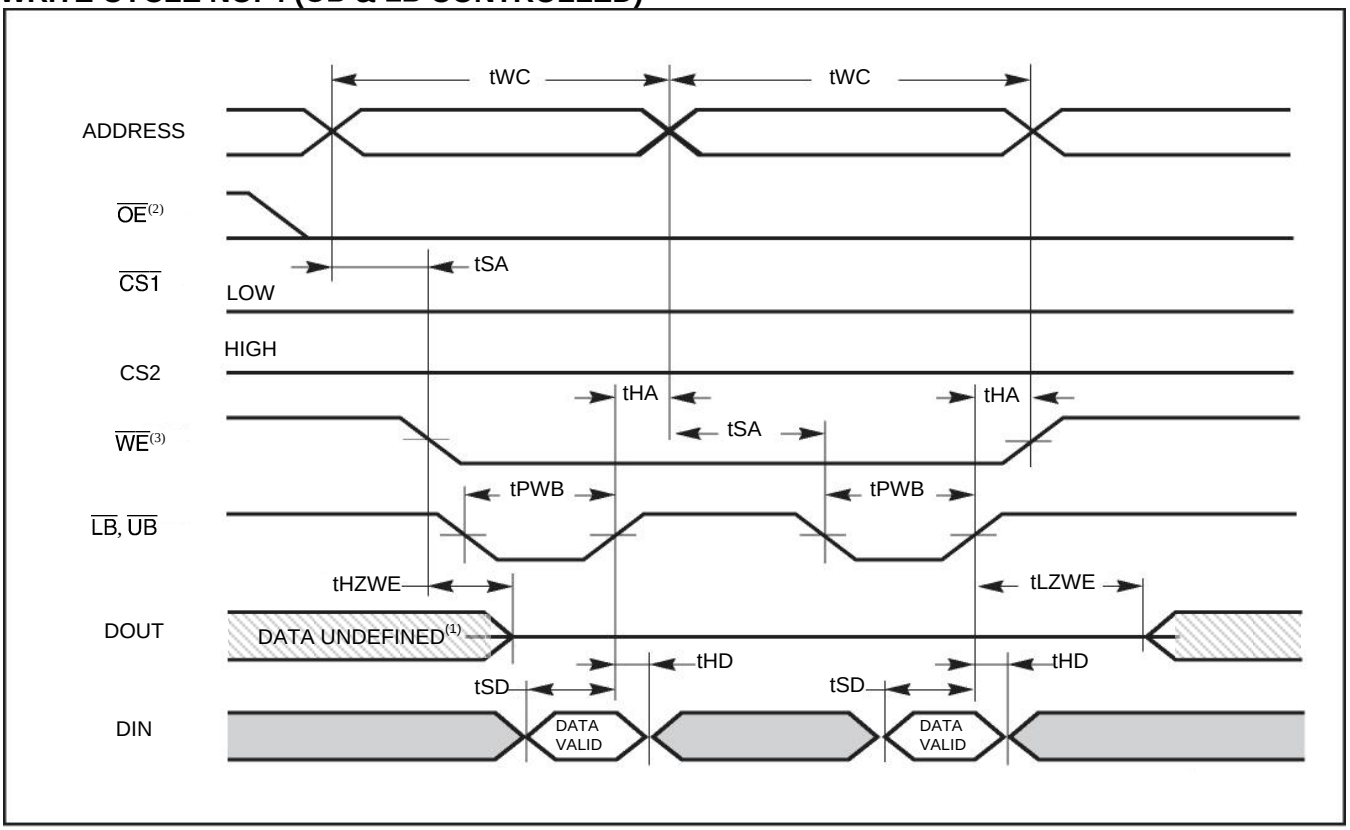
WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED: $\overline{OE}$ IS LOW DURING WRITE CYCLE)



Notes:

1. If $\overline{OE}$ is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

WRITE CYCLE NO. 4 ($\overline{UB}$ & $\overline{LB}$ CONTROLLED)



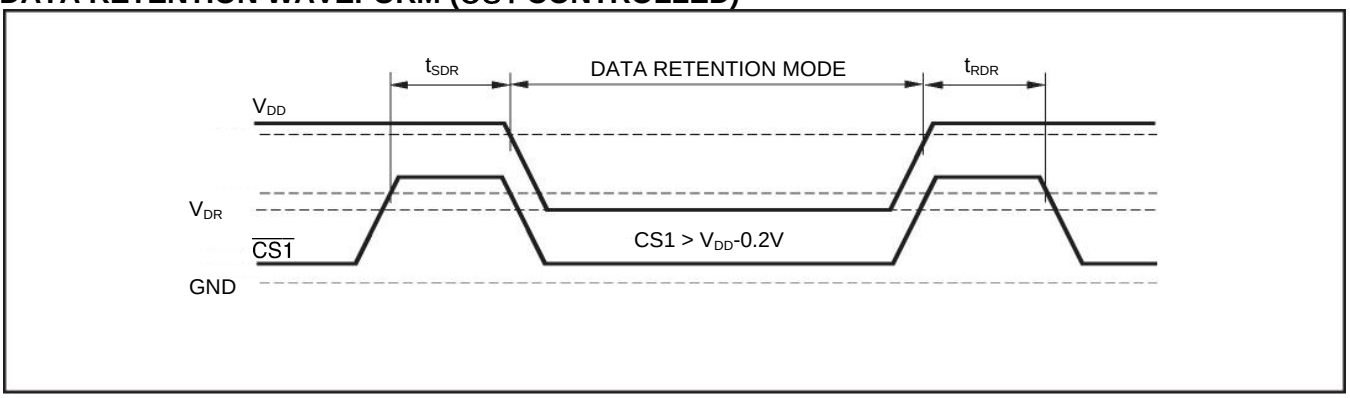
Notes:
1. If $\overline{OE}$ is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, $\overline{OE}$ is recommended to be HIGH during write period.
3. Note $\overline{WE}$ stays LOW in this example. If $\overline{WE}$ toggles, tPWE and tHZWE must be considered.

DATA RETENTION CHARACTERISTICS

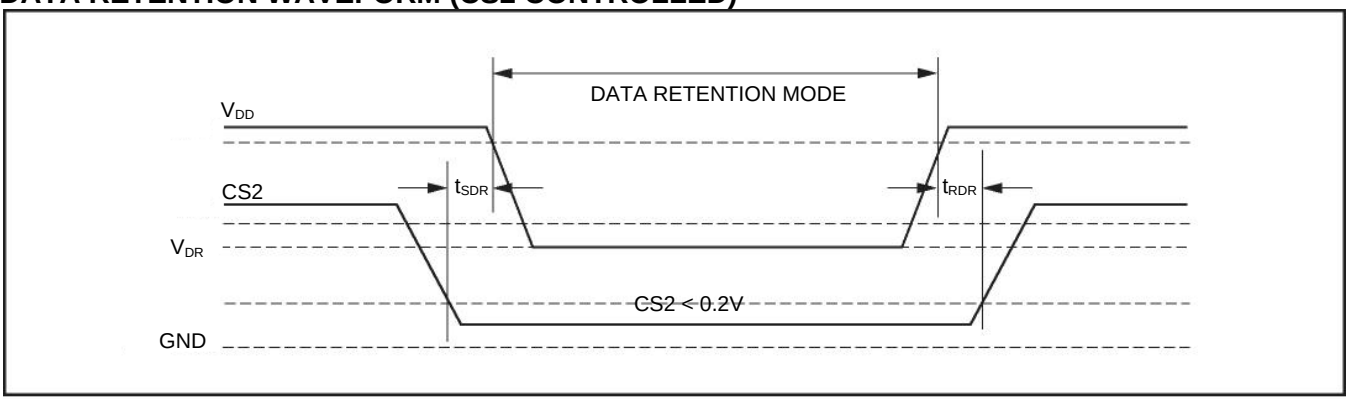
Symbol	Parameter	Test Condition	OPTION	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	IS62(5)WV102416DALL	1.5		-	V
			IS62(5)WV102416DBLL	1.5		-	V
I_{DR}	Data Retention Current	V_{DD}= V_{DR}(min), (1) 0V ≤ CS2 ≤ 0.2V, or (2) $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≥ V_{DD} - 0.2V (3) $\overline{LB}$ and $\overline{UB}$ ≥ V_{DD} -0.2V, $\overline{CS1}$ ≤ 0.2V, CS2 ≥ V_{DD} - 0.2V	Com.	-	-	50	uA
			Ind.	-	-	65	
			Auto	-	-	165	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Note:
Typical values are measured at VDD=VDR(min), TA = 25℃ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CS1}$ CONTROLLED)



DATA RETENTION WAVEFORM (CS2 CONTROLLED)



ORDERING INFORMATION

1.65V~1.98V Industrial Range (-40°C to +85°C)

Speed (ns)	Order Part No	Package
55	IS62WV102416DALL-55TI	48pin TSOP (Type I)
	IS62WV102416DALL-55TLI	48pin TSOP (Type I), Lead-free

1.65V~1.98V Automotive (A3) Range (-40°C to +125°C)

Speed (ns)	Order Part No	Package
55	IS65WV102416DALL-55TA3	48pin TSOP (Type I)
	IS65WV102416DALL-55TLA3	48pin TSOP (Type I), Lead-free

2.2V~3.6V Industrial Range (-40°C to +85°C)

Speed (ns)	Order Part No	Package
45	IS62WV102416DBLL-45TI	48pin TSOP (Type I)
	IS62WV102416DBLL-45TLI	48pin TSOP (Type I), Lead-free
55	IS62WV102416DBLL-55TLI	48pin TSOP (Type I), Lead-free

2.2V~3.6V Automotive (A3) Range (-40°C to +125°C)

Speed (ns)	Order Part No	Package
55	IS65WV102416DBLL-55CTA3	48pin TSOP (Type I), Copper Leadframe
	IS65WV102416DBLL-55CTLA3	48pin TSOP (Type I), Lead-free, Copper Leadframe