ISL15110

PLC MIMO Line Driver

FN8282
Rev 1.00
Apr 6, 2018

The ISL15110 is a dual port differential line driver developed for Power Line Communication (PLC) Multi Input Multi Output (MIMO) applications. MIMO PLC requires transmission on one or two pairs of Phase, Neutral, and Ground wires. The device is designed to drive heavy line loads while maintaining a high level of linearity required in OFDM PLC modem links. With 15.5dBm of total MIMO transmit signal power (12.5dBm per each pair) into a 50Ω line load, the drivers deliver -50dB average MTPR distortion across the output spectrum.

Each of the two differential drivers has a control pin to enable and disable its differential output. These controls allow for independent TDM operation of the two differential drivers, as required in ITU-T MIMO G.hn and related standard based PLC applications. In disable mode, the line driver output maintains a high impedance characteristic to preserve TDM receive signal integrity.

The ISL15110 includes an external IBIAS pin for quiescent current flexibility. Grounding the pin in single supply designs gives the nominal currents in the “Electrical Specifications” table starting on page 5, while inserting a resistor from pin to ground can be used to scale down the quiescent current for both ports.

The ISL15110 is available in the thermally-enhanced 20 Ld QFN and is specified for operation across the full -40°C to +85°C temperature range.

Related Literature

For a full list of related documents, visit our website

- ISL15110 product page

Features

- Dual differential drivers
- 50MHz broadband PLC G.hn
- Enable/disable control pins for TDM operation
- -50dBc average MTPR distortion
- Single supply +12V nominal operation
- Enhanced surge current handling capability
- Thermally enhanced 20 Ld QFN package
- Enable port control voltage <0.7V
- Disable port control voltage >1.7V

Applications

- Home networking over power lines
- ITU-T G.hn (G.9963) MIMO PLC

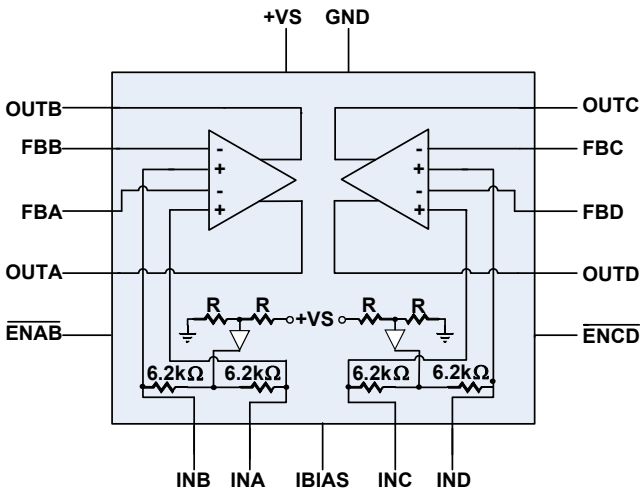


FIGURE 1. BLOCK DIAGRAM

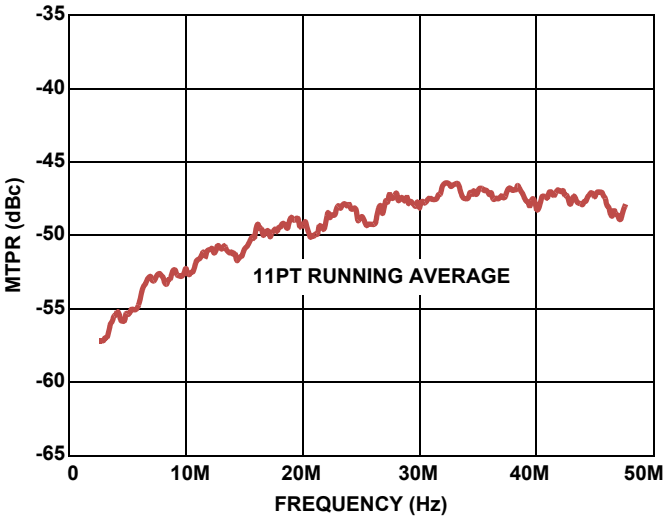


FIGURE 2. SISO 15.5dBm, 2MHz TO 50MHz MTPR TEST

Typical Application Circuit

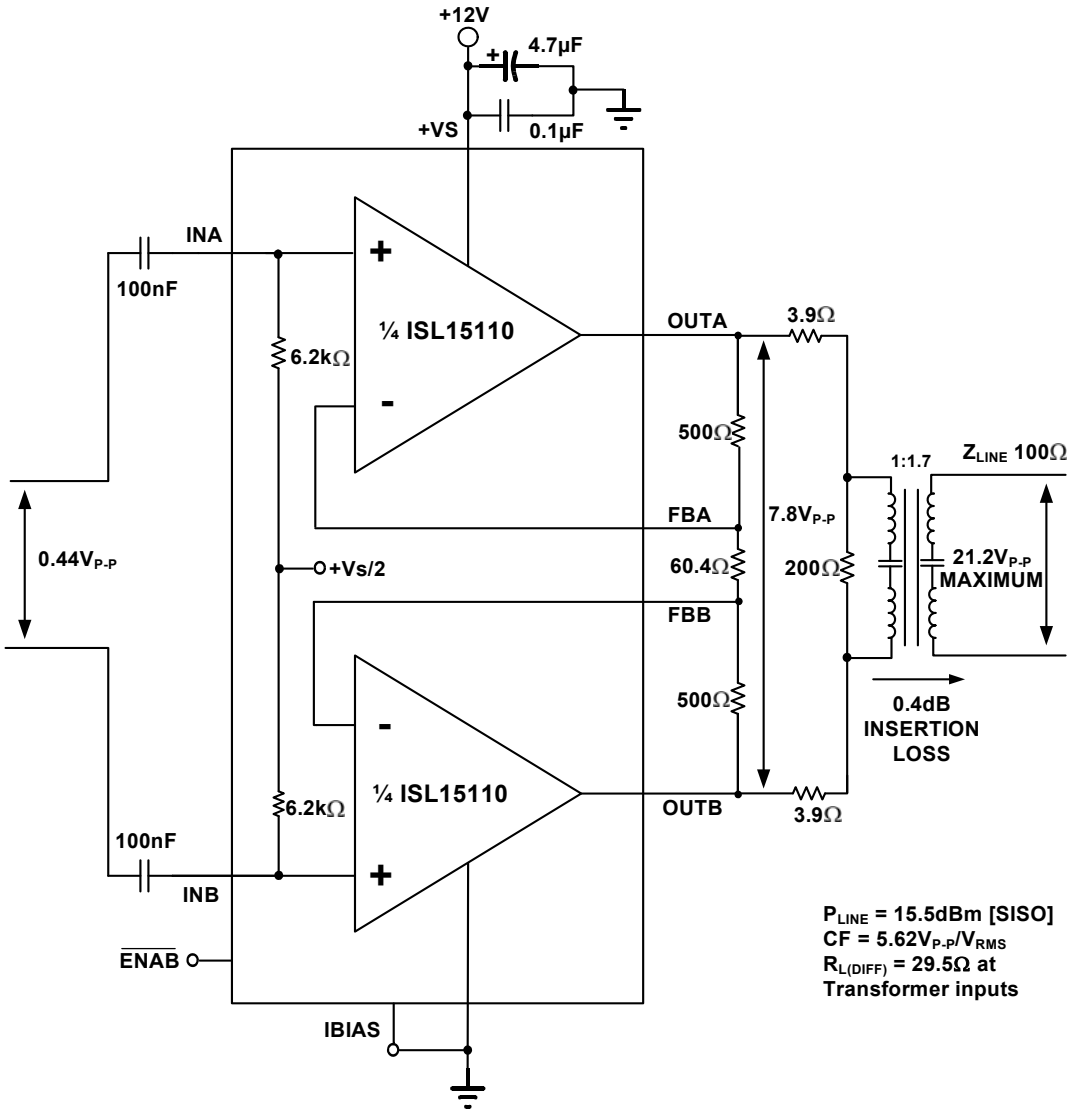
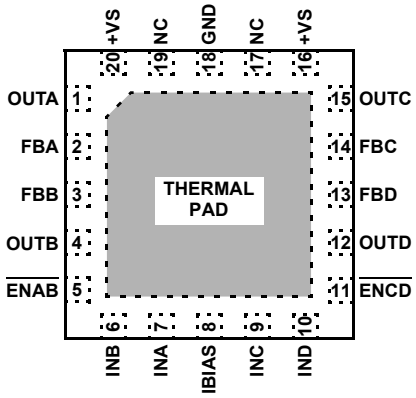


FIGURE 3. TYPICAL APPLICATION CIRCUIT (1 of 2 PORTS)

Pin Configuration

ISL15110
(20 LD QFN)
TOP VIEW



THERMAL PAD CONNECTS TO GND

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
0	THERMAL PAD	Connects to GND
1	OUTA	Amplifier A output
2	FBA	Amplifier A inverting input
3	FBB	Amplifier B inverting input
4	OUTB	Amplifier B output
5	$\overline{\text{ENAB}}$	Port 1 enable/disable control
6	INB	Amplifier B non-inverting input
7	INA	Amplifier A non-inverting input
8	IBIAS	Ports 1 and 2 quiescent current control
9	INC	Amplifier C non-inverting input
10	IND	Amplifier D non-inverting input
11	$\overline{\text{ENCD}}$	Port 2 enable/disable control
12	OUTD	Amplifier D output
13	FBD	Amplifier D inverting input
14	FBC	Amplifier C inverting input
15	OUTC	Amplifier C output
16, 20	+VS	Voltage supply
17, 19	NC	No connect
18	GND	Ground

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL15110IRZ	151 10IRZ	-40 to +85	-	20 Ld QFN	L20.4x4C
ISL15110IRZ-T7	151 10IRZ	-40 to +85	1k	20 Ld QFN	L20.4x4C
ISL15110IRZ-T13	151 10IRZ	-40 to +85	6k	20 Ld QFN	L20.4x4C

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL15110 product information page. For more information about MSL, refer to TB363.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to GND . . . . . -0.3V to +13.3V
Driver V_{IN}+ Voltage . . . . . .GND to V_S+
V_{CM} Voltage to GND . . . . . .GND to V_S+
Current Into Any input 8mA
Continuous Output Current for Long Term Reliability. 50mA
ESD Rating
Human Body Model (Tested per JESD22-A114F). 4kV
Machine Model (Tested per JESD22-A115C) 500V
Charge Device Model (Tested per JESD22-C101E). 1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5)	43	6.5
Thermal Characteristics (Typical)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
20 Ld QFN Package	4	18

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Power Dissipation . . . . . see page 14
Storage Temperature Range. . . . . .-40°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Ambient Temperature Range . . . . . .-40°C to +85°C
Junction Temperature Range . . . . . .-40°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_S = +12V, Gain = 17.6V/V, R_f = 500Ω, R_{L-DIFF} = 29.5Ω differential, I_{BIAS} = GND, T_A = +25°C. Ports are tested separately unless otherwise indicated (see Figure 3).

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
AC PERFORMANCE						
-3dB Bandwidth	BW	A_V = 12dB, [5V/V]		120		MHz
		A_V = 25dB, [17.6V/V]		80		MHz
Passband Ripple (f < 50MHz)	RIP			1		dB
Slew Rate	SR	Differential V_{OUT} from -6V to +6V		1600		V/µs
Multi-Tone Power Ratio (Power Cutback Added Back For Frequency > 30MHz)	MTPR	2MHz to 50MHz, 25kHz Tone Spacing, P_{LINE} = 15.5dBm, CF = 15dB, V_S = 10.8V, T_A = 0°C to +85°C	-43			dBc
Off State Multi-Tone Power Ratio (Power Cutback Added Back For Frequency > 30MHz)	MTPR OFF	2MHz to 50MHz, 25kHz Tone Spacing, P_{LINE} = 15.5dBm, CF = 15dB		-48		dBc
Non-Inverting Input Voltage Noise	eN	f = 1MHz		6		nV/√Hz
Non-Inverting Input Current Noise	iN+	f = 1MHz		13		pA/√Hz
Inverting Input Current Noise	iN-	f = 1MHz		50		pA/√Hz
POWER CONTROL FEATURES						
Logic High Current for $\overline{ENAB}$, $\overline{ENCD}$	IIHAB, IIHCD	$\overline{ENAB}$, $\overline{ENCD}$ = 3.3V	70	98	115	µA
Logic Low Current for $\overline{ENAB}$, $\overline{ENCD}$	IILAB, IILCD	$\overline{ENAB}$, $\overline{ENCD}$ = 0V	-5	-2	0	µA
Logic High Voltage for $\overline{ENAB}$, $\overline{ENCD}$	VIHAB, VIHCD	$\overline{ENAB}$ and $\overline{ENCD}$ Inputs [Port Disable]	1.7			V
Logic Low Voltage for $\overline{ENAB}$, $\overline{ENCD}$	VILAB, VILCD	$\overline{ENAB}$ and $\overline{ENCD}$ Inputs [Port Enable]			0.7	V
SUPPLY CHARACTERISTICS						
Supply Voltage Range	V_S	Single Supply	10.8	12	13.2	V
Supply Current - MIMO [Dual Port Operation]	I_S-MIMO	$\overline{ENAB}$, $\overline{ENCD}$ = 0V	44.5	50	56.5	mA
Supply Current - SISO [Single Port Operation]	I_S-SISO	$\overline{ENAB}$ = 3.3V and $\overline{ENCD}$ = 0V or $\overline{ENAB}$ = 0V and $\overline{ENCD}$ = 3.3V	26.5	30	33	mA

Electrical Specifications V_S = +12V, Gain = 17.6V/V, R_f = 500Ω, R_{L-DIFF} = 29.5Ω differential, I_{BIAS} = GND, T_A = +25°C. Ports are tested separately unless otherwise indicated (see Figure 3). **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Supply Current - Power Down [For Two Ports]	IS OFF	$\overline{ENAB}$, $\overline{ENCD}$ = 3.3V	7.4	8.0	9.5	mA
Maximum Power Consumption - MIMO [Dual Port Operation]	P-MIMO	$\overline{ENAB}$ = $\overline{ENCD}$ = 0V, P_L = 12.5dBm per channel		1040	1090	mW
		V_S = 13.2V		1145	1200	mW
Maximum Power Consumption - SISO [Single Port Operation]	P-SISO	$\overline{ENAB}$ = 0V, $\overline{ENCD}$ = 3.3V, P_{LA} = 15.5dBm or $\overline{ENAB}$ = 3.3V, $\overline{ENCD}$ = 0V, P_{LB} = 15.5dBm		590	720	mW
		V_S = 13.2V		650	790	mW
OUTPUT CHARACTERISTICS						
Loaded Output Swing (Single-ended)	V_{OUT} HI	R_L = 37.3Ω across output pins	10.7	10.8		V
	V_{OUT} LO	R_L = 37.3Ω across output pins		1.2	1.6	V
Output Offset Voltage Differential Mode	V_{OS-DM} Output	(OUTA - OUTB) or (OUTC - OUTD)	-100		100	mV
Output Offset Voltage Common Mode	V_{OS-CM} Output	Delta to $+V_S/2$	-75		125	mV
Output Short Circuit Current	I_{SC}	R_L = 0Ω		2000		mA
INPUT CHARACTERISTICS						
Input Offset Voltage Differential Mode	V_{OS-DM}	(INA - INB) or (INC - IND)	-6	0	+6	mV
Input Offset Voltage Common Mode	V_{OS-CM}	Delta to $+V_S/2$	-50	-18	0	mV
Non-Inverting Input Bias Current	+IB		-14	-3	+12	µA
Non-Inverting Input Bias Current Differential Mode	$+IB_{DM}$	$(+IB_A - +IB_B)$ or $(+IB_C - +IB_D)$	-2	0	+2	µA
Inverting Input Bias Current Differential Mode (Mismatch)	$-IB_{DM}$	$(-IB_A - -IB_B)$ or $(-IB_C - -IB_D)$	-50	±20	+50	µA
Common Mode Input Range at each of the 4 Non-Inverting Input Pins	CMIR	Delta to $+V_S/2$	-3	±3.5	+3	V
Common Mode Rejections for each Port V_{CM} = -3V to +3V	CMRR	V_{CM} to Differential Mode Output	48	60		dB
		V_{CM} to Common Mode Output	45	50		dB
Power Supply Rejection for each Port	PSRR	PSRR to Differential Mode Input $+V_S$ = +10.8V to +13.2V, GND = 0V, DC	73	90		dB
		PSRR to Common Mode Output Balanced shift in $±V_S$ [bipolar supply]	42	60		dB
Differential Input Impedance	$Z_{IN-DIFF}$		10	12.4	14	kΩ

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted.

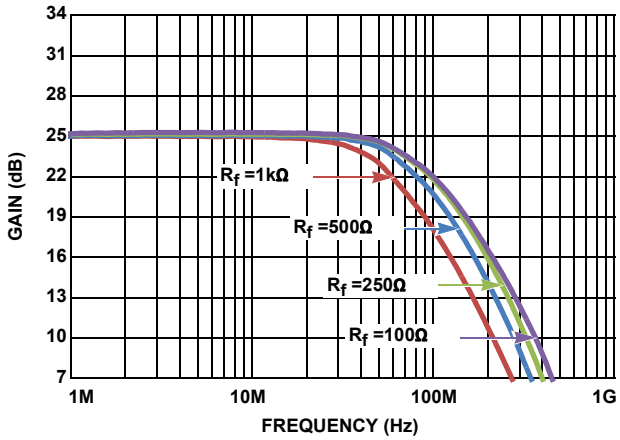


FIGURE 4. SMALL SIGNAL FREQUENCY RESPONSE vs R_f

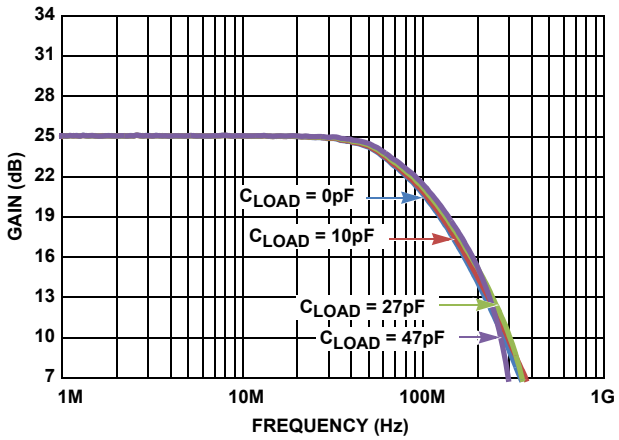


FIGURE 5. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD}

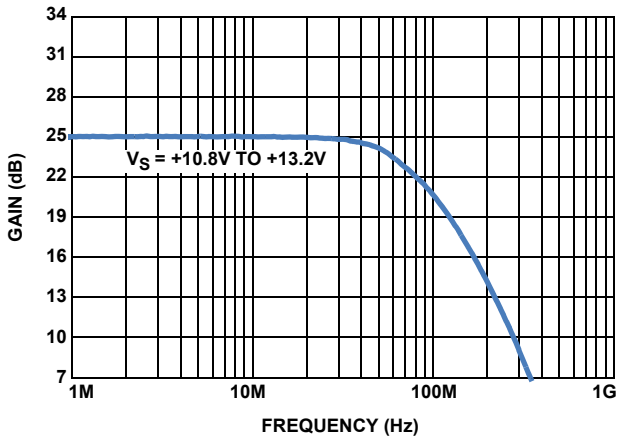


FIGURE 6. SMALL SIGNAL BW vs SUPPLY VOLTAGE

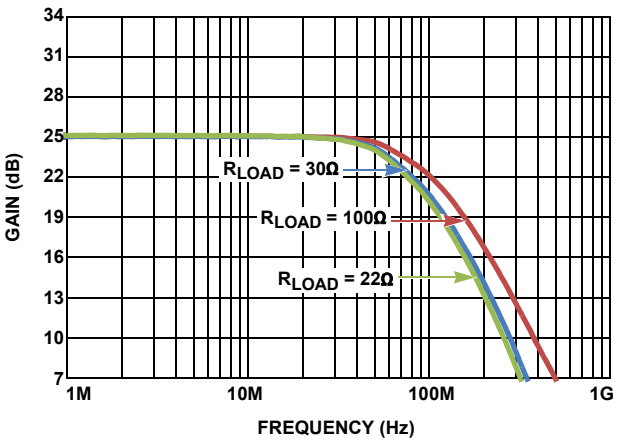


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE vs R_{LOAD}

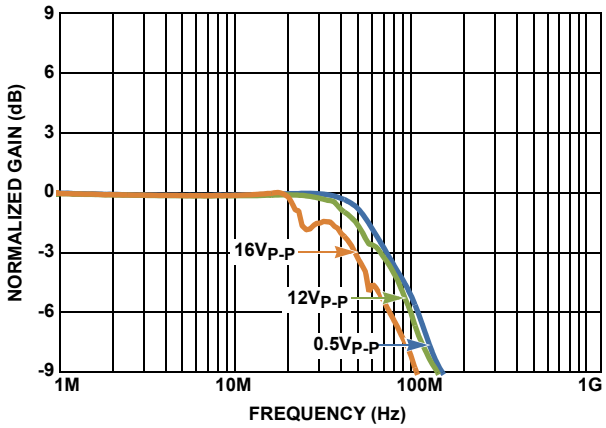


FIGURE 8. LARGE SIGNAL FREQUENCY RESPONSE

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted. **(Continued)**

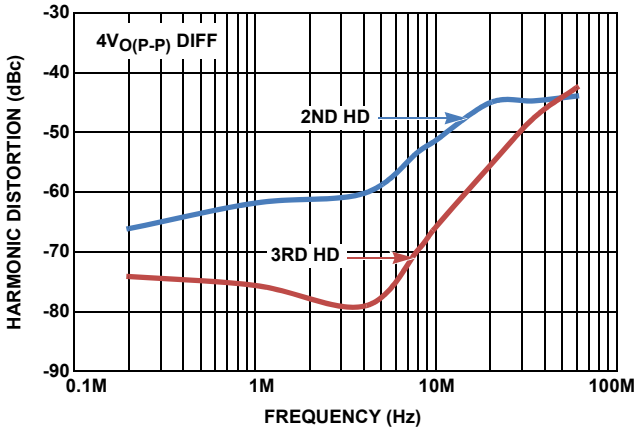


FIGURE 9. HARMONIC DISTORTION vs FREQUENCY

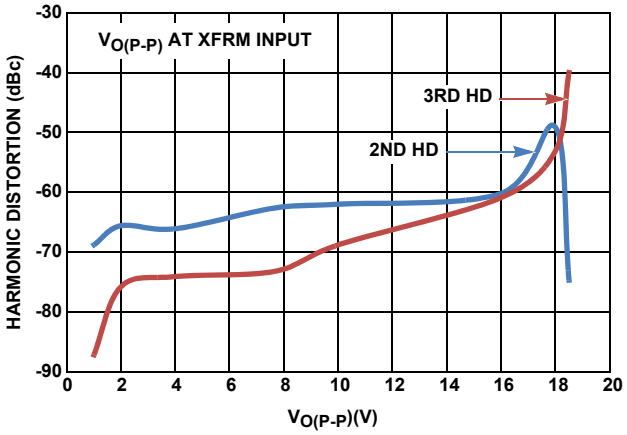


FIGURE 10. 200kHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

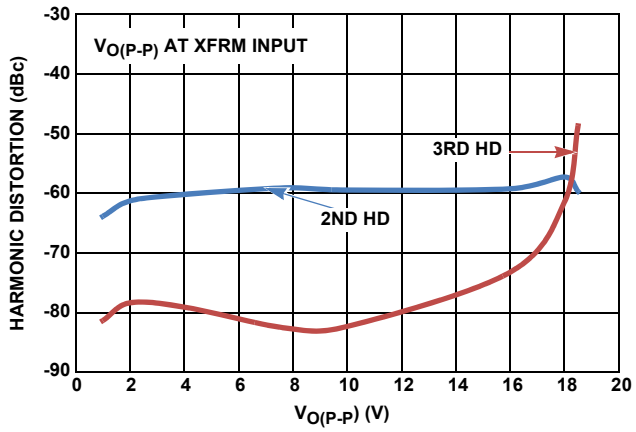


FIGURE 11. 4MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

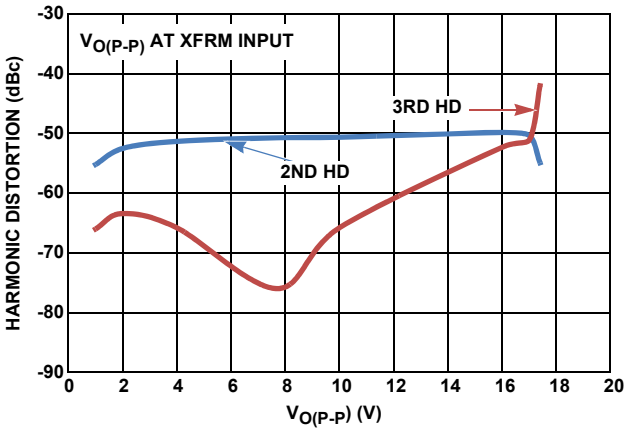


FIGURE 12. 10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

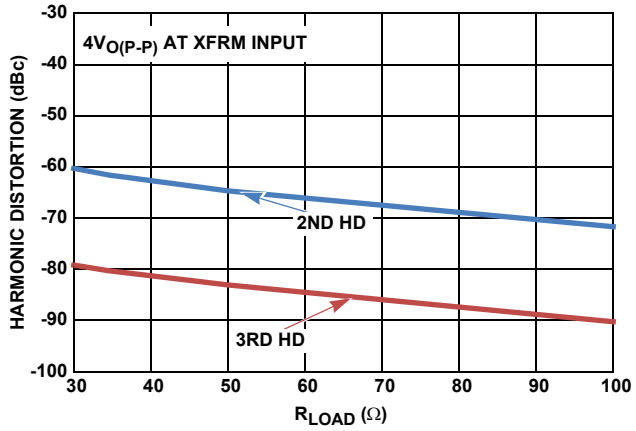


FIGURE 13. 4MHz HARMONIC DISTORTION vs R_{LOAD}

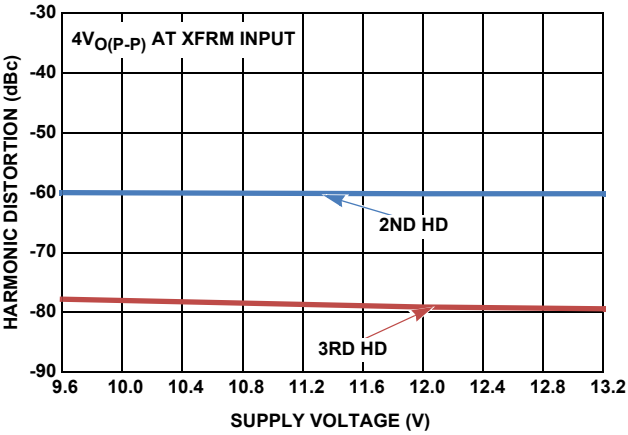


FIGURE 14. 4MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted. **(Continued)**

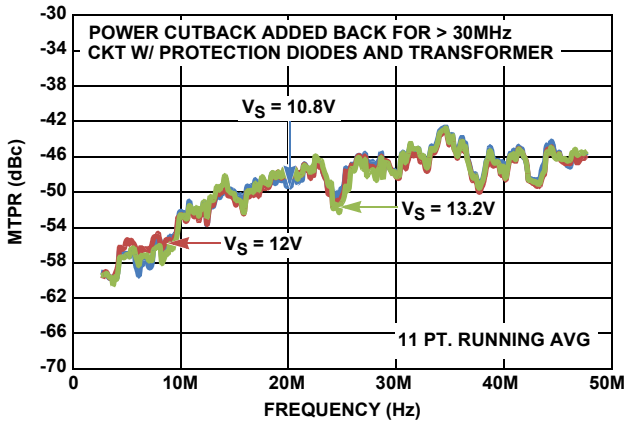


FIGURE 15. MTPR IN MIMO MODE WITH VARIOUS V_S (2MHz TO 50MHz)

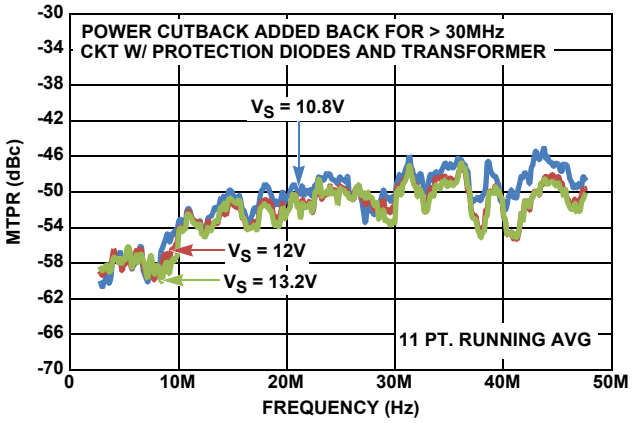


FIGURE 16. MTPR IN SISO MODE WITH VARIOUS V_S (2MHz TO 50MHz)

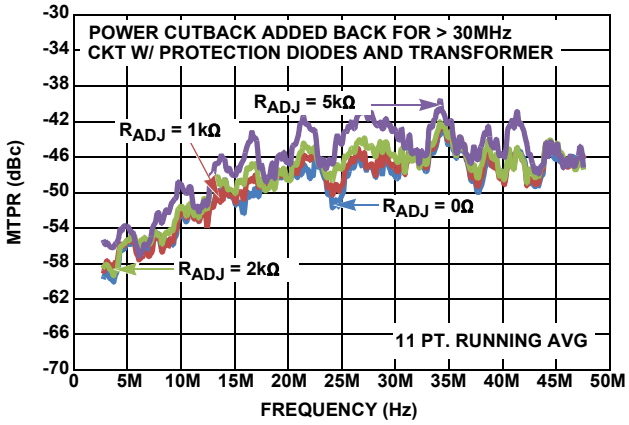


FIGURE 17. MTPR IN MIMO MODE WITH VARIOUS R_{ADJ} (2MHz TO 50MHz)

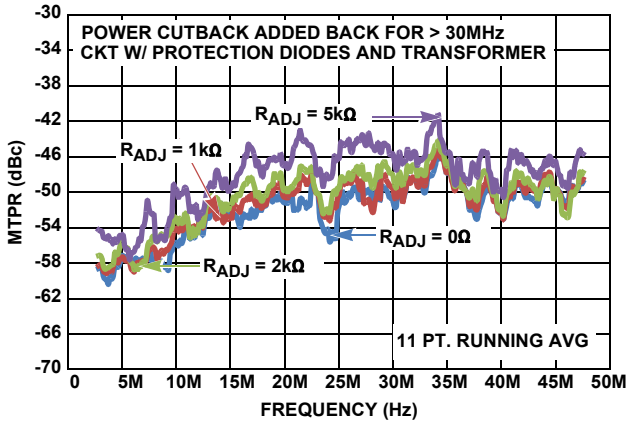


FIGURE 18. MTPR IN SISO MODE WITH VARIOUS R_{ADJ} (2MHz TO 50MHz)

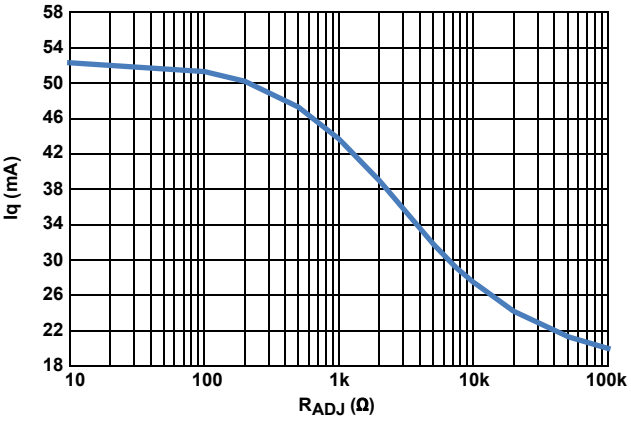


FIGURE 19. QUIESCENT CURRENT FOR I_{BIAS} (2 PORTS)

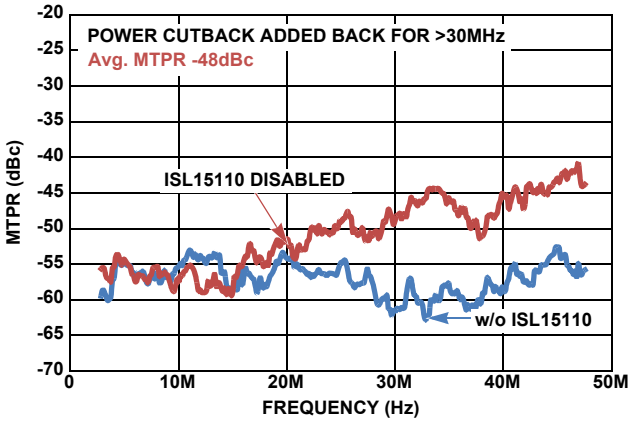


FIGURE 20. DISABLE MTPR LINEARITY AT OUTPUTS

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted. **(Continued)**

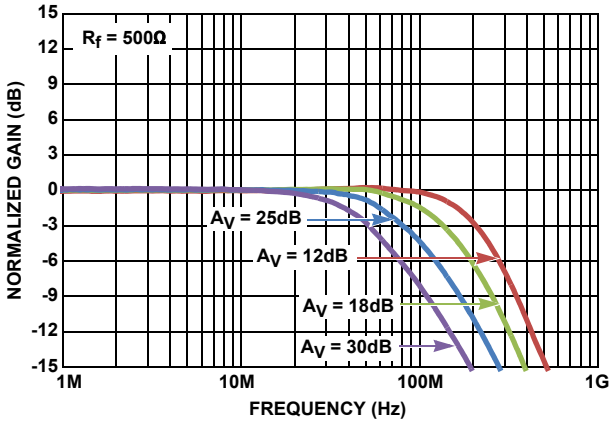


FIGURE 21. SMALL SIGNAL FREQUENCY RESPONSE vs GAINS

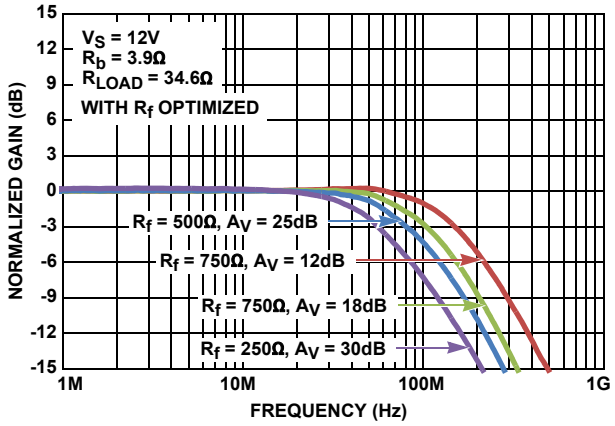


FIGURE 22. SMALL SIGNAL FREQUENCY RESPONSE vs GAINS

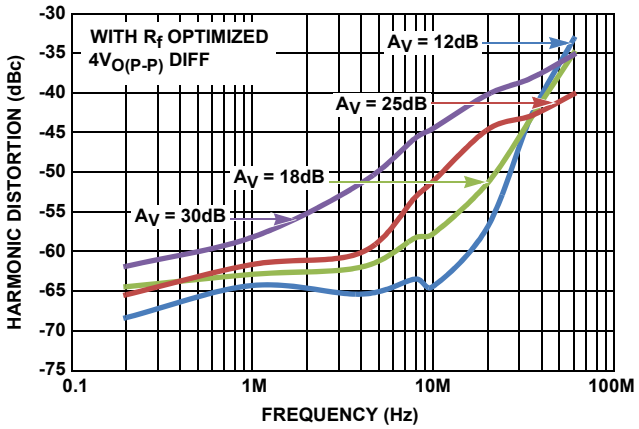


FIGURE 23. TOTAL HARMONIC DISTORTION vs FREQUENCY FOR VARIOUS GAINS

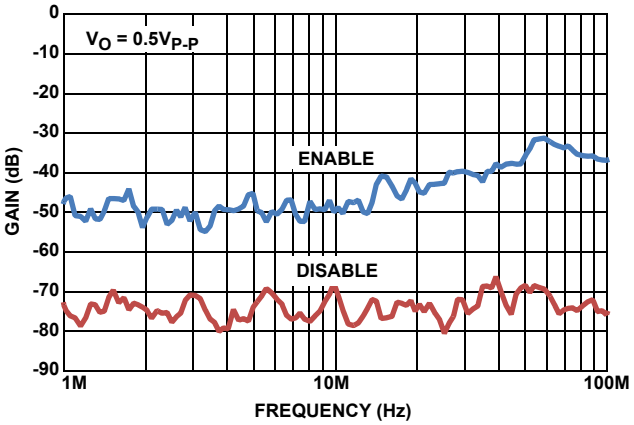


FIGURE 24. COMMON MODE INPUT TO DIFFERENTIAL OUTPUT FREQUENCY RESPONSE

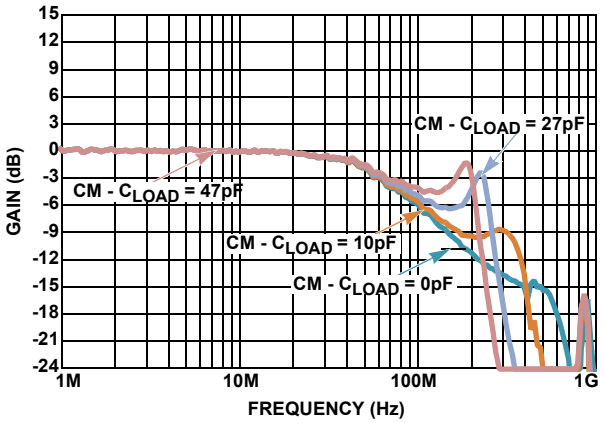


FIGURE 25. COMMON MODE SMALL SIGNAL FREQUENCY RESPONSE WITH VARIOUS C_{LOADS}

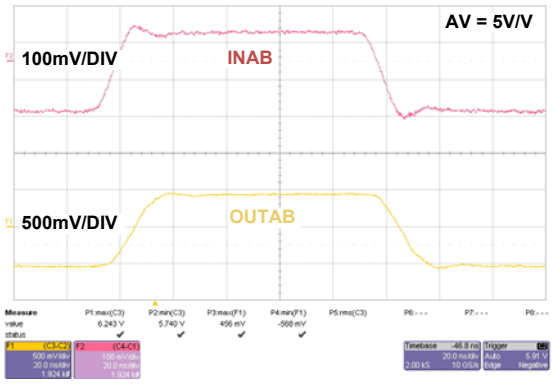


FIGURE 26. SMALL STEP RESPONSE

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted. **(Continued)**

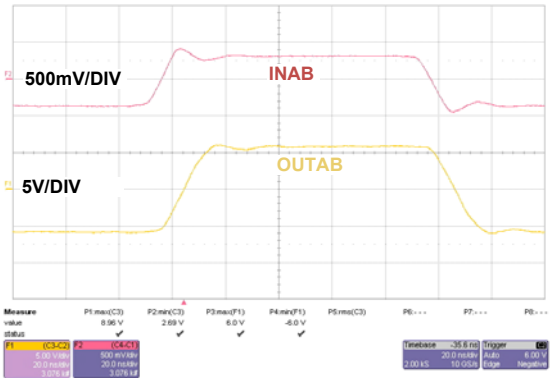


FIGURE 27. LARGE STEP RESPONSE

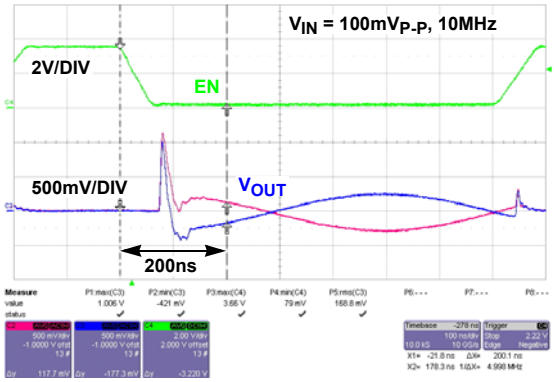


FIGURE 28. POWER ON TIME (t_{ON})

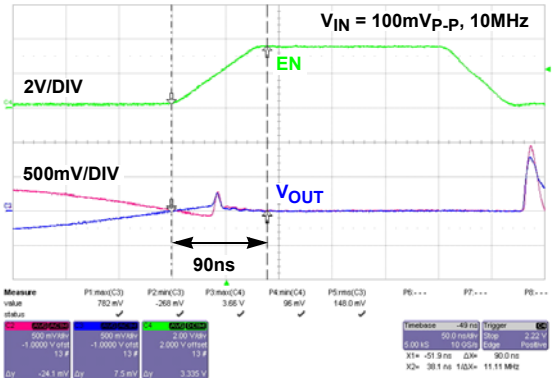


FIGURE 29. POWER OFF TIME (t_{OFF})

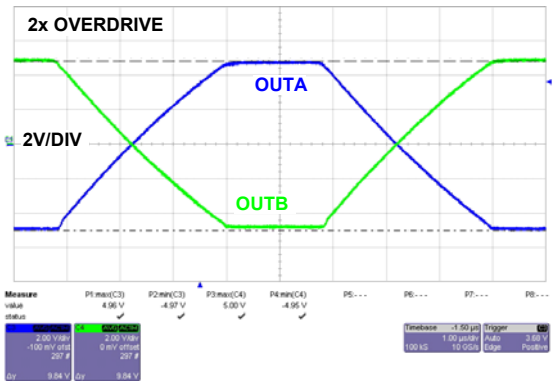


FIGURE 30. OVERDRIVE RECOVERY

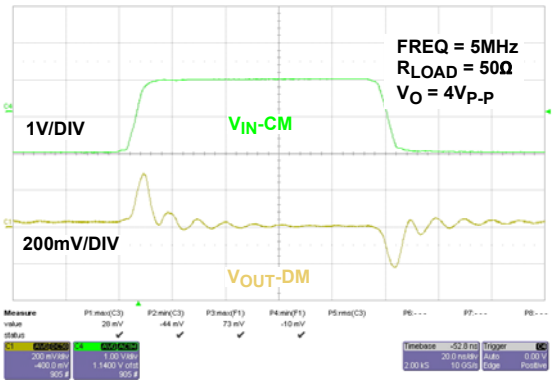


FIGURE 31. COMMON MODE INPUT TO DIFFERENTIAL OUTPUT STEP RESPONSE

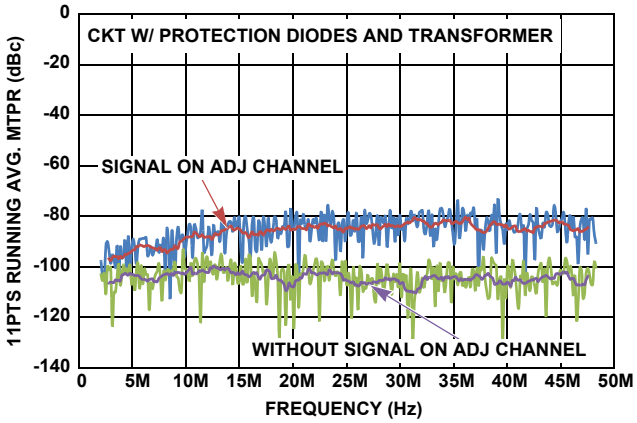


FIGURE 32. CROSSTALK IN SISO

Typical Performance Curves

V_{CC} = +12V, Gain = 17.6V/V (Differential), R_f = 500Ω, R_{LOAD} = 29.5Ω, T_A = +25°C, I_{BIAS} = 0Ω to GND (Full Power). Each Port (see Figure 3), unless otherwise noted. **(Continued)**

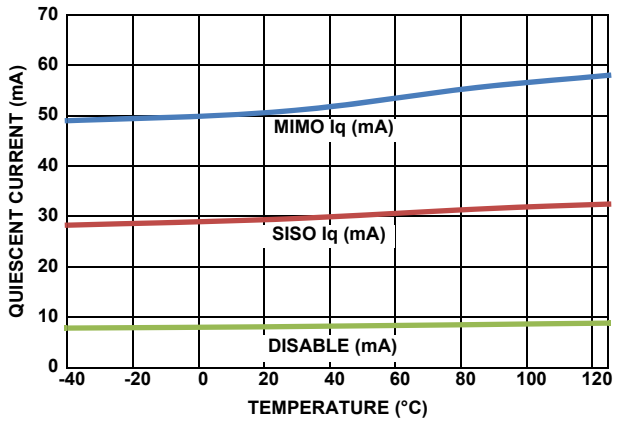


FIGURE 33. QUIESCENT CURRENT vs TEMPERATURE

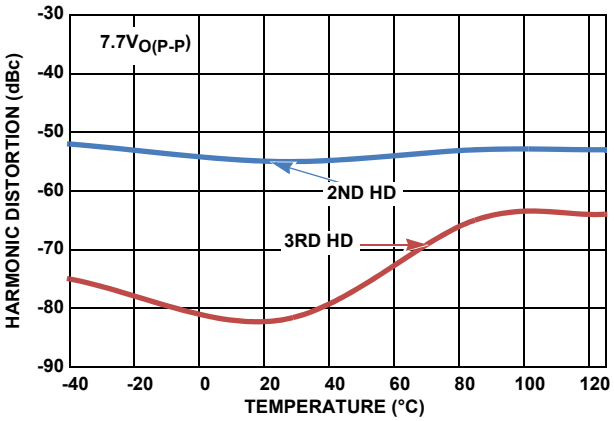


FIGURE 34. 4MHz HARMONIC DISTORTION vs TEMPERATURE

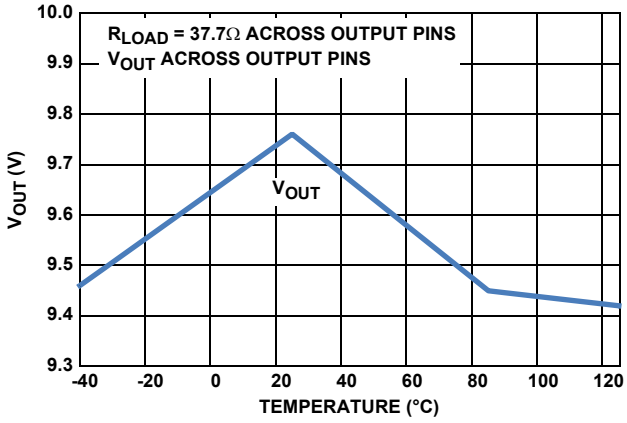


FIGURE 35. OUTPUT SWING vs TEMPERATURE

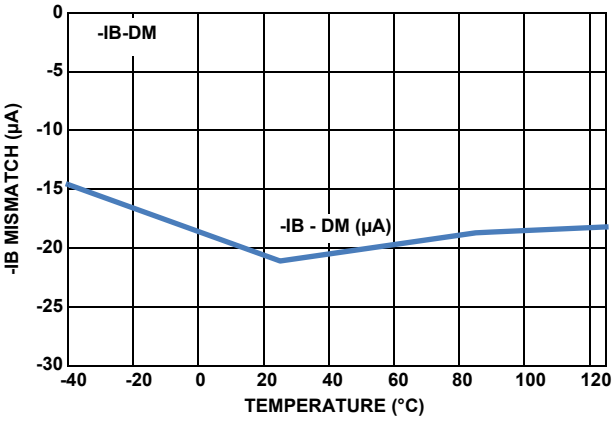


FIGURE 36. INVERTING INPUT BIAS CURRENT (MISMATCH) vs TEMPERATURE

Operation

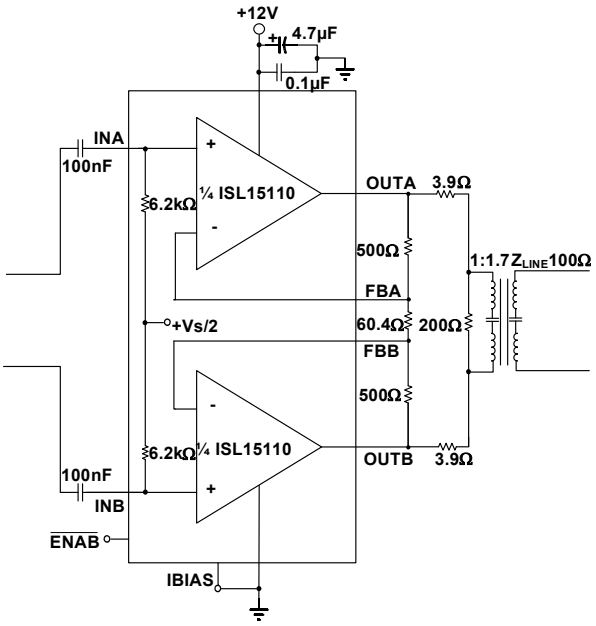


FIGURE 37. APPLICATION CIRCUIT (1 of 2 PORTS)

The ISL15110 consists of two pairs of Current Feedback Amplifiers (CFA): those used in power line communication and those used in (PLC) MIMO applications. The ISL15110 is well suited to the requirements of high output power, high full power bandwidth, and high output impedance in disable mode.

The AC characteristics are set by the 500Ω feedback resistors, as shown in Figure 37. The effects of increasing or decreasing the feedback resistors is shown in Figure 4. The ISL15110 shows a good flat response with smooth roll off with various feedback resistances. CFAs will generally roll off sooner with the increase in feedback resistance, and decreasing the feedback will peak the frequency response up and extend the bandwidth.

With the bandwidth fixed requirement by the feedback resistors, the gain can be adjusted by changing the 60.4Ω in Figure 37. The Figure 37 example sets the differential gain across OUTA, OUTB to:

$$\frac{OUTA}{INA} = \frac{500}{(60.4/2)} + 1 = 17.6\left(\frac{V}{V}\right) \quad \text{(EQ. 1)}$$

To get the gain to the input of the transformer in Figure 37, the attenuation of the resistor divider [3.9Ω and (200Ω||34.6Ω)] is added to Equation 1, in which the 34.6Ω is the input referred load of 100Ω through the turns ratio squared.

Input Biasing and Input Impedance

The ISL15110 has integrated resistors at the inputs for mid rail biasing, as shown in Figures 1 and 3. The inputs require only external AC coupling capacitors. With a 100nF coupling capacitor and an input impedance of 6.2kΩ typical, the first order high pass cut off frequency is 257Hz.

Power Control Function

Each pair of drivers can be enabled and disabled by pulling low and high, respectively, on the EN pin. Putting 1.7V and greater on the EN pin will disable the differential driver, while putting 0.8V and less on the EN pin will enable the driver.

The ISL15110 includes an external IBIAS pin for biasing the quiescent current. Grounding the pin in single supply designs gives the nominal quiescent current shown in the “Electrical Specifications” table starting on page 5, while inserting a resistor from pin to ground will scale down the quiescent current for both drivers, as shown in Figure 19 on page 9.

Multi Tone Power Ratio (MTPR)

G.hn PLC uses OFDM modulation to digitally encode data for communication. A carrier spacing of 24.41kHz is used in power lines, and 48.82kHz is used in phone lines.

In multi-tone signaling, linearity is shown in the MTPR measurement. MTPR measures the difference in power of a carrier tone vs a missing tone.

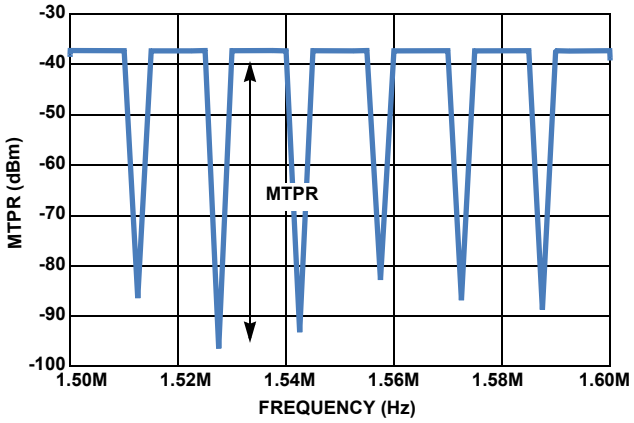


FIGURE 38. 2MHz TO 50MHz PLC SIGNAL WITH 25kHz SPACING

Figure 38 shows the ISL15110MTPR in SISO mode. The curve shows an MTPR average of five symbols with an additional 11pt running average of that average. A -45dBc worst case MTPR is measured with a -50dBc, which is the typical number across the 2MHz to 50MHz transmit band.

Disable Linearity

Unlike DSL, communication in a PLC system is half duplex, meaning one device can transmit at a time. When the line driver is not transmitting, the line driver is disabled with the receiver ready to receive. Figure 39 on page 14 shows the shared transmit and receive signal path of two ends. RBMs are resistors to limit fault currents and provide a driving impedance to the transformer, thus setting its frequency span. Their values are typically low (<10Ω). When Txa is transmitting, optimal MTPR can be received by Rxb if Txb is removed. Because Txb is present, the ideal output of the line driver is to behave at high impedance when disabled. Figure 20 on page 9 shows the linearity at the outputs with the ISL15110 disabled. An average MTPR of -48dBc is achieved.

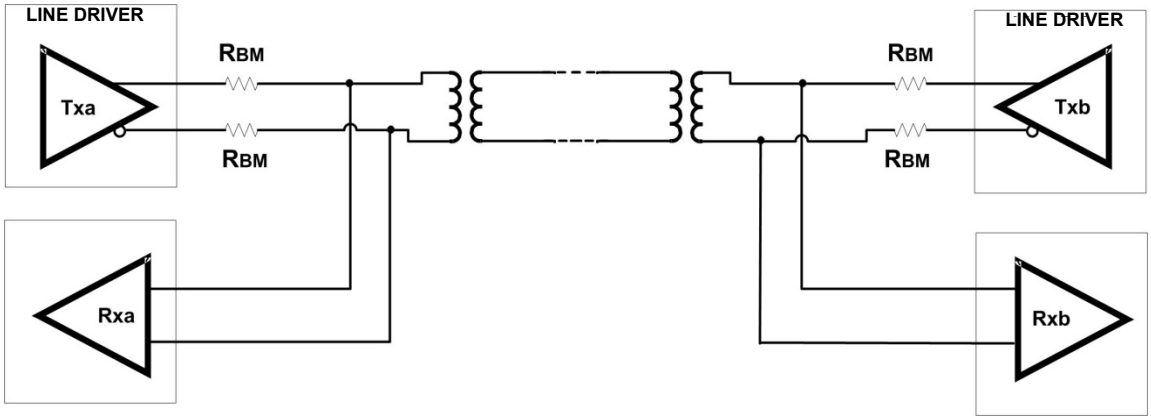


FIGURE 39. Tx and Rx SIGNAL PATH. CASE1: [Txa: ON, Rxa: OFF, Txb: OFF, Rxb: ON]. CASE2: [Txa: OFF, Rxa: ON, Txb: ON, Rxb: OFF]

Board Design Recommendation

To minimize parasitic capacitance in the ISL15110 design, lay out short output traces and select low capacitance protection devices and line transformers with low interwinding capacitance in the signal path.

The supply decoupling capacitors are also placed close to the supply pins to minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors, so close placement of the 0.1µF capacitors on the supply pin will improve dynamic performance. The higher 4.7µF value capacitors can be placed farther from the supply pins because they provide low frequency decoupling.

The thermal pad for the ISL15110 should be connected to ground in single supply applications. For good thermal control, run vias to a bottom pad to help dissipate heat away from the package. The ISL15110 evaluation board uses nine 20mil diameter vias with 10mil holes.

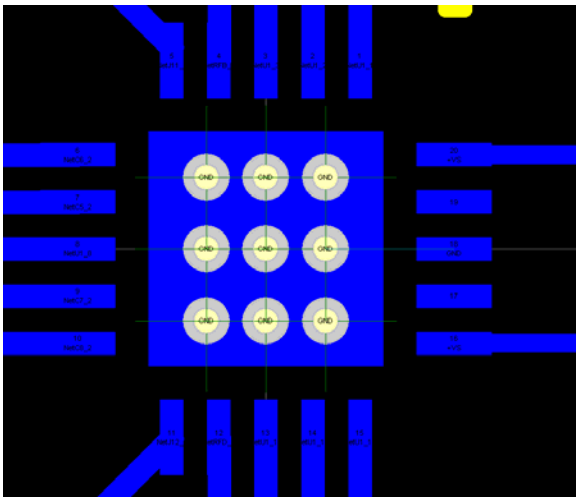


FIGURE 40. ISL15110 EVALUATION BOARD

Thermal Resistance and Power Dissipation

Thermal resistance for junction to ambient, T_{JA}, is +43°C/W. The maximum power dissipation for MIMO at the 13.2V supply is 1200mW. The ambient temperature allowed given the maximum junction temperature of +150°C is:

$$T_A = T_J - \theta_{JA} \times Pd \quad \text{(EQ. 2)}$$
$$T_A = +150°C - 43°(C/W) * 1.2 = +98.4°C$$

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Apr 6, 2018	FN8282.1	Added Related Literature section to page 1. Updated Ordering information table by adding tape and reel quantity column. Updated Note 3. Removed About Intersil section and added Renesas disclaimer.
Jan 31, 2013	FN8282.0	Initial release

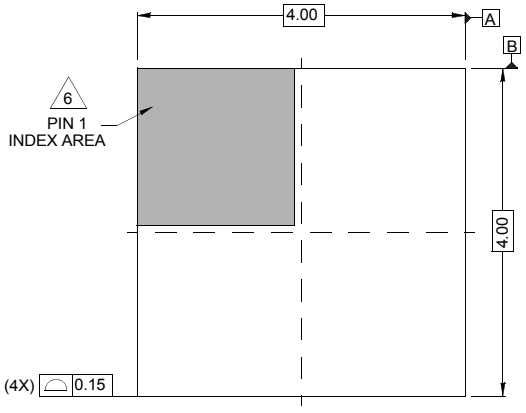
Package Outline Drawing

For the most recent package outline drawing, see L20.4x4C.

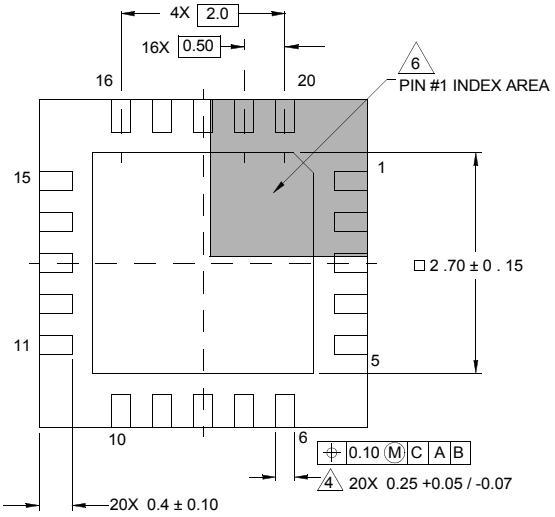
L20.4x4C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

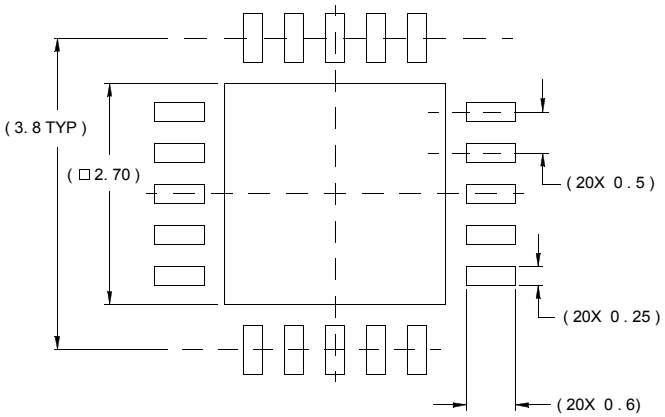
Rev 0, 11/06



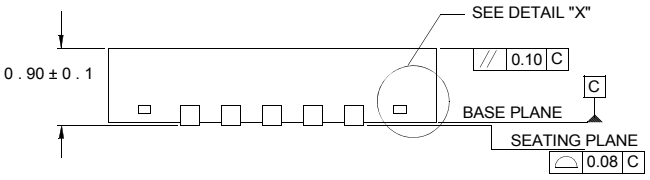
TOP VIEW



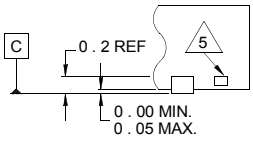
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.