

ISL2100A, ISL2101A

100V, 2A Peak, High Frequency Half-Bridge Drivers

FN6294  
Rev 4.1  
Jul 22, 2021

The ISL2100A, ISL2101A are 100V, high frequency, half-bridge N-channel power MOSFET driver ICs. They are based on the popular HIP2100, HIP2101 half-bridge drivers, but offer several performance improvements. The ISL2100A has additional input hysteresis for superior operation in noisy environments and the inputs of the ISL2101A, like those of the ISL2100A, can now safely swing to the  $V_{DD}$  supply rail. Finally, both parts are available in a very compact 9 Ld DFN package to minimize the required PCB footprint

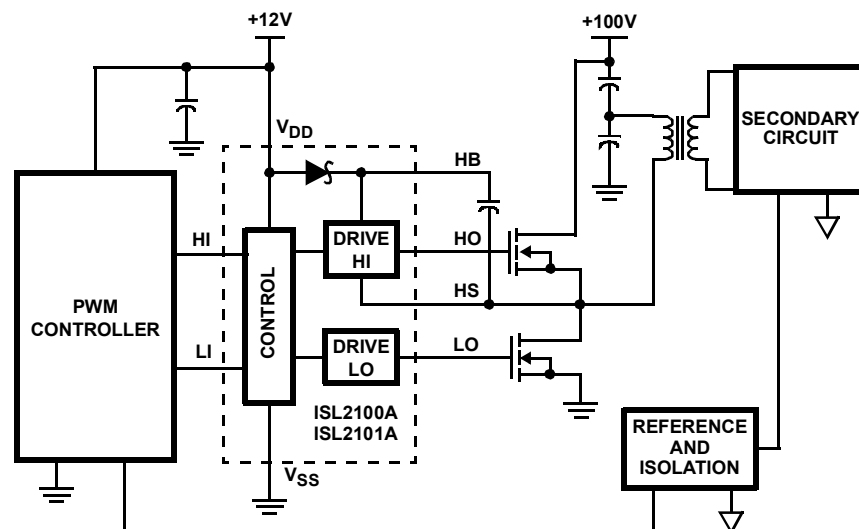
**Applications**

- Telecom Half-Bridge Converters
- Telecom Full-Bridge Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- Class-D Audio Amplifiers

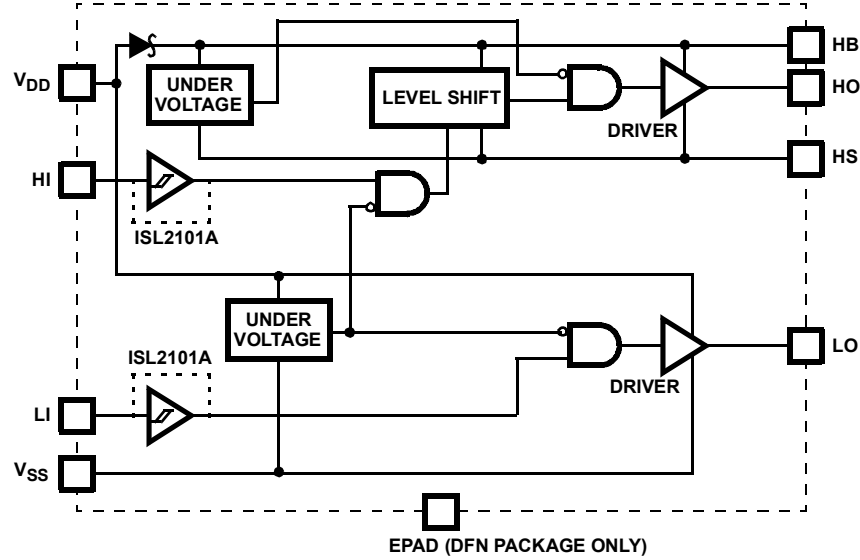
**Features**

- Drives N-Channel MOSFET Half-Bridge
- Space-Saving DFN Package
- DFN Package Compliant with 100V Conductor Spacing Guidelines per IPC-2221
- Pb-Free (RoHS compliant)
- Bootstrap Supply Max Voltage to  $114V_{DC}$
- On-Chip  $1\Omega$  Bootstrap Diode
- Fast Propagation Times for Multi-MHz Circuits
- Drives 1nF Load with Typical Rise/Fall Times of 10ns
- CMOS Compatible Input Thresholds (ISL2100A)
- 3.3V/TTL Compatible Input Thresholds (ISL2101A)
- Independent Inputs Provide Flexibility
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Voltage Range (9V to 14V)
- Supply Undervoltage Protection
- $2.5\Omega$  Typical Output Pull-Up/Pull-Down Resistance

**Application Block Diagram**



**Functional Block Diagram**



\*EPAD = EXPOSED PAD. THE EPAD IS ELECTRICALLY ISOLATED FROM ALL OTHER PINS. FOR BEST THERMAL PERFORMANCE CONNECT THE EPAD TO THE PCB POWER GROUND PLANE.

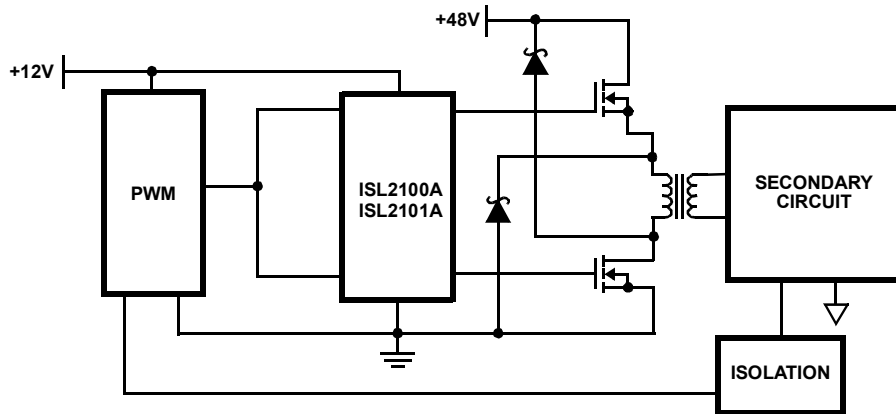


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

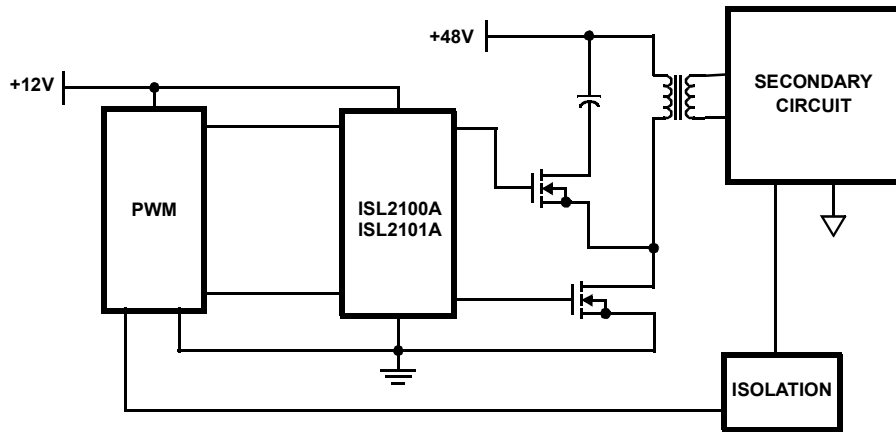


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE-CLAMP

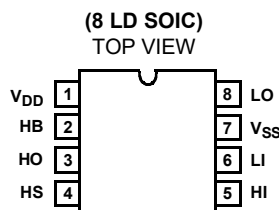
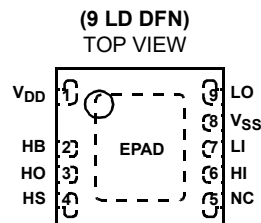
## Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL2100AAR3Z	00AZ	9 Ld 3x3 DFN	L9.3x3	Tube	-40 to +125°C
ISL2100AAR3Z-T				Reel, 6k	
ISL2101AAR3Z	01AZ			Tube	
ISL2101AAR3Z-T				Reel, 6k	
ISL2101AABZ	01ABZ	8 Ld SOIC	M8.15	Tube	
ISL2101AABZ-T				Reel, 2.5k	

### NOTES:

- See [TB347](#) for details on reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL2100A](#) and [ISL2101A](#) device pages. For more information about MSL, see [TB363](#).

## Pinouts



NOTE: EPAD = Exposed PAD.

## Pin Descriptions

SYMBOL	DESCRIPTION
V <sub>DD</sub>	Positive supply to lower gate driver. Bypass this pin to V <sub>SS</sub> .
HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-side output. Connect to gate of high-side power MOSFET.
HS	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-side input.
LI	Low-side input.
V <sub>SS</sub>	Chip negative supply, which will generally be ground.
LO	Low-side output. Connect to gate of low-side power MOSFET.
EPAD	Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

**Absolute Maximum Ratings**

Supply Voltage, $V_{DD}$ , $V_{HB} - V_{HS}$ (Notes 4, 5)	-0.3V to 18V
LI and HI Voltages (Note 5)	-0.3V to $V_{DD} + 0.3V$
Voltage on LO (Note 5)	-0.3V to $V_{DD} + 0.3V$
Voltage on HO (Note 5)	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
Voltage on HS (Continuous) (Note 5)	-1V to 110V
Voltage on HB (Note 5)	118V
Average Current in $V_{DD}$ to HB Diode	100mA

**Maximum Recommended Operating Conditions**

Supply Voltage, $V_{DD}$	9V to 14V
Voltage on HS	-1V to 100V
Voltage on HS (Repetitive Transient)	-5V to 105V
Voltage on HB	$V_{HS} + 8V$ to $V_{HS} + 14V$ and $V_{DD} - 1V$ to $V_{DD} + 100V$
HS Slew Rate	<50V/ns

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## NOTES:

- The ISL2100A-ISL2101A are capable of derated operation at supply voltages exceeding 14V. Figure 22 shows the high-side voltage derating curve for this mode of operation.
- All voltages referenced to  $V_{SS}$  unless otherwise specified.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
- For  $\theta_{JC}$ , the case temperature is measured at the center of the exposed metal pad on the package underside. See TB379 for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board.
- For  $\theta_{JC}$ , the case temperature is measured at the center top of the package. See TB379 for details.

**Electrical Specifications**  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
<b>SUPPLY CURRENTS</b>								
$V_{DD}$ Quiescent Current	$I_{DD}$	ISL2100A; LI = HI = 0V	-	0.1	0.25	-	0.3	mA
$V_{DD}$ Quiescent Current	$I_{DD}$	ISL2101A; LI = HI = 0V	-	0.3	0.45	-	0.55	mA
$V_{DD}$ Operating Current	$I_{DDO}$	ISL2100A; f = 500kHz	-	1.6	2.2	-	2.7	mA
$V_{DD}$ Operating Current	$I_{DDO}$	ISL2101A; f = 500kHz	-	1.9	2.5	-	3	mA
Total HB Quiescent Current	$I_{HB}$	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	$I_{HBO}$	f = 500kHz	-	2.0	2.5	-	3	mA
HB to $V_{SS}$ Current, Quiescent	$I_{HBS}$	LI = HI = 0V; $V_{HB} = V_{HS} = 114V$	-	0.05	1	-	10	$\mu\text{A}$
HB to $V_{SS}$ Current, Operating	$I_{HBSO}$	f = 500kHz; $V_{HB} = V_{HS} = 114V$	-	0.9	-	-	-	mA
<b>INPUT PINS</b>								
Low Level Input Voltage Threshold	$V_{IL}$	ISL2100A	3.7	4.4	-	2.7	-	V
Low Level Input Voltage Threshold	$V_{IL}$	ISL2101A	1.4	1.8	-	1.2	-	V
High Level Input Voltage Threshold	$V_{IH}$	ISL2100A	-	6.6	7.4	-	8.4	V
High Level Input Voltage Threshold	$V_{IH}$	ISL2101A	-	1.8	2.2	-	2.4	V
Input Voltage Hysteresis	$V_{IHYS}$	ISL2100A	-	2.2	-	-	-	V
Input Pull-down Resistance	$R_I$		-	210	-	100	500	k $\Omega$
<b>UNDERVOLTAGE PROTECTION</b>								
$V_{DD}$ Rising Threshold	$V_{DDR}$		6.8	7.3	7.8	6.5	8.1	V

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
DFN (Notes 6, 7)	47	3.5
SOIC (Notes 8, 9)	107	50
Max Power Dissipation at +25°C in Free Air (DFN, Note 6)	2.27W	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see TB493	

**Electrical Specifications**  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
$V_{DD}$ Threshold Hysteresis	$V_{DDH}$		-	0.6	-	-	-	V
HB Rising Threshold	$V_{HBR}$		6.2	6.9	7.5	5.9	7.8	V
HB Threshold Hysteresis	$V_{HBH}$		-	0.6	-	-	-	V
<b>BOOTSTRAP DIODE</b>								
Low Current Forward Voltage	$V_{DL}$	$I_{VDD-HB} = 100\mu\text{A}$	-	0.5	0.6	-	0.7	V
High Current Forward Voltage	$V_{DH}$	$I_{VDD-HB} = 100\text{mA}$	-	0.7	0.9	-	1	V
Dynamic Resistance	$R_D$	$I_{VDD-HB} = 100\text{mA}$	-	0.8	1	-	1.5	$\Omega$
<b>LO GATE DRIVER</b>								
Low Level Output Voltage	$V_{OLL}$	$I_{LO} = 100\text{mA}$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	$V_{OHL}$	$I_{LO} = -100\text{mA}$ , $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.3	-	0.4	V
Peak Pull-Up Current	$I_{OHL}$	$V_{LO} = 0V$	-	2	-	-	-	A
Peak Pull-Down Current	$I_{OLL}$	$V_{LO} = 12V$	-	2	-	-	-	A
<b>HO GATE DRIVER</b>								
Low Level Output Voltage	$V_{OLH}$	$I_{HO} = 100\text{mA}$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	$V_{OHH}$	$I_{HO} = -100\text{mA}$ , $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Pull-Up Current	$I_{OHH}$	$V_{HO} = 0V$	-	2	-	-	-	A
Peak Pull-Down Current	$I_{OLH}$	$V_{HO} = 12V$	-	2	-	-	-	A

**Electrical Specifications** Switching Specifications  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	$t_{LPHL}$		-	34	50	-	60	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	$t_{HPHL}$		-	31	50	-	60	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	$t_{LPLH}$		-	39	50	-	60	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	$t_{HPLH}$		-	39	50	-	60	ns
Delay Matching: Upper Turn-Off to Lower Turn-On	$t_{MON}$		1	8	-	-	16	ns
Delay Matching: Lower Turn-Off to Upper Turn-On	$t_{MOFF}$		1	6	-	-	16	ns
Either Output Rise/Fall Time (10% to 90%/90% to 10%)	$t_{RC}, t_{FC}$	$C_L = 1\text{nF}$	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V/9V to 3V)	$t_R, t_F$	$C_L = 0.1\mu\text{F}$	-	0.5	0.6	-	0.8	us
Minimum Input Pulse Width that Changes the Output	$t_{PW}$		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	$t_{BS}$		-	10	-	-	-	ns

**Timing Diagrams**

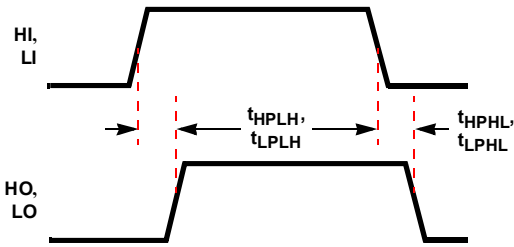


FIGURE 3. PROPAGATION DELAYS

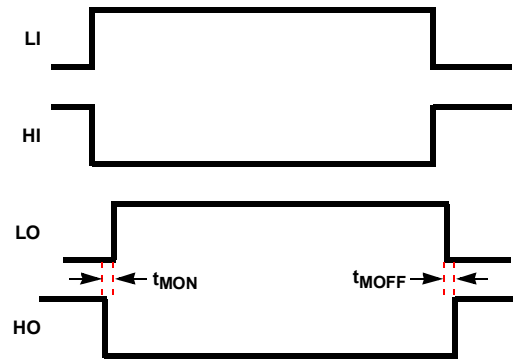


FIGURE 4. DELAY MATCHING

**Typical Performance Curves**

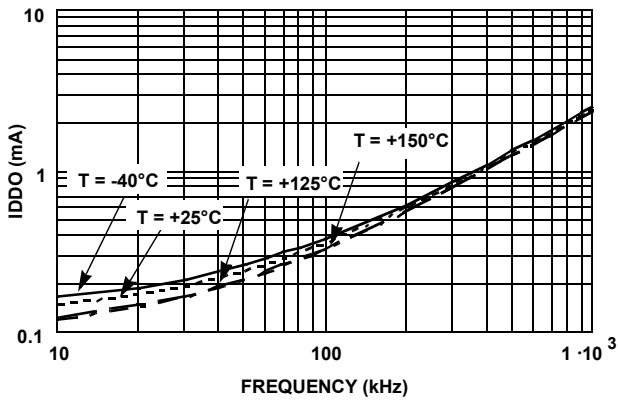


FIGURE 5. ISL2100A  $I_{DD0}$  OPERATING CURRENT vs FREQUENCY

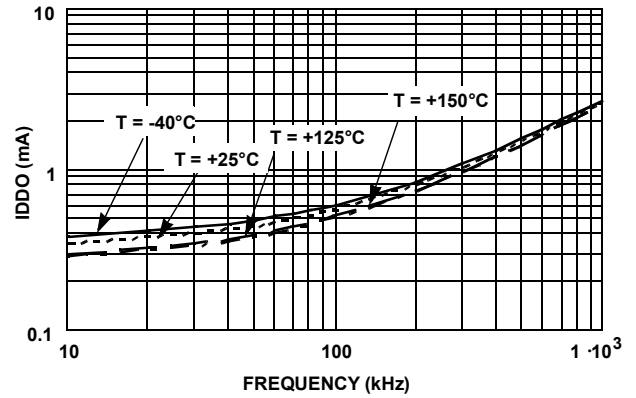


FIGURE 6. ISL2101A  $I_{DD0}$  OPERATING CURRENT vs FREQUENCY

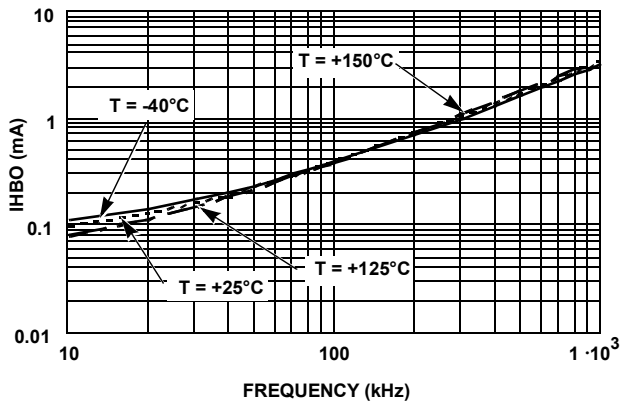


FIGURE 7.  $I_{HBO}$  OPERATING CURRENT vs FREQUENCY

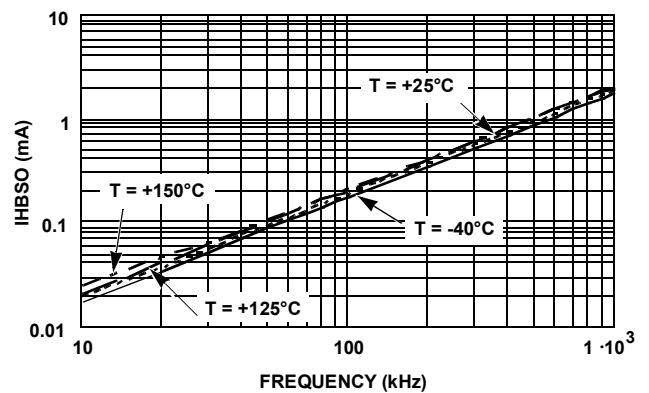


FIGURE 8.  $I_{HBSO}$  OPERATING CURRENT vs FREQUENCY

**Typical Performance Curves** (Continued)

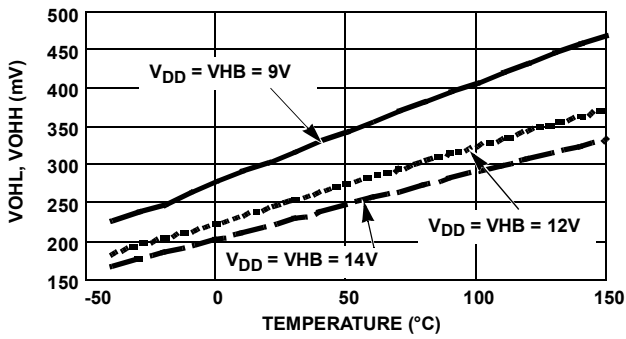


FIGURE 9. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

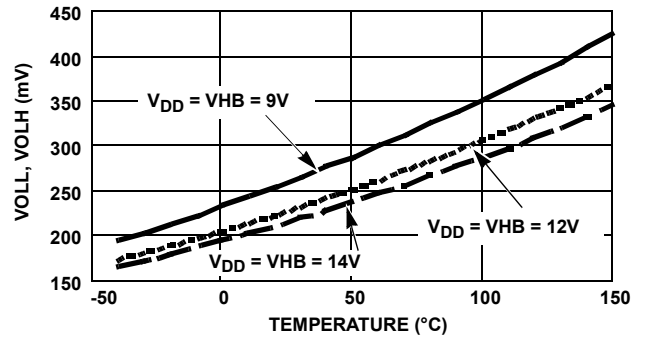


FIGURE 10. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

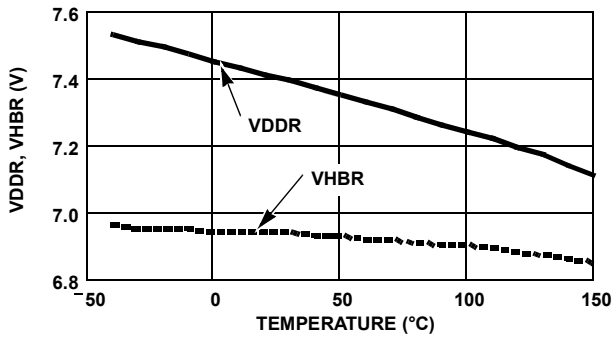


FIGURE 11. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

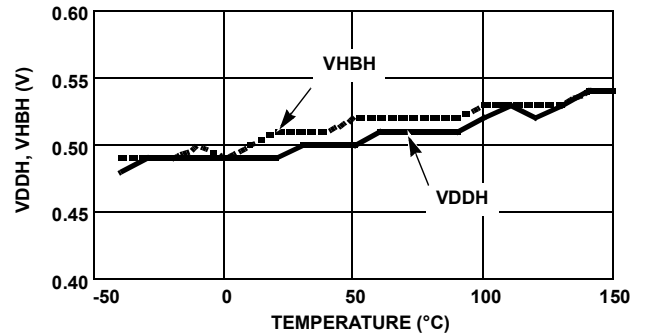


FIGURE 12. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

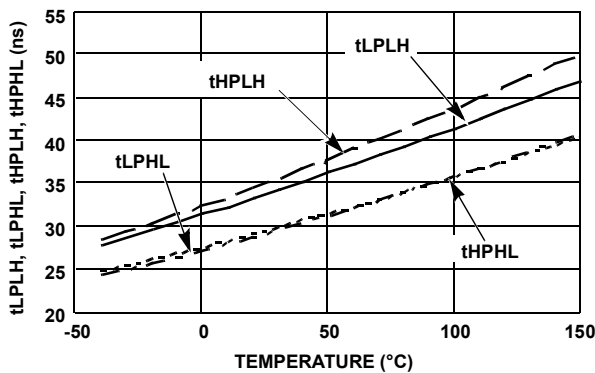


FIGURE 13. ISL2100A PROPAGATION DELAYS vs TEMPERATURE

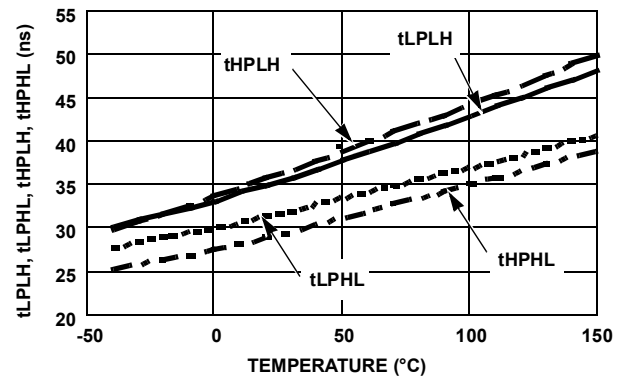


FIGURE 14. ISL2101A PROPAGATION DELAYS vs TEMPERATURE

**Typical Performance Curves** (Continued)

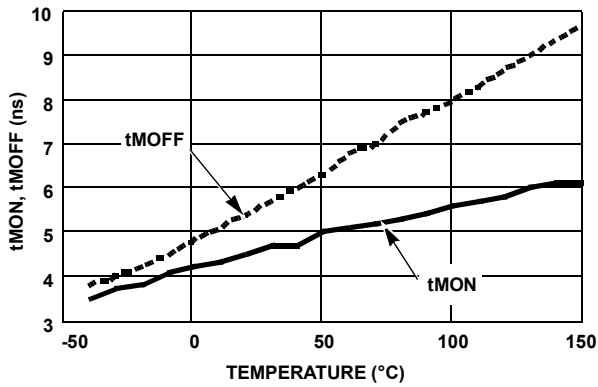


FIGURE 15. ISL2100A DELAY MATCHING vs TEMPERATURE

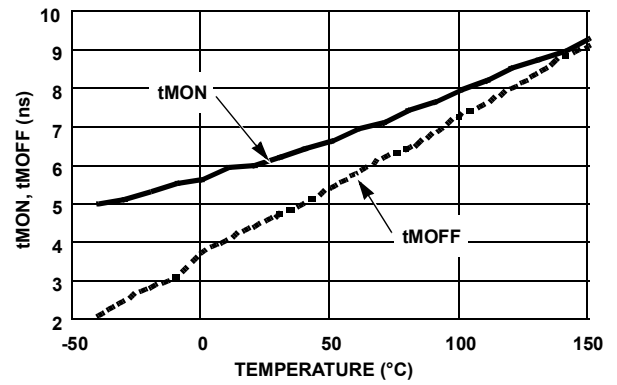


FIGURE 16. ISL2101A DELAY MATCHING vs TEMPERATURE

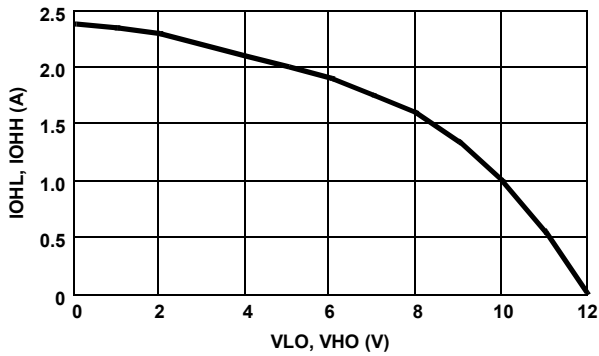


FIGURE 17. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

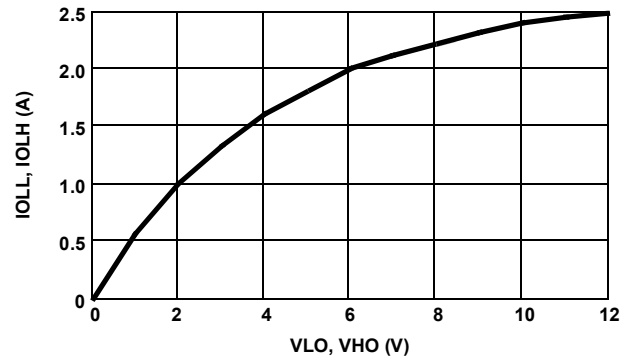


FIGURE 18. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

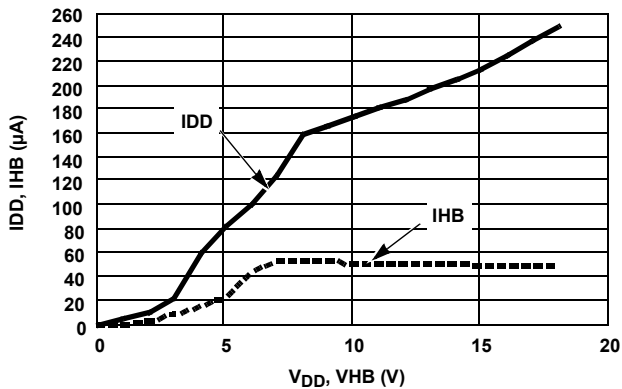


FIGURE 19. ISL2100A QUIESCENT CURRENT vs VOLTAGE

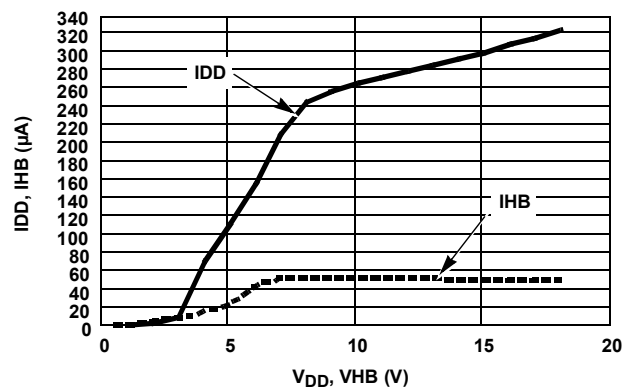


FIGURE 20. ISL2101A QUIESCENT CURRENT vs VOLTAGE



**Typical Performance Curves** (Continued)

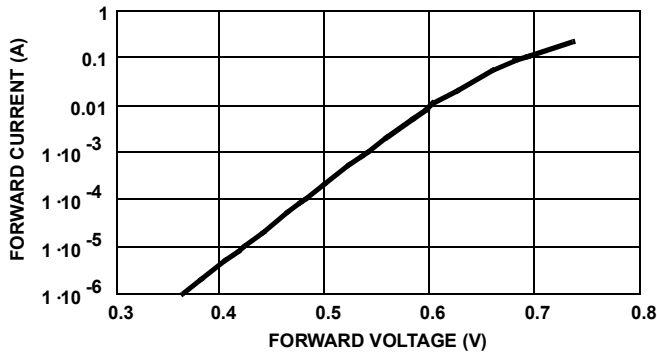


FIGURE 21. BOOTSTRAP DIODE I-V CHARACTERISTICS

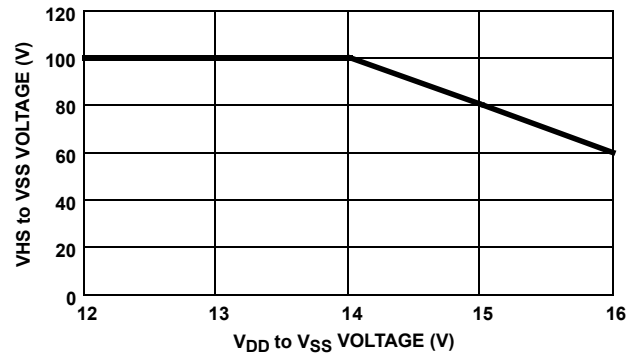


FIGURE 22. VHS VOLTAGE vs V<sub>DD</sub> VOLTAGE

**Revision History**

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Jul 22, 2021	4.1	Updated external links throughout. Updating Ordering Information table format, removed retired part, corrected typo for SOIC package. Updated SOIC Thermal Information as follows: -Changed Theta JA from 120 to 107 -Changed Theta JC from N/A to 50 -Added Notes 8 and 9 and referenced them to SOIC thermals. Removed About Intersil Updated POD L9.3x3 to the latest revision, changes are as follows: -Updated to new format with dimensions included. Also added a PCB land pattern. Added latest version of POD M8.15.
Dec 8, 2015	4.0	- Updated Ordering Information Table on page 3. - Added Revision History. - Added About Intersil Verbiage. - Updated POD L9.3X3 to latest revision changes are as follow: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).. - Updated POD M8.15 to latest revision changes are as follow: Changed Note 1 "1982" to "1994" Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern.

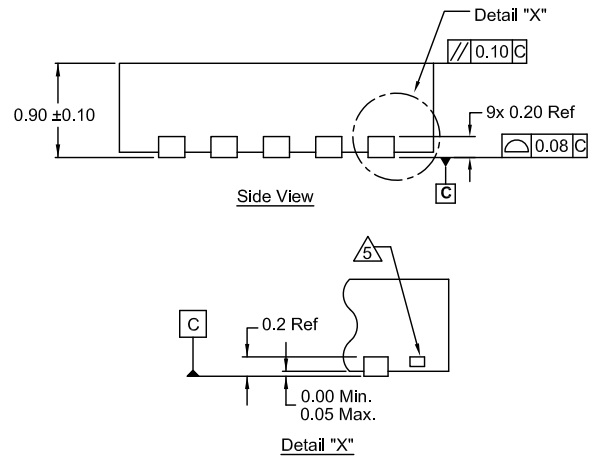
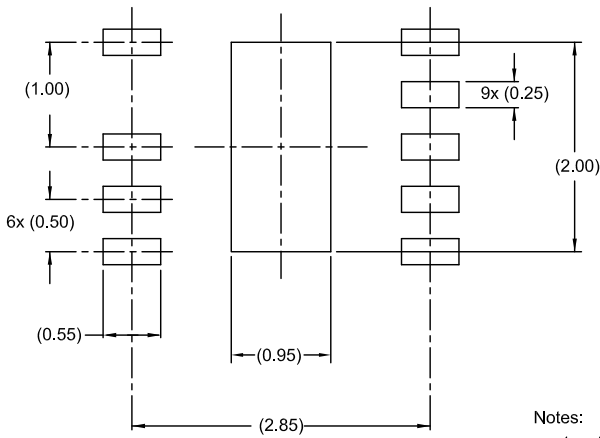
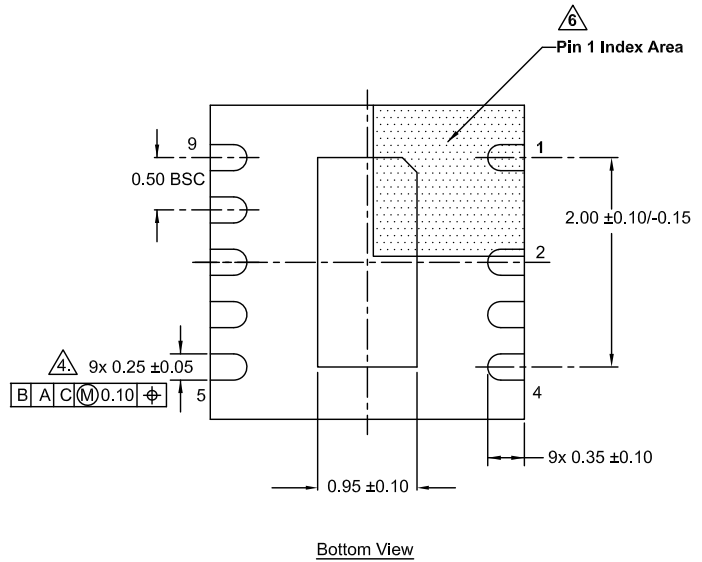
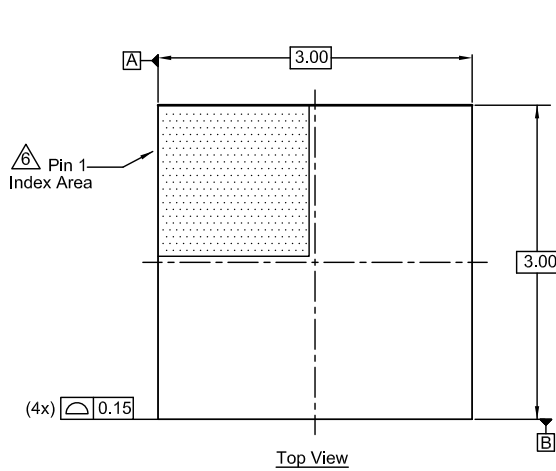
## Package Outline Drawings

For the most recent package outline drawing, see [L9.3x3](#).

L9.3x3

9 Lead Dual Flat No-Lead Plastic Package (DFN)

Rev 2, 4/20



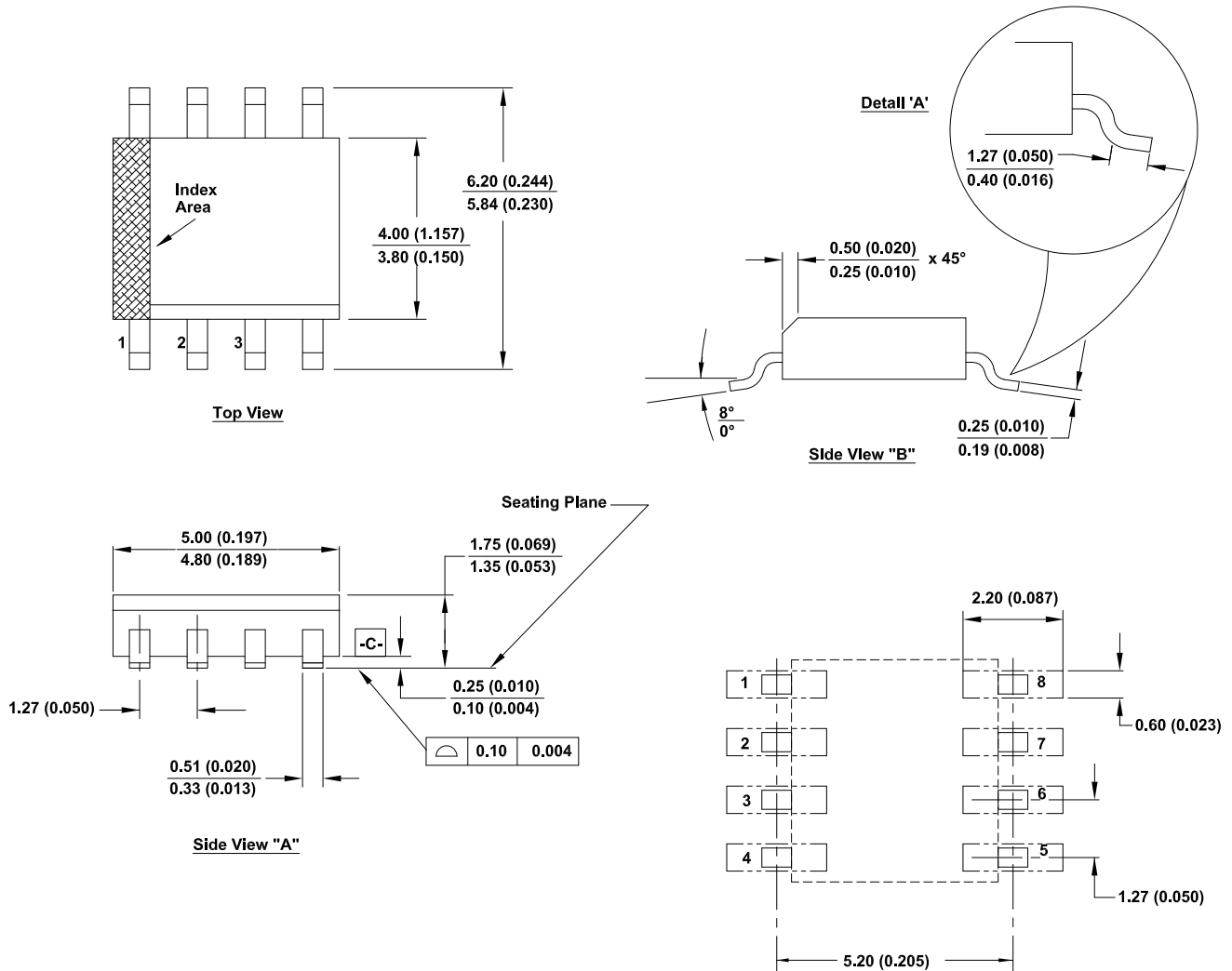
Notes:

1. Dimensions are in millimeters.  
Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal  $\pm 0.05$
- ④ This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- ⑤ Tiebar (if present) is a non-functional feature.
- ⑥ The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

For the most recent package outline drawing, see [M8.15](#).

M8.15

8 Lead Narrow Body Small Outline Plastic Package  
Rev 5, 4/2021



**NOTES:**

- 1 Dimensioning and tolerancing conform to AMSEY14.5m-1994.
- 2 Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- 3 Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- 4 The chamfer on the body is optional. If it is not present, a visual Index feature must be located within the crosshatched area.
- 5 Terminal numbers are shown for reference only.
- 6 The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
- 7 Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
- 8 This outline conforms to JEDEC publication MS-012-AA ISSUE C.