ISL28022

Precision Digital Power Monitor

FN8386
Rev 8.00
February 4, 2016

The ISL28022 is a bidirectional high-side and low-side digital current sense and voltage monitor with serial interface. The device monitors current and voltage and provides the results digitally along with calculated power. The ISL28022 provides tight accuracy of less than 0.3% for both voltage and current monitoring over the entire input range. The digital power monitor has configurable fault thresholds and measurable ADC gain ranges.

The ISL28022 handles common-mode input voltage ranging from 0V to 60V. The wide range permits the device to handle telecom, automotive and industrial applications with minimal external circuitry. Both high- and low-side ground sensing applications are easily handled with the flexible architecture.

The ISL28022 consumes an average current of just 700µA and is available in a 10 Ld MSOP package. The ISL28022 is also offered in a space saving 16 Ld QFN package. The part operates across the extended temperature range from -40°C to +125°C.

Related Literature

- AN1955, "Design Ideas for Intersil Digital Power Monitors"
- AN1875, "ISL28022 Digital Power Monitor Evaluation Kit (ISL28022EVKIT1Z)
- AN1811, "ISL28022 Digital Power Monitor 8 Site Evaluation Kit"

Features

- Bus voltage sense range . . . . . 0V to 60V
- 16-bit ∑ΔADC monitors current and voltage
- Voltage measuring error . . . . . <0.3%
- Current measuring error . . . . . <0.3%
- Handles negative system voltage
- Overvoltage/undervoltage and current fault monitoring
- I^2C/SMBus interface
- Wide V_{CC} range . . . . . 3V to 5.5V
- ESD (HBM). 8kV
- Supports high speed I^2C 3.4MHz

Applications

- Routers and servers
- DC/DC, AC/DC converters
- Battery management/charging
- Automotive power
- Power distribution
- Medical and test equipment

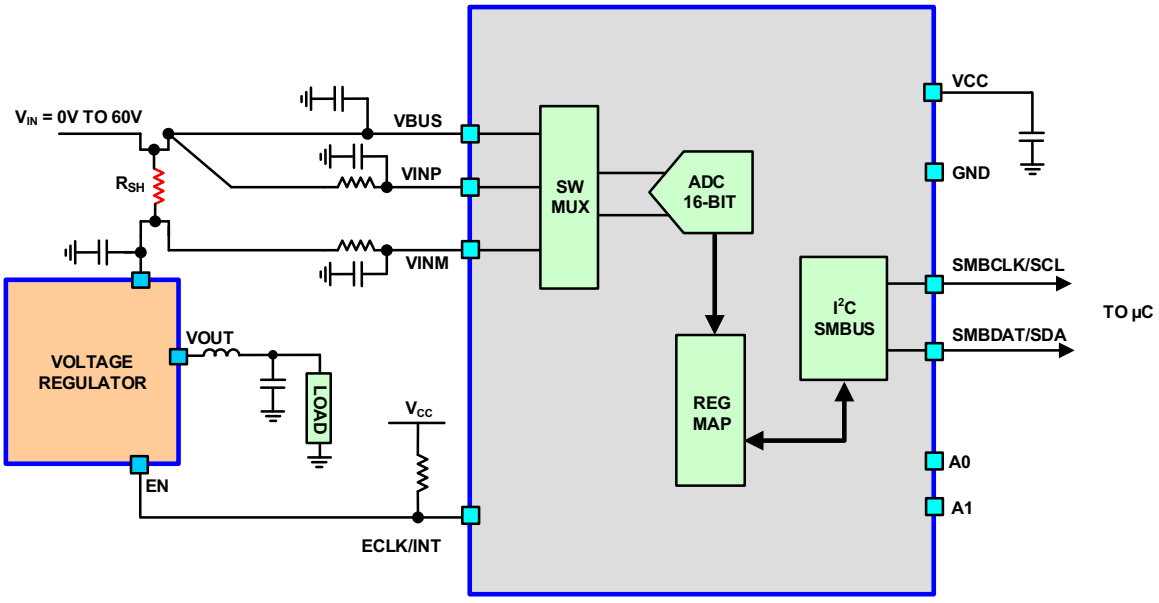

FIGURE 1. TYPICAL APPLICATION

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Block Diagram

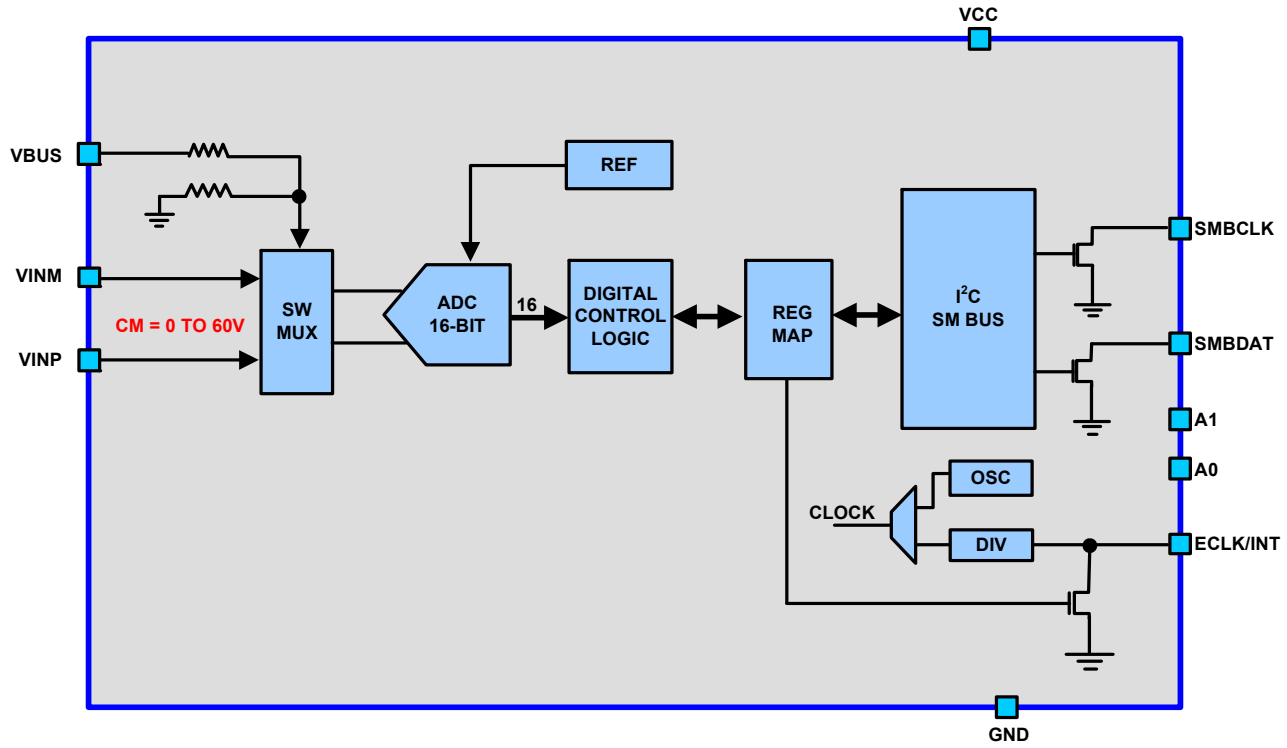


FIGURE 2. BLOCK DIAGRAM

Ordering Information

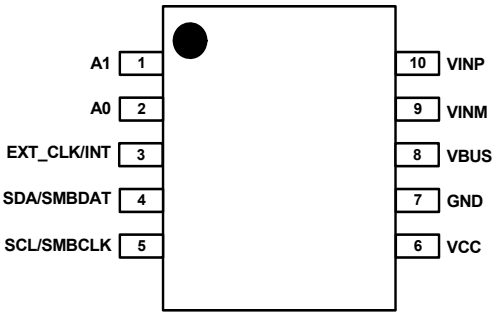
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28022FUZ	8022F	-40 to +125	10 Ld MSOP	M10.118
ISL28022FRZ	022F	-40 to +125	16 Ld QFN	L16.3x3B
ISL28022EVKIT1Z	ISL28022 Evaluation Kit (Includes Dongle Board, Generic Evaluation Board, R_{LOAD} Board)			
ISL28022MBEV1Z	ISL28022 Generic Evaluation Board			
ISL28022EV1Z	ISL28022 8-site Evaluation Board			

NOTES:

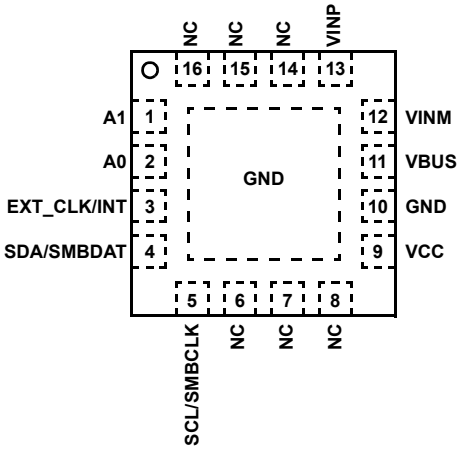
1. Add “-T” suffix for QFN 6k or MSOP 2.5k units tape and reel options. Add “-T7A” suffix for 250 units tape and reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28022. For more information on MSL please see tech brief TB363.

Pin Configurations

ISL28022
(10 LD MSOP)
TOP VIEW



ISL28022
(16 LD QFN)
TOP VIEW



Pin Descriptions

MSOP PIN NUMBER	QFN PIN NUMBER	PIN NAME	DESCRIPTION
1	1	A1	I^2C address, Bit 1
2	2	A0	I^2C address, Bit 0
3	3	EXT_CLK/INT	External ADC clock input or CPU interrupt output signal. When the pin is configured as an interrupt, the output is an open drain.
4	4	SDA/SMBDAT	I^2C serial data input/output.
5	5	SCL/SMBCLK	I^2C clock input
6	9	VCC	Positive power pin. The positive power supply to the part.
7	10	GND	Negative power pin. Can be connected to ground or a negative voltage.
8	11	VBUS	VBUS power voltage sense.
9	12	VINM	Current sense minus input.
10	13	VINP	Current sense plus input.
	6, 7, 8, 14, 15, 16	NC	No connect. No internal connection.
	Epad	GND	Negative power pin. Can be connected to ground or a negative voltage.

TABLE 1. DPM PORTFOLIO COMPARISON - ISL28022 vs ISL28023 vs ISL28025

DESCRIPTION		BASIC DIGITAL POWER MONITOR	FULL FEATURE DIGITAL POWER MONITOR	DIGITAL POWER MONITOR IN TINY PACKAGE
PART NUMBER		ISL28022	ISL28023	ISL28025
PACKAGE		MSOP10, QFN16	QFN24	WLCSP-16
Temperature Range		-40°C to +125°C	-40°C to +125°C	-40°C to +125°C
0V to 60V Input Range		0V to 60V	Opt 1: 0V to 60V Opt 2: 0V to 16V	Opt 1: 0V to 60V Opt 2: 0V to 16V
ADC		16-bit	16-bit	16-bit
+25°C Gain Error		0.30%	0.25%	0.25%
Current Measure LSB Step		10µV	2.5µV	2.5µV
+25°C Offset		75µV	30µV	30µV
Primary	Differential Shunt Input	X	X	X
Channel	Independent Bus Voltage	X	X	X
LV Aux	Differential Shunt Input		X	
Channel	Independent Bus Voltage		X	X
VBus LSB Step	Low Voltage Bus		0.25mV	0.25mV
	High Voltage Bus	4mV	1mV/0.25mV	1mV/0.25mV
External Temperature Sensor Input			X	
HV Internal Regulator ($3.3V_{OUT}$)			X	X
Fast OC/OV/UV Alert Outputs			2 Outputs	2 Outputs
Margin DAC			X	
Internal Temperature Sensor			X	X
User Select Conversion Mode/Sample Rate		X	X	X
Peak Min/Max Current Registers			X	X
Slave Address Locations		16 Addresses	55 Addresses	55 Addresses
I^2C Level Translators			X	X
PMBus			X	X
I^2C/SMBus		X	X	X
High Speed (3.4MHz) I^2C Mode		X	X	X
External Clock Input		X	X	X
Power Shutdown Mode		X	X	X

Absolute Maximum Ratings

VCC 6.0V
VBUS Voltage. 63V
Common-Mode Input Voltage (VINP, VINM) 63V
Differential Input Voltage (VINP, VINM) . . . . . ±63V
Input Voltage (Digital Pins) . . . . . (GND - 0.3V) to 5.5V
Output Voltage (Digital Pins). . . . . (GND - 0.3V) to VCC + 0.3V
Open-Drain Output Current 10mA
Open-Drain Voltage (Interrupt) 24V
ESD Rating
Human Body Model (Tested per JESD22-A114) 8kV
Machine Model (Tested per JESD22-A115). 400V
Charged Device Model (Tested per JESD22-C101). 2kV
Latch-Up (Tested per JESD-78B) . . . . . 60V at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN (Notes 4, 5)	52	6.5
10 Ld MSOP (Notes 6, 7)	150	55

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications

T_A = +25°C, V_{CC} = 3.3, VINP = V_{BUS} = 12V, V_{SENSE} = VINP-VINM = 32mV, unless otherwise specified. All voltages with respect to GND pin.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
INPUTS						
$V_{SENSEDIFF}$	Useful Full-Scale Current Sense Differential Voltage Range (VINP-VINM)	PGA gain = /1	0		±40	mV
		PGA gain = /2	0		±80	mV
		PGA gain = /4	0		±160	mV
		PGA gain = /8	0		±320	mV
V_{SHUNT_step}	LSB Step Size, Shunt Voltage			10		µV
$V_{CMSENSE}$	Current Sense Common-Mode (VINP, VINM)		0		60	V
V_{OS}	V_{SENSE} Offset Voltage	PGA gain = /1, /2, /4, /8; ADC setting = 1111		±10	±75	µV
V_{OSTC}	V_{SENSE} Offset Voltage Temperature Coefficient			0.15		µV/°C
CMRR	V_{SENSE} V_{OS} vs Common-Mode	V_{BUS} = 0V to 60V; BRNG = 2, 3	110	130		dB
PSRR	V_{SENSE} V_{OS} vs Power Supply	V_{CC} = 3V to 5V		105		dB
A_{CS}	Current Sense Gain Error			±40		m%
A_{CSTC}	Current Sense Gain Error Temperature Coefficient			±1		m%/°C
I_{VINACT}	Input Leakage, VIN Pins	Active mode (for both VINP and VINM pins)		±20		µA
I_{VINACT}	Input Leakage, VIN Pins	Power-down mode (for both VINP and VINM pins)		±0.1	±0.5	µA
V_{BUS}	Useful Bus Voltage Range	BRNG = 0	0		16	V
		BRNG = 1	0		32	V
		BRNG = 2, 3	0		60	V
V_{BUS_Step}	LSB Step Size, Bus Voltage	BRNG = 0		4		mV
V_{BUS_VCO}	V_{BUS} Voltage Coefficient			50		ppm/V
R_{VBACT}	Input Impedance, VBUS Pin	Active mode		600		kΩ

Electrical Specifications

T_A = +25°C, V_{CC} = 3.3, VINP = V_{BUS} = 12V, V_{SENSE} = VINP-VINM = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
DC ACCURACY						
	ADC Resolution (Native)	PGA gain = /1, V_{SENSE} = ±320mV		16		Bits
	Current Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Current Measurement Error Over-Temperature	T_A = -40°C to +85°C			±0.5	%
		T_A = -40°C to +125°C			±1	%
	Bus Voltage Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Bus Voltage Measurement Error Over-Temperature	T_A = -40°C to +85°C			±0.5	%
		T_A = -40°C to +125°C			±1	%
ADC TIMING SPECS						
t_S	ADC Conversion Time Mode = 5 or 6	ADC setting = 0000		72.0	79.2	µs
		ADC setting = 0001		132.0	145.2	µs
		ADC setting = 0010		258.0	283.8	µs
		ADC setting = 0011		508.0	558.8	µs
		ADC setting = 1001		1.01	1.11	ms
		ADC setting = 1010		2.01	2.21	ms
		ADC setting = 1011		4.01	4.41	ms
		ADC setting = 1100		8.01	8.81	ms
		ADC setting = 1101		16.01	17.61	ms
		ADC setting = 1110		32.01	35.21	ms
		ADC setting = 1111		64.01	70.41	ms
I^2C INTERFACE SPECIFICATIONS						
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x V_{CC}	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{CC}		V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{CC} = 5V, I_{OL} = 3mA	0	0.02	0.40	V
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{CC} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the maximum spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge Both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, VINP = V_{BUS} = 12V, V_{SENSE} = VINP-VINM = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	20		900	ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 x Cb		300	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 x Cb		300	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip		75		pF
R_{PU}	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For Cb = 400pF, maximum is about 2kΩ~2.5kΩ For Cb = 40pF, maximum is about 15kΩ~20kΩ	1			k
POWER SUPPLY						
	Operating Supply Voltage Range		3		5.5	V
I_{CCEXT}	Power Supply Current On V_{CC} Pin, Active Mode	External power supply mode, V_{CC} = 5V		0.7	1.0	mA
I_{CCPD}	Power Supply Current On V_{CC} Pin, Power-Down Mode	External power supply mode, V_{CC} = 5V		5	15	µA

NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, VINP = V_{BUS} = 12V, S(B)ADC = 15; unless otherwise specified.

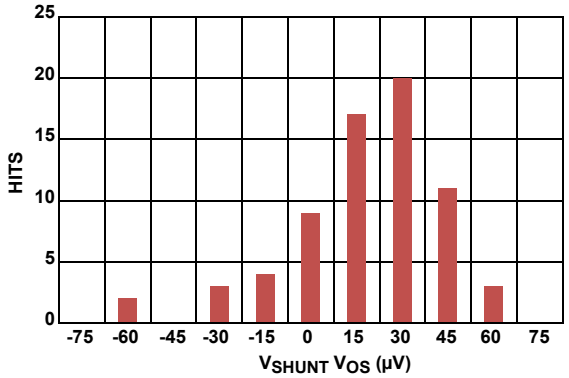


FIGURE 3. V_{SHUNT} V_{OS}

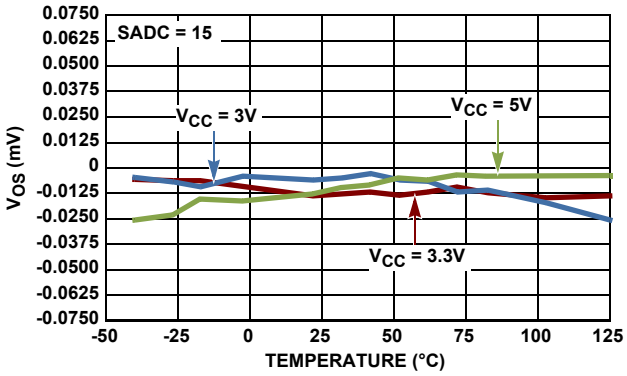


FIGURE 4. V_{SHUNT} V_{OS} vs TEMPERATURE

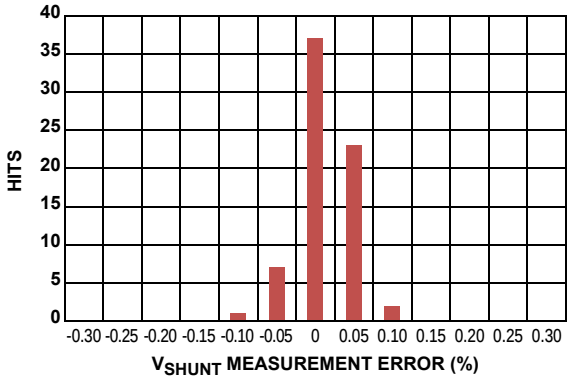


FIGURE 5. V_{SHUNT} MEASUREMENT ERROR

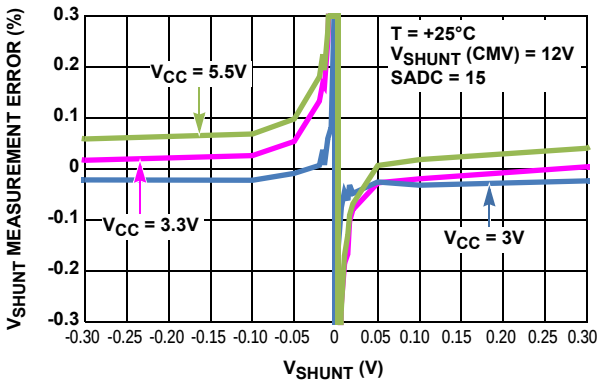


FIGURE 6. V_{SHUNT} MEASUREMENT ERROR vs V_{SHUNT} INPUT

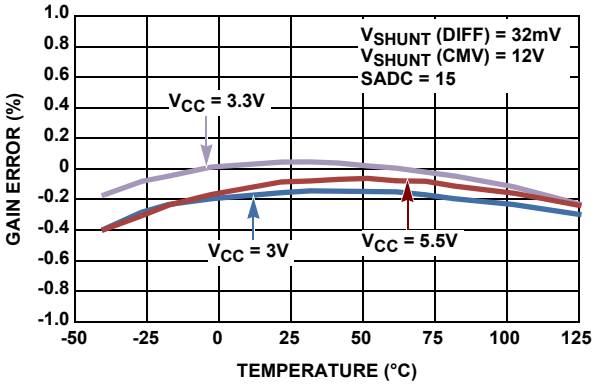


FIGURE 7. V_{SHUNT} GAIN vs TEMPERATURE

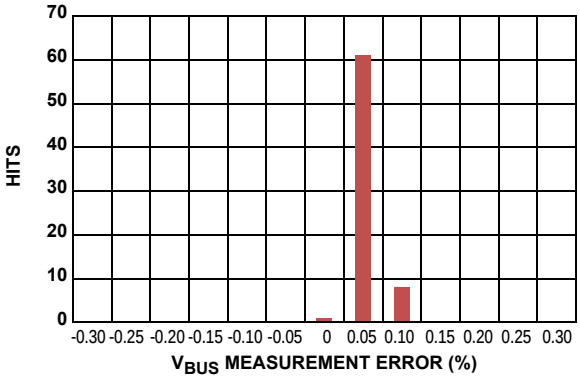


FIGURE 8. V_{BUS} MEASUREMENT ERROR DISTRIBUTION

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, VINP = V_{BUS} = 12V, S(B)ADC = 15; unless otherwise specified. **(Continued)**

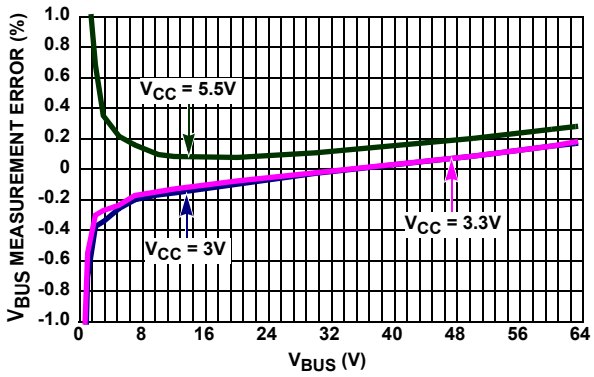


FIGURE 9. V_{BUS} MEASUREMENT ERROR vs V_{BUS} (T_A = +25°C)

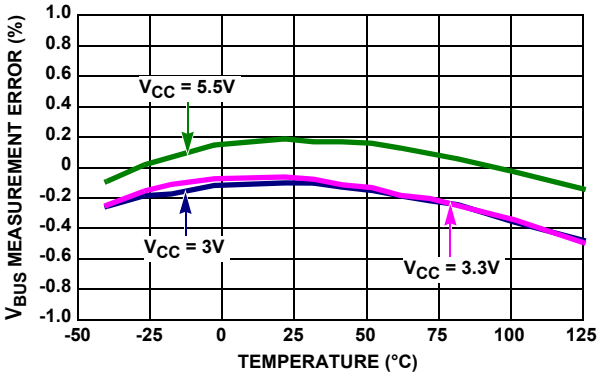


FIGURE 10. V_{BUS} MEASUREMENT ERROR vs TEMPERATURE

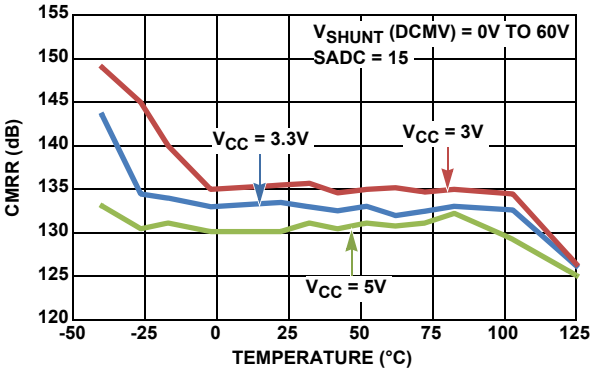


FIGURE 11. CMRR vs TEMPERATURE

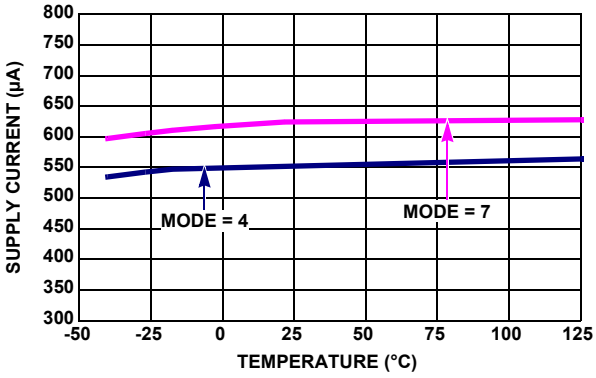


FIGURE 12. SUPPLY CURRENT vs MODE vs TEMPERATURE

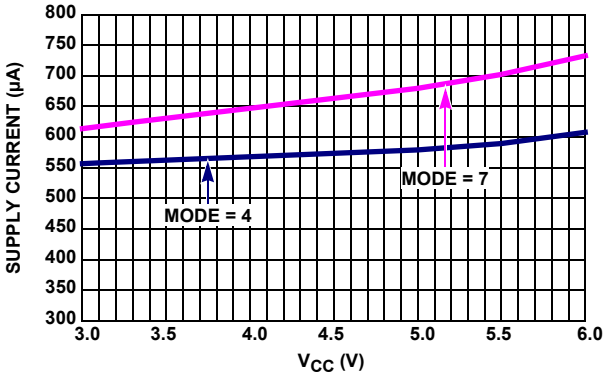


FIGURE 13. SUPPLY CURRENT vs MODE vs V_{CC}

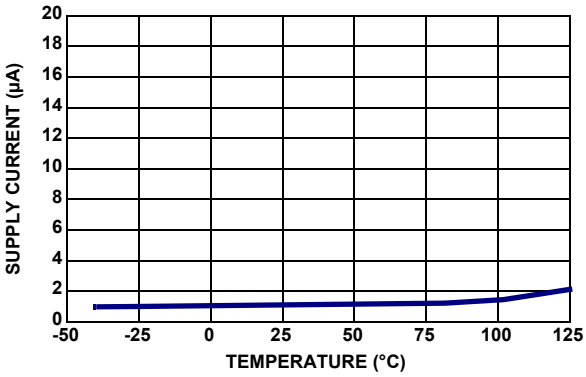


FIGURE 14. SUPPLY CURRENT vs MODE 0 vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, VINP = V_{BUS} = 12V, S(B)ADC = 15; unless otherwise specified. **(Continued)**

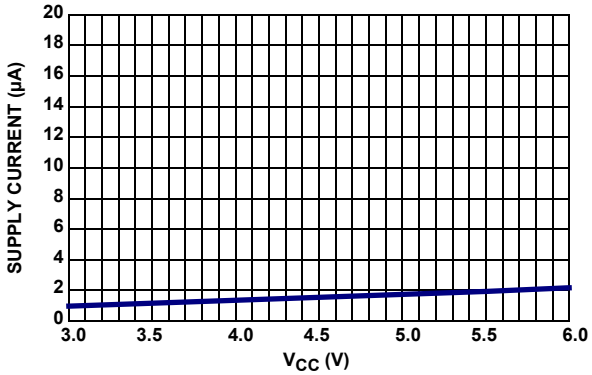


FIGURE 15. SUPPLY CURRENT vs MODE 0 vs V_{CC}

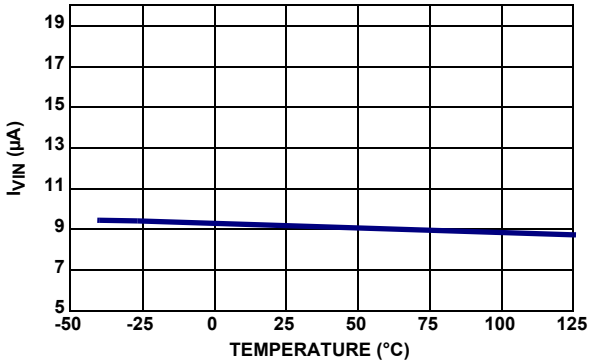


FIGURE 16. SHUNT I_{VIN} vs TEMPERATURE (MODE 5)

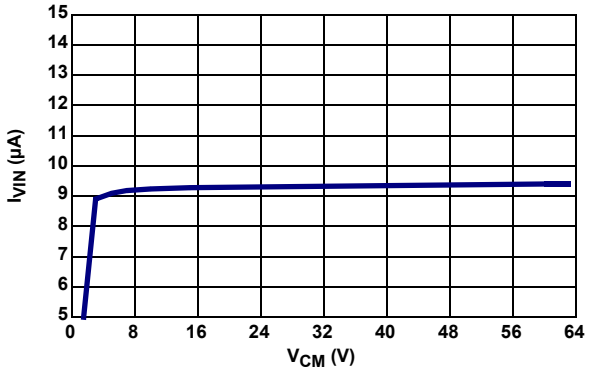


FIGURE 17. SHUNT I_{VIN} vs COMMON-MODE VOLTAGE (MODE 5)

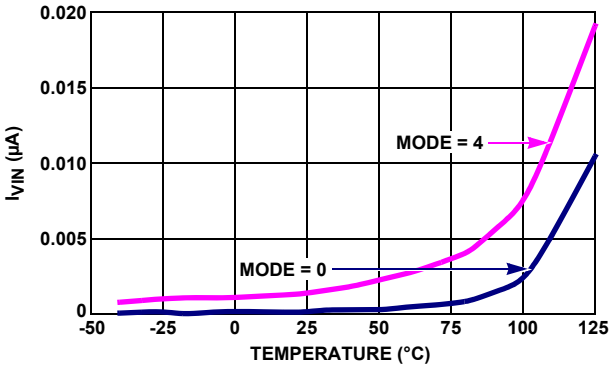


FIGURE 18. SHUNT I_{VIN} vs TEMPERATURE (MODE 0, 4)

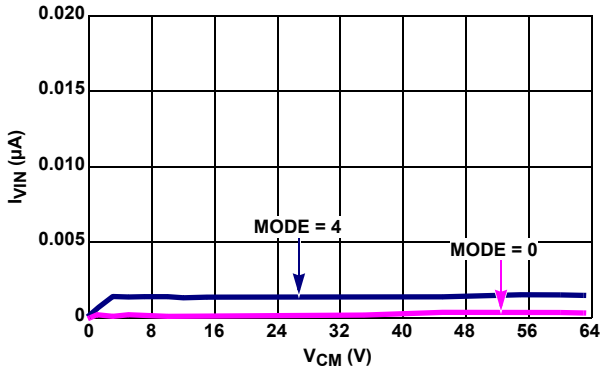


FIGURE 19. SHUNT I_{VIN} vs COMMON-MODE VOLTAGE (MODE 0, 4)

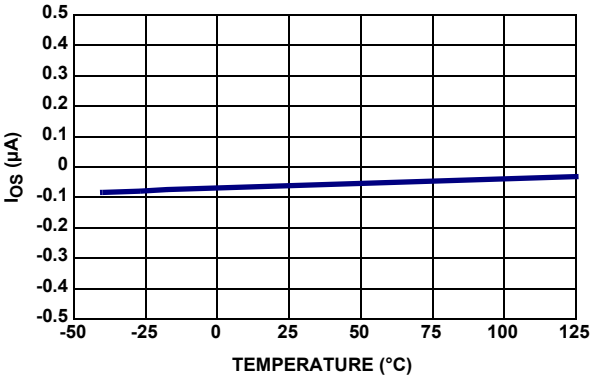


FIGURE 20. SHUNT I_{OS} vs TEMPERATURE (MODE 5)

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, VINP = V_{BUS} = 12V, S(B)ADC = 15; unless otherwise specified. **(Continued)**

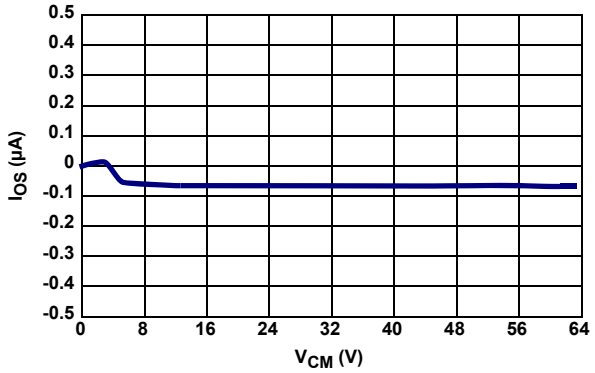


FIGURE 21. SHUNT I_{OS} vs COMMON-MODE VOLTAGE (MODE 5)

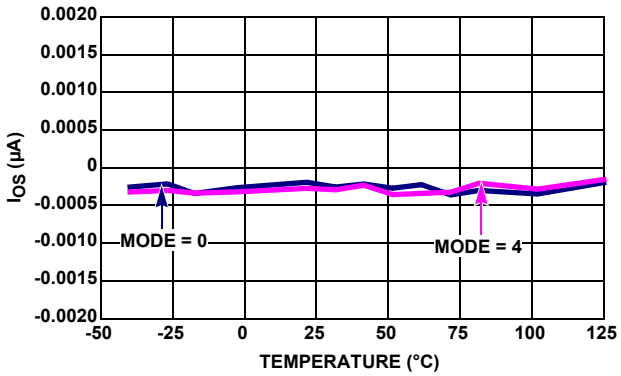


FIGURE 22. SHUNT I_{OS} vs TEMPERATURE (MODE 0, 4)

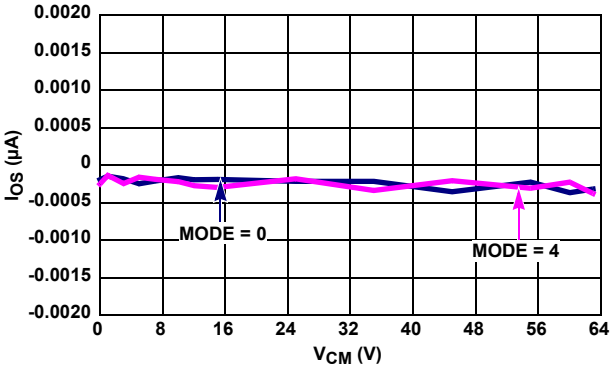


FIGURE 23. SHUNT I_{OS} vs COMMON-MODE VOLTAGE (MODE 0, 4)

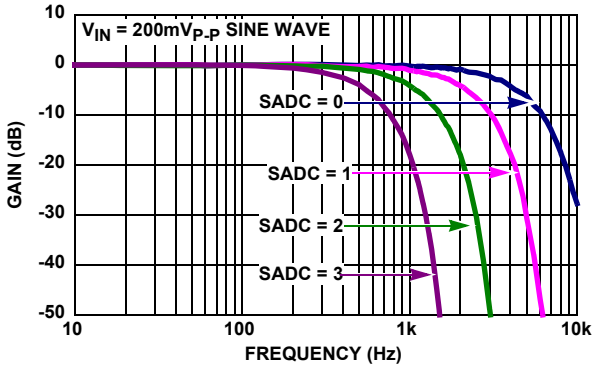


FIGURE 24. V_{SHUNT} BANDWIDTH vs SADC MODE

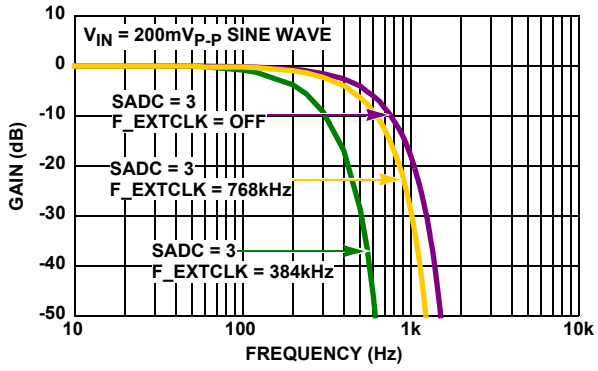


FIGURE 25. V_{SHUNT} BANDWIDTH vs EXTERNAL CLOCK FREQUENCY

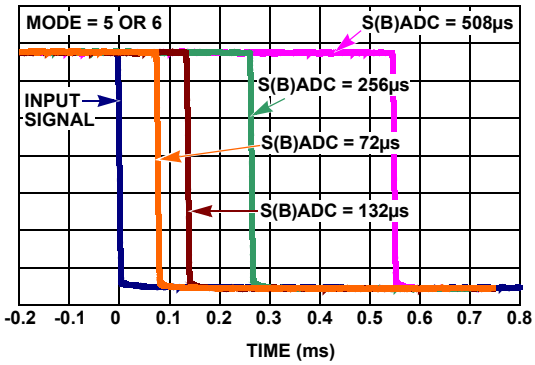


FIGURE 26. INTERRUPT TIMING

Functional Description

Overview

The ISL28022 is a Digital Power Monitor (DPM) device that is capable of measuring bidirectional currents while monitoring the bus voltage.

The DPM requires an external shunt resistor to enable current measurements. The shunt resistor translates the bus current to a voltage. The DPM measures the voltage across the shunt resistors and reports the measured value out digitally via an I^2C interface. A register within the DPM is reserved to store the value of the shunt resistor. The stored current sense resistor value allows the DPM to output the current value to an external digital device.

The ISL28022 measures bus voltage and current sequentially. The device has a power measurement functionality that multiplies current and voltage measured values. The power calculation is stored in a unique register. The power measurement allows the user to monitor power to or from the load in addition to current and voltage.

The ISL28022 can monitor supplies from 0V to 60V while operating on a chip supply ranging from 3V to 5.5V.

The ISL28022 ADC sample rate can be configured to an internal oscillator (500kHz) or a user can provide a synchronized clock.

Detailed Description

The ISL28022 consists of a two channel analog front end multiplexer, a 16-bit sigma delta ADC and digital signal processing/serial communication circuitry.

The main block within the device is a 3rd order Sigma Delta ADC. The input signal bandwidth is 1kHz, wide enough for power monitoring applications. The main block includes an internal 1.2V bandgap voltage reference that is used to drive the ADC.

The analog front end multiplexer selects the input to the ADC. The selection to the input of the ADC is either a single-ended V_{BUS} measurement or a fully differential measurement across a shunt resistor.

The digital block contains controllable registers, I^2C serial communication circuitry and a state machine. The state machine controls the behavior of the ADC acquisition, whether the acquisition is triggered or continuous. A more detailed description of the state machine states can be found in "MODE: Operating Mode" on page 15.

Functional Pin Descriptions

A1

A1 is the address select pin. A1 is one of two I^2C/SMBus slave address select pins that are multilogic programmable for a total of 16 different address combinations.

There are four selectable levels for A1, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 22 for more details in setting the slave address of the device.

A0

A0 is the address select pin. A0 is one of two I^2C/SMBus slave address select pins that are multilogic programmable for a total of 16 different address combinations.

There are four selectable levels for A0, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 22 for more details in setting the slave address of the device.

EXT_CLK/INT

EXT_CLK/INT is the External/Interrupt clock pin. EXT_CLK/INT is a bidirectional pin. The pin provides a connection to the system clock. The system clock is connected to the ADC. The acquisitions rate of the ADC can be varied through the EXT_CLK/INT pin. The pin functionality is set through a control register bit.

When the EXT_CLK/INT pin is configured as an output, the pin functionality becomes an interrupt flag to connecting devices. EXT_CLK/INT pin as an output requires a pull-up resistor to a power supply, up to 20V, for proper operation. The internal threshold detectors ($OV_{sh}/UV_{sh}/OV_b/UV_b$) signal level relative to the measured value determines the state of the INT pin.

SDA/SMBDAT

SDA/SMBDAT is the serial data input/output pin. SDA/SMBDAT is a bidirectional pin used to transfer data to and from the device. The pin is an open-drain output and may be wired with other open-drain/collector outputs. The open-drain output requires a pull-up resistor for proper functionality. The pull-up resistor should be connected to VCC of the device.

SCL/SMBCLK

SCL/SMBCLK is the serial clock input pin. The SCL/SMBCLK input is responsible for clocking in all data to and from the device.

VCC

VCC is the positive supply voltage pin. VCC is an analog power pin. VCC supplies power to the device.

GND

GND is the ground pin. All voltages internal to the chip are referenced to ground. GND should be tied to 0V for single supply applications. For dual supply applications, the pin should be connected to the most negative voltage in the application.

VBUS

VBUS is the power bus voltage input pin. The pin should be connected to the desired power supply bus to be monitored.

VINP

VINP is the shunt voltage monitor positive input pin. The pin connects to the most positive voltage of the current shunt resistor.

VINM

VINM is the shunt voltage monitor negative input pin. The pin connects to the most negative voltage of the current shunt resistor.

TABLE 2. ISL28022 REGISTER DESCRIPTIONS

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER-ON RESET VALUE (HEX)	ACCESS
00	Configuration	Power-on reset, bus and shunt ranges, ADC acquisition times, mode configuration	799F	R/W
01	Shunt Voltage	Shunt voltage measurement value	0000	R
02	Bus Voltage	Bus voltage measurement value	0000	R
03	Power	Power measurement value	0000	R
04	Current	Current measurement value	0000	R
05	Calibration Register	Register used to enable current and power measurements.	0000	R/W
06	Shunt Voltage Threshold	Min/Max shunt thresholds	7F81	R/W
07	Bus Voltage Threshold	Min/Max V_{BUS} thresholds	FF00	R/W
08	DCS Interrupt Status	Threshold interrupts	0000	R/W
09	Aux Control Register	Register to control the interrupts and external clock functionality	0000	R/W

TABLE 3. CONFIGURATION REGISTER

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RST	BRNG1	BRNG0	PG1	PG0	BADC3	BADC2	BADC1	BADC0	SADC3	SADC2	SADC1	SADC0	MODE2	MODE1	MODE0

Register Descriptions

Table 2 is the register map for the device. The table describes the function of each register and its respective value. The addresses are sequential and the register size is 16 bits (2 bytes) per address.

CONFIGURATION REGISTER

The configuration register (Table 3) controls the functionality of the chip. ADC measurable range, converter acquisition times, converter resolution and state machine modes are configurable bits within this register.

RST: Reset Bit

Configuring the reset bit (Bit 15) to a 1 generates a system reset that initializes all registers to their default values and performs a system calibration.

BRNG: Bus Voltage Range

Bits 13 and 14 of the configuration register sets the bus measurable voltage range. Table 4 shows the BRNG bit configurations versus the allowable full-scale measurement range. The shaded row is the power-up default.

TABLE 4. BRNG BIT SETTINGS

BRNG1	BRNG0	USABLE FULL SCALE RANGE (V)
0	0	16
0	1	32
1	0	60
1	1	60

PG: PGA (Shunt Voltage Only)

Bits 11 and 12 of the configuration register determines the shunt voltage measurement range. Table 5 shows the PGA bit configurations versus the allowable full-scale measurement range. The shaded row is the power-up default.

TABLE 5. PGA BIT SETTINGS

PG1	PG0	GAIN	RANGE (mV)
0	0	1	±40
0	1	÷2	±80
1	0	÷4	±160
1	1	÷8	±320

BADC: Bus ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/averaging when the ADC is configured in the V_{BUS} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15 bits. The ADC is configurable versus the number of averages. The selection ranges from 2 to 128 samples. Table 6 shows the breakdown of each BADC setting. The shaded row is the default setting upon power-up.

SADC: Shunt ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/averaging when the ADC is configured in the V_{SHUNT} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15 bits. The ADC is configurable versus number of averages. The selection ranges from 2 to 128 samples. Table 6 shows the breakdown of each SADC setting. The shaded row is the default setting upon power-up.

MODE: Operating Mode

Bits [2:0] of the configuration register controls the state machine within the chip. The state machine globally controls the overall functionality of the chip. Table 7 shows the various states the chip can be configured to, as well as the mode bit definitions to achieve a desired state. The shaded row is the default setting upon power-up.

TABLE 6. ADC SETTINGS, APPLIES TO BOTH SADC AND BADC CONTROL

ADC3	ADC2	ADC1	ADC0	MODE/SAMPLES	CONVERSION TIME
0	X	0	0	12-bit	72µs
0	X	0	1	13-bit	132µs
0	X	1	0	14-bit	258µs
0	X	1	1	15-bit	508µs
1	0	0	0	15-bit	508µs
1	0	0	1	2	1.01ms
1	0	1	0	4	2.01ms
1	0	1	1	8	4.01ms
1	1	0	0	16	8.01ms
1	1	0	1	32	16.01ms
1	1	1	0	64	32.01ms
1	1	1	1	128	64.01ms

TABLE 7. OPERATING MODE SETTINGS

MODE2	MODE1	MODE0	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	ADC off (disabled)
1	0	1	Shunt Voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

SHUNT VOLTAGE REGISTER 01H (READ-ONLY)

The shunt voltage register reports the measured value across the shunt pins (VINP and VINM) into the register. The shunt register LSB is independent of PGA range settings. The PGA setting for the shunt register masks the unused most significant bit with a sign bit. For lower range of PGA settings, multiple sign bits are returned by the DPM. Only one sign bit should be used to calculate the measured value.

Tables 8 through 11 show the weights of each bit for various PGA ranges. The tables should be used to calculate the measured value across the shunt pins from the binary to decimal domains.

To calculate the measured decimal value across the shunt, first read the shunt voltage register. Assume the PGA setting is set to the 80mV range. For this example, the reading output by the chip is 1111 1010 0000 0101. The 80mV range has three sign bits. Only one sign bit needs to be used to calculate the measured decimal value. Bits 14 and 15 are omitted from the calculation. This leaves a binary reading of 11 1010 0000 0101.

Next, multiply each bit by its respective weight. Bit0 value would be multiplied by Bit0 weight (1), Bit1 value*Bit1 weight (2), etc.

Add all the multiplied values to equate to a single number. For the binary reading 11 1010 0000 0101 this equates to -1531.

The LSB for a shunt register is 10µV. Multiplying the decimal value by the LSB weight yields the measured voltage across the shunt. A 1111 1010 0000 0101 reading equals -15.31mV measured across the shunt pins.

TABLE 8. SHUNT VOLTAGE REGISTER, PG GAIN = /8 (RANGE = 11), FULL-SCALE = ±320mV, 15 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 9. SHUNT VOLTAGE REGISTER, PG GAIN = /4 (RANGE = 10), FULL-SCALE = ±160mV, 14 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT		-16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 10. SHUNT VOLTAGE REGISTER, PG GAIN = /2 (RANGE = 01), FULL-SCALE = ±80mV, 13 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT			-8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 11. SHUNT VOLTAGE REGISTER, PG GAIN = /1 (RANGE = 00), FULL-SCALE = ±40mV, 12 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Sign	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT				-4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 12. BUS VOLTAGE REGISTER, BRNG = 10 OR 11, FULL-SCALE = 60V, 14 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CNVR	OVF
WEIGHT	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1		

TABLE 13. BUS VOLTAGE REGISTER, BRNG = 01, FULL-SCALE = 32V, 13 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT	4096	2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 14. BUS VOLTAGE REGISTER, BRNG = 00, FULL-SCALE = 16V, 12 BITS WIDE

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME		Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT		2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 15. CALIBRATION REGISTER, 05h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	0

BUS VOLTAGE REGISTER 02h (READ-ONLY)

The bus voltage register is where the DPM reports the measured value of the V_{BUS}. There are three scale ranges possible depending on the BRNG setting controlled from the configuration register (00h).

Tables 12 through 14 on page 16 are the weight bits for each BRNG setting. The binary value recorded in the Bus Voltage register is translated to a decimal value in the same way as the shunt voltage register is converted to a decimal value.

$$V_{bus} = \left[\sum_{n=2}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Vbus_{LSB} \quad \text{(EQ. 1)}$$

Equation 1 is the mathematical equation for converting the binary V_{BUS} value to a decimal value. N is the bit number. The LSB value for the V_{BUS} measurement equals 4mV across all bus range (BRNG) settings.

CNVR: Conversion Ready (Bit 1)

The conversion ready bit indicates when the ADC has finished a conversion and transferred the reading(s) to the appropriate register(s). The CNVR is only operable when the DPM is set to one of three trigger modes. The CNVR is at a low state when the conversion is in progress. The CNVR transitions and remains at a high state when the conversion is complete.

The CNVR bit is initialized or reinitialized in the following ways:

1. Writing to the configuration register.
2. Reading from power register.

OVF: Math Overflow Flag (Bit0)

The Math Overflow Flag (OVF) is a bit that is set to indicate the current or power data being read from the DPM is over-ranged and meaningless.

CALIBRATION REGISTER 05h (READ/WRITE)

To accurately read the current and power measurements from the chip, the calibration register needs to be programmed.

The calibration register value is calculated as follows:

1. Calculate the full-scale current range that is desired. This is calculated using Equation 2. R_{shunt} is the value of the shunt resistor. $Vshunt_{FS}$ is the full-scale setting that is desired. In most cases, it is the PGA full-scale range (320mV, 160mV, 80mV and 40mV) that the DPM is programmed to.

$$Current_{FS} = \frac{Vshunt_{FS}}{R_{shunt}} \quad \text{(EQ. 2)}$$

2. From the current full-scale range, the current LSB is calculated using Equation 3. Current full-scale is the outcome from Equation 2. ADC_{res} is the resolution of shunt voltage reading. The value is determined by the SADC setting in configuration register. SADC setting equal to 3 and greater will have a 15-bit resolution. The ADC_{res} value equals 2^{15} or 32768.

$$Current_{LSB} = \frac{Current_{FS}}{ADC_{res}} \quad \text{(EQ. 3)}$$

3. From Equation 3, the calibration resister value is calculated using Equation 4. The resolution of the math that is processed internally in the DPM is 4096 or 12 bits of resolution. The $Vshunt_{LSB}$ is set to 10µV. Equation 4 yields a 16-bit binary number that can be written to the calibration register. The calibration value can only be 15 bits due to the ADC_{res} value. Bit 0 of the calibration register is fixed to a value of 0. The calibration register format is represented in Table 15.

$$CalReg_{val} = integer\left[\frac{Math_{res} \cdot Vshunt_{LSB}}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right]$$

$$CalReg_{val} = integer\left[\frac{0.04096}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right] \quad \text{(EQ. 4)}$$

CURRENT REGISTER 04h (READ-ONLY)

Once the calibration register (05h) is programmed, the output current is calculated using Equation 5:

$$Current = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Current_{LSB} \quad \text{(EQ. 5)}$$

Bit is the returned value of each bit from the current register either 1 or a 0. The weight of each bit is represented in Table 16. n is the bit number. The current LSB is the value calculated from Equation 3.

POWER REGISTER 03h (READ-ONLY)

The Power register only has meaning if the calibration register (05h) is programmed. The units for the power register are in watts. The power is calculated using Equation 6:

$$Power = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Power_{LSB} \cdot 5000 \quad \text{(EQ. 6)}$$

Bit is the returned value of each bit from the power register either 1 or a 0. The weight of each bit is represented in Table 17. n is the bit number. The power LSB is calculated from Equation 7:

$$Power_{LSB} = Current_{LSB} \cdot Vbus_{LSB} \quad \text{(EQ. 7)}$$

If V_{BUS} range, BRNG, is set to 60V, the power equation in Equation 6 is multiplied by 2.

THRESHOLD REGISTERS

The Shunt Voltage or V_{BUS} threshold registers are used to set the Min/Max threshold limits that will be tested versus V_{SHUNT} or V_{BUS} readings. Measurement readings exceeding the respective V_{SHUNT} or V_{BUS} limits, either above or below, will set a register flag and perhaps an external interrupt depending on the configuration of the Interrupt Enable bit (INTREN) in register 09h. The testing of the ADC reading versus the respective threshold limits occurs once per ADC conversion.

SHUNT VOLTAGE THRESHOLD REGISTER 06h (READ/WRITE)

The V_{SHUNT} minimum and maximum threshold limits are set using one register. The shunt value readings are either positive or negative. D15 and D7 bits of Table 18 are given to represent the sign of the limit. SMX bits represent the upper limit threshold. SMN represents the lower threshold limit. Equation 8 is the calculation used to convert the V_{SHUNT} threshold binary value to decimal. Bit is the value of each bit set in the shunt threshold register. The value is either 1 or a 0. The weight of each bit is represented in Table 18. n is the bit number. The shunt voltage threshold LSB is 2.56mV.

$$Vs_{thresh} = \left[\sum_{n=0}^{7}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot VsThresh_{LSB} \quad \text{(EQ. 8)}$$

TABLE 16. CURRENT REGISTER, 04h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit 15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 17. POWER REGISTER, 03h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
WEIGHT	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 18. SHUNT VOLTAGE THRESHOLD REGISTER, 06h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	SMX6	SMX5	SMX4	SMX3	SMX2	SMX1	SMX0	Sign	SMN6	SMN5	SMN4	SMN3	SMN2	SMN1	SMN0
WEIGHT	-128	64	32	16	8	4	2	1	-128	64	32	16	8	4	2	1

TABLE 19. BUS VOLTAGE THRESHOLD REGISTER, 07h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	BMX7	BMX6	BMX5	BMX4	BMX3	BMX2	BMX1	BMX0	BMN7	BMN6	BMN5	BMN4	BMN3	BMN2	BMN1	BMN0
WEIGHT	128	64	32	16	8	4	2	1	128	64	32	16	8	4	2	1

TABLE 20. INTERRUPT STATUS REGISTER, 08h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	SMXW	SMNW	BMXW	BMNW
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 21. AUX CONTROL REGISTER, 09h

BIT	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	FORCEINTR	INTREN	ExtClkEn	ExtCLKDiv[5:0]					
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUS VOLTAGE THRESHOLD REGISTER 07h (READ/WRITE)

The V_{BUS} minimum and maximum threshold limits are set using one register. The V_{BUS} value readings range from 0V to 60V. Table 19 on page 18 shows the register configuration and bit weights for the V_{BUS} threshold register. BMX bits represent the upper limit threshold. BMN represents the lower threshold limit. Equation 9 is the calculation used to convert the V_{BUS} threshold binary value to decimal. Bit is the value of each bit set in the V_{BUS} threshold register. The value is either 1 or a 0. The weight of each bit is represented in Table 19. n is the bit number. The V_{BUS} voltage threshold LSB is 256mV.

$$Vb_{thresh} = \left[\sum_{n=0}^{7}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot VbThresh_{LSB} \quad \text{(EQ. 9)}$$

INTERRUPT STATUS REGISTER 08h (READ/WRITE)

The interrupt status register consists of a series of bit flags that indicate if an ADC reading has exceeded the readings respective limit. A 1 or high reading from a warning bit indicates the reading has exceeded the limit. To clear a warning, write a 1 or high to the set warning bit. Table 20 on page 18 shows the definition of the interrupt status register.

BMNW is the Bus voltage Minimum Warning. A “1” reading for this bit indicates the bus reading is below the bus voltage minimum threshold limit.

BMXW is the Bus voltage Maximum Warning. A “1” reading for this bit indicates the bus reading is above the bus voltage maximum threshold limit.

SMNW is the Shunt voltage Minimum Warning. A “1” reading for this bit indicates the shunt reading is below the shunt voltage minimum threshold limit.

SMXW is the Shunt voltage Maximum Warning. A “1” reading for this bit indicates the shunt reading is above the shunt voltage maximum threshold limit.

AUX CONTROL REGISTER 09h (READ/WRITE)

The Aux control register controls the functionality of the EXTCLK/INT pin of the ISL28022. Table 21 on page 18 shows the definition of the register.

FORCEINTR is the Force Interrupt bit. Programming a 1 to the bit will force a 0 or a low at the EXTCLK/INT pin.

INTREN is the Interrupt Enable bit. Programming a 1 to the bit will allow for a threshold measurement violation to set the state of the EXTCLK/INT pin. With the INTREN set, any flag set from the interrupt status register will change the state of the EXTCLK/INT pin from 1 to a 0.

EXCLKEN is the External Clock Enable bit. Setting the bit enables the external clock. This also changes the EXTCLK/INT pin from an output to an input. The internal oscillator will shut down when the bit is enabled.

EXTCLKDIV are the External Clock Divider bits. The bits control an internal clock divider that are useful for fast system clocks. The internal clock frequency from pin to chip is represented in Equation 10:

$$freq_{internal} = \frac{f_{EXTCLK}}{(EXTCLKDIV + 1) \cdot 2} \quad \text{(EQ. 10)}$$

f_{EXTCLK} is the frequency of the signal driven to the EXTCLK/INT pin. EXTCLKDIV is the decimal value of the clock divide bits.

Serial Interface

The ISL28022 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL28022 operates as a slave device in all applications.

The ISL28022 uses two bytes to transfer all reads and writes. All communication over the I^2C interface is conducted by sending the MSByte of each byte of data first, followed by the LSByte.

Protocol Conventions

For normal operation, data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 27). On power-up of the ISL28022, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL28022 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 27). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 27). A STOP condition at the end of a read operation or at the end of a write operation places the device in its standby mode.

SMBus Support

The ISL28022 supports SMBus protocol, which is a subset of the global I^2C protocol. SMBCLK and SMBDAT have the same pin functionality as the SCL and SDA pins, respectively. The SMBus operates at 100kHz.

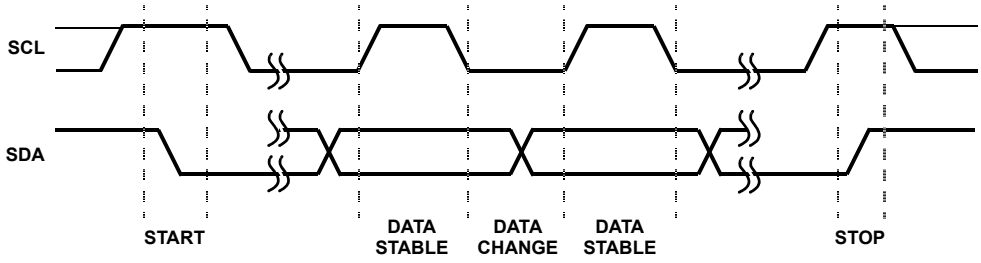


FIGURE 27. VALID DATA CHANGES, START AND STOP CONDITIONS

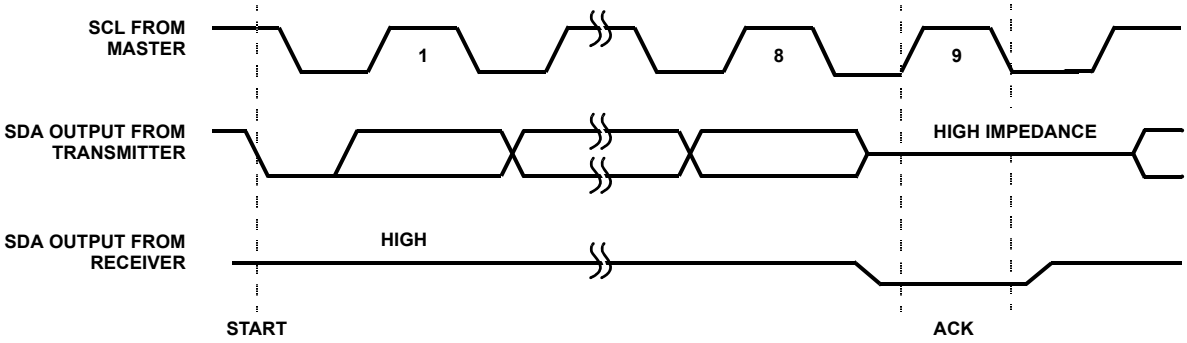


FIGURE 28. ACKNOWLEDGE RESPONSE FROM RECEIVER

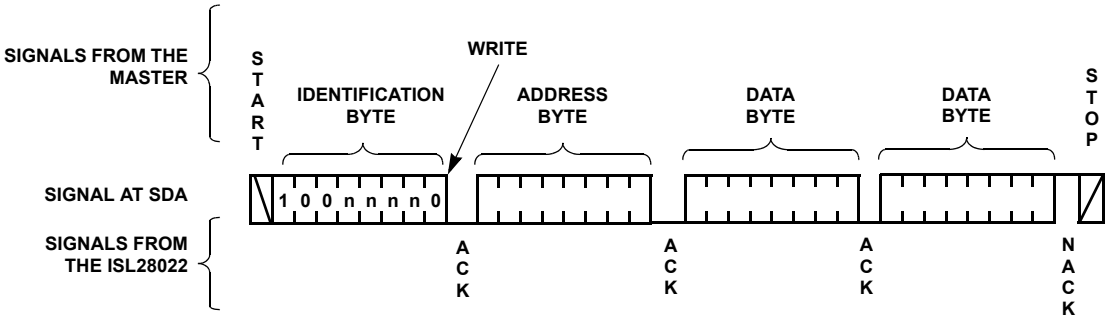


FIGURE 29. BYTE WRITE SEQUENCE (SLAVE ADDRESS INDICATED BY nnnn)

Device Addressing

Following a start condition, the master must output a slave address byte. The 7 MSBs are the device identifiers. The A0 and A1 pins control the bus address (these bits are shown in Table 22). There are 16 possible combinations depending on the A0/A1 connections. The last bit of the slave address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", a read operation is selected. A "0" selects a write operation (refer to Figure 29).

After loading the entire slave address byte from the SDA bus, the ISL28022 compares the loaded value to the internal slave address. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the slave byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the one word address byte, as shown in Figure 30.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the registers, the slave byte must be "100nnnnx" in both places.

TABLE 22. I^2C SLAVE ADDRESSES

A1	A0	SLAVE ADDRESS
GND	GND	1000 000
GND	VCC	1000 001
GND	SDA	1000 010
GND	SCL	1000 011
VCC	GND	1000 100
VCC	VCC	1000 101
VCC	SDA	1000 110
VCC	SCL	1000 111
SDA	GND	1001 000
SDA	VCC	1001 001
SDA	SDA	1001 010
SDA	SCL	1001 011
SCL	GND	1001 100
SCL	VCC	1001 101
SCL	SDA	1001 110
SCL	SCL	1001 111
Broadcast Address		0111 111

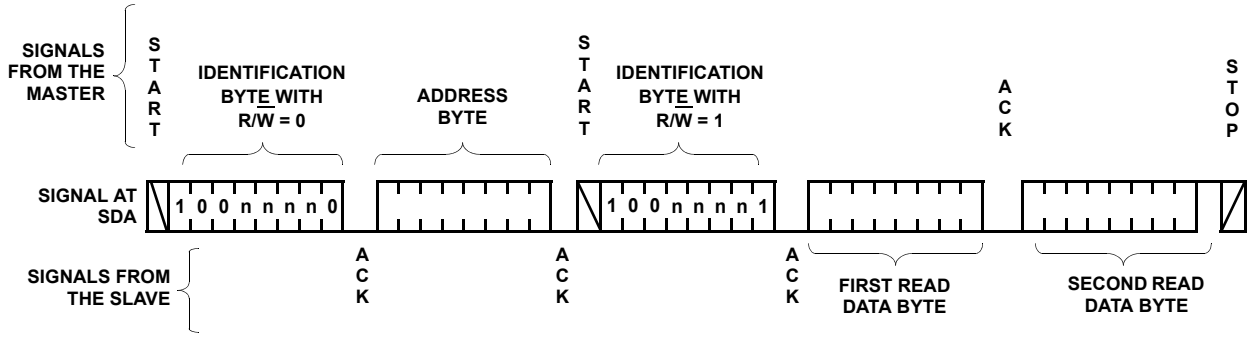


FIGURE 30. READ SEQUENCE (SLAVE ADDRESS SHOWN AS nnnn)

Write Operation

A write operation requires a START condition, followed by a valid identification byte, a valid address byte, two data bytes and a STOP condition. The first data byte contains the MSB of the data, the second contains the LSB. After each of the four bytes, the ISL28022 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A read operation consists of a three byte instruction, followed by two data bytes (see Figure 30 on page 21). The master initiates the operation issuing the following sequence: A START, the identification byte with the R/$\overline{W}$ bit set to “0”, an address byte, a second START and a second identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL28022 responds with an ACK. Then the ISL28022 transmits two data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of the first byte. The master terminates the read operation (issuing no ACK then a STOP condition) following the last bit of the second data byte (see Figure 30 on page 21).

The data bytes are from the memory location indicated by an internal pointer. This pointer’s initial value is determined by the address byte in the read operation instruction and increments by one during transmission of each pair of data bytes. The highest valid memory location is 09h, reads of addresses higher than that will not return useful data.

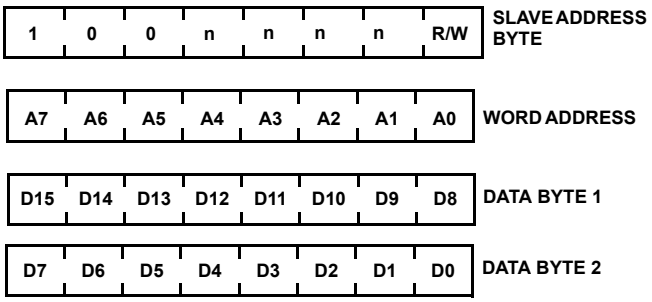


FIGURE 31. SLAVE ADDRESS, WORD ADDRESS AND DATA BYTES

Broadcast Addressing

The DPM has a feature that allows the user to configure the settings of all DPM chips at once. For example, a system has 16 DPM chips connected to an I^2C bus. A user can set the range or initiate a data acquisition in one I^2C data transaction by using a slave address of 0111 111. The broadcast feature saves time in configuring the DPM as well as measuring signal parameters in time synchronization. The broadcast should not be used for DPM read backs. This will cause all devices connected to the I^2C bus to talk to the master simultaneously.

I^2C Clock Speed

The device supports high-speed digital transactions up to 3.4Mbs. To access the high speed I^2C feature, a master byte code of 0000 1xxx is attached to the beginning of a standard frequency read/write I^2C protocol. The x in the master byte signifies a do not care state. X can either equal a 0 or a 1. The master byte code should be clocked into the chip at frequencies equal or less than 400kHz. The master code command configures the internal filters of the ISL28022 to permit data bit frequencies greater than 400kHz. Once the master code has been clocked into the device, the protocol for a standard read/write transaction is followed. The frequency at which the standard protocol is clocked in at can be as great as 3.4MHz. A stop bit at the end of a standard protocol will terminate the high speed transaction mode. Appending another standard protocol serial transaction to the data string without a stop bit, will resume the high speed digital transaction mode. Figure 32 illustrates the data sequence for the high speed mode.

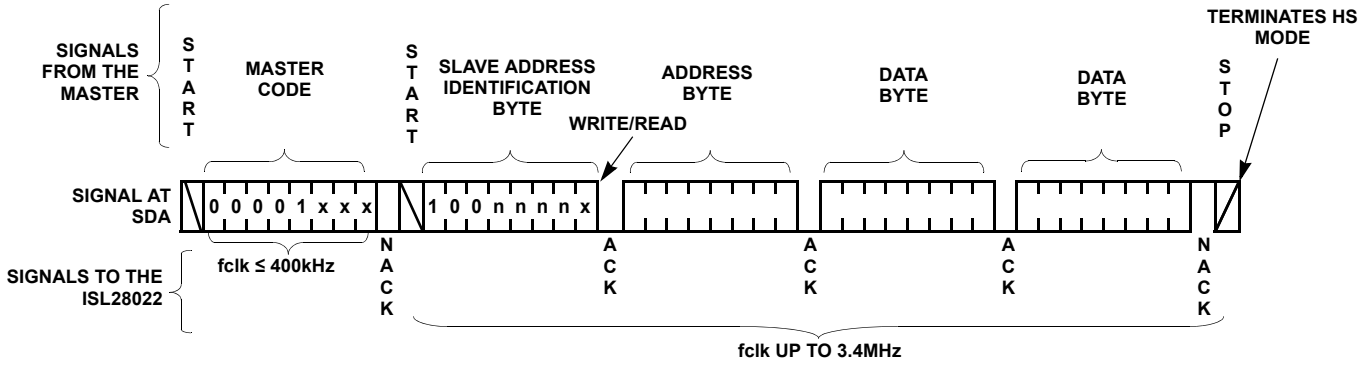


FIGURE 32. BYTE TRANSACTION SEQUENCE FOR INITIATING DATA RATES ABOVE 400kbs

Signal Integrity

The purity of the signal being measured by the ISL28022 is not always ideal. Environmental noise or noise generated from a regulator can degrade the measurement accuracy. The ISL28022 maintains a high CMRR ratio from DC to approximately 10kHz, as shown in Figure 33.

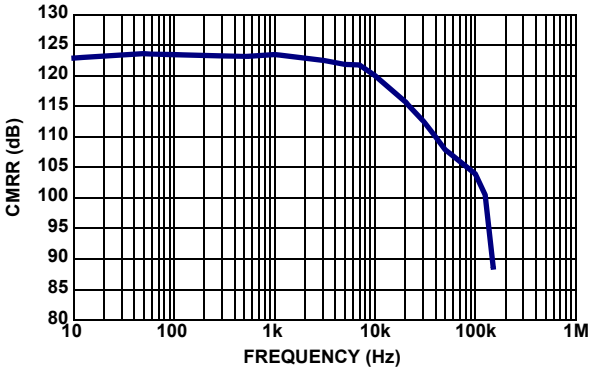


FIGURE 33. CMRR vs FREQUENCY

The CMRR vs Frequency graph best represents the response of the ISL28022 when an aberrant signal is applied to the circuit.

The graph was generated by shorting the ISL28022 input without any filtering and applying a 0V to 10V triangle wave to the Shunt inputs, VINP and VINM. The voltage shunt measurement was recorded for each frequency applied to the shunt input.

The CMRR can be improved by designing a filter stage before the ISL28022. The purpose of the filter stage is to attenuate the amplitude of the unwanted signal to the noise level of the ISL28022. Figure 34 is a simple filter example to attenuate unwanted signals.

C_{SH} and R_{SH} are single pole RC filters that differentially attenuate unwanted signals to the ISL28022. Most power monitoring applications require a shunt resistor to be low in value to measure large currents. For small shunt resistors, a large value capacitor is required to attenuate low frequency signals. Most large value capacitors are not offered in space saving packages. The corner frequency of the differential filter, C_{SH} and R_{SH}, should be designed for higher value frequency filtering.

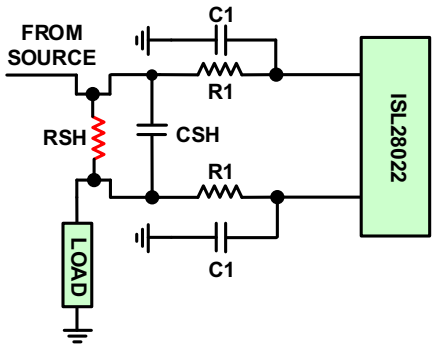


FIGURE 34. SIMPLIFIED FILTER DESIGN TO IMPROVE NOISE PERFORMANCE TO THE ISL28022

R_1 and C_1 for both inputs are single ended low pass filters. The value of the series resistor to the ISL28022 can be a larger value than the shunt resistor, R_{SH}. A larger series resistor to the input allows for a lower cutoff frequency filter design to the ISL28022. The ISL28022 can source up to 20µA of transient current in the measurement mode. The transient or switching offset current can be as large as 10µA. The switching offset current combined with the series resistance, R_1, creates an error offset voltage. A balance of the value of R_1 and the shunt measurement error should be achieved for this filter design.

The common-mode voltage of the shunt input stage ranges from 0V to 60V. The capacitor voltage rating for C_1 and C_{SH} should comply with the nominal voltage being applied to the input.

Measurement Stability vs Acquisition Time

The BADC and SADC bits within the Configuration register configures the conversion time and accuracy for the bus and shunt inputs, respectively. The faster the conversion time the less accuracy and more noise introduced into the measurement. Figure 35 is a graph that illustrates the shunt measurement variability versus a set SADC mode. The standard deviation of 2048 shunt V_{OS} measurements is used to quantify the measurement variability of each mode.

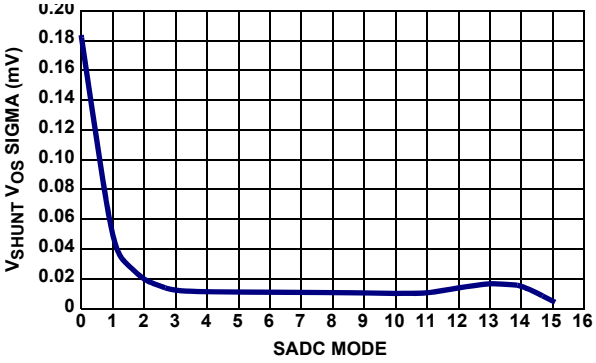


FIGURE 35. MEASUREMENT STABILITY vs SADC MODE

Fast Transients

A small isolation resistor placed between ISL28022 inputs and the source is recommended. In hot swap or other fast transient events, the amplitude of a signal can exceed the recommended operating voltage of the part due to the line inductance. The isolation resistor creates a low pass filter between the device and the source. The value of the isolation resistor should not be too large. A large value isolation resistor can effect the measurement accuracy. The offset current for shunt input can be as large as 10µA. The value of the isolation resistor combined with the offset current creates an error offset voltage at the shunt input. The input of the Bus channel is connected to the top of a precision resistor divider. The accuracy of the resistor divider determines the gain error of the Bus channel. The input resistance of the Bus channel is 600kΩ. Placing an isolation resistor of the 10Ω will change the gain error of the Bus channel by 0.0016%.

External Clock

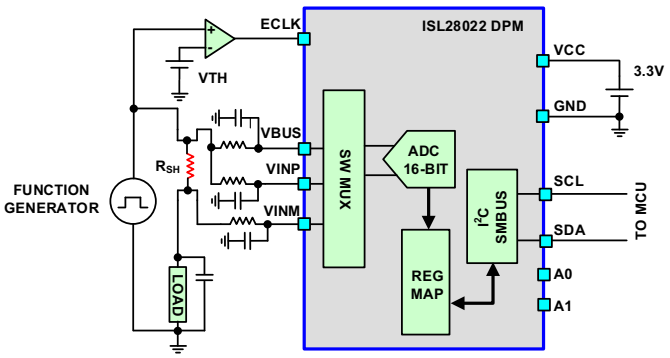


FIGURE 36. SIMPLIFIED SCHEMATIC OF THE ISL28022 SYNCHRONIZED TO A PWM SOURCE

An externally controlled clock allows measurements to be synchronized to an event that is time dependent. The event could be application generated, such as timing a current measurement to a charging capacitor in a switch regulator application or the event could be environmental. A voltage or current measurement may be susceptible to crosstalk from a controlled source. Instead of filtering the environmental noise from the measurement, another approach would be to synchronize the measurement to the source. The variability and accuracy of the measurement will improve.

The ISL28022 has the functionality to allow for synchronization to an external clock. The speed of the external clock combined with the choice of the internal chip frequency division value determines the acquisition times of the ADC. The internal system clock frequency is 500kHz. The internal system clock is also the ADC sampling clock. The acquisition times scale linearly from 500kHz. For example, an external clock frequency of 1MHz with a frequency divide setting of 2 results in acquisition times that equals the internal oscillator frequency when enabled. The internal clock frequency of the ISL28022 should not exceed 500kHz. The ADC modulator is optimized for frequencies of 500kHz and below. Operating internal clock frequencies above 500kHz result in measurement accuracy errors due to the modulator not having enough time to settle.

Suppose an external clock frequency of 1.0MHz is applied with a divide by 8 internal frequency setting, the system clock speed is 125kHz or 4x slower than internal system clock. The acquisition times for this example will increase by 4. For a S(B)ADC setting of 3, the ISL28022 will have an acquisition time of 2.032ms instead of 508µs.

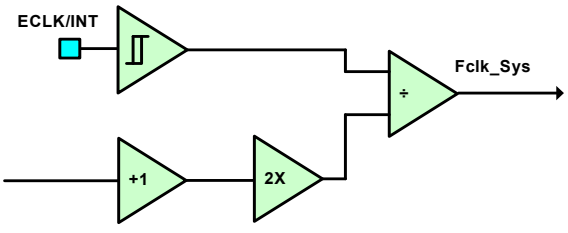


FIGURE 37. SIMPLIFIED INTERNAL BLOCK CONNECTION OF THE ECLK/INT PIN

The ECLK/INT pin connects to a buffer that drives a D-flip flop. Figure 37 illustrates a simple schematic of the ECLK/INT pin internal connection. The series of divide by 2 configured D-flip flops are controlled by the CLKDIV bits from the Aux Control Register. The buffer is a Schmitt triggered buffer. The bandwidth of the buffer is 4MHz. Figure 38 shows the bandwidth of the ECLK/INT pin.

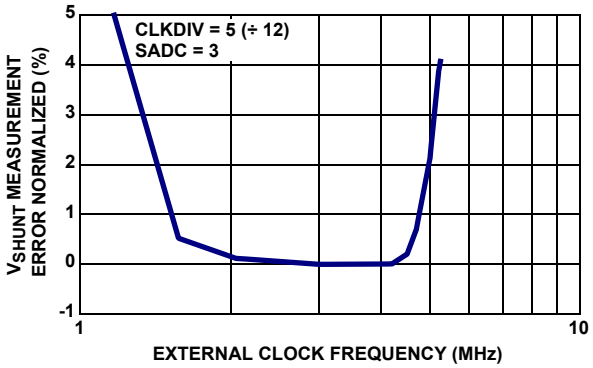


FIGURE 38. EXTERNAL CLOCK BANDWIDTH vs MEASUREMENT ACCURACY

The V_{SHUNT} measurement error degrades at ECLK frequencies above 4MHz. It is recommended that the ECLK does not exceed 4MHz. At ECLK frequencies below 2.5MHz or internal clock frequencies of 208kHz, the clock frequency to modulator is too slow allowing the charged capacitors to discharge due to parasitic leakages. The capacitor discharge results in a measurement error.

Over-Ranging

It is not recommended to operate the ISL28022 outside the set voltage range. In the event of measuring a shunt voltage beyond the maximum set range (320mV) and lower than the clamp voltage of the protection diode (1V), the measured output reading may be within the accepted range but will be incorrect.

Shunt Resistor Selection

In choosing a sense resistor, the following resistor parameters need to be considered: the resistor value, resistor temperature coefficient and resistor power rating.

The sense resistor value is a function of the full-scale voltage drop across the shunt resistor and the maximum current measured for the application. The ISL28022 has 4 voltage ranges that are controlled by programming the PGA bits within the configuration register. The PGA bits control the voltage range for the V_{SHUNT} input (VINP-VINM) of the ISL28022. Once the voltage range for the input is chosen and the maximum measurable current is known, the sense resistor value is calculated using Equation 11:

$$R_{sense} = \frac{V_{shunt\_range}}{Imeas_{Max}} \quad \text{(EQ. 11)}$$

In choosing a sense resistor, the sense resistor power rating should be taken into consideration. The physical size of a sense resistor is proportional to the power rating of the resistor. The maximum power rating for the measurement system is calculated as the V_{shunt_range} multiplied by the maximum

measurable current expected. The power rating equation is represented by Equation 12:

$$P_{res\_rating} = V_{shunt\_range} \cdot Imeas_{Max} \quad \text{(EQ. 12)}$$

A general rule of thumb is to multiply the power rating calculated in Equation 12 by 2. This allows the sense resistor to survive an event when the current passing through the shunt resistor is greater than the measurable maximum current. The higher the ratio between the power rating of the chosen sense resistor and the calculated power rating of the system (Equation 12), the less the resistor will heat up in high-current applications.

The Temperature Coefficient (TC) of the sense resistor directly degrades the current measurement accuracy. The surrounding temperature of the sense resistor and the power dissipated by the resistor will cause the sense resistor value to change. The change in resistor temperature with respect to the amount of current that flows through the resistor, is directly proportional to the ratio of the power rating of the resistor versus the power being dissipated. A change in sense resistor temperature results in a change in sense resistor value. Overall, the change in sense resistor value contributes to the measurement accuracy for the system. The change in a resistor value due to a temperature rise can be calculated using Equation 13:

$$\Delta R_{sense} = R_{sense} \cdot Rsense_{TC} \cdot \Delta Temperature \quad \text{(EQ. 13)}$$

ΔTemperature is the change in temperature in Celsius. $Rsense_{TC}$ is the temperature coefficient rating for a sense resistor. R_{sense} is the resistance value of the sense resistor at the initial temperature.

Table 23 is a shunt resistor reference table for select full-scale current measurement ranges ($Imeas_{Max}$). The table also provides the minimum rating for each shunt resistor.

TABLE 23. SHUNT RESISTOR VALUES AND POWER RATINGS FOR SELECT MEASURABLE CURRENT RANGES

R_{sense}/ P_{rating}	V_{SHUNT} RANGE (PGA SETTING)			
$Imeas_{Max}$	(PGA 00) 40mV	(PGA 01) 80mV	(PGA 10) 160mV	(PGA 11) 320mV
100µA	400Ω/4µW	800Ω/8µW	1.6kΩ/16µW	3.2kΩ/ 32µW
1mA	40Ω/40µW	80Ω/80µW	160Ω/160µW	320Ω/ 320µW
10mA	4Ω/400µW	8Ω/800µW	16Ω/1.6mW	32Ω/ 3.2mW
100mA	400mΩ/4mW	800mΩ/8mW	1.6Ω/16mW	3.2Ω/ 30mW
500mA	80mΩ/20mW	160mΩ/40mW	320mΩ/ 80mW	640mΩ/ 160mW
1A	40mΩ/40mW	80mΩ/80mW	160mΩ/ 160mW	320mΩ/ 320mW
5A	8mΩ/200mW	16mΩ/400mW	32mΩ/ 800mW	64mΩ/ 1.6W
10A	4mΩ/400mW	8mΩ/800mW	16mΩ/1.6W	32mΩ/ 3.2W
50A	0.8mΩ/2W	1.6mΩ/4W	3.2mΩ/8W	6.4mΩ/ 16W
100A	0.4mΩ/4W	0.8mΩ/8W	1.6mΩ/16W	3.2mΩ/ 32W
500A	0.08mΩ/20W	0.16mΩ/40W	0.32mΩ/80W	0.64mΩ/ 160W

It is often hard to readily purchase shunt resistor values for a desired measurable current range. Either the value of the shunt resistor does not exist or the power rating of the shunt resistor is too low. A means of circumventing the problem is to use two or more shunt resistors in parallel to set the desired current measurement range. For example, an application requires a full-scale current of 50A with a maximum voltage drop across the shunt resistor of 40mV. Table 23 shows this requires a sense resistor of 0.8mΩ, 2W resistor. Assume the power ratings and the shunt resistor values to choose from are 1mΩ/ 1W, 2mΩ/1W, and 4mΩ/1W.

Let's use a 1mΩ and a 4mΩ resistor in parallel to create the shunt resistor value of 0.8mΩ. Figure 39 shows an illustration of the shunt resistors in parallel.

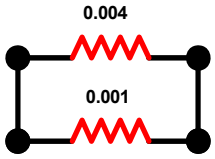


FIGURE 39. A SIMPLIFIED SCHEMATIC ILLUSTRATING THE USE OF TWO SHUNT RESISTORS TO CREATE A DESIRED SHUNT VALUE

The power to each shunt resistor should be calculated before calling a solution complete. The power to each shunt resistor is calculated using Equation 14:

$$P_{shuntRes} = \frac{V_{shunt\_range}^{2}}{R_{sense}} \quad \text{(EQ. 14)}$$

The power dissipated by the 1mΩ resistor is 1.6W. 400mW is dissipated by the 4mΩ resistor. 1.6W exceeds the rating limit of 1W for the 1mΩ sense resistor. Another approach would be to use three shunt resistors in parallel as illustrated in Figure 40.

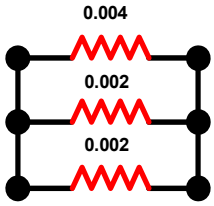


FIGURE 40. INCREASING THE NUMBER OF SHUNT RESISTORS IN PARALLEL TO CREATE A SHUNT RESISTOR VALUE REDUCES THE POWER DISSIPATED BY EACH SHUNT RESISTOR

Using Equation 14 on page 25, the power dissipated to each shunt resistor yields 0.8W for the 2mΩ shunt resistors and 0.4W for the 4mΩ shunt resistor. All shunt resistors are within the specified power ratings.

Lossless Current Sensing (DCR)

A DCR sense circuit is an alternative to a sense resistor. The DCR circuit utilizes the parasitic resistance of an inductor to measure the current to the load. A DCR circuit remotely measures the current through an inductor. The lack of components in series with the regulator to the load makes the circuit lossless.

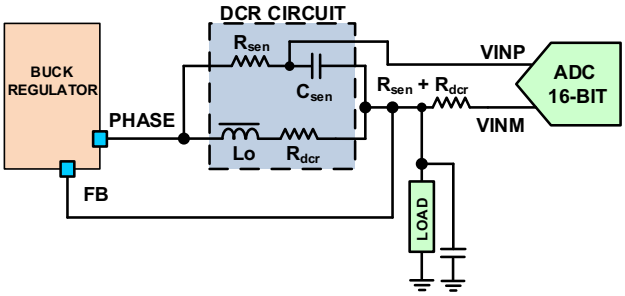


FIGURE 41. A SIMPLIFIED CIRCUIT EXAMPLE OF A DCR

A properly matched DCR circuit has an equivalent circuit seen by the ADC equals to R_{dcr} in Figure 41. Before deriving the transfer function between the inductor current and voltage seen by the ISL28022, let's review the definition of an inductor and capacitor in the Laplacian domain.

$$X_c(f) = \frac{1}{j\cdot\omega(f)\cdot C} \qquad X_L(f) = j\cdot\omega(f)\cdot L \qquad \text{(EQ. 15)}$$

X_c is the impedance of a capacitor related to the frequency and X_L is the impedance of an inductor related to frequency. ω equals to 2*π*f. f is the chop frequency dictated by the regulator. Using Ohms law, the voltage across the DCR circuit in terms of the current flowing through the inductor is defined in Equation 16.

$$V_{dcr}(f) = \left(R_{dcr} + j\cdot\omega(f)\cdot L\right)\cdot i_L \qquad \text{(EQ. 16)}$$

In Equation 16, R_{dcr} is the parasitic resistance of the inductor. The voltage drop across the inductor (Lo) and the resistor (R_{dcr}) circuit is the same as the voltage drop across the resistor (R_{sen}) and the capacitor (C_{sen}) circuit. Equation 17 defines the voltage across the capacitor (V_{csen}) in terms of the inductor current (I_L).

$$V_c(F) = \left[\frac{\left(j\cdot\omega(f)\cdot L + R_{dcr}\right)}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}}\right]\cdot I_L = R_{dcr}\cdot\left[\frac{\left[1 + \frac{(j\cdot w(f)\cdot L)}{R_{dcr}}\right]}{1 + j\cdot\omega(f)\cdot C_{sen}\cdot R_{sen}}\right]\cdot I_L$$

(EQ. 17)

The relationship between the inductor load current (I_L) and the voltage across capacitor simplifies if the following component selection holds true:

$$\frac{L}{R_{dcr}} = C_{sen}\cdot R_{sen} \qquad \text{(EQ. 18)}$$

If Equation 18 hold true, the numerator and denominator of the fraction in Equation 17 cancels reducing the voltage across the capacitor to the equation represented in Equation 19.

$$V_c = R_{dcr}\cdot i_L \qquad \text{(EQ. 19)}$$

Most inductor datasheets will specify the average value of the R_{dcr} for the inductor. R_{dcr} values are usually sub 1mΩ with a tolerance averaging 8%. Common chip capacitor tolerances average to 10%.

Inductors are constructed out of metal. Metal has a high temperature coefficient. The temperature drift of the inductor value could cause the DCR circuit to be untuned. An untuned circuit results in inaccurate current measurements along with a chop signal bleeding into the measurement. To counter the temperature variance, a temperature sensor may be incorporated into the design to track the change in component values.

A DCR circuit is good for gross current measurements. As discussed, inductors and capacitors have high tolerances and are temperature dependent which will result in less than accurate current measurements.

In Figure 41, there is a resistor in series with the ISL28022 negative shunt terminal, VINM, with the value of R_{sen} + R_{dcr}. The resistor's purpose is to counter the effects of the bias current from creating a voltage offset at the input of the ADC.

Layout

The layout of a current measuring system is equally important as choosing the correct sense resistor and the correct analog converter. Poor layout techniques can result in severed traces, signal path oscillations, magnetic contamination, which all contribute to poor system performance.

TRACE WIDTH

Matching the current carrying density of a copper trace with the maximum current that will pass through is critical in the performance of the system. Neglecting the current carrying capability of a trace will result in a large temperature rise in the trace and the loss in system efficiency due to the increase in resistance of the copper trace. In extreme cases, the copper

trace could be severed because the trace could not pass the current. The current carrying capability of a trace is calculated using Equation 20:

$$\text{Trace}_{\text{width}} = \frac{\left(\frac{\text{Imax}}{k \cdot \Delta T^{0.44}}\right)^{\frac{1}{0.725}}}{\text{Trace}_{\text{Thickness}}} \quad \text{(EQ. 20)}$$

I_{max} is the largest current expected to pass through the trace. ΔT is the allowable temperature rise in Celsius when the maximum current passes through the trace. $\text{Trace}_{\text{Thickness}}$ is the thickness of the trace specified to the PCB fabricator in mils. A typical thickness for general current carrying applications (<100mA) is 0.5oz copper or 0.7mils. For larger currents, the trace thickness should be greater than 1.0oz or 1.4mils. A balance between thickness, width and cost needs to be achieved for each design. The coefficient k in Equation 20 changes depending on the trace location. For external traces, the value of k equals 0.048 while for internal traces the value of k reduces to 0.024. The k values and Equation 20 are stated per the ANSI IPC-2221(A) standards.

TRACE ROUTING

It is always advised to make the distance between voltage source, sense resistor and load as close as possible. The longer the trace length between components will result in voltage drops between components. The additional resistance will reduce the efficiency of a system.

The bulk resistance, ρ, of copper is 0.67µΩ/in or 1.7µΩ/cm at +25°C. The resistance of trace can be calculated from Equation 21:

$$R_{\text{trace}} = \rho \cdot \frac{\text{Trace}_{\text{length}}}{\text{Trace}_{\text{width}} \cdot \text{Trace}_{\text{thickness}}} \quad \text{(EQ. 21)}$$

Figure 42 illustrates each dimension of a trace.

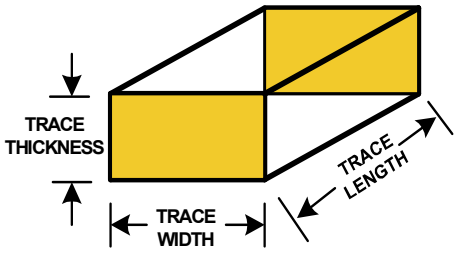


FIGURE 42. ILLUSTRATION OF THE TRACE DIMENSIONS FOR A STRIP LINE TRACE

For example, assume a trace has 2oz of copper or 2.8mil thickness, a width of 100mil and a length of 0.5in. Using Equation 21, the resistance of the trace is approximately 2mΩ. Assume 1A of current is passing through the trace. A 2mV voltage drop would result from trace routing.

Current flowing through a conductor will take the path of least resistance. When routing a trace, avoid orthogonal connections for current bearing traces.

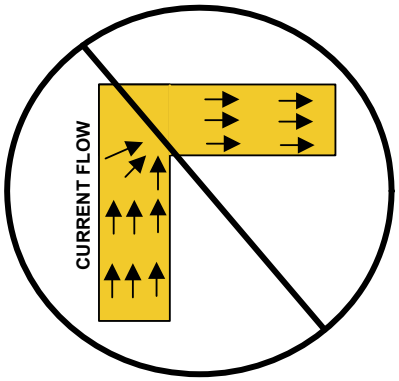


FIGURE 43. AVOID ROUTING ORTHOGONAL CONNECTIONS FOR TRACES THAT HAVE HIGH CURRENT FLOWS

Orthogonal routing for high current flow traces will result in current crowding, localized heating of the trace and a change in trace resistance (see Figure 43).

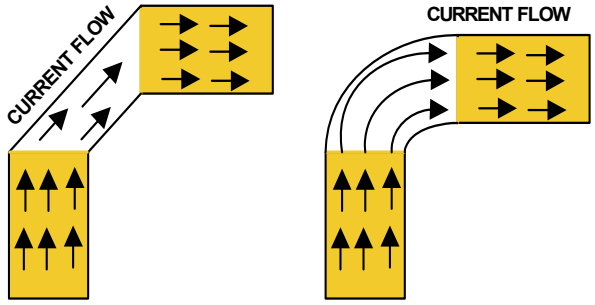


FIGURE 44. USE ARCS AND 45 DEGREE TRACES TO SAFELY ROUTE TRACES WITH LARGE CURRENT FLOWS

The utilization of arcs and 45° traces in routing large current flow traces will maintain uniform current flow throughout the trace. Figure 44 illustrates the routing technique.

CONNECTING SENSE TRACES TO THE CURRENT SENSE RESISTOR

Ideally, a 4 terminal current sense resistor would be used as the sensing element. Four terminal sensor resistors can be hard to find in specific values and in sizes. Often a two terminal sense resistor is designed into the application.

Sense lines are high impedance by definition. The connection point of a high impedance line reflects the voltage at the intersection of a current bearing trace and a high impedance trace. The high impedance trace should connect at the intersection where the sense resistor meets the landing pad on the PCB. The best place to make current sense line connection is on the inner side of the sense resistor footprint. The illustration of the connection is shown in Figure 45 on page 28. Most of the current flow is at the outer edge of the footprint. The current ceases at the point the sense resistor connects to the landing pad. Assume the sense resistor connects at the middle of the each landing pad, this leaves the inner half of the each landing pad with little current flow. With little current flow, the inner half of each landing pad is classified as high impedance and perfect for a sense connection.

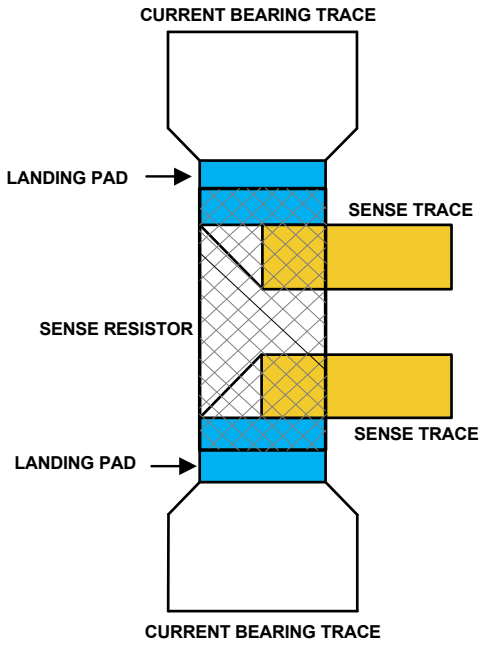
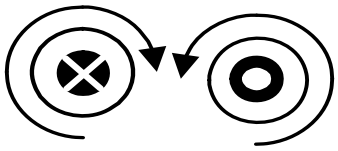


FIGURE 45. CONNECTING THE SENSE LINES TO A CURRENT SENSE RESISTOR

Current sense resistors are often smaller than the width of the traces that connect to the footprint. The trace connecting to the footprint is tapered at a 45° angle to control the uniformity of the current flow.

MAGNETIC INTERFERENCE

The magnetic field generated from a trace is directly proportional to the current passing through the trace and the distance from the trace the field is being measured at. Figure 46 illustrates the direction the magnetic field flows versus current flow.



$$B = \frac{\mu_o \cdot I}{2 \cdot \pi \cdot r}$$

FIGURE 46. THE CONDUCTOR ON THE LEFT SHOWS THE MAGNETIC FIELD FLOWING IN A CLOCKWISE DIRECTION FOR CURRENTS FLOWING INTO THE PAGE. A CURRENT FLOW OUT OF THE PAGE HAS A COUNTER CLOCKWISE MAGNETIC FLOW

The equation in Figure 46 determines the magnetic field, B, the trace generates in relation to the current passing through the trace, I, and the distance the magnetic field is being measured from the conductor, r. The permeability of air, μ_o, is $4\pi*10^{-7}$ H/m.

When routing high-current traces, avoid routing high impedance traces in parallel with high-current bearing traces. A means of limiting the magnetic interference from high-current traces is to closely route the paths connected to and from the sense resistor. The magnetic fields will cancel outside the two traces and add between the two traces. Figure 47 illustrates a layout that is less sensitive to magnetic field interference.

If possible, do not cross traces with high-current. If a trace crossing cannot be avoided, cross the trace in an orthogonal manor and the furthest layer from the current bearing trace. The interference from the current bearing trace will be limited.

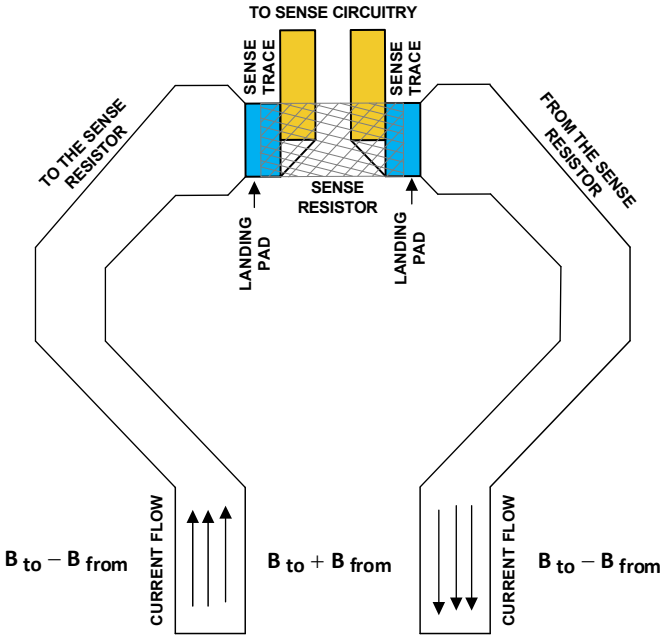


FIGURE 47. CLOSELY ROUTED TRACES THAT CONNECT TO THE SENSE RESISTOR REDUCES THE MAGNETIC INTERFERENCE SOURCED FROM THE CURRENT FLOWING THROUGH THE TRACES

A Trace as a Sense Resistor

In previous sections, the resistance and the current carrying capabilities of a trace were discussed. In high current sense applications, a design may utilize the resistivity of a current sense trace as the sense resistor. This section will discuss how to design a sense resistor from a copper trace.

Suppose an application needs to measure current up to 200A. The design requires the least amount of voltage drop for maximum efficiency. The full-scale voltage range of 40mV (PGA 00) is chosen. From Ohms law, the sense resistor is calculated to be 200µΩ. The power rating of the resistor is calculated to be 8W. Assume the PCB trace thickness of the board equals 2oz/2.8mils and the maximum temperature rise of the trace is 20°C. Using Equation 20 on page 27, the calculated trace width is 2.192in. The trace width, thickness and the desired sense resistor value is known. Utilizing Equation 21 on page 27, the trace length is calculated to be 1.832in.

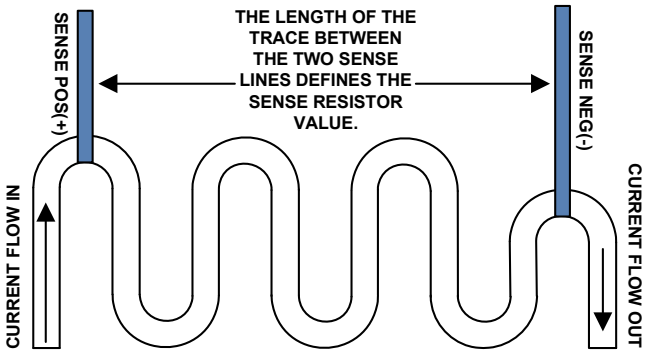


FIGURE 48. ILLUSTRATES A LAYOUT EXAMPLE OF A CURRENT SENSE RESISTOR MADE FROM A PCB TRACE

Figure 48 illustrates a layout example of a current sense resistor defined by a PCB trace. The serpentine pattern of the resistor reduces current crowding as well as limiting the magnetic interference caused by the current flowing through the trace.

The width of the trace in Figure 48 illustration would equal 2.192in and the length between the sense lines equals 1.832in.

The width of the resistor is long for some applications. A means of shortening the trace width is to connect two traces in parallel. For calculation ease, assume the resistive traces are routed on the outside layers of a PCB. Using Equations 20 and 21 on page 27, the width of the trace is reduced from 2.192in to 1.096in.

When using multiple layers to create a trace resistor, use multiple vias to keep the trace potentials between the two conductors the same. Vias are highly resistive compared to a copper trace. Multiple vias should be employed to lower the voltage drop due to current flowing through resistive vias. Figure 49 illustrates a layout technique for a multiple layered trace sense resistor.

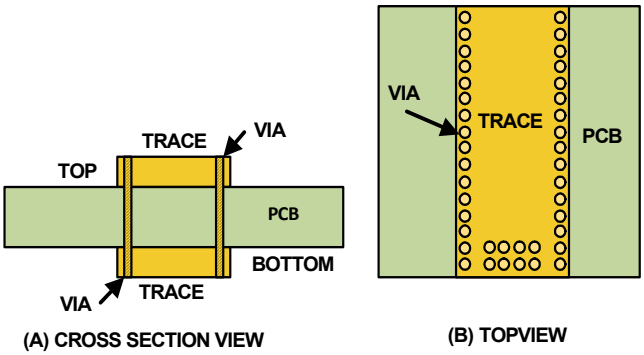


FIGURE 49. ILLUSTRATES A LAYOUT EXAMPLE OF A MULTIPLE LAYER TRACE RESISTOR

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
February 4, 2016	FN8386.8	Changed the Polarity of the CNVR bit from High to Low when the ADC is making a conversion. See section "CNVR: Conversion Ready (Bit 1)" on page 17 Changed in "Write Operation" on page 22 the description of the first byte of data sent to the ISL28022 from LSB to MSB. The second byte of data was changed from MSB to LSB. In Figure 32 on page 22, added an ACK to the diagram before the repeat start.
October 2, 2015	FN8386.7	Changed in Table 15 on page 16, Bit D0 from "FS0" to "0". Added statement in number 3 (second to the last sentence of "Calibration Register 05h (Read/Write)" on page 17, which reads "The calibration value..."
June 17, 2015	FN8386.6	Added Related Literature section on page 1. Added DPM Portfolio Comparison table on page 5. Removed Typical Applications section and made into an application note (AN1955).
February 20, 2015	FN8386.5	Electrical Specifications table on page 7- DC accuracy under Test Conditions: Updated VSENSE from ±300mV to ±320mV. Table 5 on page 14: Changed in range (mV) column from ±300 to ±320. Table 8 on page 16 updated "FULL-SCALE in title from ±300mV to ±320mV. Equation 1 on page 17: Changed n=0 to n=2. Calibration Register 05h (Read/Write) section on page 17 above equation 2, changed range: (300mV, 160mV, 80mV and 40mV) to (320mV, 160mV, 80mV and 40mV). Over-ranging section on page 24: Updated maximum set range from (300mV) to (320mV). Table 22 on page 24 changed PG11 from 300mV to 320mV. Point Of Load Power Monitor section on page 29: Changed shunt voltage from 300mV to 320mV. Equation 22 on page 28: Changed value from 0.30 to 0.32. page 31 updated V_{shunt} range from 300mV to 320mV.
June 9, 2014	FN8386.4	Equation 17 on page 26 added I_L before = R_{dcr} Figure 42 on page 27 changed "Of a Strip" to "For a Strip" Figure 47 on page 28 changed "Current flow" to "A current flow" Last sentence in paragraph following Figure 46 on page 28 and second sentence in paragraph under Equation 28 on page 32 changed "10^{7}" to "10^{-7}"
April 17, 2014	FN8386.3	Text revisions done in section "Signal Integrity" on page 23. Added section "Lossless Current Sensing (DCR)" on page 26 and "Monitoring MultiCell Battery Levels Using the ISL28022 Broadcast Command" on page 36. Updated the Ordering Information on page 3 by removing R-spec parts.
October 10, 2013	FN8386.2	Added sections from "Shunt Resistor Selection" on page 24 to "An Efficiency Measurement Using the ISL28022 Broadcast Feature" on page 35.
April 26, 2013	FN8386.1	Added R-spec parts to ordering information and updated verbiage in About Intersil.
April 16, 2013	FN8386.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

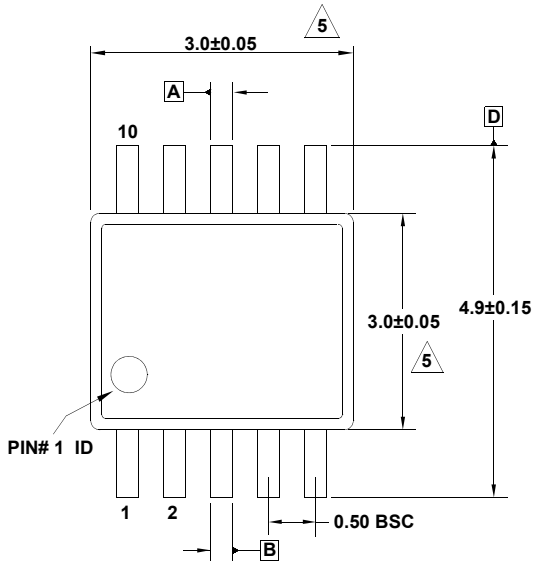
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

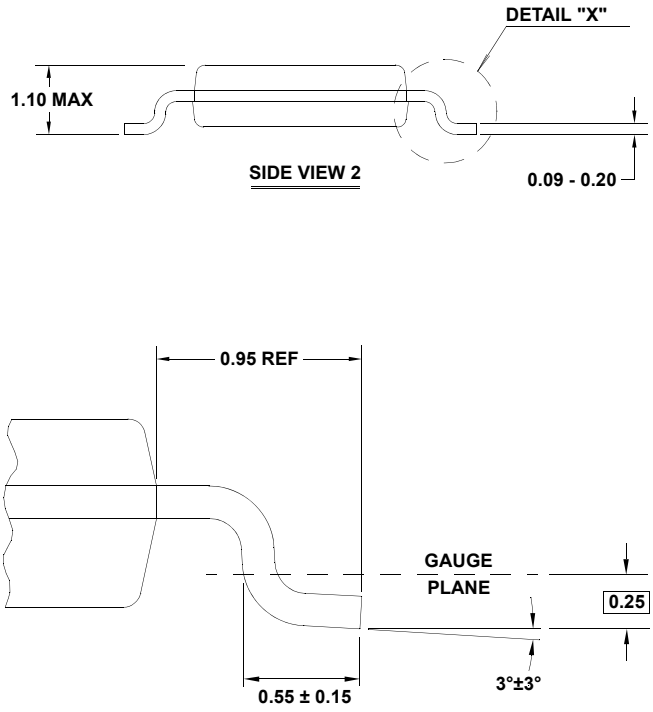
M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

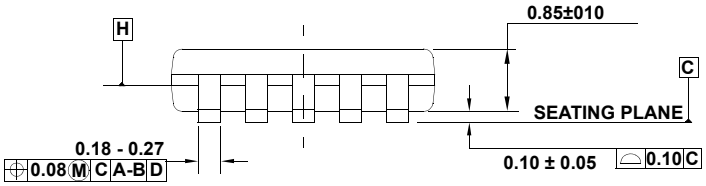
Rev 1, 4/12



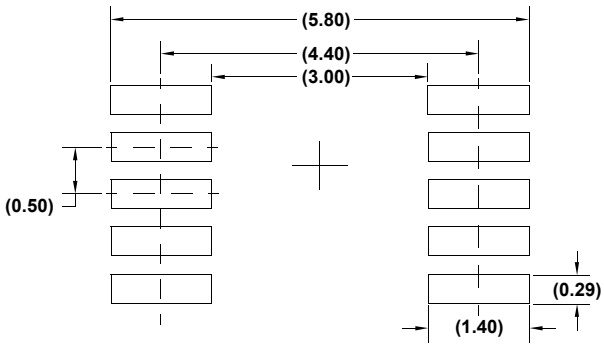
TOP VIEW



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.