ISL28118M

40V Extended Temperature Range, Precision Single-Supply, Rail-to-Rail Output, Operational Amplifier

FN7858
Rev 1.00
March 7, 2014

The ISL28118M is a single, low-power precision amplifier optimized for single-supply applications over the extended temperature range of -55°C to +125°C. This device features a common mode input voltage range extending to 0.5V below the V- rail, a rail-to-rail differential input voltage range for use as a comparator, and rail-to-rail output voltage swing, which makes it ideal for single-supply applications where input operation at ground is important.

The ISL28118M features low power, low offset voltage, and low temperature drift, making it the ideal choice for applications requiring both high DC accuracy and AC performance. The op amp is designed to operate over a single supply range of 3V to 40V or a split supply voltage range of +1.8V/-1.2V to ±20V. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications include precision instrumentation, data acquisition, precision power supply controls, and industrial controls.

The ISL28118M is offered in the 8 Ld MSOP package and operate over the extended temperature range of -55°C to +125°C.

Features

- Rail-to-rail output . . . . <10mV
- Below-ground (V-) input capability to -0.5V
- Rail-to-rail input differential voltage range for comparator applications
- Single-supply range . . . . 3V to 40V
- Low current consumption 850µA
- Low noise voltage. . . . . 5.6nV/√Hz
- Low noise current. . . . . 355fA/√Hz
- Low input offset voltage . . . . 150µV Max.
- Superb offset voltage temperature drift. . . . 1.2µV/°C, Max.
- Operating temperature range. . . . .-55°C to +125°C
- No phase reversal

Applications

- Precision instruments
- Medical instrumentation
- Data acquisition
- Power supply control
- Industrial process control

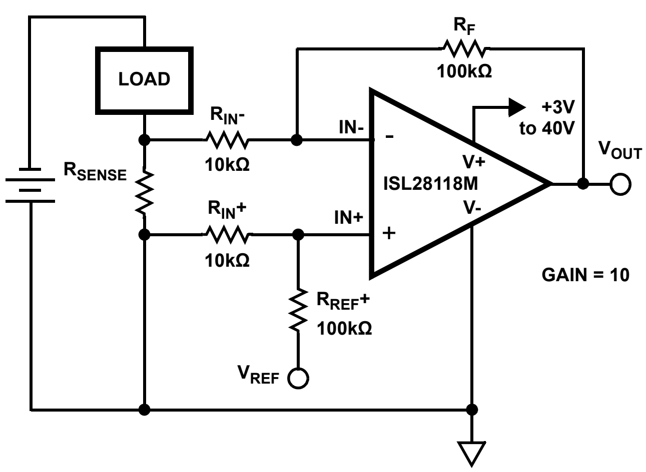

FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, LOW-SIDE CURRENT SENSE AMPLIFIER

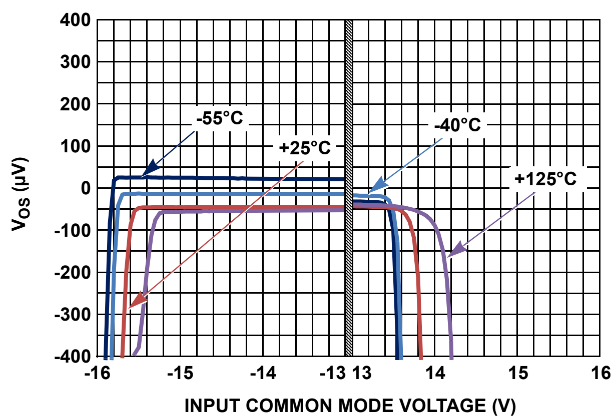

FIGURE 2. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, -40°C to +125°C, V_S = ±15V

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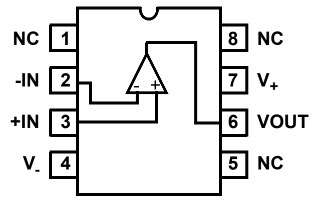
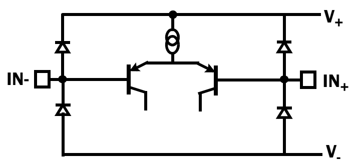
Pin Configurations

ISL28118M
(8 LD MSOP)
TOP VIEW

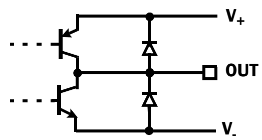


Pin Descriptions

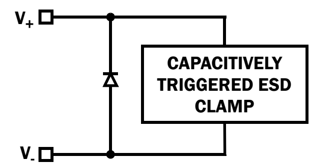
ISL28118M (8 LD MSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	+IN	1	Amplifier A non-inverting input
2	-IN	1	Amplifier A inverting input
6	VOUT	2	Amplifier A output
4	V_-	3	Negative power supply
7	V_+	3	Positive power supply
1, 5, 8	NC	-	No Connect



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28118MUZ	8118M	-55 to +125	8 Ld MSOP	M8.118B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL28118M. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . .42V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Voltage . . . . .42V or V_- - 0.5V to V_+ + 0.5V
Max/Min Input Current . . . . ±20mA
Output Short-Circuit Duration (1 output at a time) . . . . Indefinite
ESD Tolerance
- Human Body Model (Tested per JESD22-A114F). 3kV
- Machine Model (Tested per JESD22-A115-A). 300V
- Charged Device Model (Tested per CDM-22CI0ID). 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld MSOP Package (Notes 4, 5)	165	57

Storage Temperature Range. . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . .+150°C
Supply Voltage . . . . 3V (+1.8V/-1.2V) to 40V (±20V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications, V_S ±15

V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage		-150	25	150	µV
			-270		**270**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient		**-1.2**	**0.2**	**1.2**	µV/°C
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		118		dB
		V_{CM} = V_- to V_+ -1.8V	102	118		dB
			97			dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	109	124		dB
			105			dB
A_{VOL}	Open-Loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground	120	136		dB
			114			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ			70	mV
					85	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ			110	mV
					120	mV
I_S	Supply Current/Amplifier	R_L = Open		0.85	1.2	mA
					1.6	mA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		16		mA

Electrical Specifications, V_S ±15

V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		28		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**3**		**40**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		4		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz, V_S = ±18V		8.5		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
in	Current Noise Density	f = 1kHz, V_S = ±18V		355		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}		±1.2		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs

Electrical Specifications, V_S ±5V

V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage		-150	25	150	µV
			-270		**270**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient		**-1.2**	**0.2**	**1.2**	µV/°C
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		119		dB
		V_{CM} = V_- to V_+ -1.8V	101	117		dB
			96			dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, V_{CMIR} = Valid Input Voltage	108	124		dB
			103			dB

Electrical Specifications, V_S ±5V V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
A_{VOL}	Open-Loop Gain	V_O = -3V to +3V, R_L = 10kΩ to ground	120	132		dB
			110			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 10kΩ			38	mV
					45	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 10kΩ			65	mV
					70	mV
I_S	Supply Current/Amplifier	R_L = Open		0.85	1.1	mA
					1.4	mA
I_{SC+}	Output Short Circuit Source Current	R_L = 10Ω to V_-		13		mA
I_{SC-}	Output Short Circuit Sink Current	R_L = 10Ω to V_+		20		mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV$_{P-P}$; R_L = 2k		3.2		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		320		nV$_{P-P}$
e_n	Voltage Noise Density	f = 10Hz		9		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		5.7		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		5.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		5.5		nV/√Hz
in	Current Noise Density	f = 1kHz		380		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		±1		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV$_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV$_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 4V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		4		µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

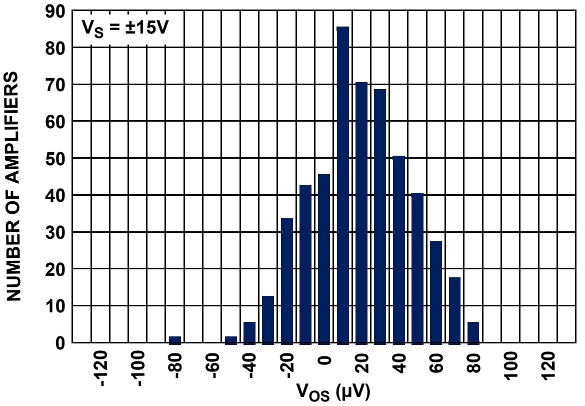


FIGURE 3. ISL28118M INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±15V

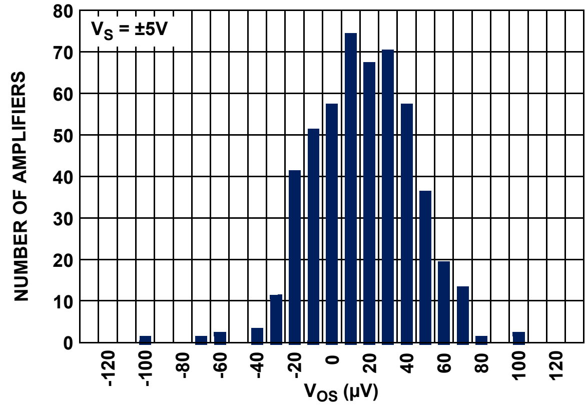


FIGURE 4. ISL28118M INPUT OFFSET VOLTAGE DISTRIBUTION, V_S = ±5V

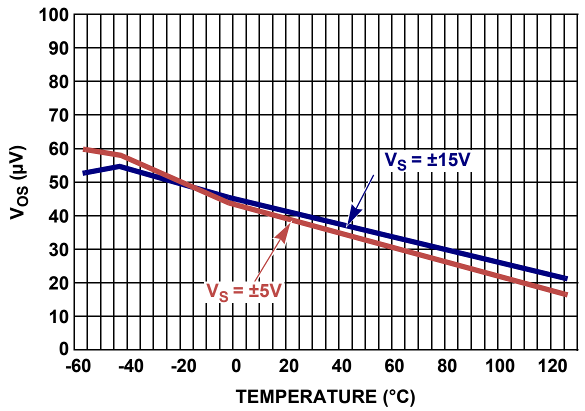


FIGURE 5. V_{OS} vs TEMPERATURE

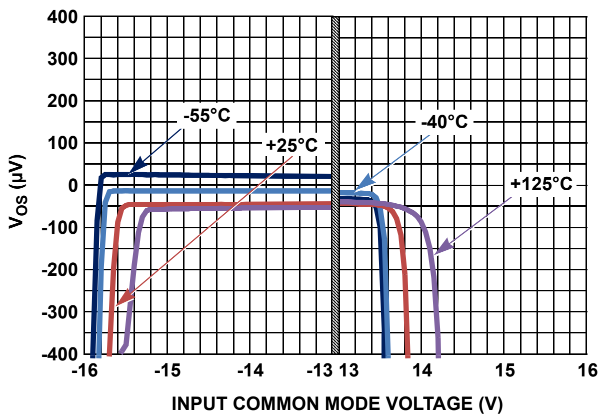


FIGURE 6. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, -55°C to +125°C, V_S = ±15V

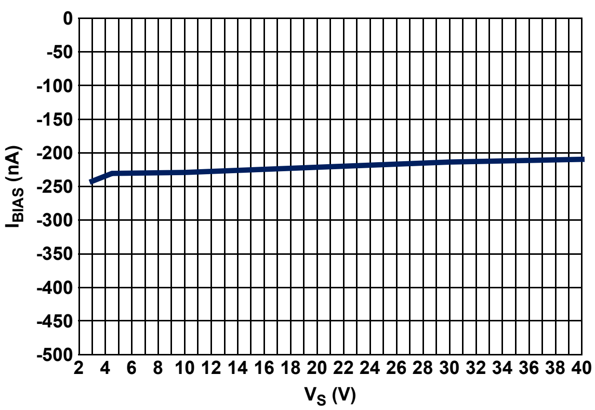


FIGURE 7. I_{BIAS} vs V_S

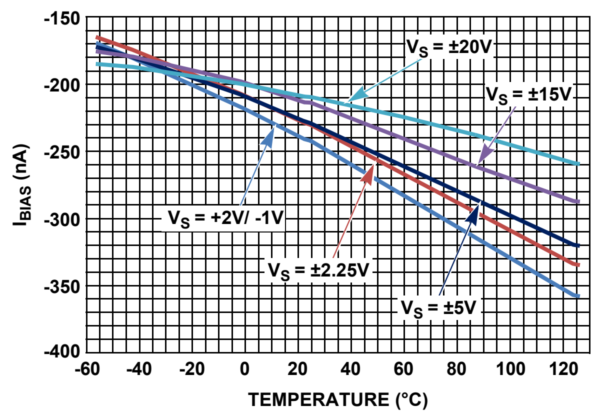


FIGURE 8. I_{BIAS} vs TEMPERATURE vs SUPPLY

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

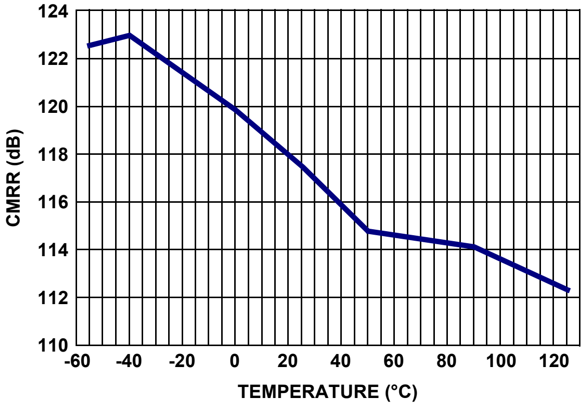


FIGURE 9. ISL28118M CMRR vs TEMPERATURE, V_S = ±15V

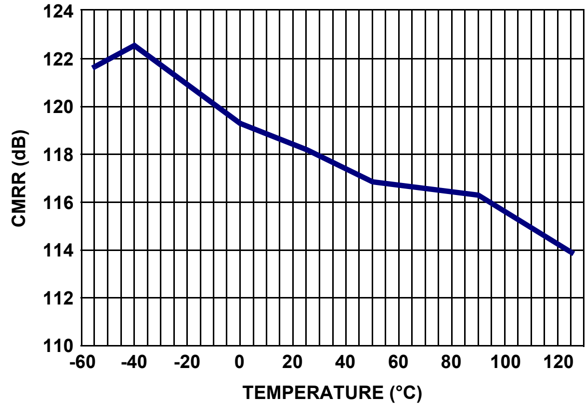


FIGURE 10. ISL28118M CMRR vs TEMPERATURE, V_S = ±5V

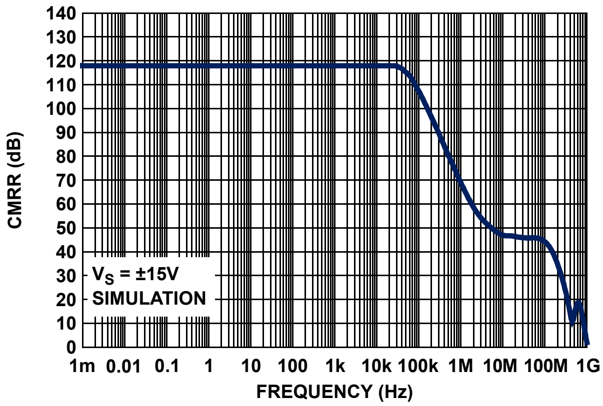


FIGURE 11. CMRR vs FREQUENCY, V_S = ±15V

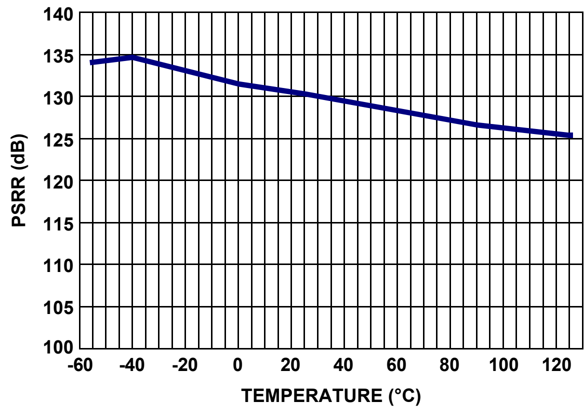


FIGURE 12. PSRR vs TEMPERATURE, V_S = ±15V

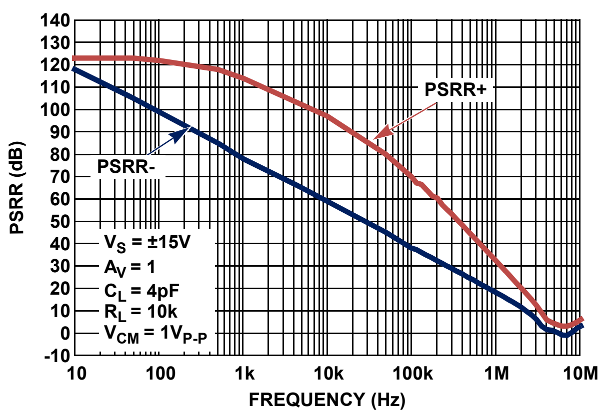


FIGURE 13. PSRR vs FREQUENCY, V_S = ±15V

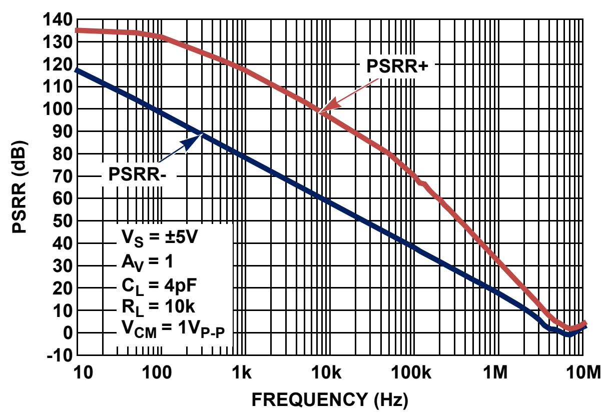


FIGURE 14. PSRR vs FREQUENCY, V_S = ±5V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

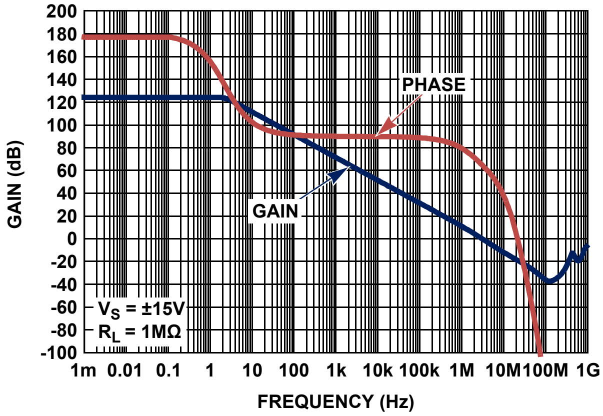


FIGURE 15. OPEN-LOOP GAIN, PHASE vs FREQUENCY, V_S = ±15V

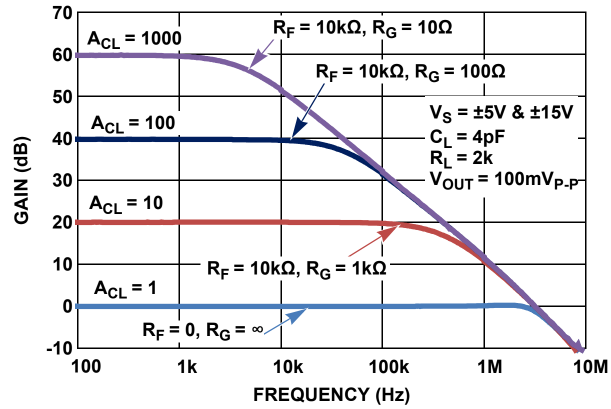


FIGURE 16. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

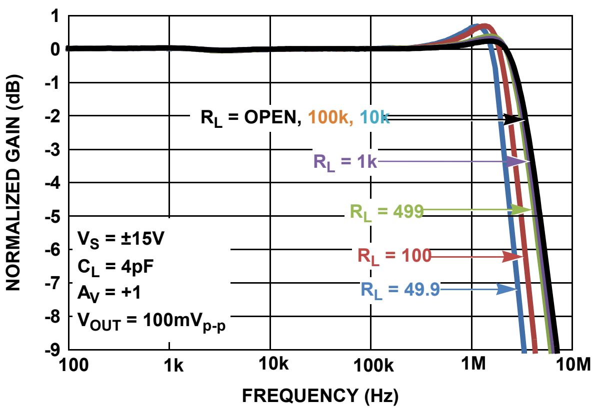


FIGURE 17. GAIN vs FREQUENCY vs R_L, V_S = ±15V

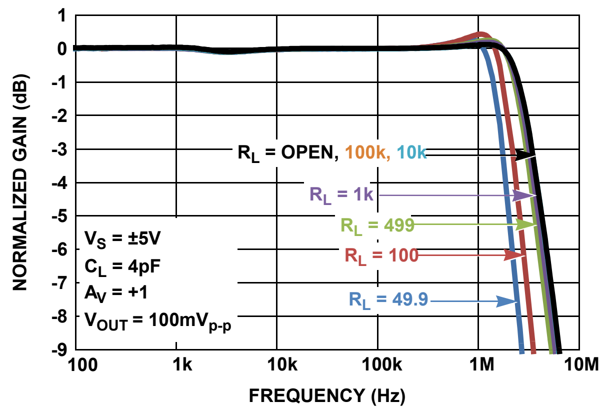


FIGURE 18. GAIN vs FREQUENCY vs R_L, V_S = ±5V

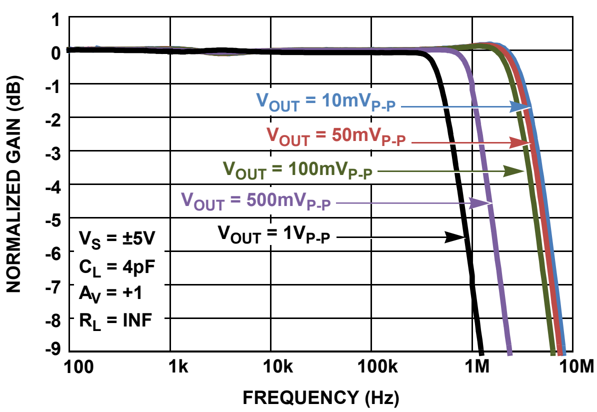


FIGURE 19. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

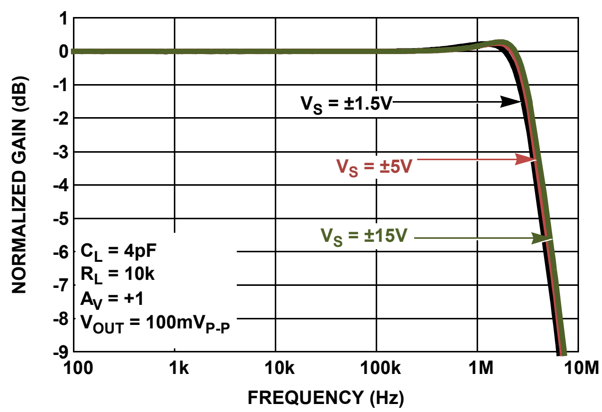


FIGURE 20. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

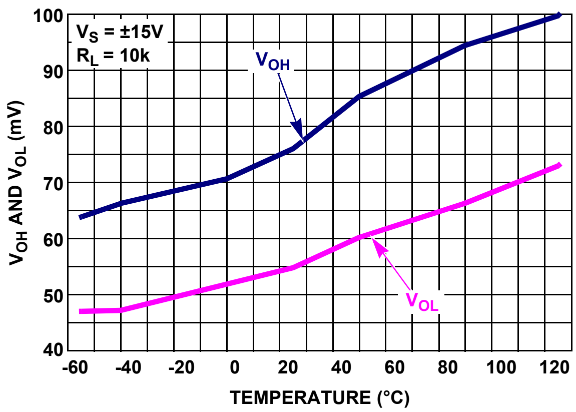


FIGURE 21. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, V_S = ±15V, R_L = 10k

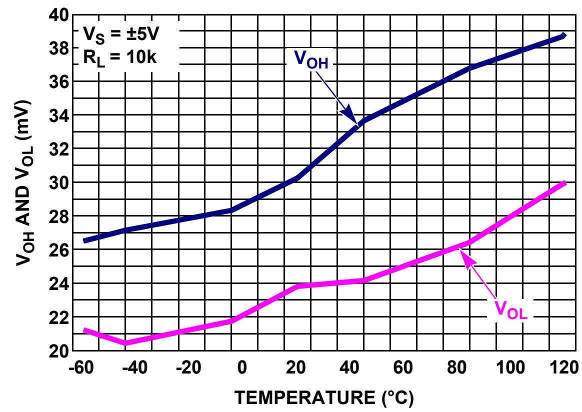


FIGURE 22. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, V_S = ±5V, R_L = 10k

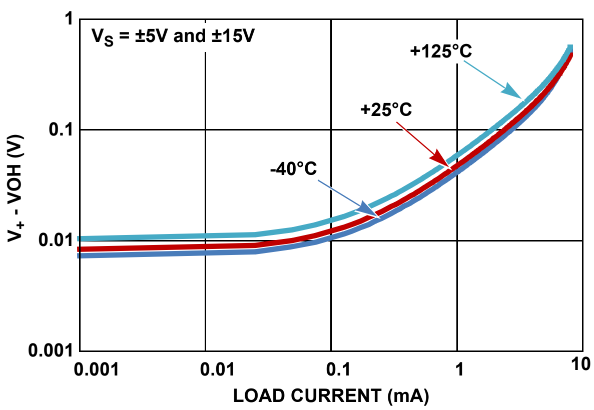


FIGURE 23. OUTPUT OVERHEAD VOLTAGE HIGH vs LOAD CURRENT, -40°C to +125°C, V_S = ±5V AND ±15V

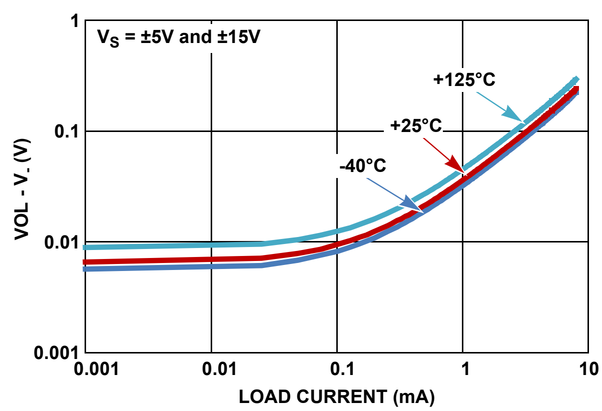


FIGURE 24. OUTPUT OVERHEAD VOLTAGE LOW vs LOAD CURRENT, -40°C to +125°C, V_S = ±5V AND ±15V

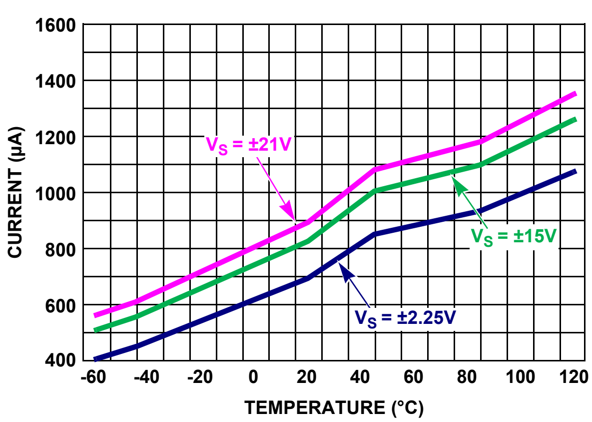


FIGURE 25. ISL28118M SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

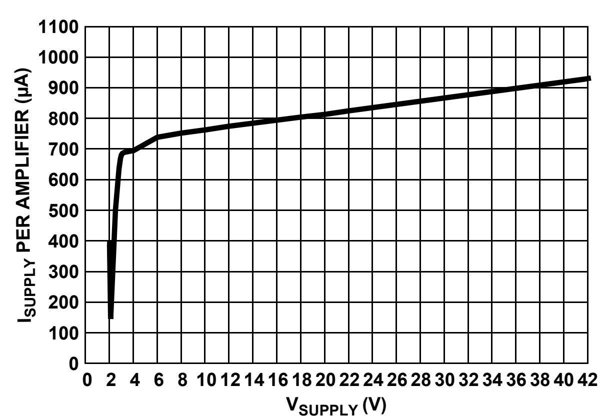


FIGURE 26. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

$V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

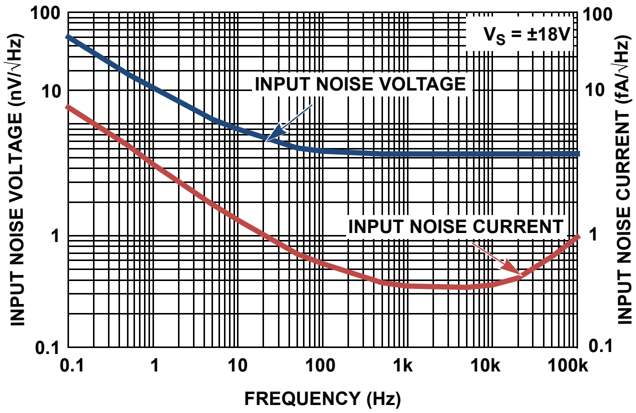


FIGURE 27. INPUT NOISE VOLTAGE (en) AND INPUT NOISE CURRENT (in) vs FREQUENCY, $V_S = \pm18V$

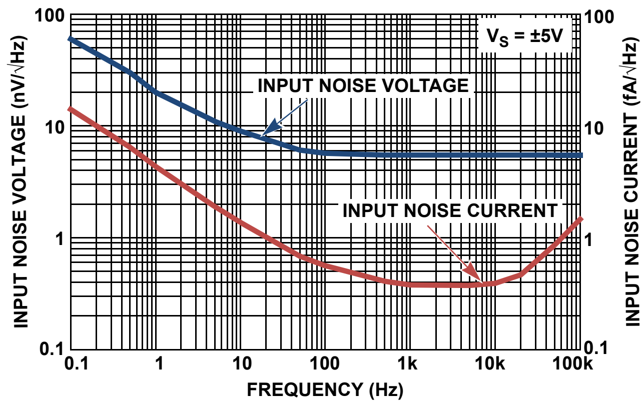


FIGURE 28. INPUT NOISE VOLTAGE (en) AND INPUT NOISE CURRENT (in) vs FREQUENCY, $V_S = \pm5V$

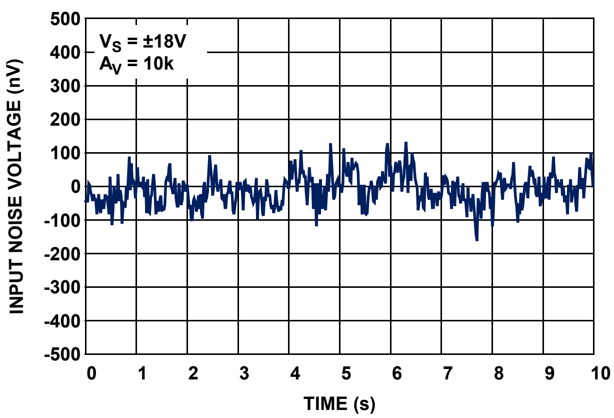


FIGURE 29. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm18V$

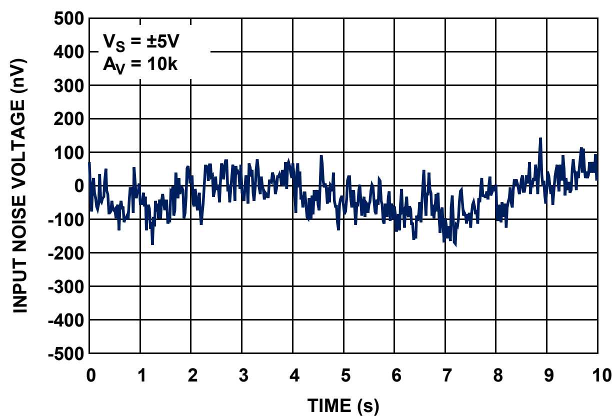


FIGURE 30. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm5V$

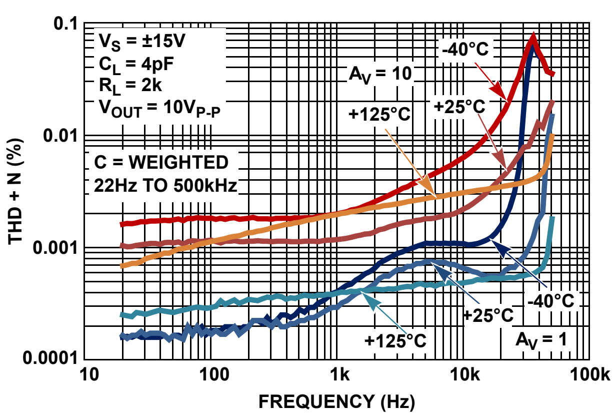


FIGURE 31. THD+N vs FREQUENCY vs TEMPERATURE, $A_V = 1,10$, $R_L = 2k$

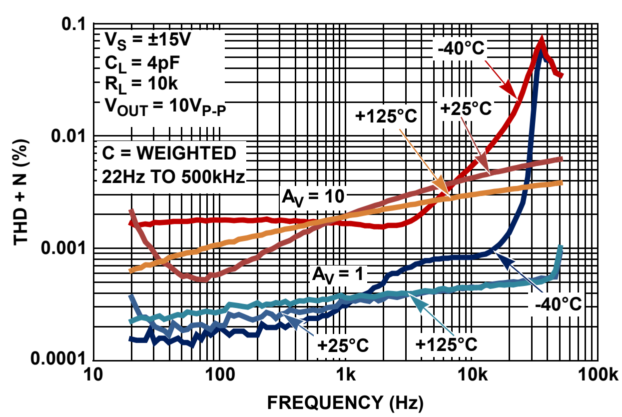


FIGURE 32. THD+N vs FREQUENCY vs TEMPERATURE, $A_V = 1, 10, R_L = 10k$

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

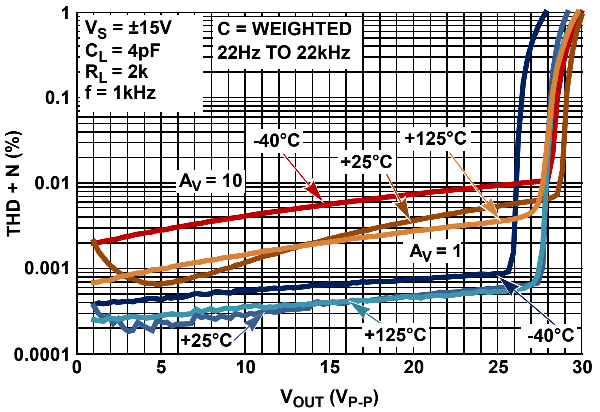


FIGURE 33. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 2k

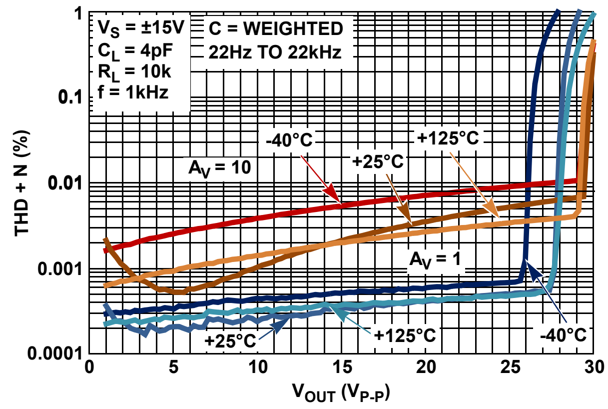


FIGURE 34. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 10k

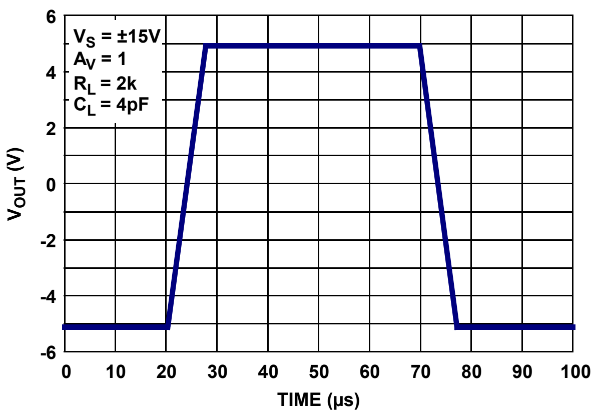


FIGURE 35. LARGE SIGNAL 10V STEP RESPONSE, $V_S = \pm15V$

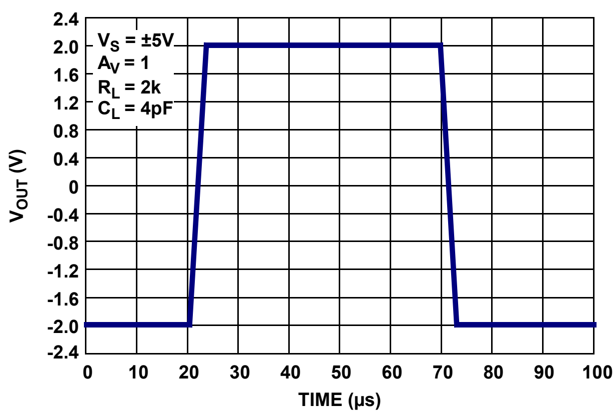


FIGURE 36. LARGE SIGNAL 4V STEP RESPONSE, $V_S = \pm5V$

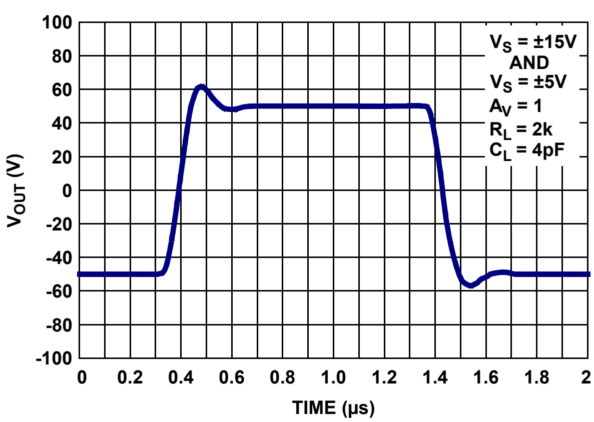


FIGURE 37. SMALL SIGNAL TRANSIENT RESPONSE, $V_S = \pm5V, \pm15V$

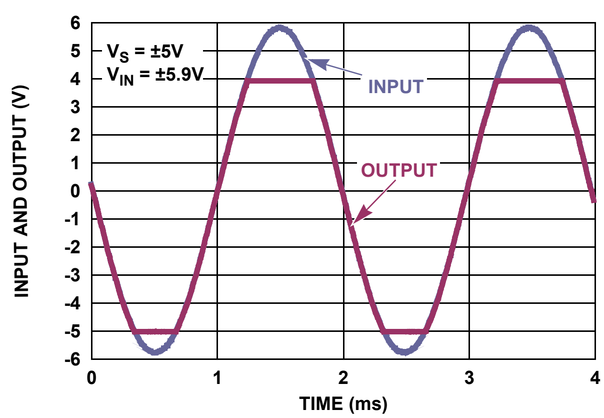


FIGURE 38. NO PHASE REVERSAL

Typical Performance Curves $V_S = \pm 15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

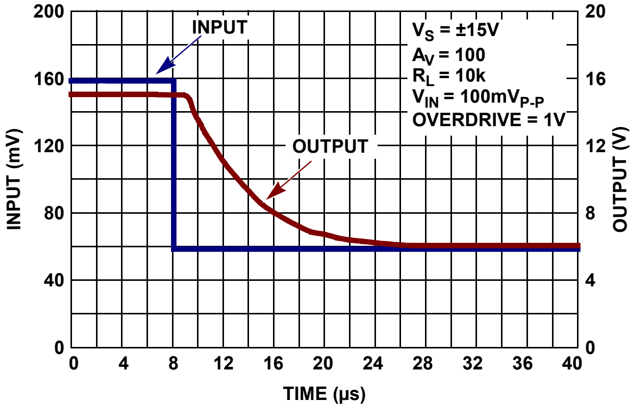


FIGURE 39. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 15V$

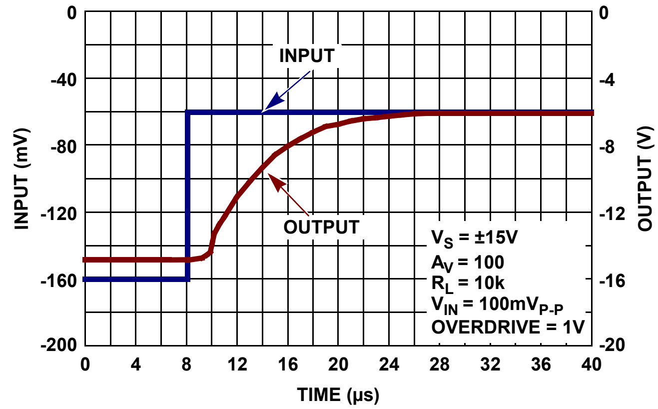


FIGURE 40. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 15V$

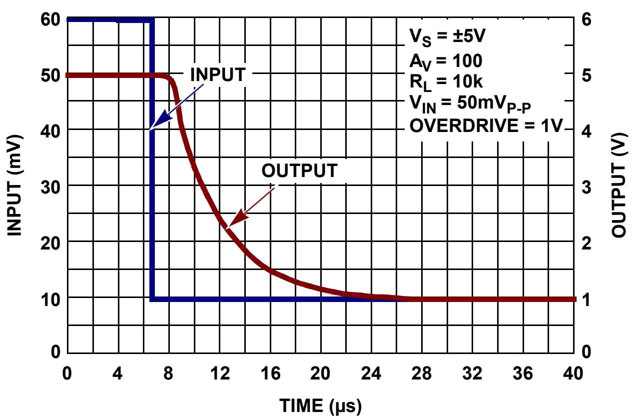


FIGURE 41. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 5V$

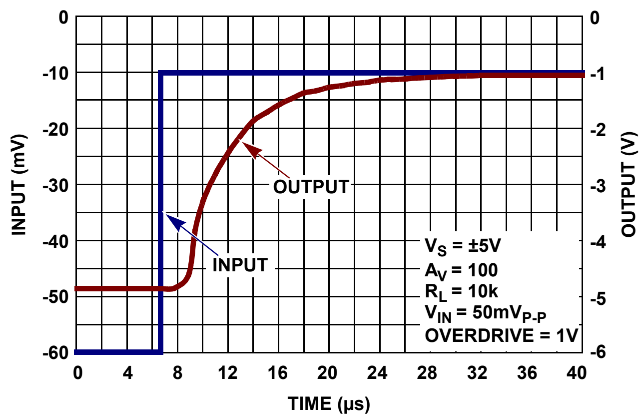


FIGURE 42. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S = \pm 5V$

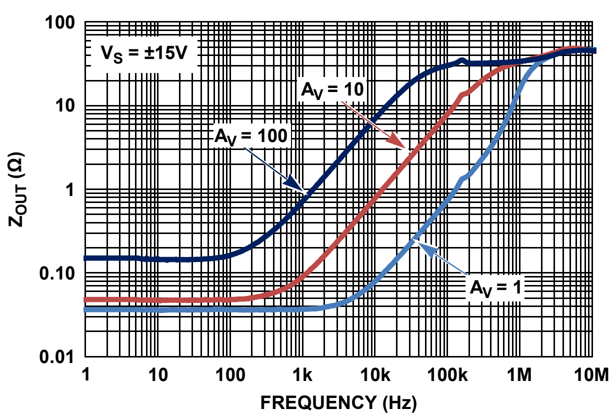


FIGURE 43. OUTPUT IMPEDANCE vs FREQUENCY, $V_S = \pm 15V$

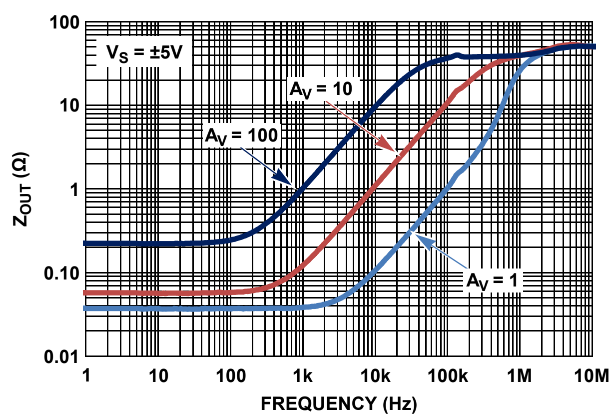


FIGURE 44. OUTPUT IMPEDANCE vs FREQUENCY, $V_S = \pm 5V$

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified. **(Continued)**

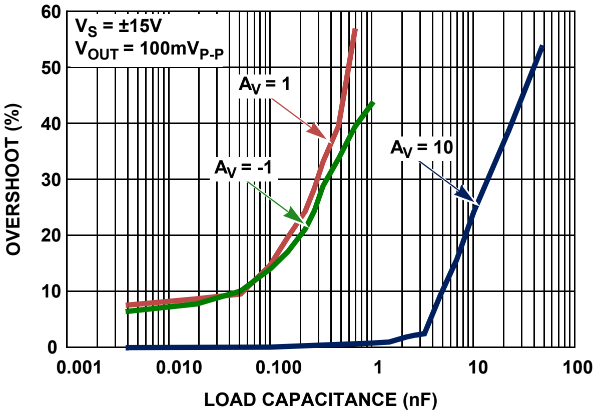


FIGURE 45. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±15V

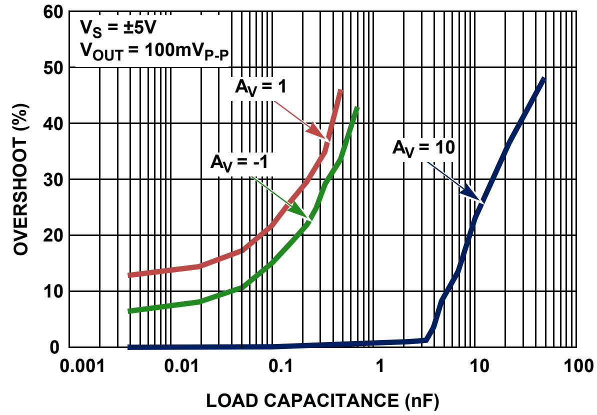


FIGURE 46. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±5V

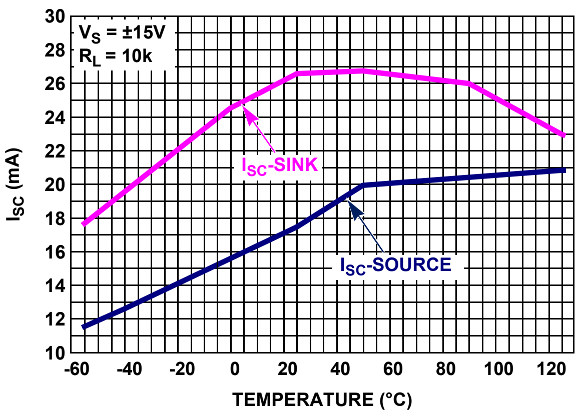


FIGURE 47. ISL28118M SHORT CIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

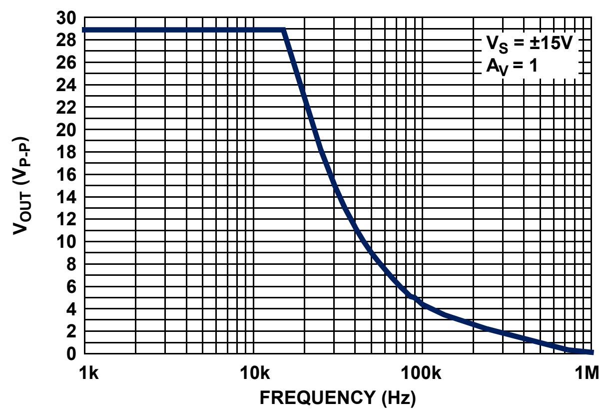


FIGURE 48. MAX OUTPUT VOLTAGE vs FREQUENCY

Applications Information

Functional Description

The ISL28118M is a 3.2MHz, single-supply, rail-to-rail output amplifier with a common mode input voltage range extending to a range of 0.5V below the V- rail. The input stage is optimized for precision sensing of ground-referenced signals in single-supply applications. The input stage is able to handle large input differential voltages without phase inversion, making this amplifier suitable for high-voltage comparator applications. The bipolar design features high open loop gain, excellent DC input/output temperature stability with a low quiescent current of 850µV, and low temperature drift. The op amp is fabricated in a new precision 40V complementary bipolar DI process and is immune from latch-up.

Operating Voltage Range

The op amp is designed to operate over a single supply range of 3V to 40V or a split supply voltage range of +1.8V, -1.2V to ±20V. The device is fully characterized at 10V (±5V) and 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" beginning on page 7.

The input common mode voltage to the V+ rail (V+ -1.8V over the full temperature range) may limit amplifier operation when operating from split V+ and V- supplies. Figure 6 shows the common mode input voltage range variation over-temperature.

Input Stage Performance

The ISL28118M PNP input stage has a common mode input range extending up to 0.5V below ground at +25°C (Figure 6). Full amplifier performance is guaranteed with input voltage down to ground (V-) over the -55°C to +125°C temperature range. For common mode voltages down to -0.5V below ground (V-), the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance, and DC accuracy when amplifying low-level, ground-referenced signals.

The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage (max 42V) and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high-voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications, without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions is avoided.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current-limiting resistors may be needed at each input terminal (see Figure 49, $R_{IN}+$, $R_{IN}-$) to limit current through the power-supply ESD diodes to 20mA.

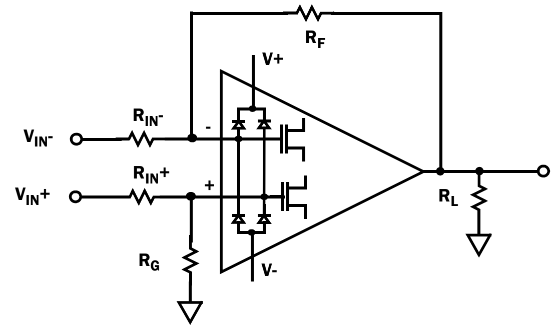


FIGURE 49. INPUT ESD DIODE CURRENT LIMITING

Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 15mV when the total output load (including feedback resistance) is held below 50µA. With ±15V supplies, this can be achieved by using feedback resistor values >300kΩ.

The output stage is internally current limited. The amplifiers can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well when driving capacitive loads (Figures 45 and 46). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 35% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28118M is immune to output phase reversal for input voltage to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (Figure 38).

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \qquad \text{(EQ. 2)}$$

where:

- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28118M SPICE Model

Figure 50 shows the SPICE model schematic and Figure 51 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise voltage, slew rate, CMRR, and gain and phase. The DC parameters are I_{OS}, total supply current, and output voltage swing. The model uses typical parameters given in the "Electrical Specifications" table beginning on page 4. The AVOL is adjusted for 136dB with the dominant pole at 0.6Hz. The CMRR is set at 120dB, f = 50kHz. The input stage models the actual device to present an accurate AC representation. The model is configured for an ambient temperature of +25°C.

Figures 52 through 66 show the characterization vs simulation results for the noise voltage, open loop gain phase, closed loop gain vs frequency, gain vs frequency vs RL, CMRR, large signal 10V step response, small signal 0.1V step, and output voltage swing ±15V supplies.

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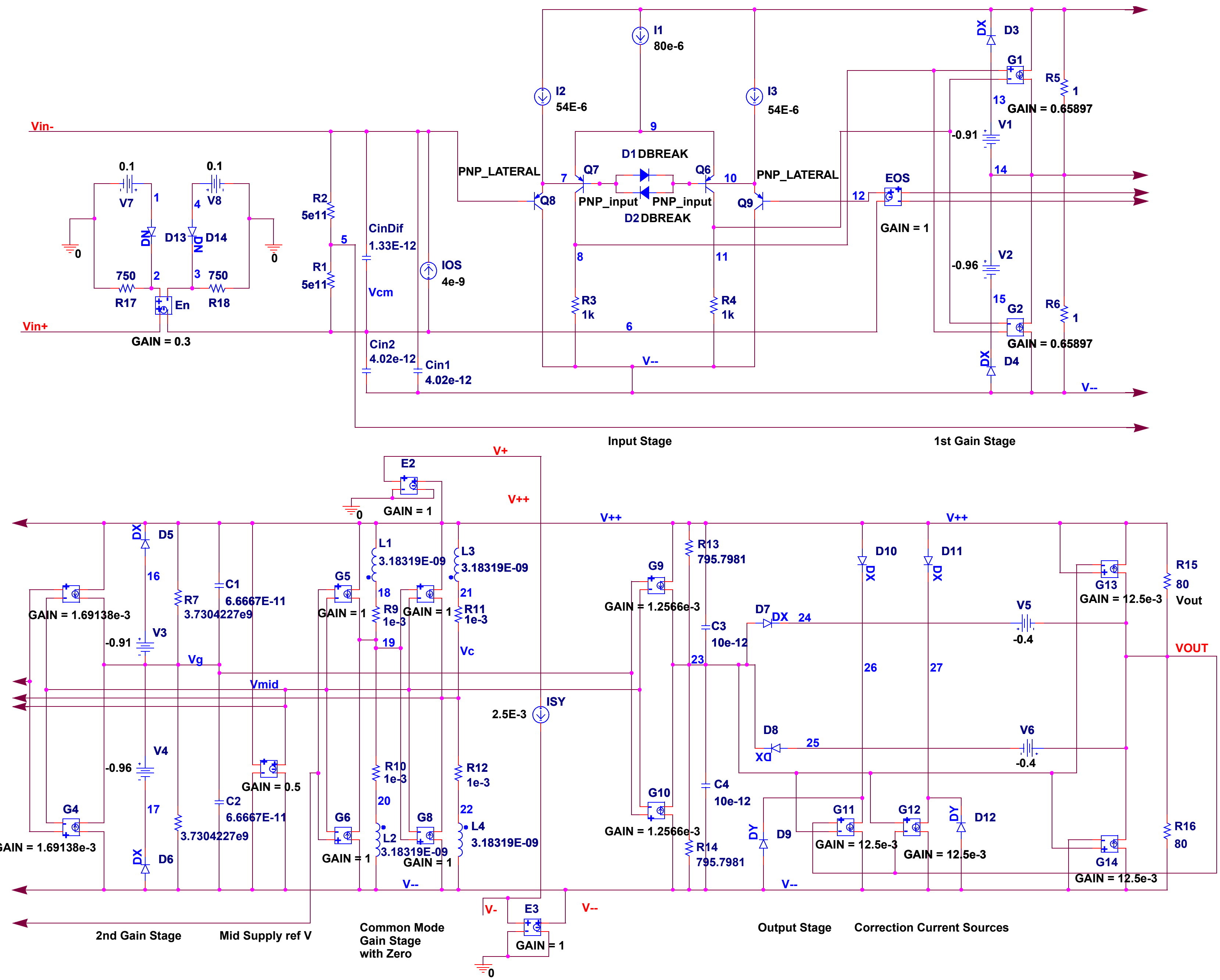

FIGURE 50. SPICE SCHEMATIC

```
*ISL28118_218 Macromodel - covers
following *products
*ISL28118
*ISL28218
*
*Revision History:
* Revision B, LaFontaine January 22 2014
* Model for Noise, supply currents, CMRR
*120dB f = 40kHz, AVOL 136dB f = 0.5Hz
* SR = 1.2V/us, GBWP 4MHz.
*Copyright 2011 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT"
*Use of this model indicates your acceptance
*with the terms and provisions in the License
*Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance
characteristics *under a wide range of
external circuit *configurations using
compatible simulation *platforms – such as
iSim PE.
*
*Device performance features supported by
this *model:
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances,
*Open loop gain and phase,
*Closed loop bandwidth and frequency
*response,
*Loading effects on closed loop frequency
*response,
*Input noise terms including 1/f effects,
*Slew rate,
*Input and Output Headroom limits to I/O
*voltage swing,
*Supply current at nominal specified supply
*voltages,
*
*Device performance features NOT
supported *by this model:
*Harmonic distortion effects,
*Output current limiting (current will limit at
*40mA),
*Disable operation (if any),
*Thermal effects and/or over temperature
*parameter variation,
*Limited performance variation vs. supply
*voltage is modeled,
*Part to part performance variation due to
*normal process parameter spread,
*Any performance difference arising from
*different packaging,
*Load current reflected into the power supply
*current.

* source ISL28118_218 SPICEmodel
*
* Connections:        +input
*                       |   -input
*                       |   |   +Vsupply
*                       |   |   |   -Vsupply
*                       |   |   |   |   output
.subckt ISL28118_218  Vin+ Vin-V+ V- VOUT
* source ISL28118_218_presubckt_0
*
*Voltage Noise
E_En       VIN+ 6 2 0 0.3
D_D13      1 2 DN
D_D14      1 2 DN
V_V7       1 0 0.1
V_V8       4 0 0.1
R_R17      2 0  750
*R_R18      3 0  750
*
*Input Stage
Q_Q6       11 10 9 PNP_input
Q_Q7       8 7 9 PNP_input
Q_Q8       V-- VIN- 7 PNP_LATERAL
Q_Q9       V-- 12 10 PNP_LATERAL
I_I1       V++ 9 DC 80e-6
I_I2       V++ 7 DC 54E-6
I_I3       V++ 10 DC 54E-6
I_IOS      6 VIN- DC 4e-9
D_D1       7 10 DBREAK
D_D2       10 7 DBREAK
R_R1       5 6  5e11
R_R2       VIN- 5  5e11
R_R3       V-- 8  1000
R_R4       V-- 11  1000
C_Cin1     V-- VIN-  4.02e-12
C_Cin2     V-- 6  4.02e-12
C_CinDif   6 VIN-  1.33E-12
*
*1st Gain Stage
G_G1       V++ 14 8 11 0.65897
G_G2       V-- 14 8 11 0.65897
V_V1       13 14 -0.91
V_V2       14 15 -0.96
D_D3       13 V++ DX
D_D4       V-- 15 DX
R_R5       14 V++  1
R_R6       V-- 14  1
*
*2nd Gain Stage
G_G3       V++ VG 14 VMID 1.69138e-3
G_G4       V-- VG 14 VMID 1.69138e-3
V_V3       16 VG -0.91
V_V4       VG 17 -0.96
D_D5       16 V++ DX
D_D6       V-- 17 DX
R_R7       VG V++  3.7304227e9
R_R8       V-- VG  3.7304227e9
C_C1       VG V++  6.6667E-11
C_C2       V-- VG  6.6667E-11
*
*Mid supply Ref
E_E2       V++ 0 V+ 0 1
E_E3       V-- 0 V- 0 1
E_E4       VMID V-- V++ V-- 0.5
I_ISY      V+ V- DC 0.85E-3
*
*Common Mode Gain Stage with Zero
G_G5       V++ 19 5 VMID 1
G_G6       V-- 19 5 VMID 1
G_G7       V++ VC 19 VMID 1
G_G8       V-- VC 19 VMID 1
E_EOS      12 6 VC VMID 1
L_L1       18 V++  3.18319E-09
L_L2       20 V--  3.18319E-09
L_L3       21 V++  3.18319E-09
L_L4       22 V--  3.18319E-09
R_R9       19 18  1e-3
R_R10      20 19  1e-3
R_R11      VC 21  1e-3
R_R12      22 VC  1e-3
*
*Pole Stage
G_G9       V++ 23 VG VMID 1.2566e-3
G_G10      V-- 23 VG VMID 1.2566e-3
R_R13      23 V++  795.7981
R_R14      V-- 23  795.7981
C_C3       23 V++  10e-12
C_C4       V-- 23  10e-12
*
*Output Stage with Correction Current
Sources
G_G11      26 V-- VOUT 23 12.5e-3
G_G12      27 V-- 23 VOUT 12.5e-3
G_G13      VOUT V++ V++ 23 12.5e-3
G_G14      V-- VOUT 23 V-- 12.5e-3
D_D7       23 24 DX
D_D8       25 23 DX
D_D9       V-- 26 DY
D_D10      V++ 26 DX
D_D11      V++ 27 DX
D_D12      V-- 27 DY
V_V5       24 VOUT -0.4
V_V6       VOUT 25 -0.4
R_R15      VOUT V++  80
R_R16      V-- VOUT  80
.model PNP_LATERAL pnp(is=1e-016
bf=250 va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0
af=1)
.model PNP_input pnp(is=1e-016 bf=100
va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0
af=1)
.model DBREAK D(bv=43 rs=1)
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28118_218
```

FIGURE 51. SPICE NET LIST

Characterization vs Simulation Results

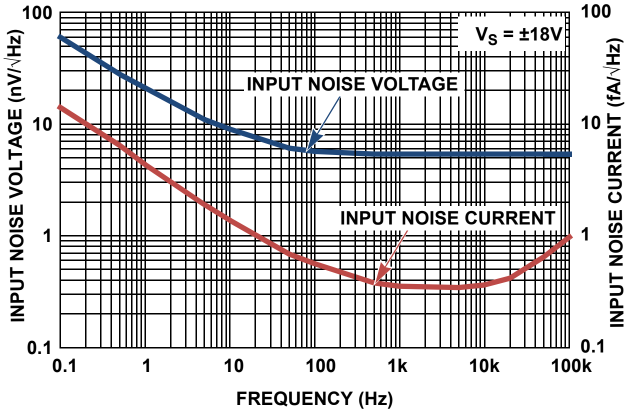

FIGURE 52. CHARACTERIZED INPUT NOISE VOLTAGE

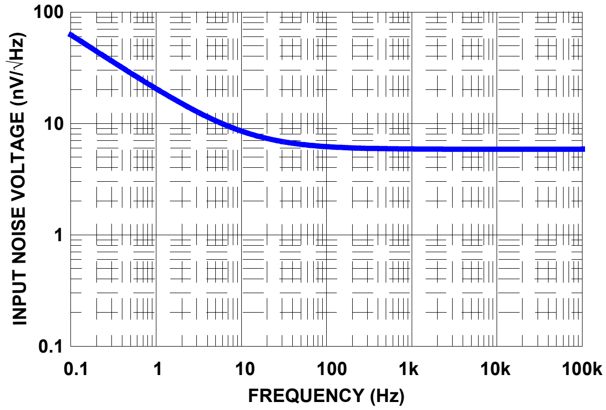

FIGURE 53. SIMULATED INPUT NOISE VOLTAGE

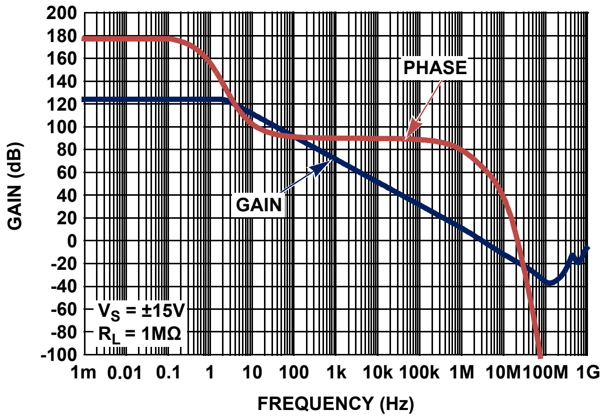

FIGURE 54. CHARACTERIZED OPEN-LOOP GAIN, PHASE vs FREQUENCY

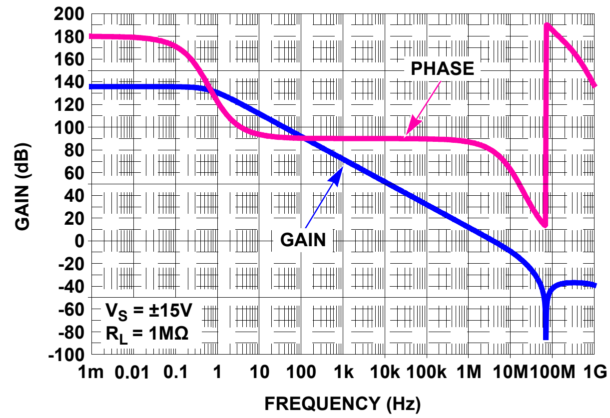

FIGURE 55. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

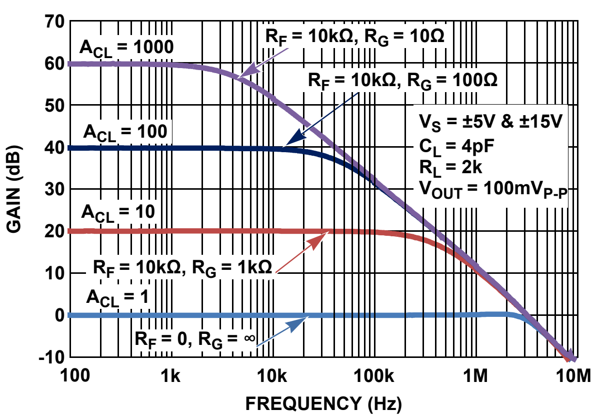

FIGURE 56. CHARACTERIZED CLOSED-LOOP GAIN vs FREQUENCY

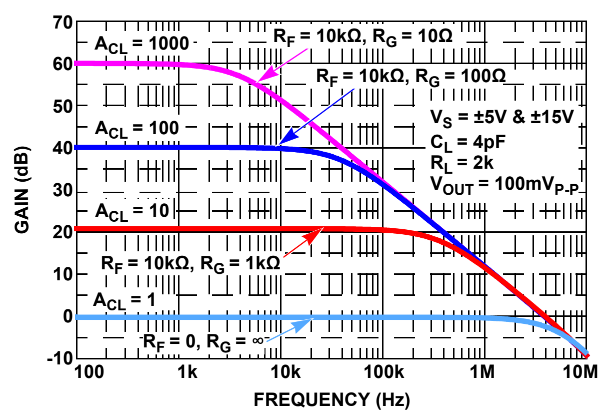

FIGURE 57. SIMULATED CLOSED-LOOP GAIN vs FREQUENCY

Characterization vs Simulation Results (Continued)

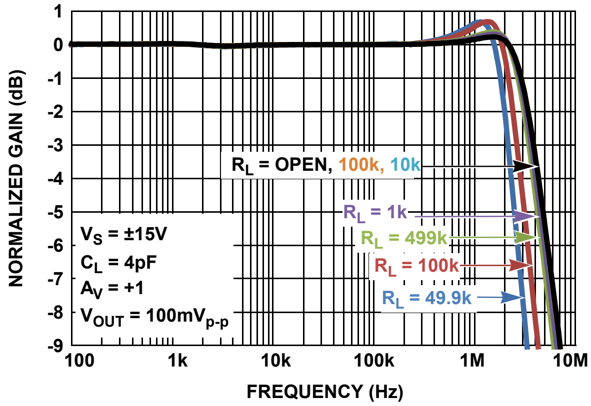

FIGURE 58. CHARACTERIZED GAIN vs FREQUENCY vs R_L

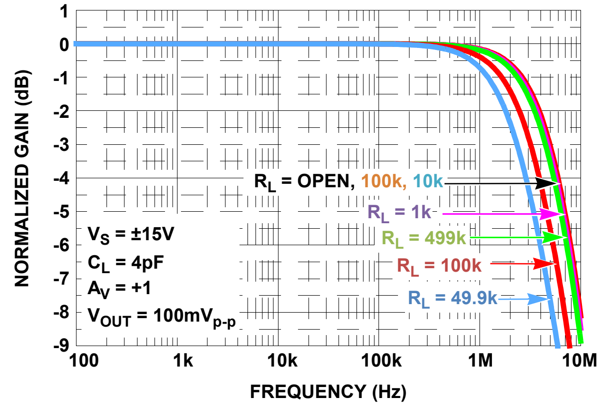

FIGURE 59. SIMULATED GAIN vs FREQUENCY vs R_L

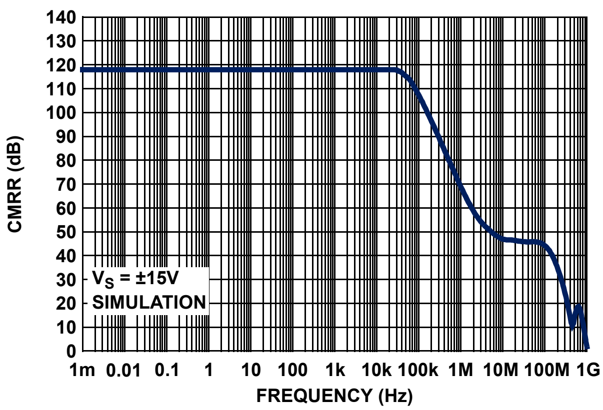

FIGURE 60. CHARACTERIZED CMRR vs FREQUENCY

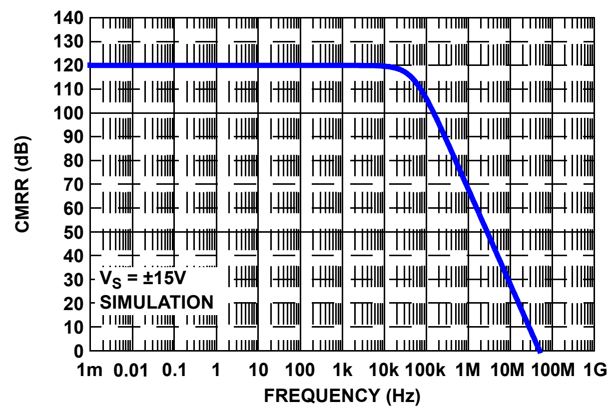

FIGURE 61. SIMULATED CMRR vs FREQUENCY

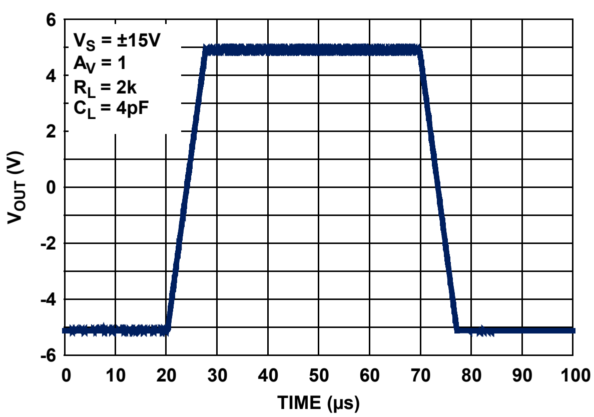

FIGURE 62. CHARACTERIZED LARGE-SIGNAL 10V STEP RESPONSE

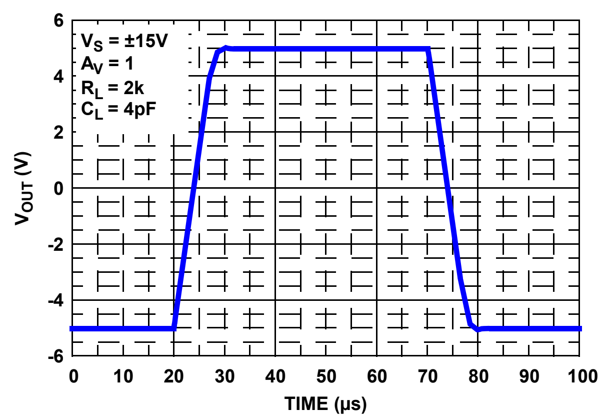

FIGURE 63. SIMULATED LARGE-SIGNAL 10V STEP RESPONSE

Characterization vs Simulation Results (Continued)

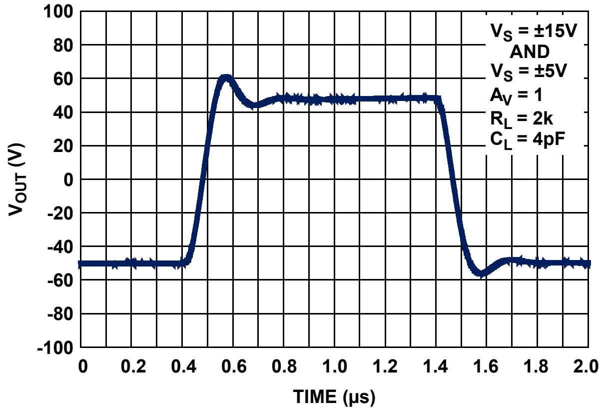

FIGURE 64. CHARACTERIZED SMALL-SIGNAL TRANSIENT RESPONSE

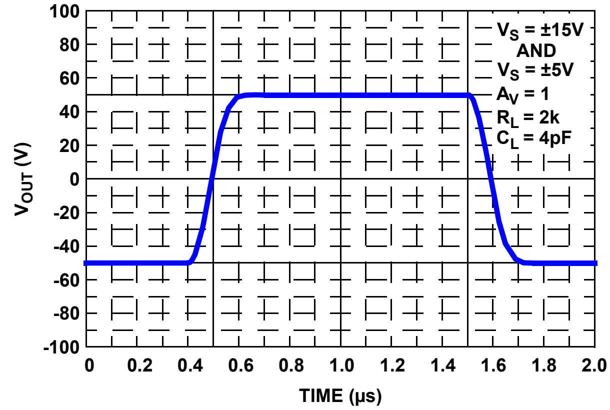

FIGURE 65. SIMULATED SMALL-SIGNAL TRANSIENT RESPONSE

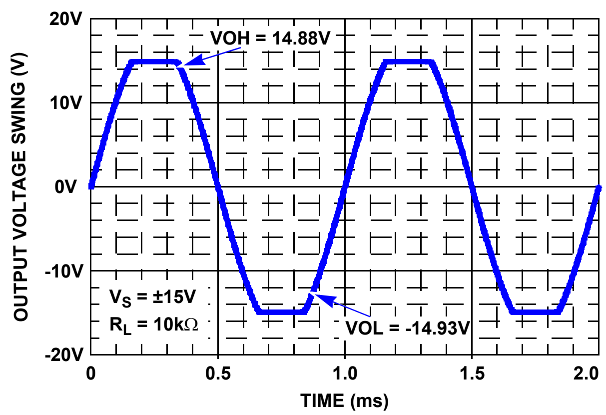

FIGURE 66. SIMULATED OUTPUT VOLTAGE SWING

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 7, 2014	FN7858.1	Updated Spice model netlist on page 18. Changed POD: FROM M8.118: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" To M8.118B: Correct lead dimension in side view 2 from 0.15 - 0.05mm to 0.15+/-0.05mm
May 11, 2011	FN7858.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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