

ISL282X7SOICEVAL2Z

Evaluation Board

AN1509  
Rev 0.00  
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Introduction

The ISL282X7SOICEVAL2Z evaluation board is a design platform containing all the circuitry needed to characterize critical performance parameters of the ISL282X7 operational amplifiers in SOIC-8 package, using a variety of user defined test circuits.

The ISL282X7 operational amplifiers feature low bias current, low noise, and low offset and temperature drift.

Reference Documents

- ISL28207 Data Sheet, [FN6631](#)
- ISL28217 Data Sheet, [FN6632](#)
- ISL28227 Data Sheet, [FN6633](#)

Evaluation Board Key Features

The ISL282X7SOICEVAL2Z is designed to enable the IC to operate from a single supply, +4.5VDC to +40VDC or from split supplies, ±2.25VDC to ±20V. The board is configured for a dual op amp connected for differential input with a closed loop gain of 10. A single external reference voltage (VREF) pin and provisions for a user-selectable voltage divider - filter are included.

Power Supplies (Figure 1)

External power connections are made through the +V, -V, VREF and Ground connections on the evaluation board. For single supply operation, the -V and Ground pins are tied together to the power supply negative terminal. For split supplies, +V and -V terminals connect to their respective power supply terminals. De-coupling capacitors C2 and C4 connect to their respective supplies through R16 and R31 zero-ohm resistors.

These resistors are 0Ω but can be changed by the user to provide additional power supply filtering, or to reduce the voltage rate-of-rise to less than ±1V/μs. Two additional capacitors, C3 and C5 are connected close to the part to filter out high frequency noise. Anti-reverse diode D1 protects the circuit in the case of accidental polarity reversal.

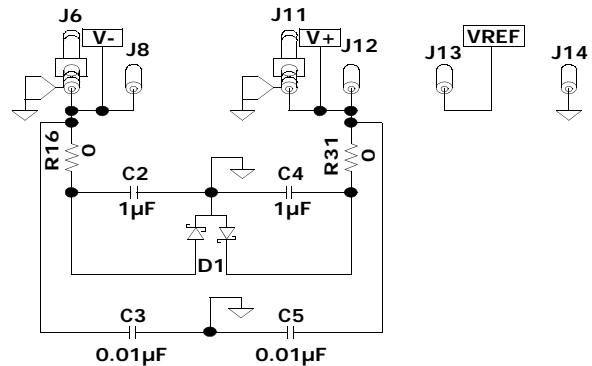


FIGURE 1. POWER SUPPLY CIRCUIT

Amplifier Configuration (Figure 2)

The schematic of 1/2 of the op-amp with the components supplied is shown in Figure 2. The circuit implements a differential input amp with a closed loop gain of 10. The circuit can operate from a single supply or from dual supplies. The VREF pin must be connected to ground to establish a ground referenced input for dual supply operation, or can be externally set to any reference level for single supply operation. VREF should not be left floating.

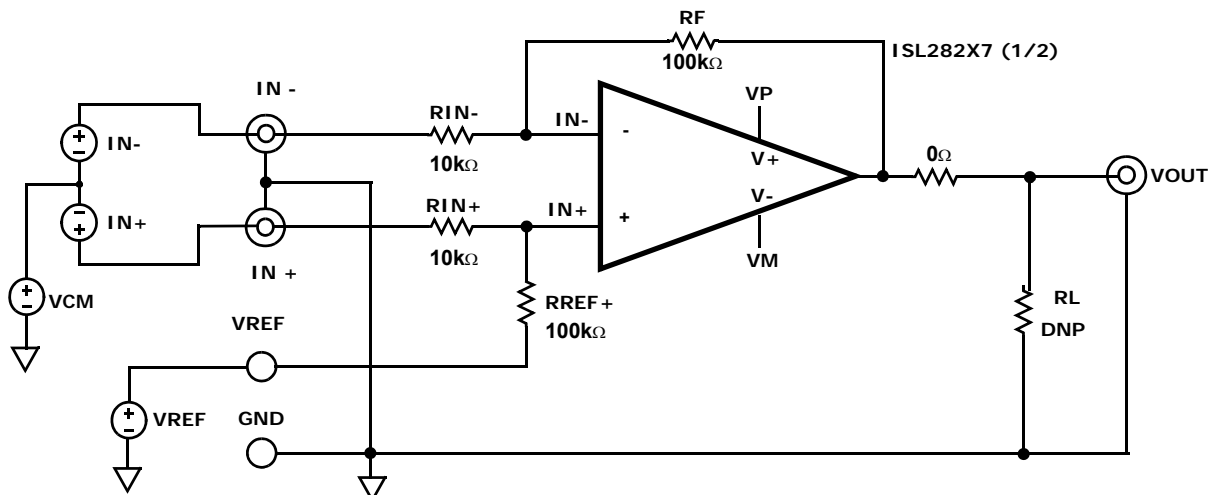


FIGURE 2. BASIC AMPLIFIER CONFIGURATION

## User-selectable Options (Figures 3 and 4)

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier VREF, inputs, outputs, and the amplifier feedback loops. The Inputs (Figure 3) have additional resistor and capacitor, and jumper placements for loading and/or measurement of frequency sensitive parameters.

The outputs (Figure 4) have additional resistor and capacitor placements for loading.

NOTE: Operational amplifiers are sensitive to output capacitance and may oscillate. In the event of oscillation, reduce output capacitance by using shorter cables, or add a resistor in series with the output.

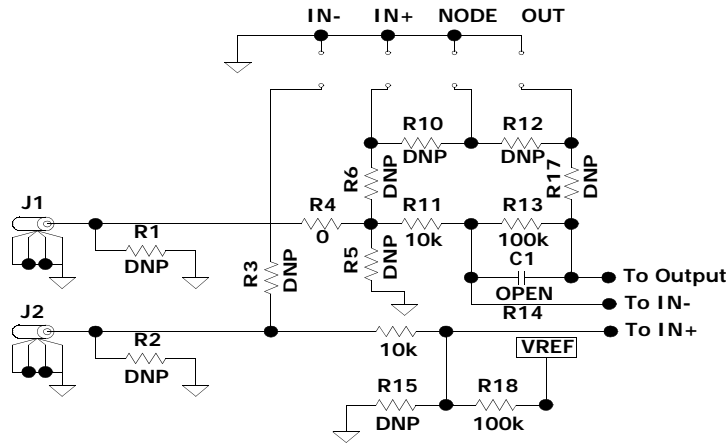


FIGURE 3. INPUT STAGE (1/2)

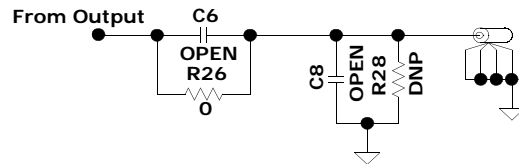


FIGURE 4. OUTPUT STAGE (1/2)

TABLE 1. ISL282X7SOICEVAL2Z COMPONENTS PARTS LIST

DEVICE #	DESCRIPTION	COMMENTS
C2, C4	CAP, SMD, 0805, 1 $\mu$ F, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C3, C5	CAP, SMD, 0603, 0.01 $\mu$ F, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C1, C6-C10	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	User selectable capacitors - not populated
D1	DIODE-RECTIFIER, SMD, SOD-123, 2P, 40V, 0.5A, ROHS	Reverse Power Protection
U1 (ISL28207FBZ)	OP AMP, SOIC, ROHS	
U1 (ISL28217FBZ)	OP AMP, SOIC, ROHS	
U1 (ISL28227FBZ)	OP AMP, SOIC, ROHS	
R1-R3, R5-R8, R10, R12, R15, R17, R20, R22, R28-R30, R32, R34-R36	RESISTOR, SMD, 0603, 0.1%, MF, DNP-PLACE HOLDER	User selectable resistors - not populated
R5, R18	RES, SMD, 0603, 0 $\Omega$ , 1/10W, TF, ROHS	Zero ohm user selectable resistors
R11, R14, R21, R24	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Gain resistors
R13, R18, R19, R23	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Gain resistors

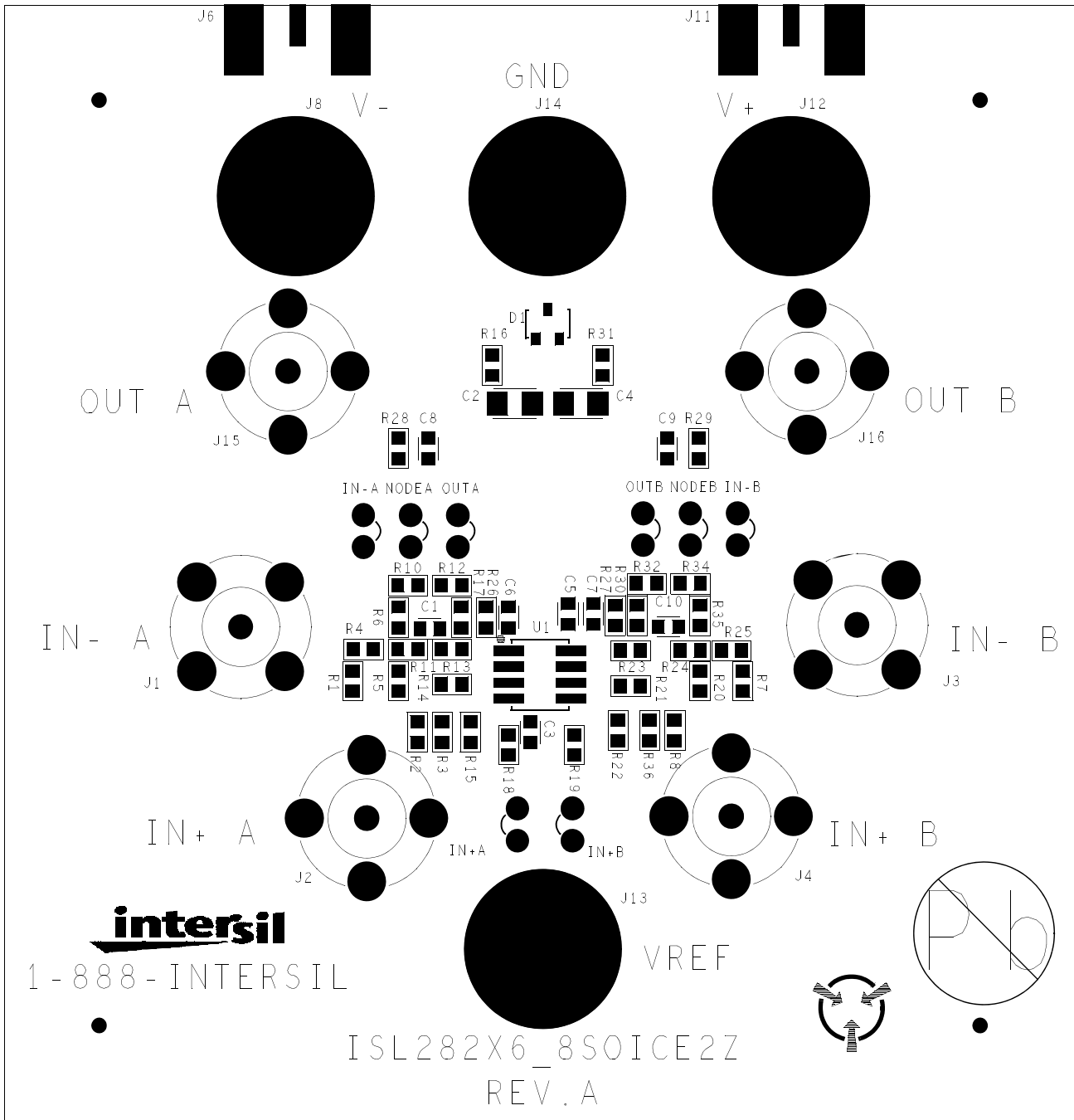


FIGURE 5. ISL282X7SOICEVAL2Z TOP VIEW

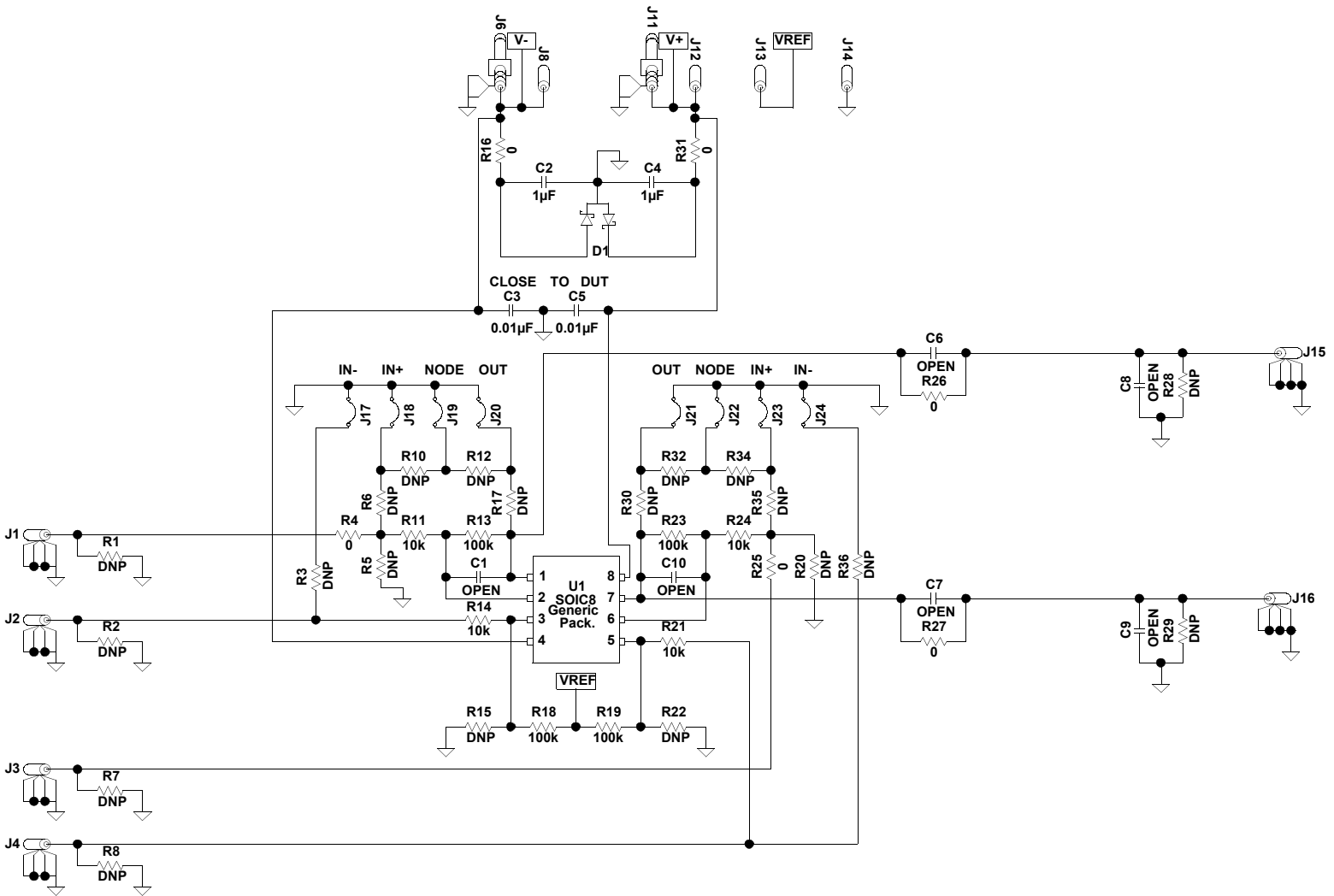


FIGURE 6. ISL282X7SOICEVAL2Z SCHEMATIC DIAGRAM