ISL32610E, ISL32611E, ISL32612E

±16.5kV ESD Protected, 1.8V, Micro Power, +125°C, 1/8 Unit Load, RS-485/RS-422 Differential Receivers

FN7869
Rev.2.00
Sep 26, 2019

The ISL32610E, ISL32611E, ISL32612E are ±16.5kV IEC61000 ESD protected, fractional unit load (UL), 1.8V powered, single differential receivers (Rx) for balanced data communication using the RS-485 and RS-422 standards. With their 85µA supply currents, the receivers are optimized for low power applications, and deliver the lowest supply currents of any available single Rx IC (see Figure 1).

To improve performance in low data rate applications with slow signal transitions, these Rx feature symmetrical switching points (±200mV) and increased hysteresis. The symmetrical switching points eliminate the duty cycle distortion introduced by full-failsafe type receivers (see Figure 2), while the larger hysteresis increases noise immunity.

The receivers present a 1/8 unit load to the data bus, which allows up to 256 devices on the network for large node count systems (for example, process automation, remote meter reading systems). The ISL32611E/ISL32612E Rx output is tri-statable using the $\overline{RE}$/RE input.

The receiver inputs feature a failsafe-if-open design, which ensures a logic high Rx output if Rx inputs are floating. Data rates up to 256kbps are achievable with this device at V_{CC} = 1.8V.

See Table 1 for a summary of each device's features. For a companion 1.8V differential transmitter in a SOT-23 package, reference the ISL32613E datasheet.

Features

- Wide Supply Voltage Range . . . . . 1.8V to 3.6V
- Ultra Low Quiescent Supply Current . . . . 110µA (maximum)
- IEC61000 ESD Protection on RS-485 Bus Pins . . . . ±16.5kV
  - Class 3 ESD Level on all Other Pins. . . . . >8kV HBM
- Symmetrical Switching Thresholds for Less Duty Cycle Distortion (see Figure 2)
- Larger Hysteresis for Improved Noise Immunity 70mV
- Data Rates up to 256kbps (1.8V) or 500kbps (3.3V)
- 1/8 Unit Load Allows up to 256 Devices on the RS-485 Bus
- Specified for +125°C Operation
- Three-State Rx Output Available
- 5V tolerant logic inputs
- Pb-Free (RoHS Compliant)

Applications

- Industrial/Process Control Networks, Factory Automation
- High Node Count Networks
- Space Constrained Systems
- Building Environmental Control Systems

Related Literature

For a full list of related documents, visit our website:

- ISL32610E, ISL32611E, and ISL32612E device pages

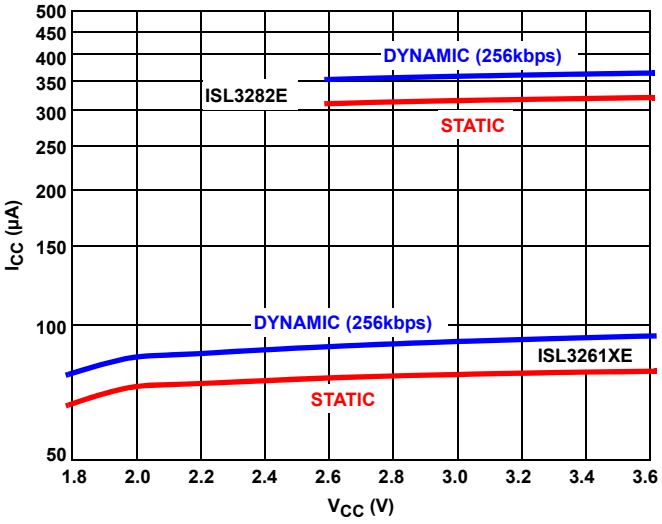


FIGURE 1. ISL3261XE REDUCES OPERATING I_{CC} BY A FACTOR OF 4 FROM PREVIOUS GENERATION RECEIVER ICs, AND OPERATES WITH SUPPLY VOLTAGES AS LOW AS 1.8V

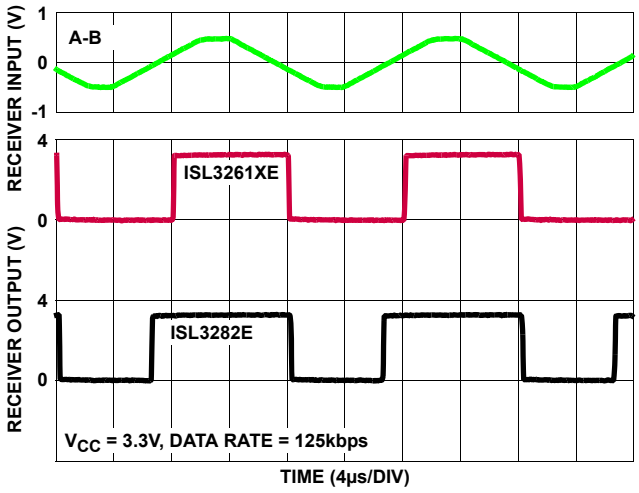
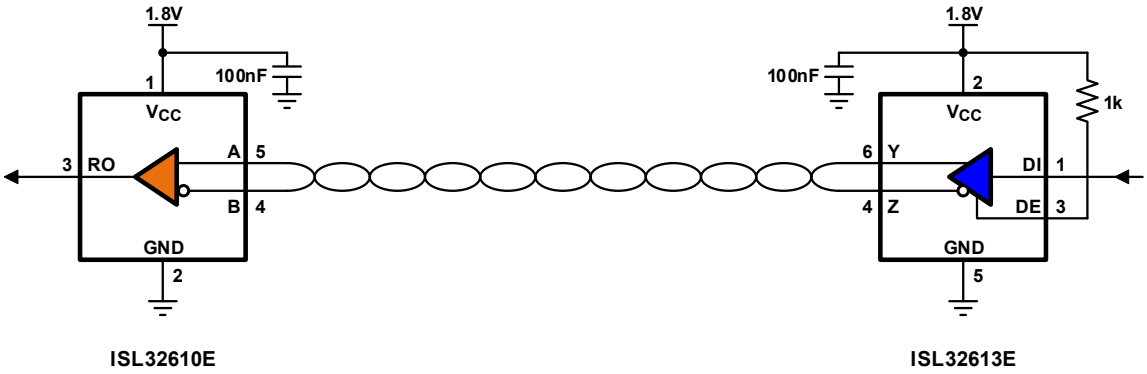


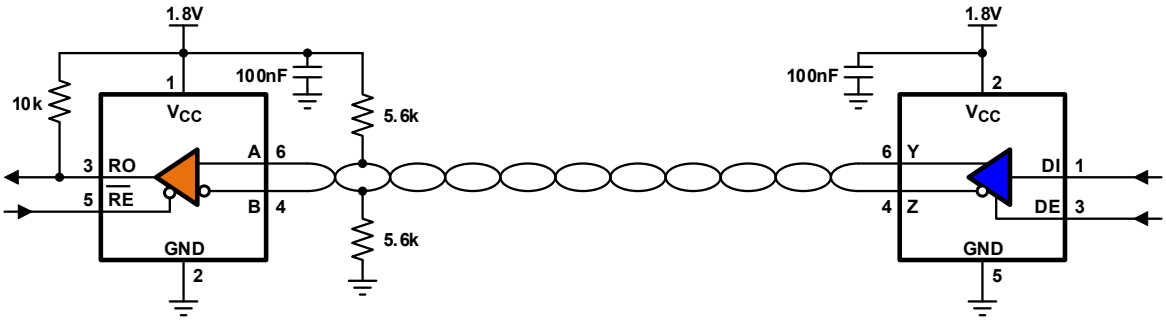
FIGURE 2. COMPARED WITH A FULL-FAILSAFE RECEIVER, THE SYMMETRICAL RX THRESHOLDS OF THE ISL3261XE DELIVER LESS OUTPUT DUTY CYCLE DISTORTION WHEN DRIVEN WITH SLOW INPUT SIGNALS

Typical Operating Circuits



ISL32610E ISL32613E

FIGURE 3. POINT-TO-POINT LINK WITH FIXED ENABLE-PINS



ISL32611E ISL32613E

FIGURE 4. POINT-TO-POINT LINK WITH PROGRAMMABLE ENABLE-PINS

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL32610EFHZ-T	610F	-40 to +125	3k	5 Ld SOT-23	P5.064
ISL32610EFHZ-T7A	610F	-40 to +125	250	5 Ld SOT-23	P5.064
ISL32611EFHZ-T	611F	-40 to +125	3k	6 Ld SOT-23	P6.064
ISL32611EFHZ-T7A	611F	-40 to +125	250	6 Ld SOT-23	P6.064
ISL32612EFHZ-T	612F	-40 to +125	3k	6 Ld SOT-23	P6.064
ISL32612EFHZ-T7A	612F	-40 to +125	250	6 Ld SOT-23	P6.064

NOTES:

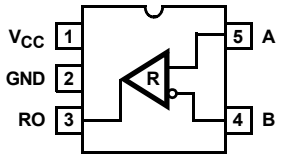
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see ISL32610E, ISL32611E, ISL32612E.device pages. For more information about MSL, see TB363.
4. The part marking is located on the bottom of the part.

TABLE 1. SUMMARY OF FEATURES

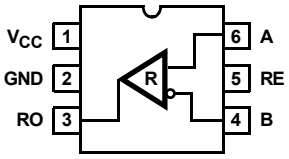
PART NUMBER	CONFIGURATION	NUMBER OF DEVICES ALLOWED ON BUS	1.8V, 3.3V DATA RATE (kbps)	Rx ENABLE?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	PIN COUNT
ISL32610E	Rx Only	256	256, 500	No	85	No	5
ISL32611E	Rx Only	256	256, 500	Yes, Active Low	85	Yes	6
ISL32612E	Rx Only	256	256, 500	Yes, Active High	85	Yes	6

Pin Configurations

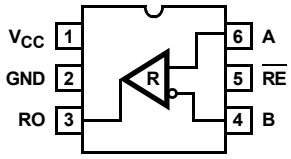
ISL32610E
(5 LD SOT-23)
TOP VIEW



ISL32612E
(6 LD SOT-23)
TOP VIEW



ISL32611E
(6 LD SOT-23)
TOP VIEW



Truth Table

RECEIVING		
INPUTS		OUTPUT
$\overline{RE}$ / RE (Note 12)	A-B	RO
0 / 1	≥ +0.2V	1
0 / 1	≤ -0.2V	0
0 / 1	Inputs Open	1
1 / 0	X	High-Z (Note 5)

NOTE:
5. Low Power Shutdown Mode (Note 10, except for the ISL32610E)

Pin Descriptions

PIN NAME	PIN NUMBER			FUNCTION
	ISL32610E	ISL32611E	ISL32612E	
V_{CC}	1	1	1	System power supply input (1.8V to 3.6V).
GND	2	2	2	Ground connection.
RO	3	3	3	Receiver output: If A > B by at least 0.2V, RO is high; if A < B by 0.2V or more, RO is low; RO = High if A and B are unconnected (floating).
B	4	4	4	±16.5kV IEC61000 ESD protected, inverting differential receiver input.
$\overline{RE}$	-	5	-	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the enable function isn't needed, connect $\overline{RE}$ to GND. $\overline{RE}$ is internally pulled low.
RE	-	-	5	Receiver output enable. RO is enabled when RE is high; RO is high impedance when RE is low. If the enable function is not needed, connect RE to V_{CC} through a 1kΩ or greater resistor. RE is internally pulled high.
A	5	6	6	±16.5kV IEC61000 ESD Protected, noninverting differential receiver input.

Absolute Maximum Ratings

V_{CC} to Ground 7V
Input Voltages
  $\overline{RE}$, RE . . . . . -0.3V to 7V
  A, B . . . . . -8V to +12.5V
Output Voltages
  RO . . . . . -0.3V to (V_{CC} +0.3V)
ESD Rating . . . . . See "ESD PERFORMANCE" on page 6
Latch-Up (per JESD78, Level 2, Class A) . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 Package (Note 6, 7)	190	120
6 Ld SOT-23 Package (Note 6, 7)	177	120

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
Supply Voltage . . . . . 1.8V to 3.3V
Common-Mode Input Voltage
  V_{CC} = 1.8V . . . . . -2V to +2V
  V_{CC} = 3.3V . . . . . -7V to +12V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
7. For θ_{JC}, the case temperature location is taken at the package top center.

Electrical Specifications

Test Conditions: V_{CC} = 1.8V; typical values are at V_{CC} = 1.8V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** (Note 9)

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
DC CHARACTERISTICS								
Logic Input High Voltage (Note 12)	V_{IH}	$\overline{RE}$, RE	V_{CC} = 1.8V	Full	**1.2**	-	-	V
			3V ≤ V_{CC} ≤ 3.6V	Full	**2**	-	-	V
Logic Input Low Voltage (Note 12)	V_{IL}	$\overline{RE}$, RE	V_{CC} = 1.8V	Full	-	-	**0.45**	V
			3V ≤ V_{CC} ≤ 3.6V	Full	-	-	**0.8**	V
Logic Input Current (Note 12)	I_{IN1}	$\overline{RE}$, RE	V_{CC} = 1.8V	Full	**-6**	-	**6**	µA
			V_{CC} ≤ 3.6V	Full	**-12**	-	**12**	µA
Input Current (A, B) (Note 11)	I_{IN2}	V_{CC} = 0V or 1.8V	V_{IN} = 2V	Full	-	-	**60**	µA
			V_{IN} = -2V	Full	**-60**	-	-	µA
		V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	-	**125**	µA
			V_{IN} = -7V	Full	**-100**	-	-	µA
Receiver Differential Threshold Voltage	V_{TH}	-2V ≤ V_{CM} ≤ 2V	V_{CC} = 1.8V	Full	**-0.2**	-	**0.2**	V
		-7V ≤ V_{CM} ≤ 12V	3V ≤ V_{CC} ≤ 3.6V	Full	**-0.2**	-	**0.2**	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V	V_{CC} = 1.8V	Full	-	70	-	mV
			3V ≤ V_{CC} ≤ 3.6V	Full	-	70	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -1mA, V_{ID} = 200mV		Full	**V_{CC} - 0.4**	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 2mA, V_{ID} = -200mV		Full	-	-	**0.4**	V
Three-State (High Impedance) Receiver Output Current (Note 12)	I_{OZR}	0V ≤ V_O ≤ V_{CC}		Full	**-1**	-	**1**	µA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	-	-	**30**	mA
No-Load Supply Current	I_{CC}	$\overline{RE}$ = 0V or RE = V_{CC}	V_{CC} = 1.8V	Full	-	85	**110**	µA
			3V ≤ V_{CC} ≤ 3.6V	Full	-	-	**135**	µA
Shutdown Supply Current (Note 10, 12)	I_{SHDN}	ISL32611, $\overline{RE}$ = V_{CC}, V_{CC} ≥ 1.8V		Full	-	-	**2**	µA
		ISL32612, RE = 0V	V_{CC} = 1.8V	Full	-	-	**7**	µA
			V_{CC} ≤ 3.6V	Full	-	-	**14**	µA

Electrical Specifications Test Conditions: V_{CC} = 1.8V; typical values are at V_{CC} = 1.8V, T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** (Note 9) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
SWITCHING CHARACTERISTICS								
Maximum Data Rate	f_{MAX}	V_{ID} = ±1V, V_{CM} = 0V, (Figure 5)	V_{CC} = 1.8V	Full	**256**	-	-	kbps
			3V ≤ V_{CC} ≤ 3.6V	Full	**500**	-	-	kbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 5)	V_{CC} = 1.8V	Full	-	210	**1000**	ns
			V_{CC} = 3.3V	25	-	200	-	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 5)	V_{CC} = 1.8V	Full	-	3	**125**	ns
			V_{CC} = 3.3V	25	-	6	-	ns
Receiver Enable to Output High	t_{ZH}	C_L = 15pF, SW = GND, (Figure 6, Note 12)	V_{CC} = 1.8V	Full	-	1100	**4000**	ns
			V_{CC} = 3.3V	25	-	1500	-	ns
Receiver Enable to Output Low	t_{ZL}	C_L = 15pF, SW = V_{CC}, (Figure 6, Note 12)	V_{CC} = 1.8V	Full	-	1100	**4000**	ns
			V_{CC} = 3.3V	25	-	1500	-	ns
Receiver Disable from Output High	t_{HZ}	C_L = 15pF, SW = GND, (Figure 6, Note 12)	V_{CC} = 1.8V	Full	-	15	**75**	ns
			V_{CC} = 3.3V	25	-	6	-	ns
Receiver Disable from Output Low	t_{LZ}	C_L = 15pF, SW = V_{CC}, (Figure 6, Note 12)	V_{CC} = 1.8V	Full	-	15	**75**	ns
			V_{CC} = 3.3V	25	-	6	-	ns
ESD PERFORMANCE								
RS-485 Pins (A, B)		IEC61000-4-2, Air-Gap Discharge Method		25	-	±16.5	-	kV
		IEC61000-4-2, Contact Discharge Method		25	-	±9	-	kV
		Human Body Model, From Bus Pins to GND		25	-	±16.5	-	kV
All Pins		Human Body Model (Tested per JESD22-A114E)		25	-	±8	-	kV
		Machine Model (Tested per JESD22-A115-A)		25	-	±400	-	V

NOTES:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
9. Currents into device pins are positive; currents out of device pins are negative. Voltages are referenced to ground unless otherwise specified.
10. The ISL32611E enters SHDN whenever $\overline{RE}$ switches high, and the ISL32612E enters SHDN whenever RE switches low.
11. Devices meeting these limits are denoted as 1/8 unit load (1/8 UL)" transceivers. The RS-485 standard allows up to 32 unit loads on the bus, so there can be 256 1/8 UL devices on a bus.
12. Not applicable to the ISL32610E.

Test Circuits and Waveforms

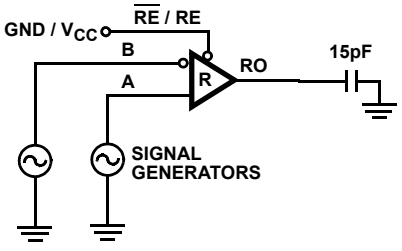


FIGURE 5A. TEST CIRCUIT

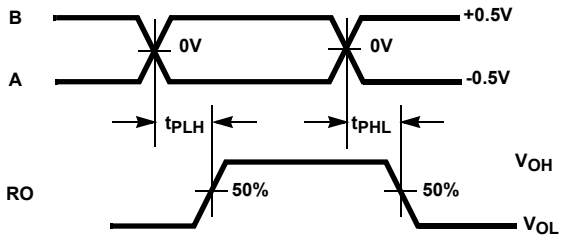
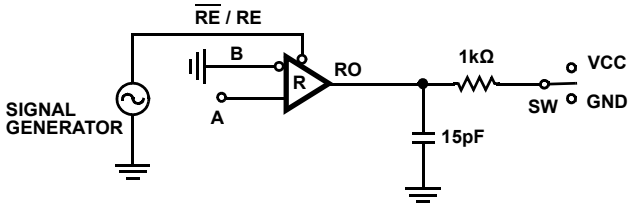


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY AND DATA RATE

Test Circuits and Waveforms (Continued)



PARAMETER	A	SW
t_{HZ}	+1V	GND
t_{LZ}	-1V	V_{CC}
t_{ZH}	+1V	GND
t_{ZL}	-1V	V_{CC}

FIGURE 6A. TEST CIRCUIT

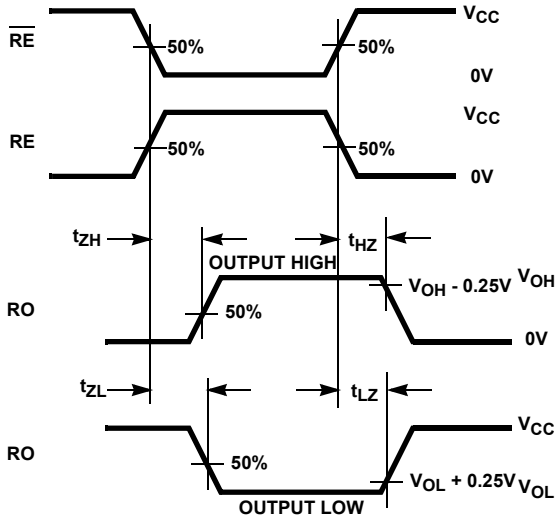


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES (EXCLUDING ISL32610E)

Typical Performance Curves T_A = +25°C; Unless Otherwise Specified

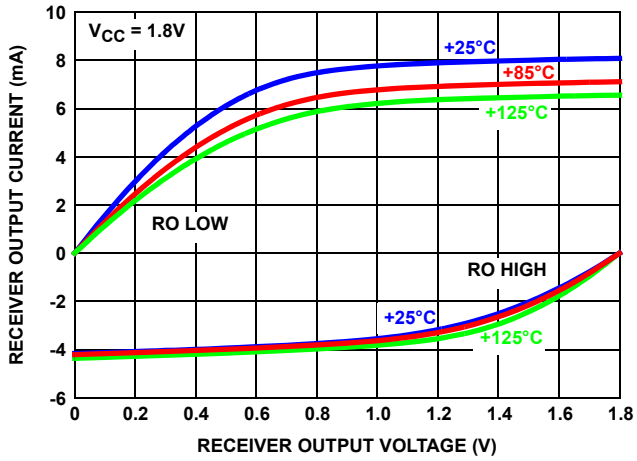


FIGURE 7. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE (V_{CC} = 1.8V)

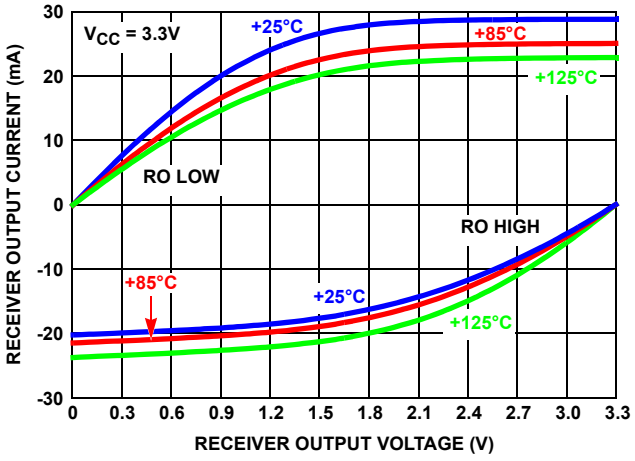


FIGURE 8. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE (V_{CC} = 3.3V)

Typical Performance Curves T_A = +25°C; Unless Otherwise Specified

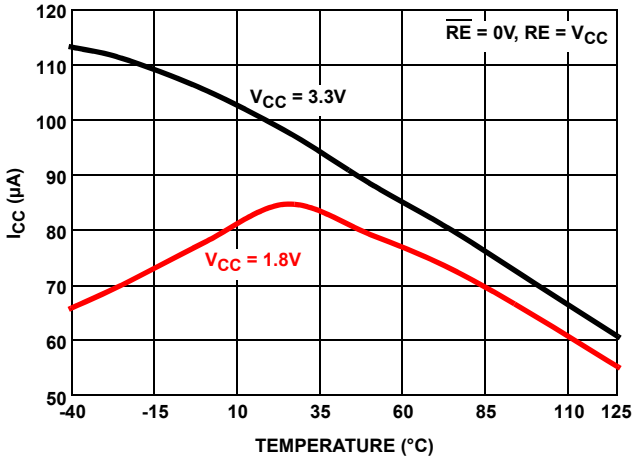


FIGURE 9. STATIC SUPPLY CURRENT vs TEMPERATURE

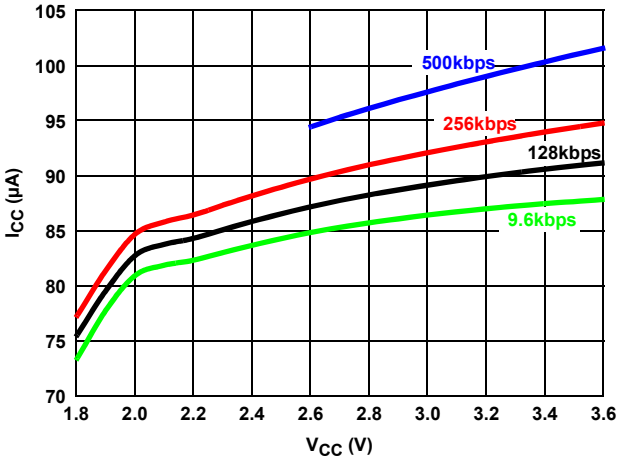


FIGURE 10. DYNAMIC SUPPLY CURRENT vs SUPPLY VOLTAGE AT DIFFERENT DATA RATES

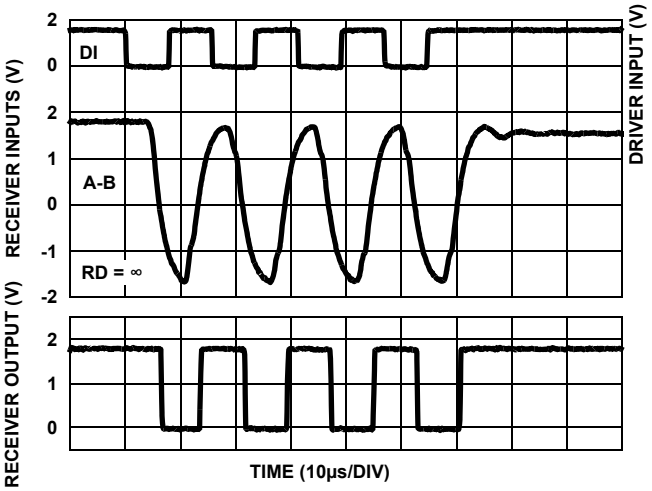


FIGURE 11. ISL32613E AND ISL32611E PERFORMANCE WITH V_{CC} = 1.8V, 128kbps, 2000' (610m) CAT 5 CABLE

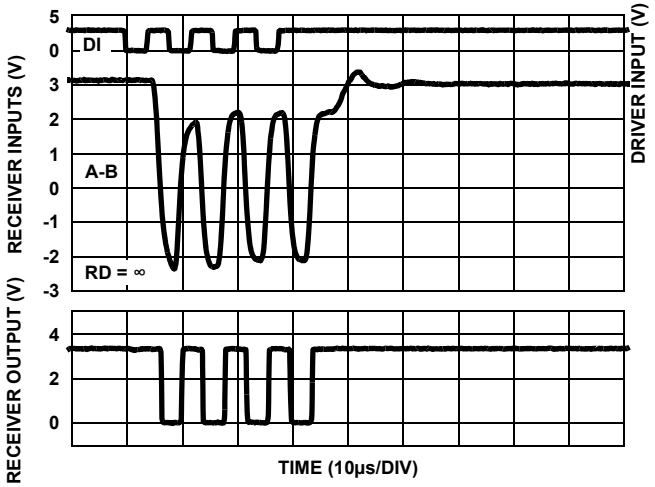


FIGURE 12. ISL32613E AND ISL32611E PERFORMANCE WITH V_{CC} = 3.3V, 256kbps, 3000' (915m) CAT 5 CABLE

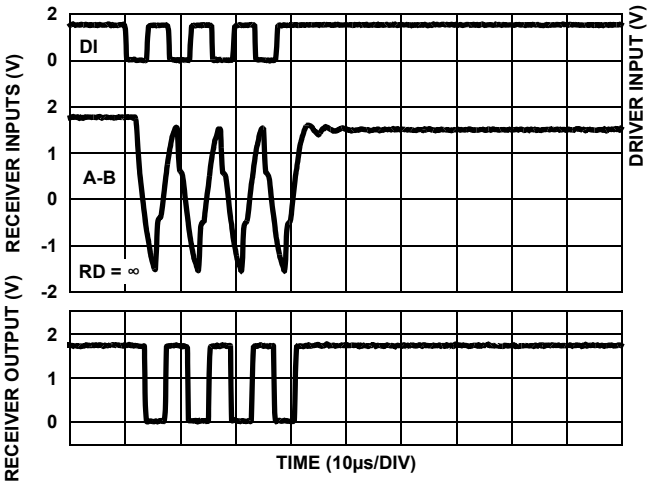


FIGURE 13. ISL32614E AND ISL32611E PERFORMANCE WITH V_{CC} = 1.8V, 256kbps, 1000' (305m) CAT 5 CABLE

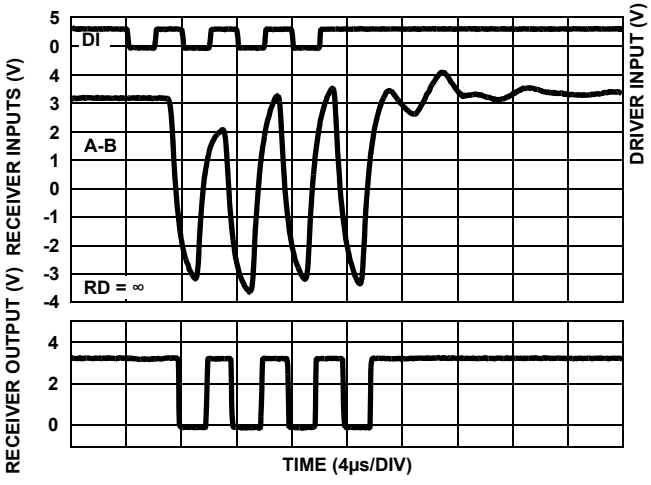


FIGURE 14. ISL32614E AND ISL32611E PERFORMANCE WITH V_{CC} = 3.3V, 500kbps, 2000' (610m) CAT 5 CABLE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP) :

GND

PROCESS:

Si Gate BiCMOS

Application Information

Features

The ISL3261xE devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 standards. The symmetrical ±200mV switching thresholds of the receivers deliver less duty cycle distortion than similar receivers with a full-failsafe design (for example, skewed low/high input thresholds, (such as -200mV/-20mV), which increase the high bit width). This distortion is especially noticeable when the Rx is driven by slow input transitions (see Figure 2).

The symmetrical input thresholds also allow more room for increased input hysteresis, thereby increasing the Rx noise immunity. The 70mV hysteresis of this Rx is twice the amount specified for most full-failsafe devices.

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ, and it is eight times the RS-485 Unit Load (UL)" requirement of 12kΩ minimum. Therefore, the products are known as one-eighth UL" receivers, and there can be up to 256 of the devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages (CMV) of ±2V with V_{CC} = 1.8V, and with CMVs of -7V to +12V for V_{CC} ≥ 2.7V.

All the receivers include a failsafe-if-open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating). As mentioned previously, the full-failsafe function is not implemented to deliver output duty cycles that better match the input.

Receivers support data rates up to 256kbps (V_{CC} = 1.8V) or 500kbps (V_{CC} ≥ 3V), and receiver outputs of the ISL32611E and ISL32612E are three-statable using the active low $\overline{RE}$ or active high RE input.

Data Rate Recommendations

When coupled with the ISL32613E or ISL32614E 1.8V transmitter ICs, the receivers are useful for networks up to 4000' (1220m) long, or for data rates up to 500kbps. For 4000' distances with V_{CC} = 1.8V, the ISL32613E can be used with any of these receivers at data rates ≤ 50kbps. With V_{CC} = 3.3V, any transmitter/receiver combination operates over 4000' at rates up to 128kbps. Shorter networks allow data rates up to 500kbps, as shown in Figures 11, 12, 13 and 14.

Network termination resistors are only recommended for networks operating at V_{CC} ≥ 2.7V, and using termination resistors may allow for higher data rates.

Low Power Shutdown Mode (ISL32611E and ISL32612E)

The devices use a fraction of the power required by most differential receivers (see Figure 1), but they also include a shutdown feature that reduces the already low quiescent I_{CC} even further. The ISL32611E and ISL32612E enter shutdown whenever the receiver is disabled (RE = GND or $\overline{RE}$ = V_{CC}).

ESD Protection

All pins on the devices include class 3 (>6kV) Human Body Model (HBM) ESD protection structures, but the bus pins (Rx inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±16.5kV HBM and ±16.5kV IEC61000. The bus pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. The new ESD structures protect the device whether or not it is powered up, and without degrading the common-mode range. This built-in ESD protection eliminates the need for board-level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the bus pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The smaller value current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's bus pins allows the design of equipment meeting level 4 criteria without the need for additional board-level protection on the I/O port.

AIR-GAP DISCHARGE TEST METHOD

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The A and B pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The ISL32610E, ISL32611E, and ISL32612E survive ±9kV contact discharges on the bus pins.

Revision History

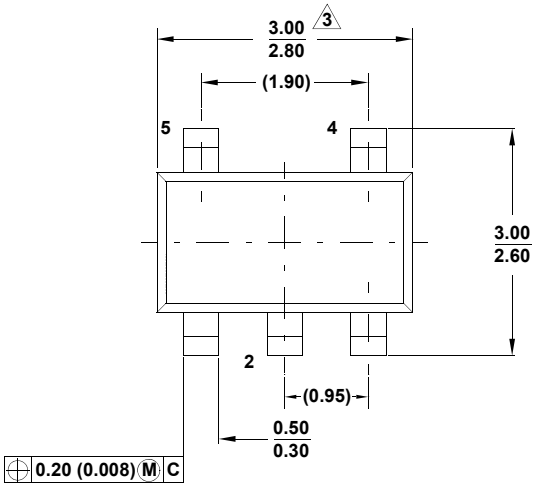
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 26, 2019	FN7869.2	Updated Figures 3 and 4 and removed note on page2.
Feb 15, 2019	FN7869.1	Added Related Literature section Updated Typical Operating Circuit and added a second. Updated links throughout document. Removed About Intersil section. Updated disclaimer.
Oct 21, 2011	FN7869.0	Initial Release

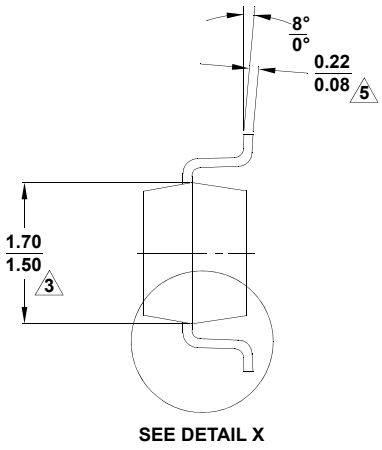
Package Outline Drawings

For the most recent package outline drawing, see P5.064.

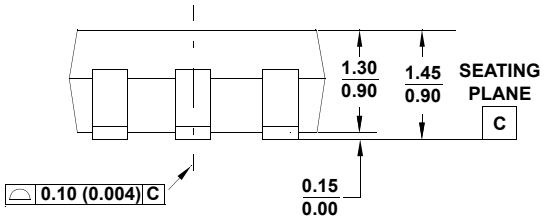
P5.064
5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 3, 4/11



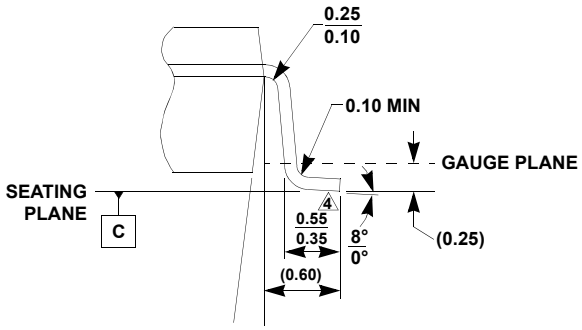
TOP VIEW



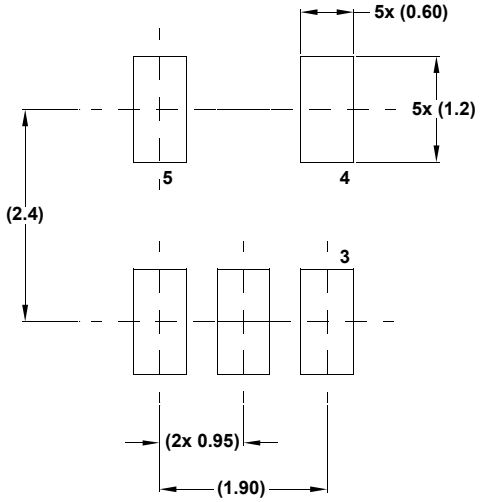
END VIEW



SIDE VIEW



DETAIL "X"



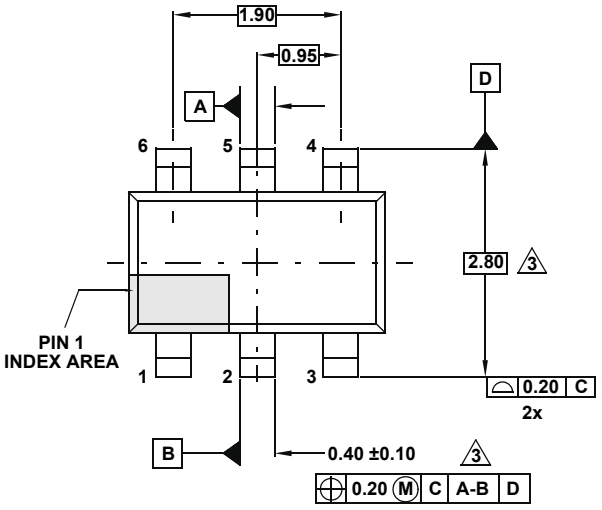
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

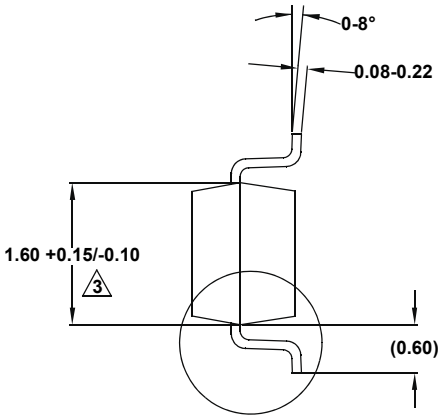
1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER. Dimensions in ( ) for reference only.

P6.064
6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 4, 2/10

For the most recent package outline drawing, see P6.064.

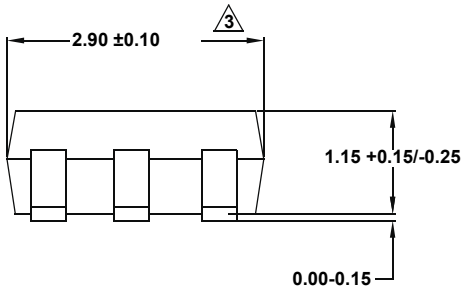


TOP VIEW

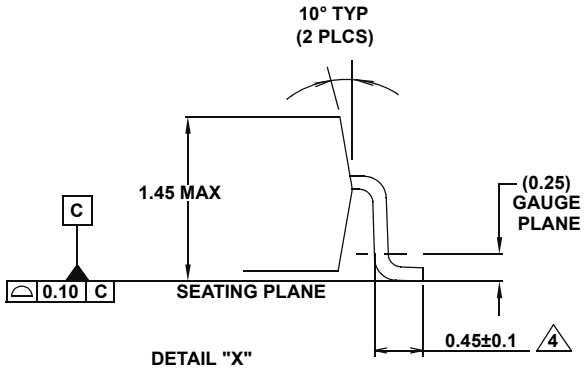


SEE DETAIL X

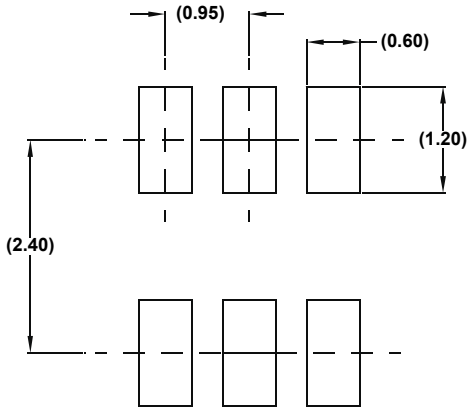
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. Package conforms to JEDEC MO-178AB.