ISL33001, ISL33002, ISL33003

I2C Bus Buffer with Rise Time Accelerators and Hot Swap Capability

FN7560
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The ISL33001, ISL33002, ISL33003 are 2-Channel Bus Buffers that provide the buffering necessary to extend the bus capacitance beyond the 400pF maximum specified by the I^2C specification. In addition, the ISL33001, ISL33002, ISL33003 feature rise time accelerator circuitry to reduce power consumption from passive bus pull-up resistors and improve data-rate performance. All devices also include hot swap circuitry to prevent corruption of the data and clock lines when I^2C devices are plugged into a live backplane, and the ISL33002 and ISL33003 add level translation for mixed supply voltage applications. The ISL33001, ISL33002, ISL33003 operate at supply voltages from +2.3V to +5.5V at a temperature range of -40°C to +85°C.

Summary of Features

PART NUMBER	LEVEL TRANSLATION	ENABLE PIN	READY PIN	ACCELERATOR DISABLE
ISL33001	No	Yes	Yes	No
ISL33002	Yes	No	No	Yes
ISL33003	Yes	Yes	No	No

Features

- 2 Channel I^2C compatible bi-directional buffer
- +2.3VDC to +5.5VDC supply range
- >400kHz operation
- Bus capacitance buffering
- Rise time accelerators
- Hot swapping capability
- ±6kV Class 3 HBM ESD protection on all pins
- ±12kV HBM ESD protection on SDA/SCL pins
- Enable pin (ISL33001 and ISL33003)
- Logic level translation (ISL33002 and ISL33003)
- READY logic pin (ISL33001)
- Accelerator disable pin (ISL33002)
- Pb-free (RoHS Compliant) 8 Ld SOIC (ISL33001 only), 8 Ld TDFN (3mmx3mm) and 8 Ld MSOP packages
- Low quiescent current . . . . . 2.1mA typ
- Low shutdown current . . . . . 0.5µA typ

Applications

- I^2C bus extender and capacitance buffering
- Server racks for telecom, datacom, and computer servers
- Desktop computers
- Hot-swap board insertion and bus isolation

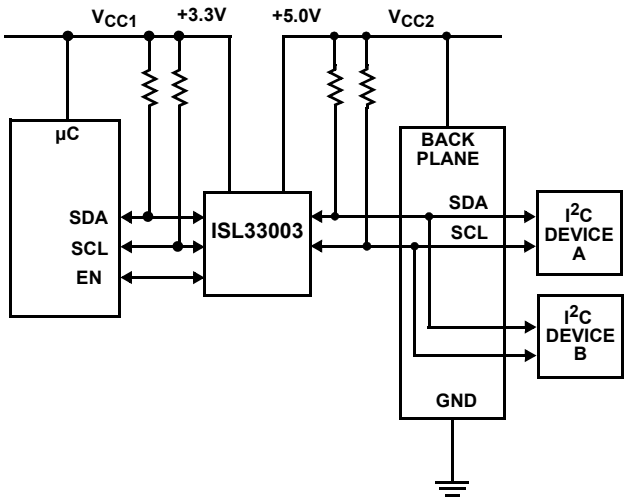

FIGURE 1. TYPICAL OPERATING CIRCUIT

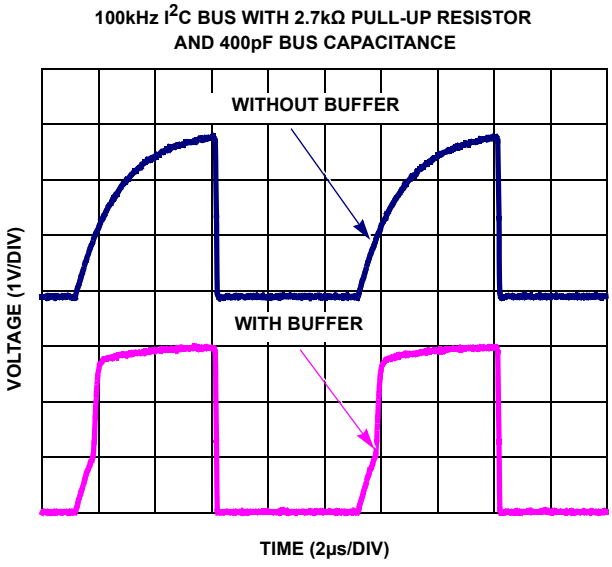

FIGURE 2. BUS ACCELERATOR PERFORMANCE

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Ordering Information

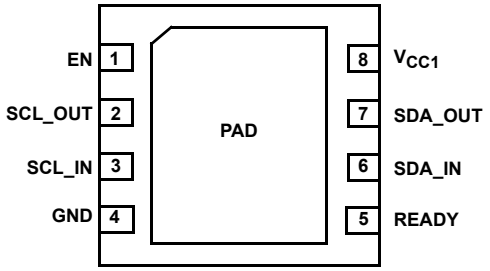
PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL33001IRTZ	3001	8 Ld TDFN (0.65mm Pitch)	L8.3x3A	Tube	-40 to +85°C
ISL33001IRTZ-T				Reel, 6k	
ISL33001IRT2Z	01R2	8 Ld TDFN (0.5mm Pitch)	L8.3x3H	Tube	
ISL33001IRT2Z-T				Reel, 6k	
ISL33001IBZ	33001 IBZ	8 Ld SOIC	M8.15	Tube	
ISL33001IBZ-T				Reel, 2.5k	
ISL33001IUZ	33001	8 Ld MSOP	M8.118	Tube	
ISL33001IUZ-T				Reel, 2.5k	
ISL33002IRTZ	3002	8 Ld TDFN (0.65mm Pitch)	L8.3x3A	Tube	
ISL33002IRTZ-T				Reel, 6k	
ISL33002IRT2Z	02R2	8 Ld TDFN (0.5mm Pitch)	L8.3x3H	Tube	
ISL33002IRT2Z-T				Reel, 6k	
ISL33002IUZ	33002	8 Ld MSOP	M8.118	Tube	
ISL33002IUZ-T				Reel, 2.5k	
ISL33003IRTZ	3003	8 Ld TDFN (0.65mm Pitch)	L8.3x3A	Tube	
ISL33003IRTZ-T				Reel, 6k	
ISL33003IRT2Z	03R2	8 Ld TDFN (0.5mm Pitch)	L8.3x3H	Tube	
ISL33003IRT2Z-T				Reel, 6k	
ISL33003IUZ	33003	8 Ld MSOP	M8.118	Tube	
ISL33003IUZ-T				Reel, 2.5k	
ISL33001MSOPEVAL1Z	ISL33001 Evaluation Board				
ISL33002MSOPEVAL1Z	ISL33002 Evaluation Board				
ISL33003MSOPEVAL1Z	ISL33003 Evaluation Board				

NOTES:

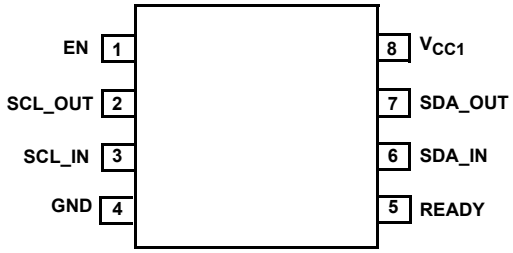
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL33001, ISL33002, and ISL33003 product information pages. For more information about MSL, see TB363.

Pin Configurations

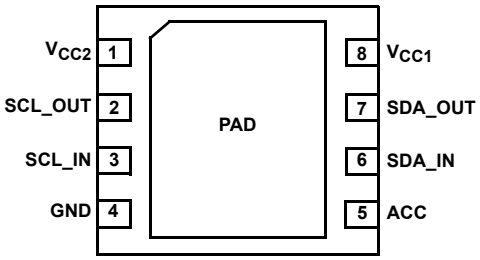
ISL33001
(8 LD TDFN)
TOP VIEW



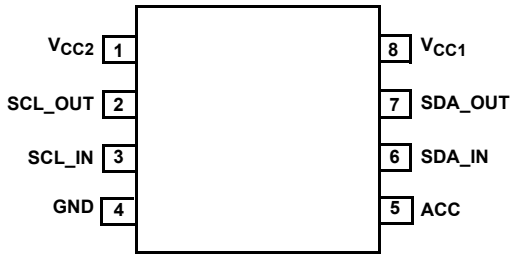
ISL33001
(8 LD SOIC, MSOP)
TOP VIEW



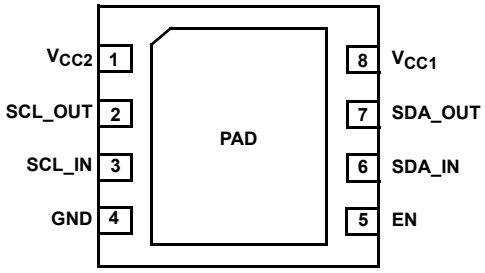
ISL33002
(8 LD TDFN)
TOP VIEW



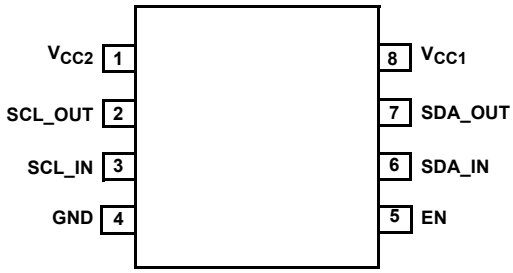
ISL33002
(8 LD MSOP)
TOP VIEW



ISL33003
(8 LD TDFN)
TOP VIEW



ISL33003
(8 LD MSOP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	FUNCTION	NOTES
V_{CC1}	8	V_{CC1} power supply, +2.3V to +5.5V. Decouple V_{CC1} to ground with a high frequency 0.01µF to 0.1µF capacitor.	
V_{CC2}	1	V_{CC2} power supply, +2.3V to +5.5V. Decouple V_{CC2} to ground with a high frequency 0.01µF to 0.1µF capacitor. In level shifting applications, SDA_OUT and SCL_OUT logic thresholds are referenced to V_{CC2} supply levels. Connect pull-up resistors on these pins to V_{CC2}.	ISL33002 (8 LD TDFN, 8 LD MSOP) ISL33003 (8 LD TDFN, 8 LD MSOP)
GND	4	Device Ground Pin	
EN	1	Buffer Enable Pin. Logic “0” disables the device. Logic “1” enables the device. Logic threshold referenced to V_{CC1}.	ISL33001 (8 LD TDFN, 8 LD SOIC, MSOP)
	5		ISL33003 (8 LD TDFN, 8 LD MSOP)
READY	5	Buffer active ‘Ready’ open drain logic output. When buffer is active, READY is high impedance. When buffer is inactive, READY is low impedance to ground. Connect to 10kΩ pull-up resistor to V_{CC1}.	ISL33001 only
ACC	5	Rise Time Accelerator Enable Pin. Logic “0” disables the accelerator. Logic “1” enables the accelerator. Logic threshold referenced to V_{CC1}.	ISL33002 only
SDA_IN	6	Data I/O Pins	
SDA_OUT	7		
SCL_IN	3	Clock I/O Pins	
SCL_OUT	2		
PAD		Thermal pad should be connected to ground or floated.	Thermal Pad; TDFN only

Absolute Maximum Ratings (All voltages referenced to GND)

V_{CC1}, V_{CC2} ..... -0.3V to +7V
SDA_IN, SCL_IN, SDA_OUT, SCL_OUT, READY ..... -0.3V to +7V
EN, ACC ..... -0.3V to +(V_{CC1} + 0.3)V
Maximum Sink Current (SDA and SCL Pins) 20mA
Maximum Sink Current (READY pin) 7mA
Latch-Up Tested per JESD78, Level 2, Class A ..... 85°C
ESD Ratings ..... See "ESD PROTECTION" on page 7

Operating Conditions

Temperature Range, T_A ..... -40°C to +85°C
V_{CC1} and V_{CC2} Supply Voltage Range ..... +2.3V to +5.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 5, 6) (0.50mm Pitch)	47	4
8 Ld TDFN Package (Notes 5, 6) (0.65mm Pitch)	48	6
8 Ld MSOP Package (Notes 4, 7)	151	50
8 Ld SOIC Package (Notes 4, 7)	120	56

Maximum Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C
Pb-Free Reflow Profile ..... see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
6. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the case temperature location is taken at the package top center.

Electrical Specifications

V_{EN} = V_{CC1}, V_{CC1} = +2.3V to +5.5V, V_{CC2} = +2.3V to +5.5V, unless otherwise noted (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
POWER SUPPLIES							
V_{CC1} Supply Range	V_{CC1}		Full	**2.3**	-	**5.5**	V
V_{CC2} Supply Range	V_{CC2}	ISL33002 and ISL33003	Full	**2.3**	-	**5.5**	V
Supply Current from V_{CC1}	I_{CC1}	V_{CC1} = 5.5V; ISL33001 only (Note 11)	Full	-	2.1	**4.0**	mA
		V_{CC1} = V_{CC2} = 5.5V; ISL33002 and ISL33003 (Note 11)	Full	-	2.0	**3.0**	mA
Supply Current from V_{CC2}	I_{CC2}	V_{CC2} = V_{CC1} = 5.5V; ISL33002 and ISL33003 (Note 11)	Full	-	0.22	**0.6**	mA
V_{CC1} Shutdown Supply Current	I_{SHDN1}	V_{CC1} = 5.5V, V_{EN} = GND; ISL33001 only	Full	-	0.5	-	µA
		V_{CC1} = V_{CC2} = 5.5V, V_{EN} = GND; ISL33003 only (Note 13)	Full	-	0.05	-	µA
V_{CC2} Shutdown Supply Current	I_{SHDN2}	V_{CC1} = V_{CC2} = 5.5V, V_{EN} = GND, ISL33003 only (Note 13)	Full	-	0.06	-	µA
START-UP CIRCUITRY							
Precharge Circuitry Voltage	V_{PRE}	SDA and SCL pins floating	Full	**0.8**	1	**1.2**	V
Enable High Threshold Voltage	V_{EN_H}		+25	-	0.5*V_{CC}	0.7*V_{CC}	V
Enable Low Threshold Voltage	V_{EN_L}		+25	0.3*V_{CC}	0.5*V_{CC}	-	V
Enable Pin Input Current	I_{EN}	Enable from 0V to V_{CC1}, ISL33001 and ISL33003	Full	**-1**	0.1	**1**	µA
Enable Delay, On-Off	t_{EN-HL}	ISL33001 and ISL33003 (Note 10)	+25	-	10	-	ns
Enable Delay, Off-On	t_{EN-LH}	ISL33001 and ISL33003 (Figure 3)	+25	-	86	-	µs
Bus Idle Time	t_{IDLE}	(Figure 4, Note 12)	Full	**50**	83	**150**	µs
Ready Pin OFF State Leakage Current	I_{OFF}	ISL33001 only	+25	**-1**	0.1	**1**	µA
Ready Delay, On-Off	$t_{READY-HL}$	ISL33001 only (Note 10)	+25	-	10	-	ns

Electrical Specifications V_{EN} = V_{CC1}, V_{CC1} = +2.3V to +5.5V, V_{CC2} = +2.3V to +5.5V, unless otherwise noted (Note 8). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Ready Delay, Off-On	$t_{READY-LH}$	ISL33001 only (Note 10)	+25	-	10	-	ns
Ready Output Low Voltage	V_{OL_READY}	V_{CC1} = +2.5V, I_{PULLUP} = 3mA; ISL33001 only	Full	-	-	**0.4**	V
RISE-TIME ACCELERATORS							
Transient Accelerator Current	I_{TRAN_ACC}	V_{CC1} = 2.7V, V_{CC2} = 2.7V ; (ACC = 0.7*V_{CC1} for ISL33002 only) (Figure 8)	+25	-	5	-	mA
Accelerator Pin Enable Threshold	V_{ACC_EN}	ISL33002 only	+25	-	0.5*V_{CC1}	0.7*V_{CC1}	V
Accelerator Pin Disable Threshold	V_{ACC_DIS}	ISL33002 only	+25	0.3*V_{CC1}	0.5*V_{CC1}	-	V
Accelerator Pin Input Current	I_{ACC}	ISL33002 only	+25	-1	0.1	1	µA
Accelerator Delay, On-Off	t_{PDOFF}	ISL33002 only (Note 10)	+25	-	10	-	ns
ESD PROTECTION							
SDA, SCL I/O Pins		Human Body Model, SDA and SCL pins to ground only (JESD22-A114)	+25	-	±12	-	kV
All Pins		Machine Model (JESD22-A115)	+25	-	±400	-	V
		Class 3 HBM ESD (JESD22-A114)	+25		±6	-	kV
INPUT-OUTPUT CONNECTIONS							
Input Low Threshold	V_{IL}	V_{CC1} = V_{CC2}, 10kΩ to V_{CC1} on SDA and SCL pins	+25	-	-	0.3*V_{CC1}	V
Input-Output Offset Voltage	V_{OS}	V_{CC1} = 3.3V, 10kΩ to V_{CC1} on SDA and SCL pins, V_{INPUT} = 0.2V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 5)	Full	**0**	50	**150**	mV
Output Low Voltage	V_{OL}	V_{CC1} = 2.7V, V_{INPUT} = 0V, I_{SINK} = 3mA on SDA/SCL pins; V_{CC2} = 2.7V, ISL33002 and ISL33003 (Figure 6)	Full	-	-	**0.4**	V
Buffer SDA and SCL Pins Input Capacitance	C_{IN}	(Figure 27)	+25	-	10	-	pF
Input Leakage Current	I_{LEAK}	SDA and SCL pins = V_{CC1} = 5.5V; V_{CC2} = 5.5V, ISL33002 and ISL33003	Full	**-5**	0.1	**5**	µA
TIMING CHARACTERISTICS							
SCL/SDA Propagation Delay High-to-Low	t_{PHL}	C_{LOAD} = 100pF, 2.7kΩ to V_{CC1} on SDA and SCL pins, V_{CC1} = 3.3V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 7)	+25	0	27	100	ns
SCL/SDA Propagation Delay Low-to-High	t_{PLH}	C_{LOAD} = 100pF, 2.7kΩ to V_{CC1} on SDA and SCL pins, V_{CC1} = 3.3V; V_{CC2} = 3.3V, ISL33002 and ISL33003 (Figure 7)	+25	0	2	26	ns

NOTES:

8. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Typical value determined by design simulations. Parameter not tested.
11. Buffer is in the connected state.
12. ISL33002 and ISL33003 limits established by characterization. Not production tested.
13. If the V_{CC1} and V_{CC2} voltages diverge, then the shut down I_{CC} increases on the higher voltage supply.

Test Circuits and Waveforms

- SDA_OUT and SCL pins connected to V_{CC}
- Enable Delay Time Measured on ISL33001 only
- ISL33003 performance inferred from ISL33001
- If $t_{DELAY1} < t_{EN-LH}$ then $t_{DELAY2} = t_{EN-LH} + t_{IDLE} + t_{READY-LH}$
- If $t_{DELAY1} > t_{EN-LH}$ then $t_{DELAY2} = t_{EN-LH} + t_{READY-LH}$

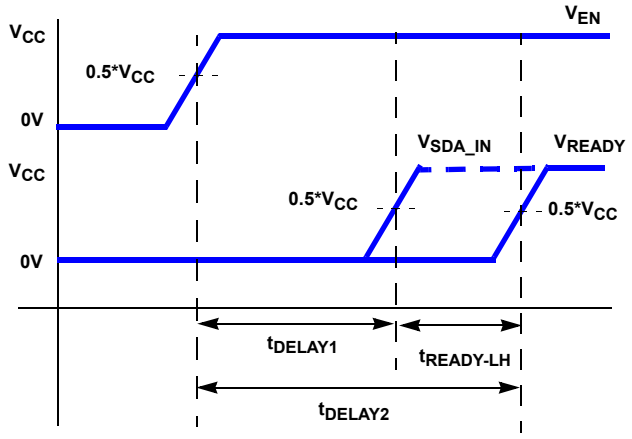


FIGURE 3. ENABLE DELAY TIME

- $V_{SDA\_IN} = V_{SDA\_OUT} = V_{SCL\_OUT} = V_{EN} = V_{CC}$
- EN Logic Input must be high for t > Enable Delay (t_{EN_LH}) prior to SCL_IN transition
- Bus Idle Time Measured on ISL33001 only
- ISL33002 and ISL33003 performance inferred from ISL33001

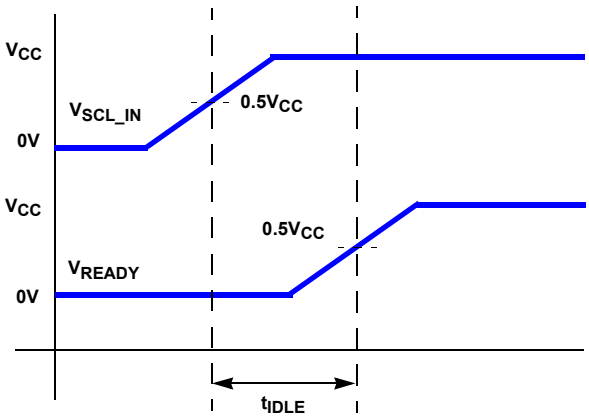


FIGURE 4. BUS IDLE TIME

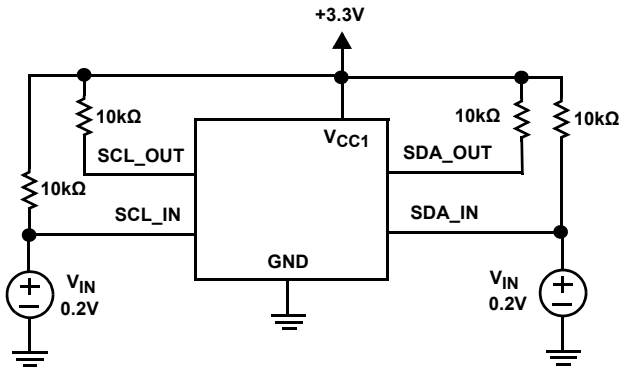


FIGURE 5A. TEST CIRCUIT

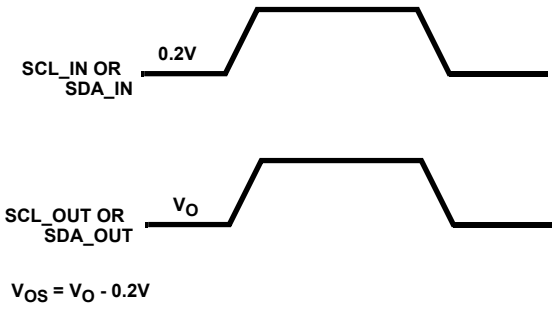


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. INPUT TO OUTPUT OFFSET VOLTAGE

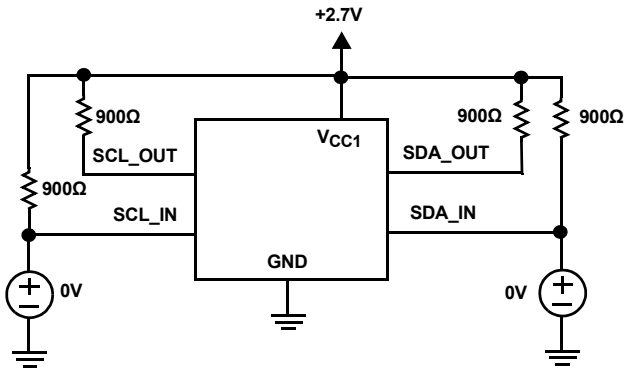


FIGURE 6A. TEST CIRCUIT

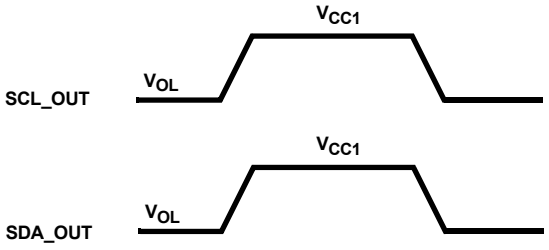


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. OUTPUT LOW VOLTAGE

Test Circuits and Waveforms (Continued)

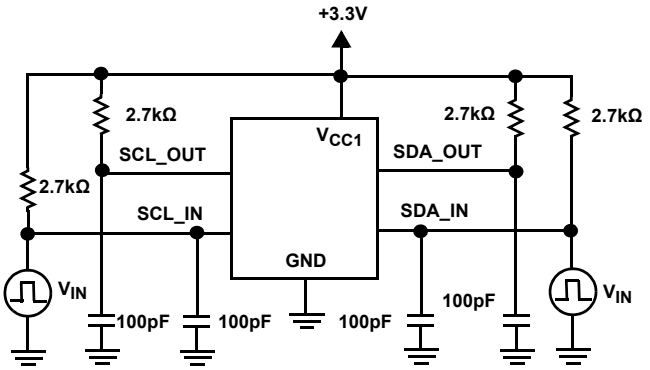
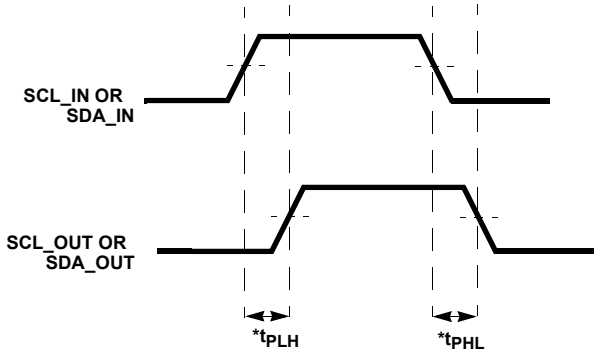


FIGURE 7A. TEST CIRCUIT



*Propagation delay measured between 50% of V_{CC1}

FIGURE 7B. MEASUREMENT POINTS

FIGURE 7. PROPAGATION DELAY

$I_{TRAN\_ACC} = C\Delta V/\Delta t$
$\Delta V/\Delta t$ is for only the accelerator portion of the waveform

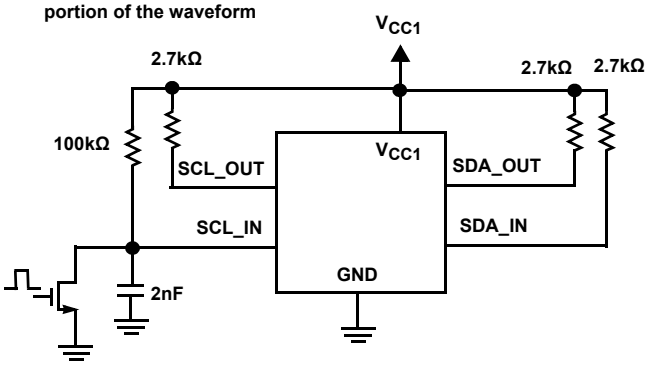


FIGURE 8. ACCELERATOR CURRENT TEST CIRCUIT

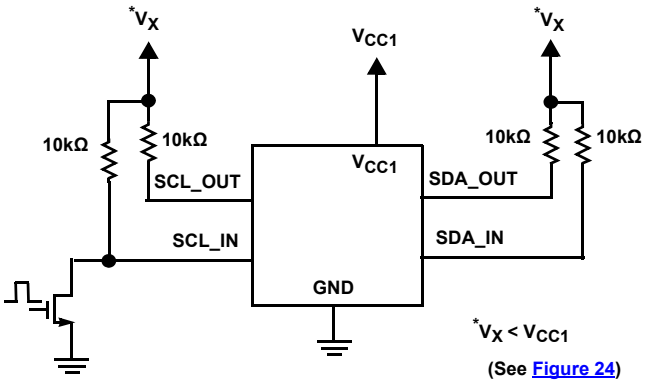


FIGURE 9. ACCELERATOR PULSE WIDTH TEST CIRCUIT

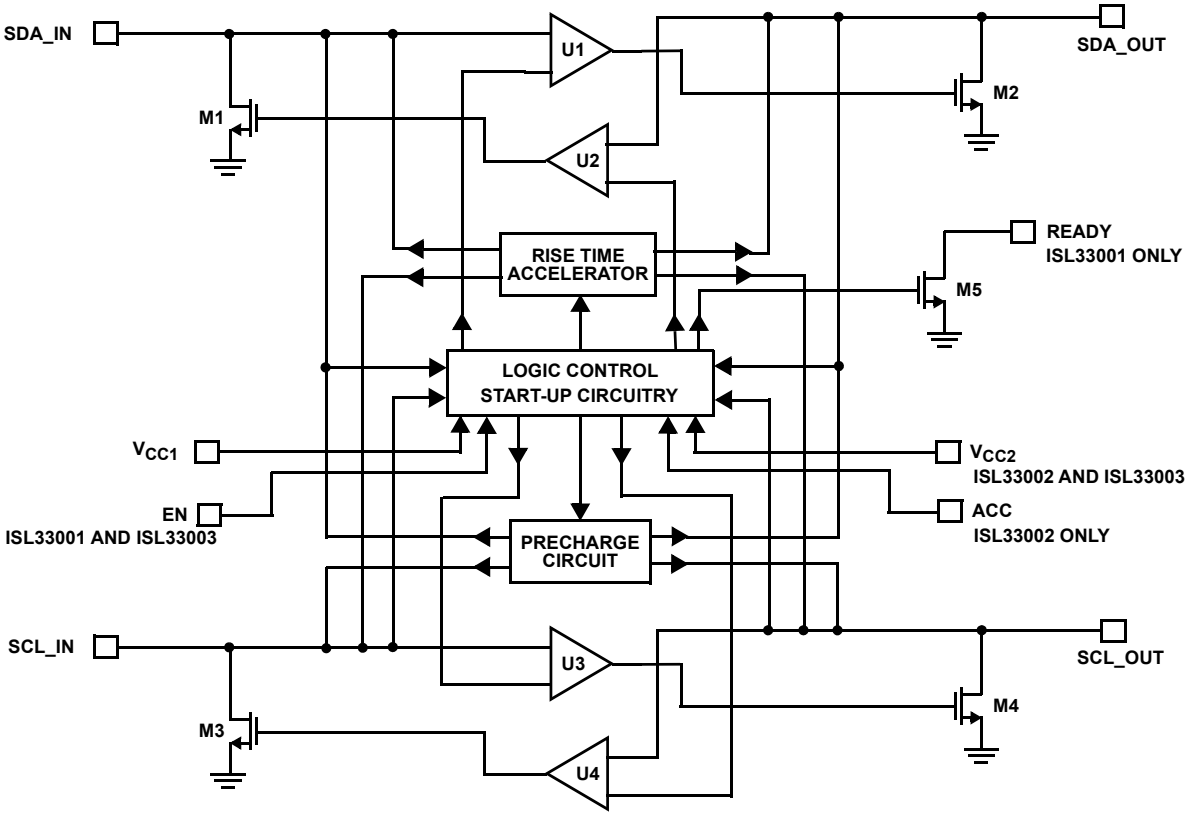


FIGURE 10. CIRCUIT BLOCK DIAGRAM

Application Information

The ISL33001, ISL33002, ISL33003 ICs are 2-Wire Bidirectional Bus Buffers designed to drive heavy capacitive loads in open-drain/open-collector systems. The ISL33001, ISL33002, ISL33003 incorporate rise time accelerator circuitry that improves the rise time for systems that use a passive pull-up resistor for logic HIGH. These devices also feature hot swapping circuitry for applications that require hot insertion of boards into a host system (i.e., servers racks and I/O card modules). The ISL33001 features a logic output flag (READY) that signals the status of the buffer and an EN pin to enable or disable the buffer. The ISL33002 features two separate supply pins for voltage level shifting on the I/O pins and a logic input to disable the rise time accelerator circuitry. The ISL33003 features an EN pin and the level shifting functionality.

I^2C and SMBUS Compatibility

The ISL33001, ISL33002, ISL33003 ICs are I^2C and SMBUS compatible devices, designed to work in open-drain/open-collector bus environments. The ICs support both clock stretching and bus arbitration on the SDA and SCL pins. They are designed to operate from DC to more than 400kHz, supporting Fast Mode data rates of the I^2C specification.In addition, the buffer rise time accelerators are designed to increase the capacitive drive capability of the bus. With careful choosing of components, driving a bus with the I^2C specified maximum bus capacitance of 400pF at 400kHz data rate is possible.

Start-Up Sequencing and Hot Swap Circuitry

The ISL33001, ISL33002, ISL33003 buffers contain undervoltage lock out (UVLO) circuitry that prevents operation of the buffer until the IC receives the proper supply voltage. For V_{CC1} and V_{CC2}, this voltage is approximately 1.8V on the rising edge of the supply voltage. Externally driven signals at the SDA/SCL pins are ignored until the device supply voltage is above 1.8V. This prevents communication errors on the bus until the device is properly powered up. The UVLO circuitry is also triggered on the falling edge when the supply voltage drops below 1.7V.

Once the IC comes out of the UVLO state, the buffer remains disconnected until it detects a valid connection state. A valid connection state is either a BUS IDLE condition (see Figure 4) or a STOP BIT condition (a rising edge on SDA_IN when SCL_IN is high) along with the SCL_OUT and SDA_OUT pins being logic high.

Note: For the ISL33001 and ISL33003 with EN pins, after coming out of UVLO, there will be an additional delay from the enable circuitry if the EN pin voltage is not rising at the same time as the supply pins (see Figure 3) before a valid connection state can be established.

Coming out of UVLO but prior to a valid connection state, the SDA and SCL pins are pre-charged to 1V to allow hot insertion. Because the bus at any time can be between 0V and V_{CC}, pre-charging the I/O pins to 1V reduces the maximum differential voltage from the buffer I/O pin and the active bus. The pre-charge circuitry reduces system disturbance when the IC is hot plugged into a live back plane that may have the bus communicating with other devices.

Note: For The ISL33001 and ISL33003 with EN pins, the pre-charge circuitry is active only after coming out of UVLO and having the device enabled.

Connection Circuitry

Once a valid connection condition is met, the buffer is active and the input stage of the SDA/SCL pins is controlled by external drivers. The output of the buffer will follow the input of the buffer. The directionality of the IN/OUT pins are not exclusive (bi-directional operation) and functionally behave identical to each other. Being a two channel buffer, the SDA and SCL pins also behave identically. In addition, the SDA and SCL portions of the buffer are independent from each other. The SDA pins can be driven in one direction while the SCL pins can be driven opposite.

Refer to Figure 10 for the operation of the bi-directional buffer. When the input stage of the buffer on one side is driven low by an external device, the output of the buffer drives an open-drain transistor to pull the ‘output’ pin low. The ‘output’ pin will continue to be held low by the transistor until the external driver on the ‘input’ releases the bus.

To prevent the buffer from entering a latched condition where both internal transistors are actively pulling the I/O pins low, the buffer is designed to be active in only one direction. The buffer logic circuitry senses, which input stage is being externally driven low and sets that buffer to be the active one. For example, referring to Figure 10, if SDA_OUT is externally driven low, buffer U2 will be active and buffer U1 is inactive. M1 is turned on to drive SDA_IN low, effectively buffering the signal from SDA_OUT to SDA_IN. The low signal at the input of U1 will not turn M2 on because U1 remains inactive, preventing a latch condition.

Buffer Output Low and Offset Voltage

By design, when a logic input low voltage is forced on the input of the buffer, the output of the buffer will have an input to output offset voltage. The output voltage of the buffer is determined by Equation 1:

$$V_{OUT} = V_{IN} + V_{OS} + [V_{CC}/R_{PULL\text{-}UP} \times r_{ON}] \quad \text{(EQ. 1)}$$

Where V_{OS} is the buffer internal offset voltage, $R_{Pull\text{-}Up}$ is the pull-up resistance on the SDA/SCL pin to V_{CC} and r_{ON} is the ON-resistance of the buffer’s internal NMOS pull-down device. The last term of the equation is the additional voltage drop developed by sink current and the internal resistance of the transistor. The V_{OS} of the buffer can be determined by Figures 21, 22 and is typically 40mV. Reducing the pull-up resistor values increases the sink current and increases the output voltage of the buffer for a given input low voltage (Figures 19, through 22).

Rise Time Accelerators

The ISL33001, ISL33002, ISL33003 buffer rise time accelerators on the SDA/SCL pins improve the transient performance of the system. Heavy load capacitance or weak pull-up resistors on an Open-Drain bus cause the rise time to be excessively long, which leads to data errors or reduced data rate performance. The rise time accelerators are only active on the low-to-high transitions and provide an active constant current source to slew the voltage on the pin quickly (Figure 23).

The rise time accelerators are triggered immediately after the buffer release threshold (approximately 30% of V_{CC}) on both sides of the buffer is crossed. Once triggered, the accelerators are active for a defined pulse width (Figure 24) with the current source turning off as it approaches the supply voltage.

Enable Pin (ISL33001 and ISL33003)

When driven high, the enable pin puts the buffer into its normal operating state. After power-up, EN high will activate the bus pre-charge circuitry and wait for a valid connection state to enable the buffer and the accelerator circuitry.

Driving the EN pin low disables the accelerators, disables the buffer so that signals on one side of the buffer will be isolated from the other side, disables the pre-charge circuit and places the device in a low power shutdown state.

READY Logic Pin (ISL33001 Only)

The READY pin is a digital output flag for signaling the status of the buffer. The pin is the drain of an Open-Drain NMOS. Connect a resistor from the READY pin to V_{CC1} to provide the high pull-up. The recommended value is 10kΩ.

When the buffer is disabled by having the EN pin low or if the start-up sequencing is not complete, the READY pin will be pulled low by the NMOS. When the buffer has the EN pin high and a valid connection state is made at the SDA/SCL pins, the READY pin will be pulled high by the pull-up resistor. The READY pin is capable of sinking 3mA when pulled low while maintaining a voltage of less than 0.4V.

ACC Accelerator Pin (ISL33002 Only)

The ACC logic pin controls the rise time accelerator circuitry of the buffer. When ACC is driven high, the accelerators are enabled and will be triggered when crossing the buffer release threshold. When ACC is driven low, the accelerators are disabled.

For lightly loaded buses, having the accelerators active may cause ringing or noise on the rising edge transition. Disabling the accelerators will have the buffers continue to perform level shifting with the V_{CC1} and V_{CC2} supplies and provide capacitance buffering.

Propagation Delays

On a low-to-high transition, the rising edge signal is determined by the bus pull-up resistor, load capacitance, and the accelerator current from the ISL33001, ISL33002, ISL33003 buffer. Prior to the accelerators becoming active, the buffer is connected and the output voltage will track the input of the buffer. When the accelerators activate the buffer connection is released and the signal on each side of the buffer rises independently. The accelerator current on both sides of the buffer will be equal. If the pull-up resistance on both sides of the buffer are also equal, then differences in the rise time will be proportional to the difference in capacitive loading on the two sides.

Because the signals on each side of the buffer rise independently, the propagation delay can be positive or negative. If the input side rises slowly relative to the output (i.e., heavy capacitive loading on the input and light load on the output) then the propagation delay t_{PLH} is negative. If the output side rises slowly relative to the input, t_{PLH} is positive.

For high-to-low transitions, there is a finite propagation delay through the buffer from the time an external low on the input drives the NMOS output low. This propagation delay will always be positive because the buffer connect threshold on the falling edge is below the measurement points of the delay. In addition to the propagation delay of the buffer, there will be additional delay from the different capacitive loading of the buffer. Figures 25 and 26 show how the propagation delay from high-to-low, t_{PHL}, is affected by V_{CC} and capacitive loading.

The buffer's propagation delay times for rising and falling edge signals must be taken into consideration for the timing requirements of the system. SETUP and HOLD times may need to be adjusted to take into account excessively long propagation delay times caused by heavy bus capacitances.

Pull-Up Resistor Selection

While the ISL33001, ISL33002, ISL33003 2-Channel buffers are designed to improve the rise time of the bus in passive pull-up systems, proper selection of the pull-up resistor is critical for system operation when a buffer is used. For a bus that is operating normally without active rise time circuitry, using the ISL33001, ISL33002, ISL33003 buffer allows larger pull-up resistor values to reduce sink currents when the bus is driving low. However, choose a pull-up resistor value of no larger than 20kΩ regardless of the bus capacitance seen on the SDA/SCL lines. The Bus Idle or Stop Bit condition requires valid logic high voltages to give a valid connection state. Pull-up resistor values 20kΩ or smaller are recommended to overcome the typical 150kΩ impedance of the pre-charge circuitry, delivering valid high levels.

Level Shifting from 3.3V to 1.8V

While the ISL3300x level shifters operate down to 2.3V, it is possible to interface the ISL33002 to 1.8V sensors and micro controller I/O without causing overshoot on the SCL and SDA outputs. This is because the ISL33002 is the only device that allows its accelerators to be disabled. The ISL33001 and ISL33003, whose accelerators are always active, cause overshoot on the I^2C outputs that trigger the ESD cells of a 1.8V slave device at the applied clock and data rates.

Figure 11 depicts the ISL33002, whose accelerators are disabled by connecting the ACC pin (Pin 5) to ground.

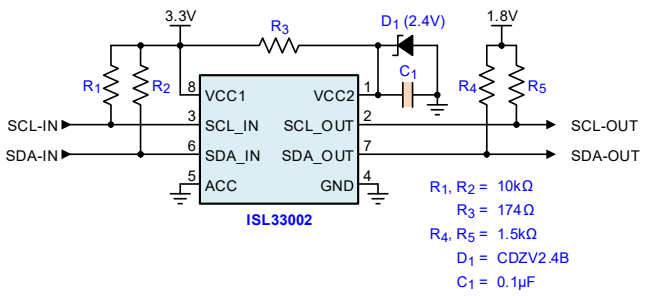


FIGURE 11. LEVEL SHIFTING 3.3V I^2C SIGNALS AT THE INPUT TO 1.8V SIGNALS AT THE OUTPUT

Figure 12 shows the corresponding input and output signals.

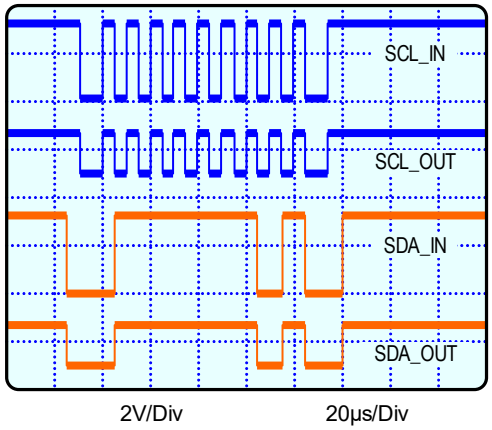


FIGURE 12. 3.3V INPUT AND 1.8V OUTPUT SIGNALS FOR DISABLED ACCELERATOR

With its accelerators disabled, the ISL33002 behaves like a standard I^2C buffer, whose high output steady states are purely determined by the external 1.8V supply through the pull-up resistors, R_4 and R_5. As shown in Figure 12, both I^2C outputs are without overshoot.

The supply of the output side (VCC2) is reduced to 2.4V, just 0.1V above the specified minimum supply level. This ensures reliable device operation, but also minimizes the distance between VCC2 and the external 1.8V bus voltage, which eases the internal biasing of the output switches.

VCC2 can be generated either by a separate 2.4V power supply, or by deriving it from VCC1 using a 2.4V Zener diode and series resistor, R_3. The 100nF buffer capacitance, C_1, is needed to provide sufficient supply current during the switching of the output stages.

Typical Performance Curves

$C_{IN} = C_{OUT} = 10pF$, $V_{CC1} = V_{CC2} = V_{CC}$, $T_A = +25°C$; Unless Otherwise Specified.

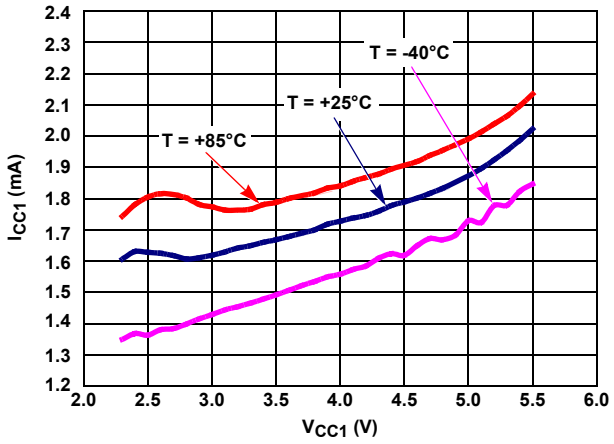


FIGURE 13. I_{CC1} ENABLED CURRENT vs V_{CC1} (ISL33001)

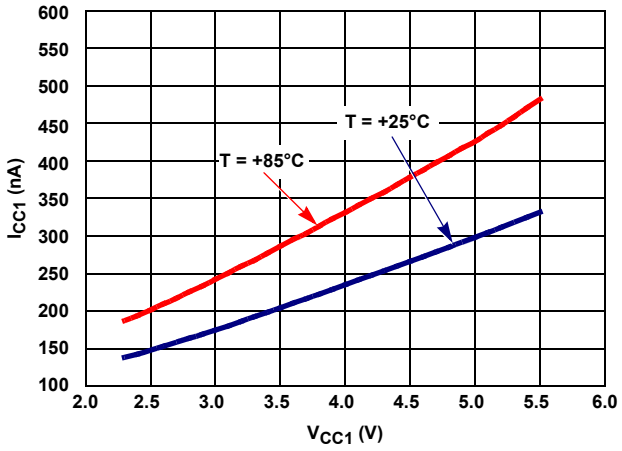


FIGURE 14. I_{CC1} DISABLED CURRENT vs V_{CC1} (ISL33001)

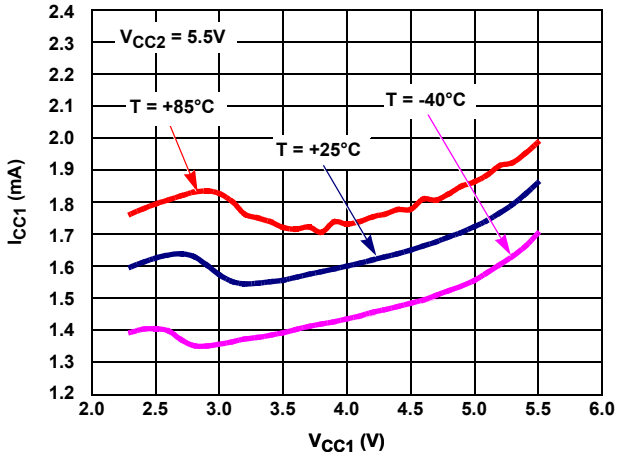


FIGURE 15. I_{CC1} ENABLED CURRENT vs V_{CC1} (ISL33002 AND ISL33003)

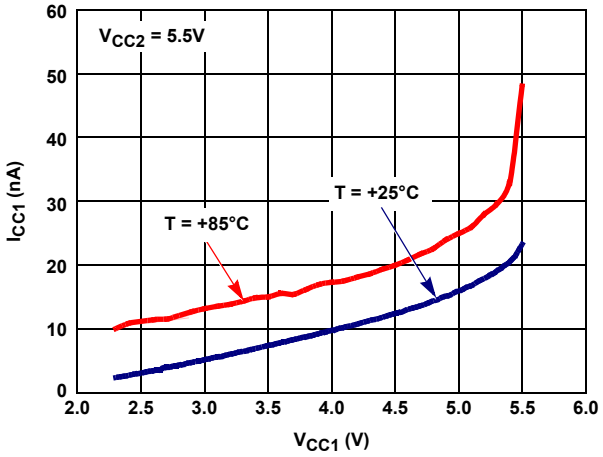


FIGURE 16. I_{CC1} DISABLED CURRENT vs V_{CC1} (ISL33003)

Typical Performance Curves (Continued)

$C_{IN} = C_{OUT} = 10pF$, $V_{CC1} = V_{CC2} = V_{CC}$, $T_A = +25°C$; Unless Otherwise

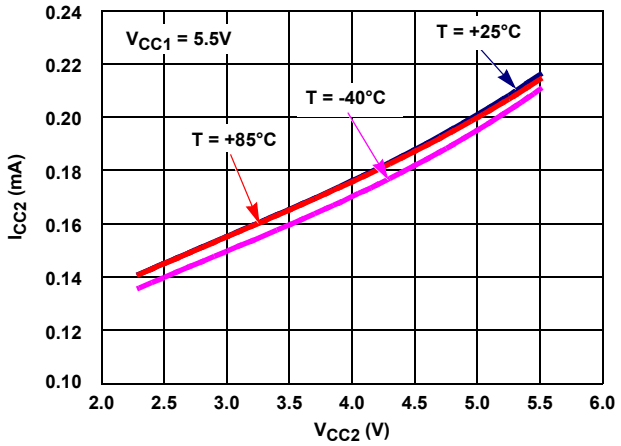


FIGURE 17. I_{CC2} ENABLED CURRENT vs V_{CC2} (ISL33002 AND ISL33003)

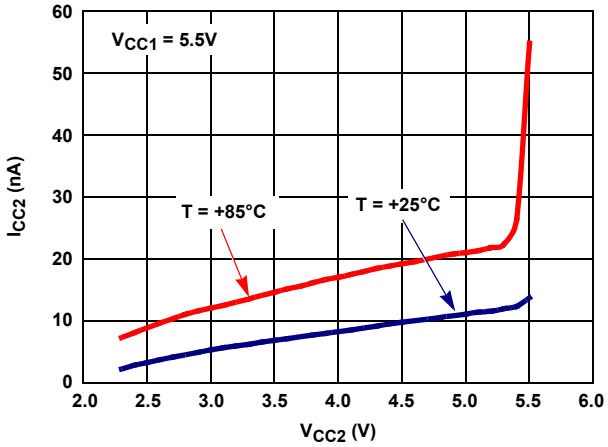


FIGURE 18. I_{CC2} DISABLED CURRENT vs V_{CC2} (ISL33003)

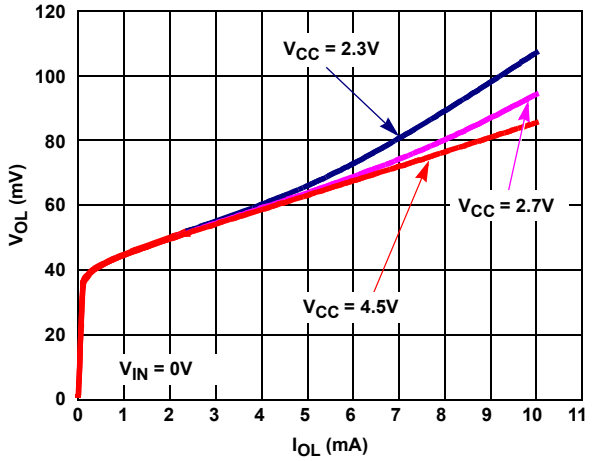


FIGURE 19. SDA/SCL OUTPUT LOW VOLTAGE vs SINK CURRENT vs V_{CC}

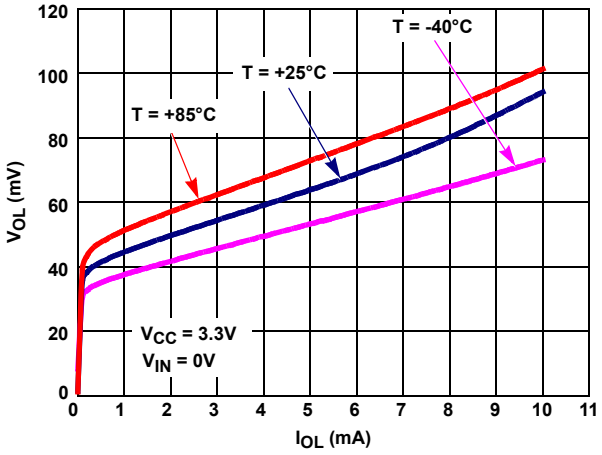


FIGURE 20. SDA/SCL OUTPUT LOW VOLTAGE vs SINK CURRENT vs TEMPERATURE

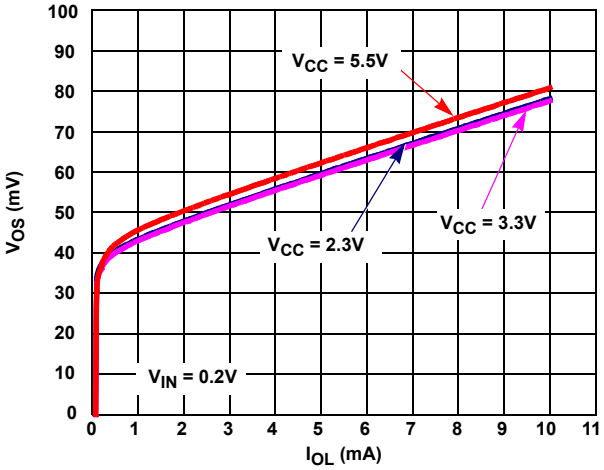


FIGURE 21. INPUT TO OUTPUT OFFSET VOLTAGE vs SINK CURRENT vs V_{CC}

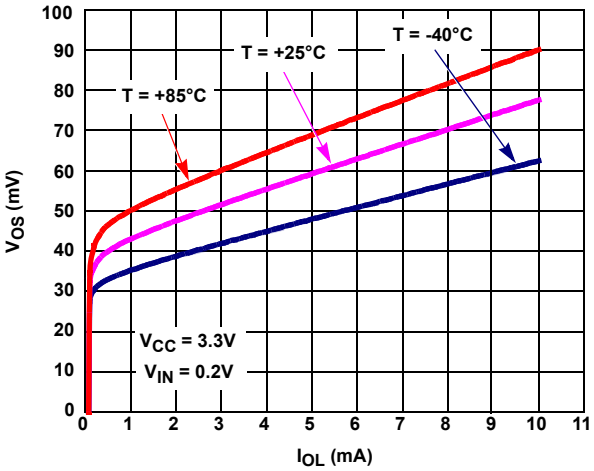


FIGURE 22. INPUT TO OUTPUT OFFSET VOLTAGE vs SINK CURRENT vs TEMPERATURE

Typical Performance Curves (Continued) $C_{IN} = C_{OUT} = 10pF$, $V_{CC1} = V_{CC2} = V_{CC}$, $T_A = +25°C$; Unless Otherwise

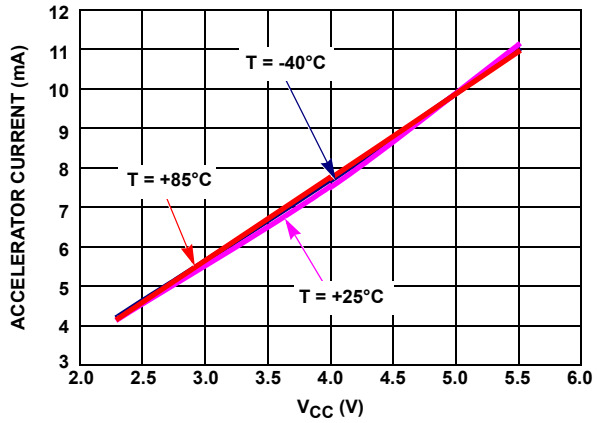


FIGURE 23. ACCELERATOR PULL-UP CURRENT vs V_{CC}

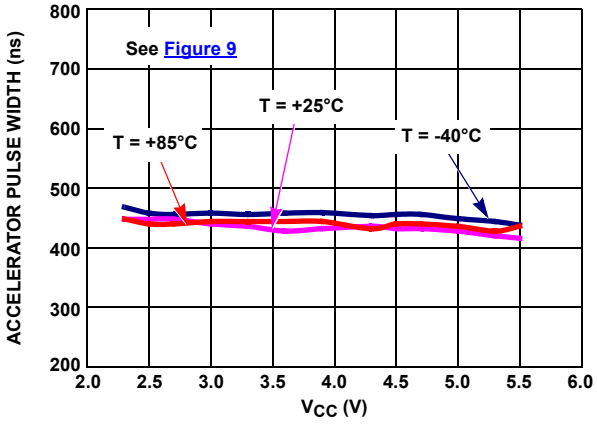


FIGURE 24. ACCELERATOR PULSE WIDTH vs V_{CC}

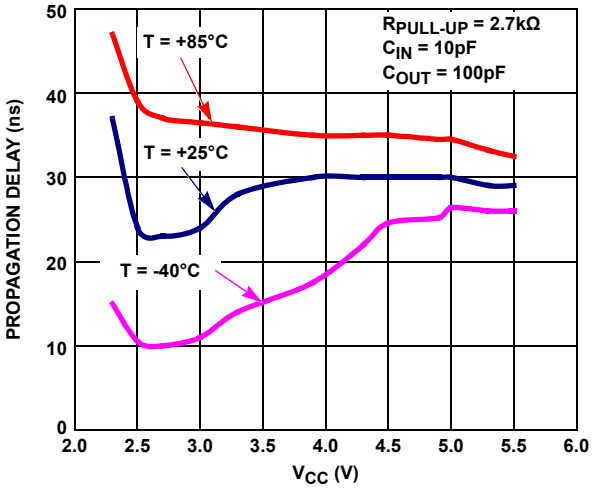


FIGURE 25. PROPAGATION DELAY H-L vs V_{CC}

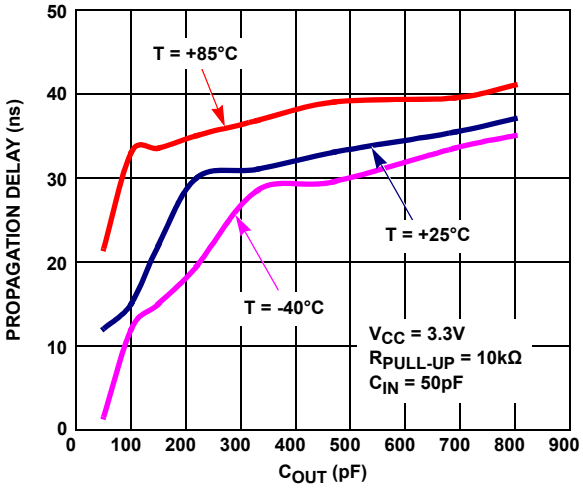


FIGURE 26. PROPAGATION DELAY H-L vs C_{OUT}

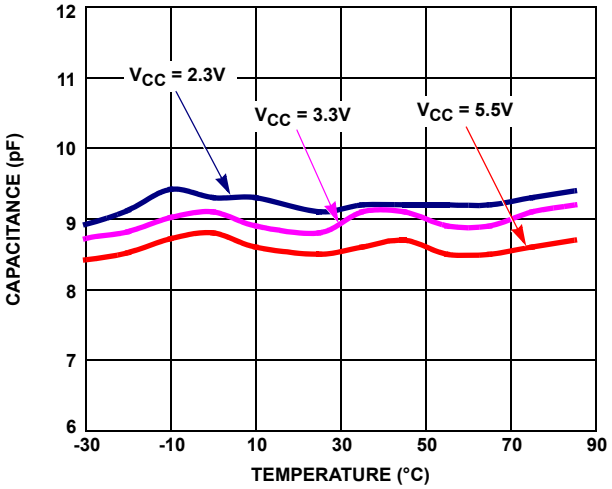


FIGURE 27. SDA/SCL PIN CAPACITANCE vs TEMPERATURE vs V_{CC}

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

PROCESS:

0.25µm CMOS

Revision History

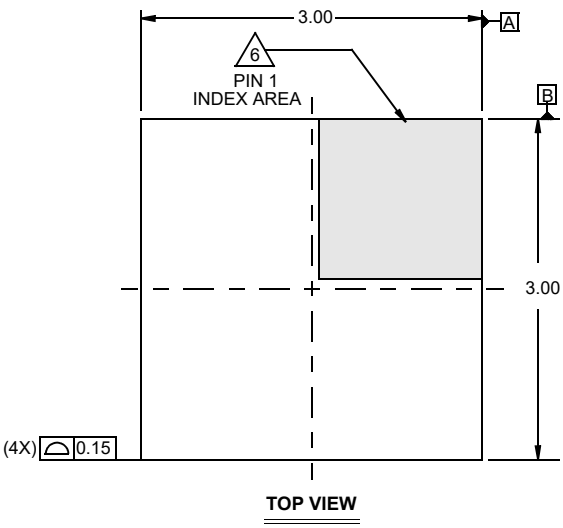
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
Feb 24, 2022	6.01	Removed Related Literature and About Intersil sections. Added TOC. Updated Ordering Information Table by applying new formatting, updating notes, and adding parts. Added Level Shifting from 3.3V to 1.8V section. Updated PODs L8.6x6H and L8.3x3A to the latest version, changes are as follows: - Tiebar Note updated Updated POD M8.118 to the latest version, changes are as follows: -Corrected typo in the side view 1 updating package thickness tolerance from ±010 to ±0.10. Updated POD M8.15 to the latest version, changes are as follows: -Added the coplanarity spec into the drawing.
July 11, 2014	6.00	In “Features” on page 1, changed “Low quiescent Current” from “2.2mA” to “2.1mA”. On page 6, added “Pb-Free Reflow Profile” entry to “Thermal Info” section. In “Electrical Spec” table on page 6, changed “V_{CC}” to “V_{CC1}” in the “Supply Current from V_{CC2}” row. In “Electrical Spec” table on page 7, for parameter “Input Low Threshold”, moved the “TYP” column entry to the “MAX” column. On page 8, Figure 4, clarified the associated notes. On page 9, Figure 8, changed “I_{ACC}” to I_{TRAN_ACC}”, and noted that the $\Delta V/\Delta t$ is for the accelerator portion of the waveform.
December 19, 2013	5.00	Added Note 13 at the end of the "Elec Spec" table on page 7 as follows: “13. If the Vcc1 and Vcc2 voltages diverge, then the shut-down Icc increases on the higher voltage supply." Added reference "(Note 13)" after "ISL33003 only" in rows for Vcc1 and Vcc2 "Shut-down Supply current" parameters (last 2 rows of "Power Supplies" section) on page 6.
October 12, 2012	4.00	Changed “SDA_IN, SCL_IN...0.3V to +(V_{CC1} + 0.3)V, SDA_OUT, SCL_OUT...0.3V to +(V_{CC2} + 0.3)V, ENABLE, READY, ACC...0.3V to +(V_{CC1} + 0.3)V” to “SDA_IN, SCL_IN, SDA_OUT, SCL_OUT, READY...0.3V to +7V; ENABLE, ACC...0.3V to +(V_{CC1} + 0.3)V”, in the Absolute Maximum Ratings section at the top of page 6. Removed “Pb-free Reflow Profile” and link from “Thermal Information” section at the top of page 6. Added “open drain” and “Connect to 10kΩ pull-up resistor to V_{CC1}.”, in Pin Descriptions in the READY section on page 3.
October 11, 2011	3.00	Converted to new datasheet template. Changed Title of datasheet from: “2-Wire Bus Buffer With Rise Time Accelerators and Hot Swap Capability” to: I^2C Bus Buffer with Rise Time Accelerators and Hot Swap Capability Pg 1, added to Related Literature: AN1637, “Level Shifting Between 1.8V and 3.3V Using I2C Buffers” Replaced POD M8.118 Rev 3 with Rev 4 due to the following changes: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" Replaced POD M8.15 Rev 1 with Rev 3 due to the following changes: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Figure 3 (was Fig1) - Added: - If tDELAY1 < tEN-LH then tDELAY2 = tEN-LH + tIDLE + tREADY-LH - If tDELAY1 > tEN-LH then tDELAY2 = tEN-LH + tREADY-LH and replaced graph
September 13, 2010	2.00	Added SOIC package information to datasheet for ISL33001.
April 30, 2010	1.00	Changed typical value of “Supply Current from V_{CC1}” on page 6 for ISL33001 only from 2.2mA to 2.1mA. Changed typical value of “Input-Output Offset Voltage” on page 7 from 100mV to 50mV.
March 18, 2010	0.00	Initial Release.

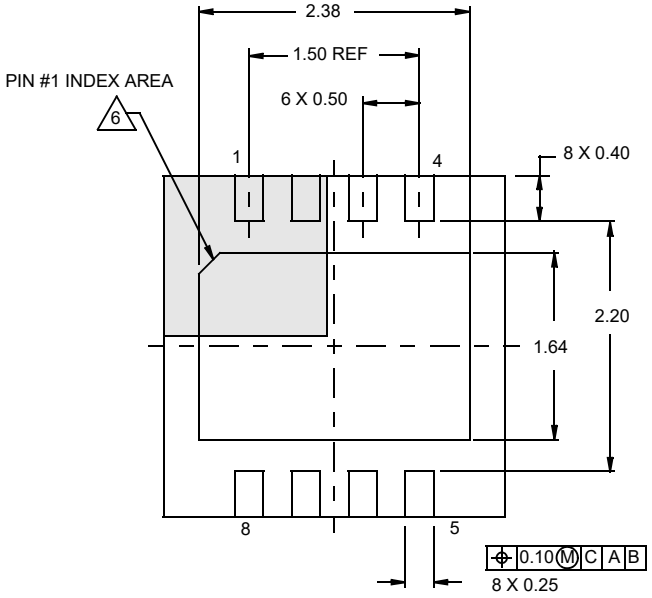
Package Outline Drawings

For the most recent package outline drawing, see L8.3x3H.

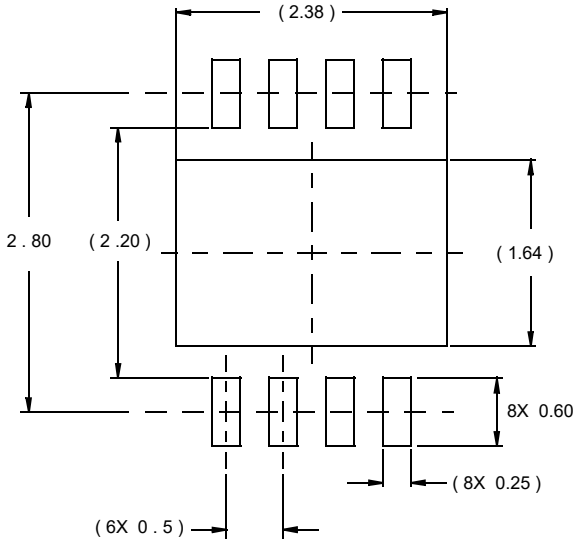
L8.3x3H
8 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 1, 5/15



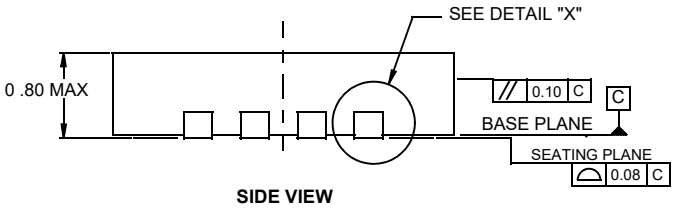
TOP VIEW



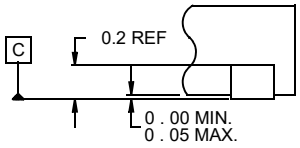
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



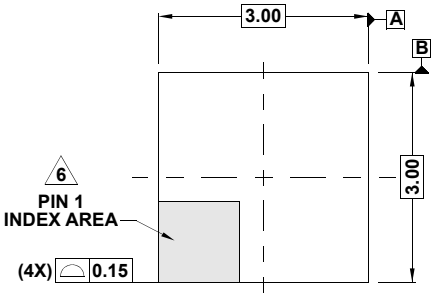
DETAIL "X"

NOTES:

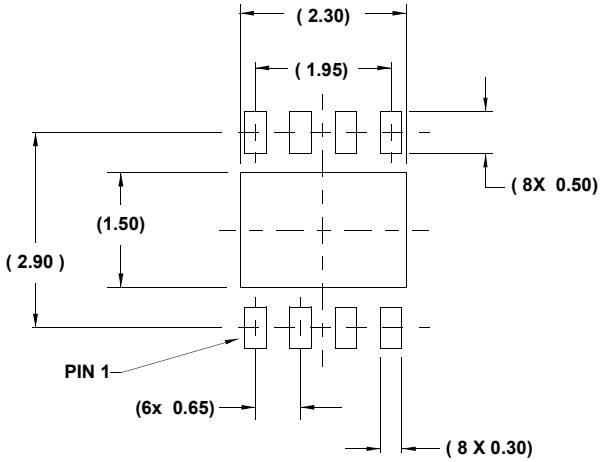
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see L8.3x3A.

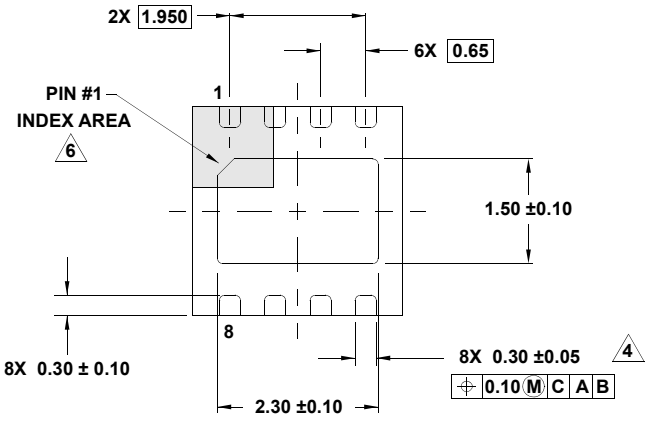
L8.3x3A
8 Lead Thin Dual Flat No-Lead Plastic Package
Rev 5, 5/15



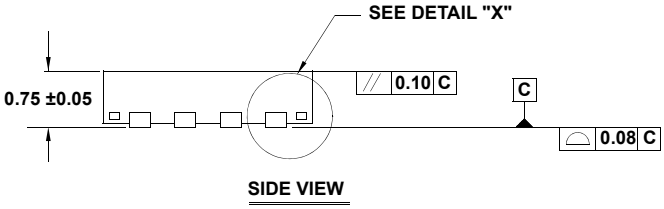
TOP VIEW



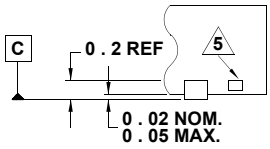
TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW



SIDE VIEW



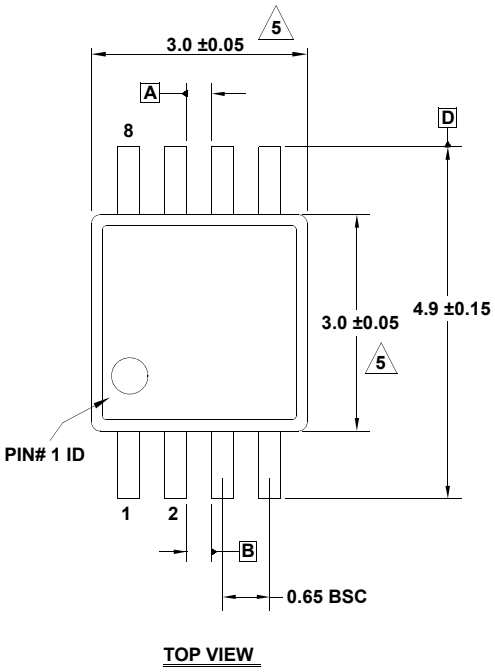
DETAIL "X"

NOTES:

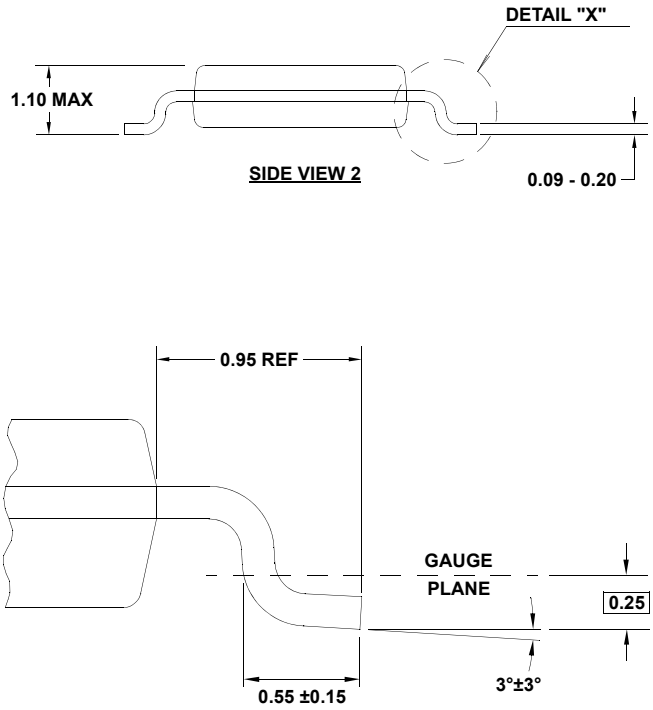
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.20mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 WEEC-2 except for the foot length.

For the most recent package outline drawing, see M8.118.

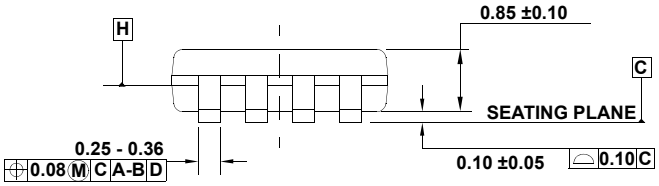
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



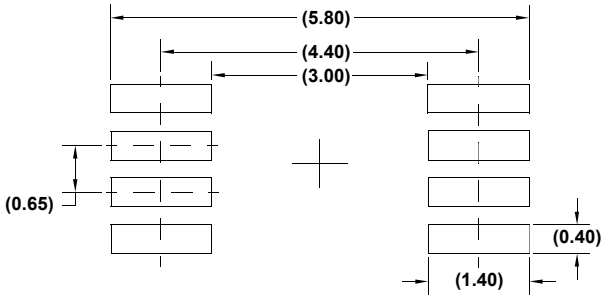
TOP VIEW



DETAIL "X"



SIDE VIEW 1



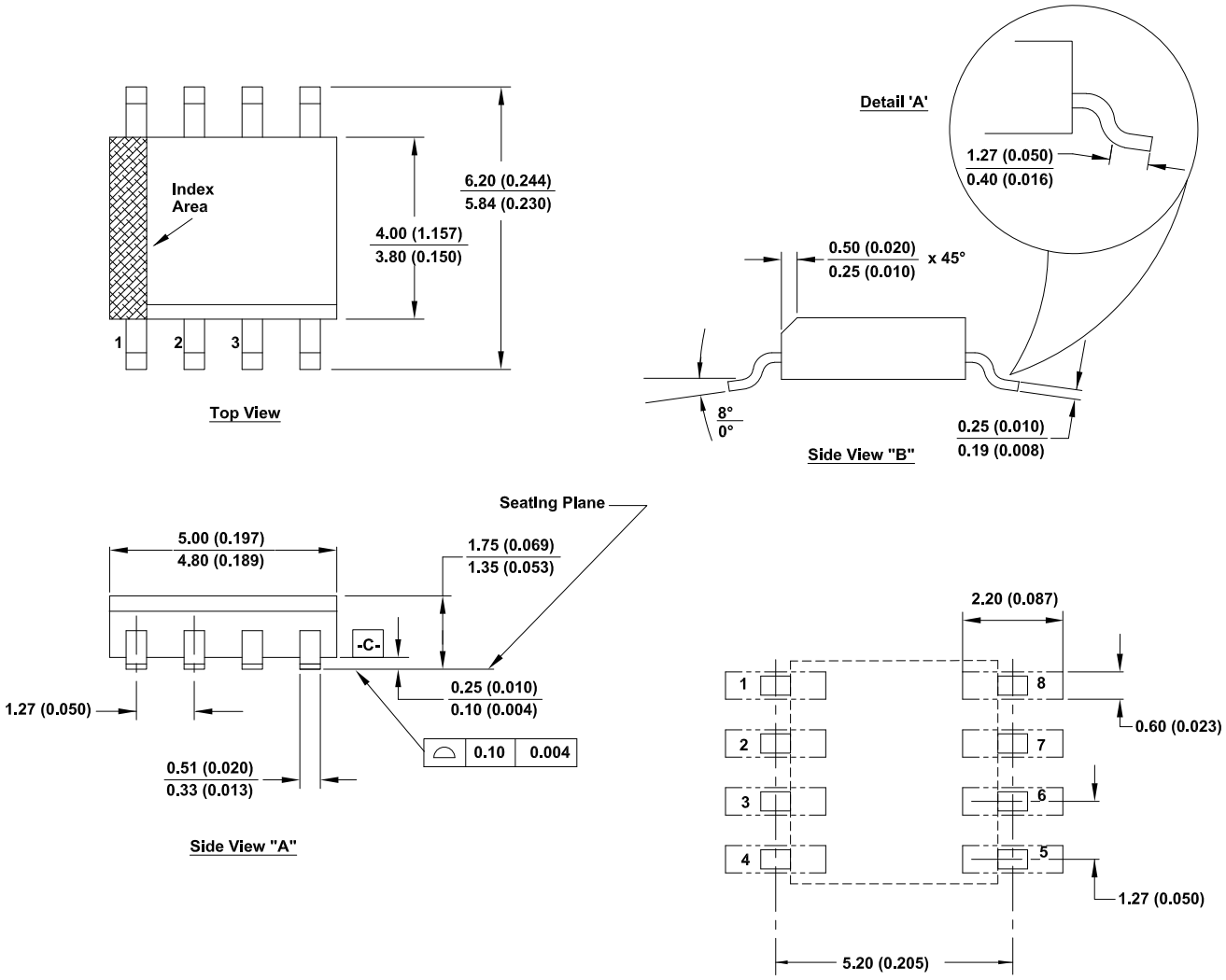
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see M8.15.

M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 5, 4/2021



NOTES:

1. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
2. Package length does not include mold flash, protrustion or gate burrs. Mold flash, protrustion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrustions. Interlead flash and protrustions shallnot exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. if it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 Inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.