ISL34341KIT1Z, ISL76321ARZ-EVAL1Z

Evaluation Kit

AN1455
Rev. 2.00
Jan 31, 2011

Overview

This manual covers both the ISL34341 and ISL76321 evaluation kits. These kits enable the user to exercise the SerDes in a lab environment and to see the high speed and parallel signals conveniently on an oscilloscope. Contents of the kit are shown in Figure 1.

Schematics and a software GUI can be downloaded from:

http://www.intersil.com/data/EV/ISL34341_Eval_Kit_Software.zip

There are slight differences between the ISL34341 and ISL76321 kits. The ISL76321 uses a Molex cable instead of Rosenberger which the ILS34341 uses. Unless specifically mentioned, ISL76321 can be substituted anywhere you see ISL34341.

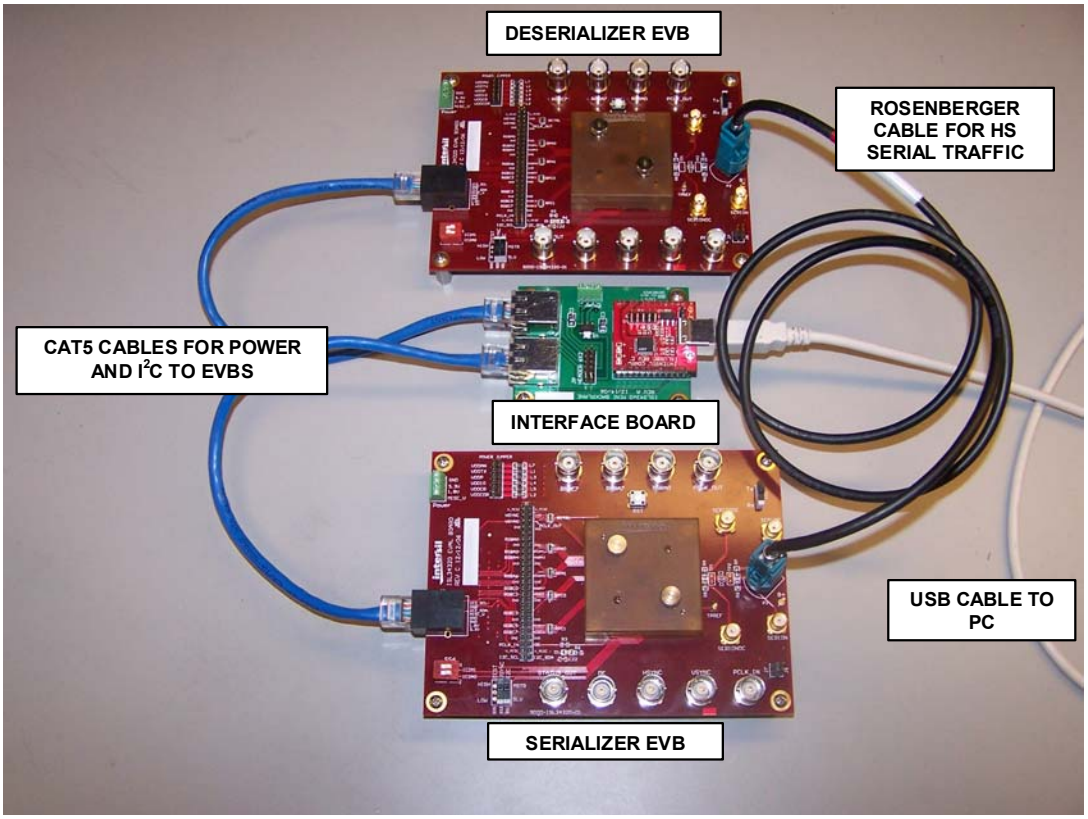

FIGURE 1. KIT CONTENTS

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TABLE 1. NOMENCLATURE

SHORTHAND	REFERS TO:	WHY SO SPECIFIC?
ser.PCLK_IN	PCLK_IN device pin. SerDes is in video serializer mode.	We are referring to the device pin specifically and not the BNC connector. There are several paths on the EVB to the device pin.
serEVB.PCLK_IN	BNC connector labeled PCLK_IN. SerDes is in video serializer mode.	This BNC is factory configured to be a sense output.
des.PCLK_IN	PCLK_IN device pin. SerDes is in video deserializer mode.	We are referring to the device pin specifically and not the BNC connector. There are several paths on the EVB to the device pin.
desEVB.PCLK_IN	BNC connector labeled PCLK_IN. SerDes is in video deserializer mode.	This BNC is factory configured to be a high impedance input.

Nomenclature

For user convenience, many connectors and switches on the evaluation board are labeled with the device pin name. However, occasions arise when we need to distinguish between the connector and the device pin. The nomenclature in Table 1 is adopted when specificity is needed.

The evaluation boards also have provisions for user customization. Unless otherwise indicated, all discussion of functions and settings assume the evaluation boards are in the factory shipped state. Any reference to the ISL34340 should be treated as the ISL34341. The ISL34340 is an older device that has a subset of the ISL34341 functionality and is no longer available.

Evaluation Kit Usage

The ISL34341 Evaluation Kit is designed to be flexible in order to allow for examination of our chip in several different ways. The ISL34341 device has built in patterns that can be activated through I^2C write to the appropriate register. There are built in patterns that are designed for scoping the serial data as well as a built in PRBS generator and detector. It should be noted that these features are always available even in a completed system for testing or debug.

The user also has the ability of injecting video of the same type as the target application. By using these two methods, we believe that evaluation of the ISL34341 can be done both quickly and effectively.

USER SUPPLIED VIDEO SIGNALS

The serializer needs video of valid format to function and must match the PCLK frequency of the ISL343xx device; see the device datasheet for details. Such signals may be provided by either attaching a raw RGB driver to J20 using a ribbon cable or by driving VSYNC, HSYNC, and PCLK pins on J20 (not BNCs) using additional function generators. If DATAEN is not supplied, it needs to be strapped to VDD33. The BNC connectors on the serializer board are sense “outputs” only (to hook up to scopes).

An LCD panel may be connected to J20 to view the deserializer video output.

Video data is not required as the 8b/10b encoding will create the necessary transitions for the link to operate properly. The side channel and I^2C master mode can both be evaluated in this state.

TEST MODE SIGNALS

There are 4 built in test patterns that can be accessed by the user through the I^2C interface. Three patterns are fixed repeating high, low and mixed frequency patterns. These are most useful for direct observation on an oscilloscope through the SMAs at either end of the cable. In addition, there is a build in PRBS generator and PRBS detector. These can be conveniently used together to evaluate different lengths or types qualities of cables at different frequencies. This is initiated in the Tx chip in register 0x06. There is an 8-bit error counter that records PRBS errors register 0x07, which is read from the Rx board. This register self clears upon reading. “PRBS GUI Setups” on page 12 shows the setups for the Tx and Rx chips for running the PRBS.

REQUIRED EQUIPMENT

1. 3.3V Power Supply, 1A – applied to the I^2C hub
2. 50MHz function generator – supply PCLK_IN to both boards
3. Windows PC with USB– configure the device through the I^2C bus
4. 500MHz oscilloscope– minimum for signal observation

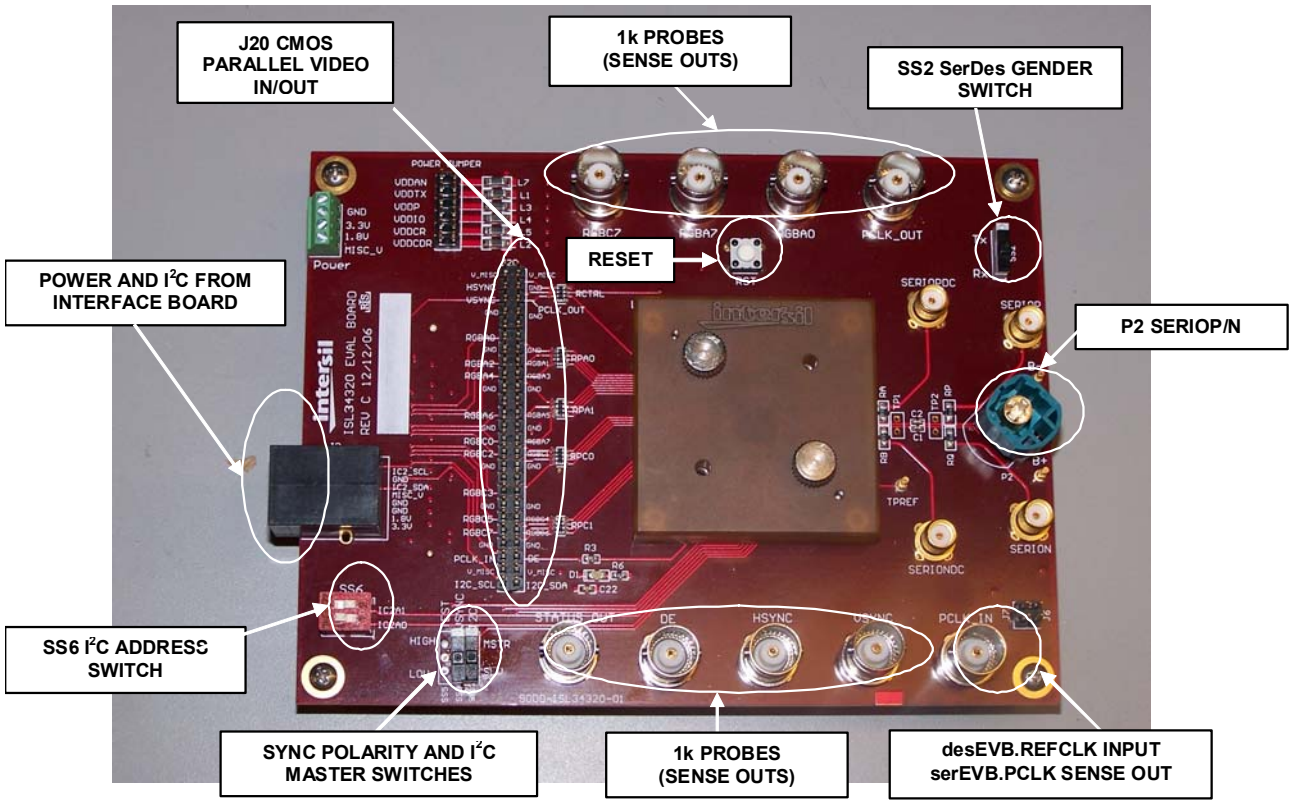


FIGURE 2. EVALUATION BOARD

Evaluation Board

Each kit contains 2 evaluation boards (EVB); one for serializer and another for deserializer.

SerDes GENDER SELECTION

The gender of the SerDes is set by the SS2 switch (as shown in Table 2) and come preset from the factory. Although the SerDes and EVBs are interchangeable for video serialization and deserialization functions, there are two differences to keep in mind:

1. **Rosenberger connector polarity**. Due to the design of the Rosenberger HSD cable, signals fed in pins 1+3 come out at pins 2+4. To accommodate this, one of the evaluation boards has P2 rotated 90°. By convention, this is the deserializer EVB.
2. **PCLK_IN BNC** on the desEVB is an *input* to hook up an external function generator to supply the REFCLK to the deserializer. For the serEVB, this BNC is a sense output to monitor incoming ser.PCLK.

TABLE 2. SS2 SETTINGS

SS2 SETTING	SerDes FUNCTION	EVALUATION BOARD NAME
TX	Video Serializer	serEVB
RX	Video Deserializer	desEVB

POWERING EVB

The EVB provides as direct access as possible to all the pins. As such, there are no power protection devices.

Misapplied power (reverse, overvoltage) can severely damage the SerDes.

The EVB may be powered in any **one** of the following manners:

1. J2, the “Ethernet” connector. This is the default method using the Interface Board provided.
2. Green POWER terminal block.
3. J1, the 100 pin stacking connector.

TABLE 3. EVB POWER NODES

POWER NODE	SILKSCREEN LABELS	FUNCTION
VDD1V8	1.8V	SerDes supply
VDD3V3	3.3V	SerDes supply
V_MISC	MISC_V	J20 (usually to power LCD panel), STATUS LED, crystal oscillator

The VDD1V8 and VDD3V3 are further split into individual domains for each of the supply pins on the SerDes. The 6x2 header labeled “POWER JUMPER” provides a convenient place to monitor the voltages. Current of each supply pin can be individually measured by cutting the shorting traces on the back of the board opposite this jumper.

BNC SENSE OUTPUTS (BUILT-IN 1k PROBES)

Critical signals are “probed” by 950Ω resistors and brought to BNC and SMA connectors. When connected to a scope set to 50Ω inputs, these form a “built-in 1k probe” that allows the viewing of these signals with high fidelity – as if one were probing right at the pins of the device. The built-in probes side-step the hassle of clip-type probes with ground clips. Furthermore, all of the built-in probes are matched to maintain their timing relationships relative to each other.

When using a scope of the proper bandwidth (generally >1GHz), rise times and signal integrity of the probed signal are not degraded. Lower frequency scopes may be used for debugging when only functionality matters and signal integrity is of secondary concern.

The built-in 1k probes form a resistor divider with the 50Ω input of the scope and attenuate the signal by a factor of 20. Therefore, a convenient setting is at 100mV/div., which translates to 2V/div.

J20 50 PIN HEADER FOR EXTERNAL HOOKUP

J20 is the 50 pin header that provides access to all of the pins on the SerDes, except for SERIOP/N. Uses include:

1. Connecting external RGB generator or LCD
2. Hooking a scope probe tip
3. Connecting to logic analyzer

J1 100 PIN HEADER FOR EXTERNAL HOOKUP

J1 is a stacking board-to-board connector providing same connectivity as J20. The mating connector is AMP 5-179031-4.

DesEVB.PCLK_IN BNC

The PCLK_IN BNC is not terminated for compatibility reasons and thus looks like a high-impedance input with direct connection to des.PCLK_IN. Lab function generators generally have 50Ω source impedance and assume a 50Ω load. Therefore, when driving a high impedance, the actual voltages will be double the instrument setting. *3V setting = 6V actual*!

CAUTION: To avoid accidentally overvoltaging the SerDes.PCLK_IN, use an in line BNC terminator or solder on a 50Ω resistor at RCIT location.

If a 50Ω resistor is soldered at RCIT, just be aware of this load when driving from J20 or J1. Most CMOS drivers cannot drive such a low load.

SerEVB.PCLK_IN BNC

This is a 1k sense output. To change it to an input, replace RCI1 with a 0Ω jumper. The same cautions in driving DesEVB.PCLK_IN apply in this case.

CRYSTAL

The 6 pin footprint Y1 can accommodate 5mmx7mm crystal oscillators of either 6 pin (Epson SG-9001CA series) or 4 pin (Abracon ASV series). To take advantage of the built in POR circuit, the clock needs to be inhibited until after the chip is fully powered up. A hard reset (reset button) after power and clock will work just as well. Specifically, the existence of spread spectrum switch on the evaluation board does not imply that the SerDes will work with spread spectrum clocking.

JP3 resistor jumper should be moved to complete the path between des.PCLK_IN and the crystal. From the factory, JP3 is connecting J20 and J1 to des.PCLK_IN.

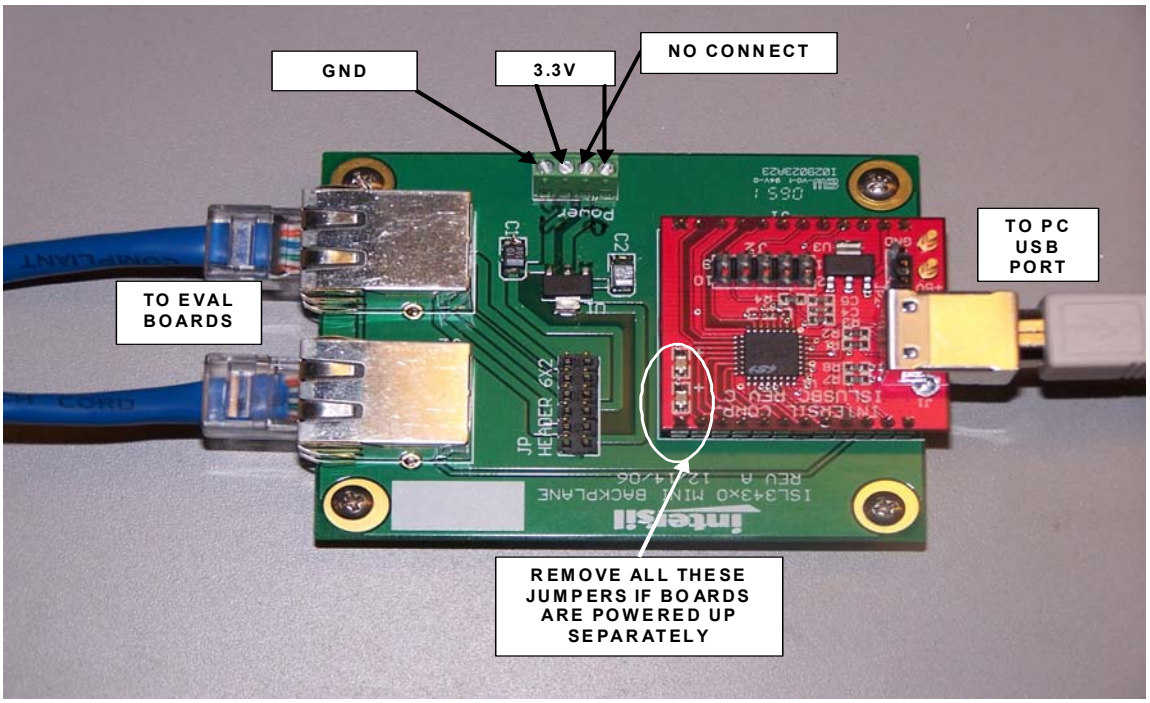


FIGURE 3. INTERFACE BOARD

Interface Board

The interface board shown in Figure 3 provides:

1. 3.3V and 1.8V power to evaluation boards from a single external 3.3V supply. There are two connections for the 3.3V supply. One connects to the regulator and the SerDes and the other connects to VMisc which is used to power the status LED and an on board oscillator if used.
2. USB to I^2C bridge for PC

Power and I^2C are distributed to the evaluation boards via the CAT-5 cables, which are chosen for their wide availability (there are no high speed signals in these cables).

To power the evaluation boards from the interface board, all the jumpers in the 6x2 header must be installed. When powering the evaluation boards by other means, these jumpers **must be removed** to disconnect the power coming from the interface board if the interface board will still be used to provide connection to the PC.

Setup

Evaluation Board Setup

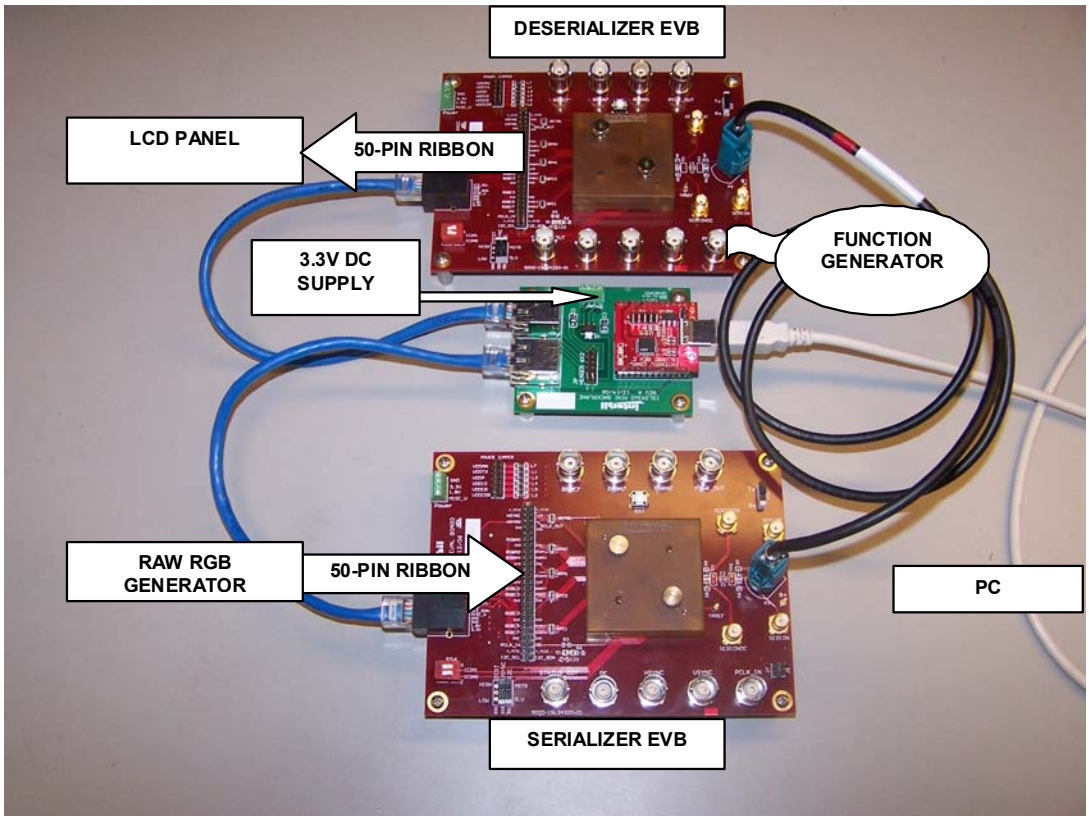


FIGURE 4. MAIN SETUP CONNECTIONS

- Raw RGB generator to serEVB.J20 through user's ribbon cable
- LCD panel or (other sink) to desEVB.J20 through user's ribbon cable
- 3.3V DC supply to Interface Board
- PC to Interface Board via USB cable
- SerEVB and desEVB to interface board via Ethernet cables
- SerEVB and devEVB via Rosenberger cable

It is almost redundant to mention that in this system, if any of the components are not working properly, or not connected, the result is "there is no image" or "I can't communicate via I^2C". The remaining subsections help the user ensure that each component is set up properly. Conversely, when things don't work, this section would be a good debug guide.

VSYNC/HSYNC Polarity Setup

For the serializer to transport video properly, it must know the polarity of the VSYNC and HSYNC signals supplied by the RGB driver. Symptoms of improper polarity setting can range from no transport to partial transport (missing colors).

Check and adjust VSYNC and HSYNC polarity on serEVB as follows:

1. Connect external RGB driver to J20.
2. Connect scope to HSYNC and VSYNC BNCs.
3. SS4 and SS3 switches should be set in HIGH position for the active low polarities seen in Figure 5:

FIGURE 5. ACTIVE LOW POLARITY EXAMPLE

4. SS4 and SS3 switches should be set in LO position for the active high polarities seen in Figure 6.

FIGURE 6. ACTIVE HIGH POLARITY EXAMPLE

On the desEVB, SS4 and SS3 control the deserializer's VSYNC and HSYNC output polarities.

PCLK Polarity Setup

A grainy or intermittent image is usually due to improper PCLK polarity. The serEVB.PCLK_IN and des.PCLK_OUT BNCs provide a convenient way to see the PCLK edge accurately in relation to the RGB, VSYNC, HSYNC, DE signals. The SerDes can adjust PCLK active edge only via I^2C register setting.

I^2C Local Access

To set registers locally via I^2C, the following must be in place:

- des.PCLK_IN (REF_CLK) must be supplied to the desEVB via BNC, J20, or J1
- ser.PCLK_IN must be supplied to serEVB via J20 or J1 (not BNC)
- SS1 must be set to SLV position.
- Set I^2C address of serEVB to 0x60 (all SS6 dip switches set to 0)
- Set I^2C address of desEVB to 0x62 (SS6 dip switch IC2A0 = 1 all others set to 0)

GUI Installation

The GUI allows setting and viewing the SerDes I^2C registers from the PC. To install:

1. Run file Intersil_I2C_Comm_Installer_V316.exe
2. In your installation directory, find Intersil_I2C_Comm_V316.exe and create a shortcut.
3. Move the shortcut to your desktop or another convenient location.

Quickstart

Assuming a raw RGB source is hooked up to J20, this section provides a sample startup procedure.

TABLE 4. SCOPE SETUP FOR BOARD DEBUG

CHANNEL	SIGNAL	CONNECTION TYPE
Ch1	ser.PCLK_IN	BNC
Ch2	ser.DE	BNC
Ch3	ser.VSYNC	BNC
Ch4	des.VSYNC	BNC

1. Scope settings

- All channels 100mV/div., DC 50Ω coupling.
- Time base 100ns/div.
- Trigger on rising edge of Ch3 (ser.VSYNC)
- Measure Ch1 frequency (ser.PCLK_IN)

2. External function generator to provide REFCLK

- Connect to des.PCLK-IN through BNC cable
- Set function generator to the measured frequency from scope Ch1 (ser.PCLK_in).
- Set amplitude to 1.0V (refer to “DesEVB.PCLK_IN BNC” on page 5 for caution statement)

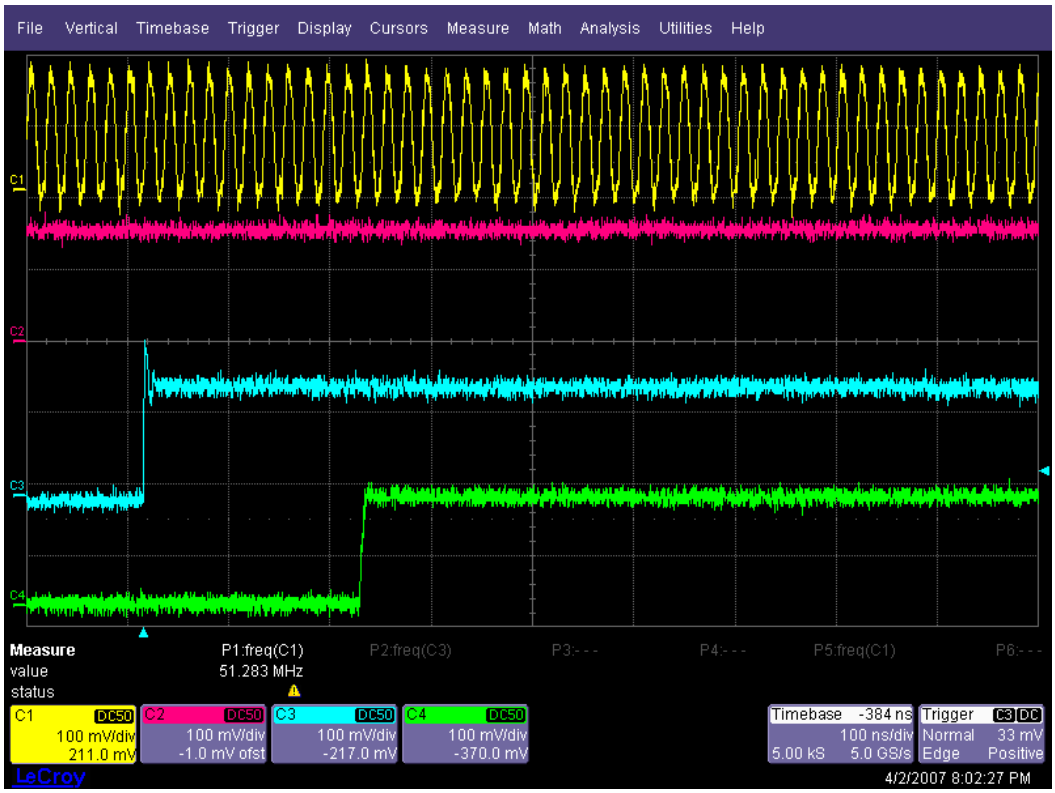
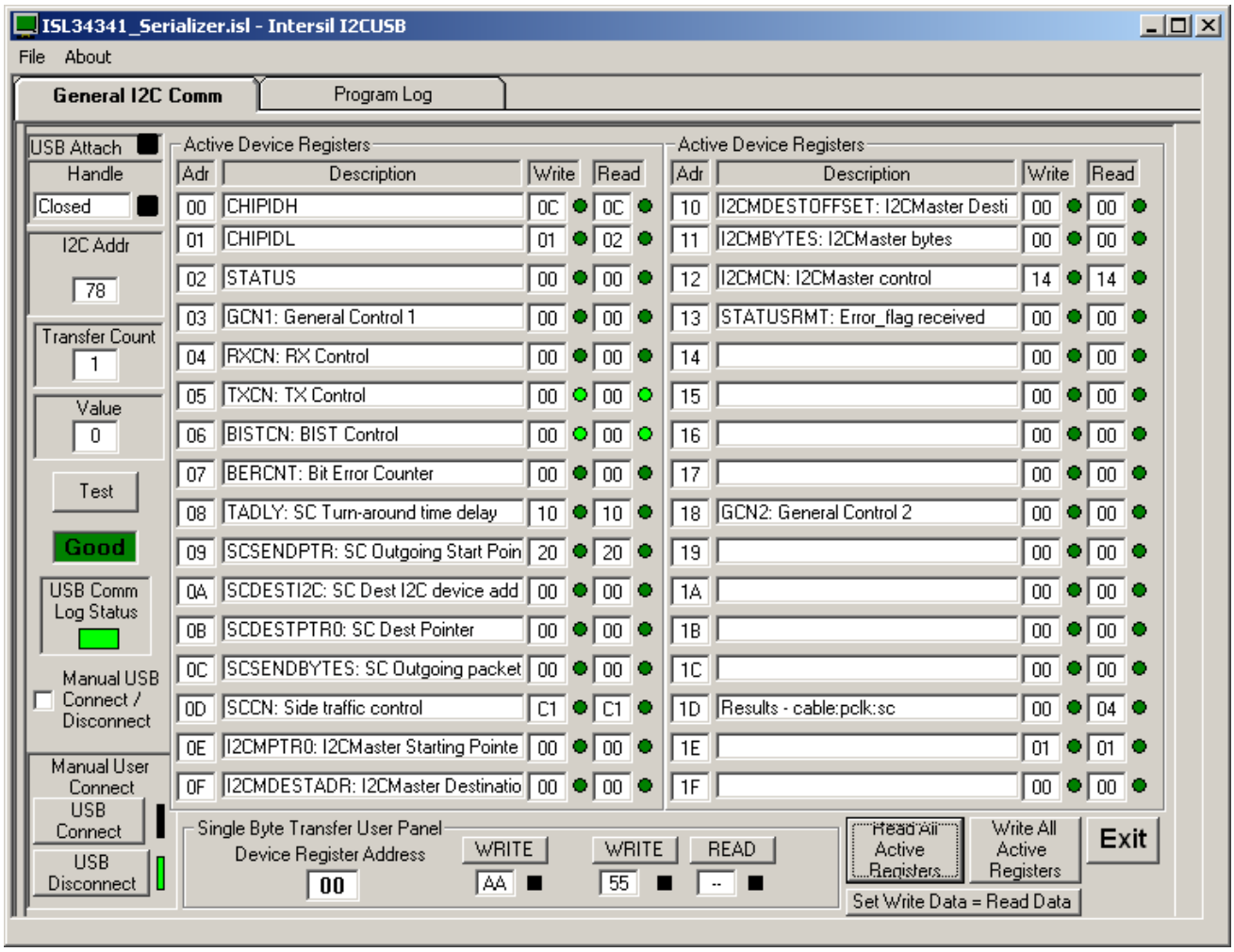


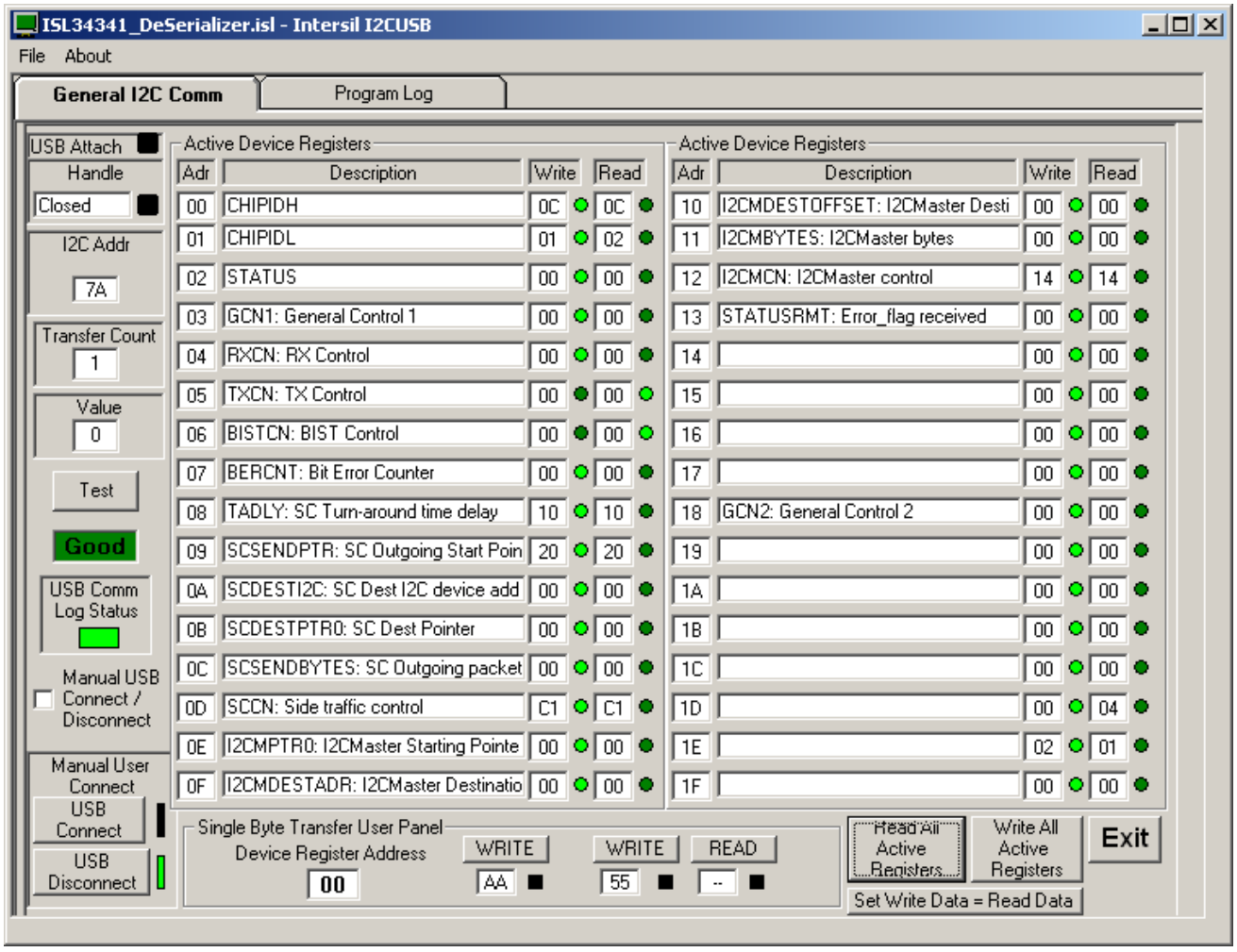
FIGURE 7. SCREEN SHOT OF WORKING SETUP

GUI Usage

Open two instances of the GUI so that one controls the serializer and another the deserializer. The two GUIs will communicate through the same Interface Board. Register file definitions set the “personality” of the generic GUI.

- Open the GUI, double click “Intersil_I2C_Comm_V316.exe”.
- Load the register map definition file: ISL34341_Serializer.isl (File->Open->Comm Register Definitions)
- Register maps are located in: /”install directory”/ REG_ISL_Files
- Make sure I^2C Addr matches the value of the serializer evaluation board
- Click on TEST button and make sure the status box below it turns green, “Pass”.
- You must click on the TEST button if the I^2C Addr is changed.





- Open a second GUI “Intersil_I2C_Comm_V316.exe”
- Load a register map definition ISL34341_Deserializer.isl

If you chose I^2C addresses other than the register map defaults, make sure that the serializer and deserializer are not the same. The chip addresses are changed in the cell labeled “I2C Addr”. This is a very flexible tool. Registers may be written individually or all together. To write a single register click in any cell in the “write” column. Delete the content of that cell and then type the new value for that register followed by a carrage return. The ball to the right of that cell shows the status of the latest operation, will turn green after a successful write. To read a register, mouse click in any cell in the read column and that cell is updated with that registers current value.

Any cell in the window can be altered. If you wish to read or write the device ram the register address can be changed in the “Adr” column and that ram location can read or modified like any other register.

All cells in this tool can be saved to an ascii file and later recalled. This is how the default templates were generated. To save all the cells click on the “File” pulldown and click “Save. Selecet a suitable name as it is not a good idea to modify the default template. When the template is loaded the register values are those that were saved previously. These may not reflect the actual values in the registers. There are two buttons “Read All Active Registers” and “Write All Active Registers” that read or write all 32 registers in the sheet. It is a good idea to click “Write All Active Registers” and then “Read All Active Registers” after loading a template so there are no differences between the GUI and the serdes devices.

PRBS GUI Setups

Figure 8 and Figure 9 show the GUI setup for the serializer and deserializer when running the PRBS. The PRBS setup condition changes from the register defaults are shown inside red circles. The error count is an 8 bit value read in the deseralizer register 0x07 and is circled in green.

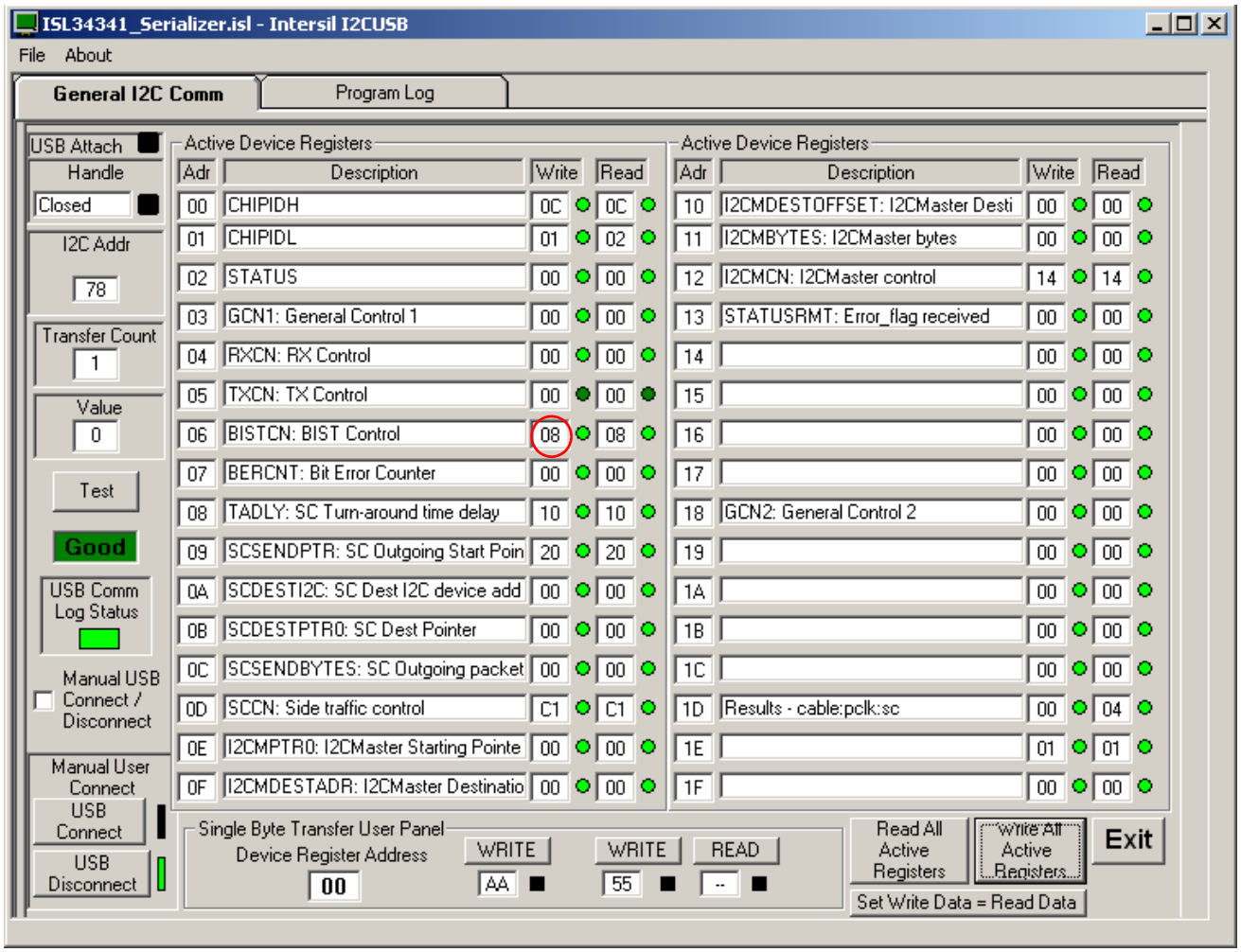


FIGURE 8. SERIALIZER CONFIGURATION

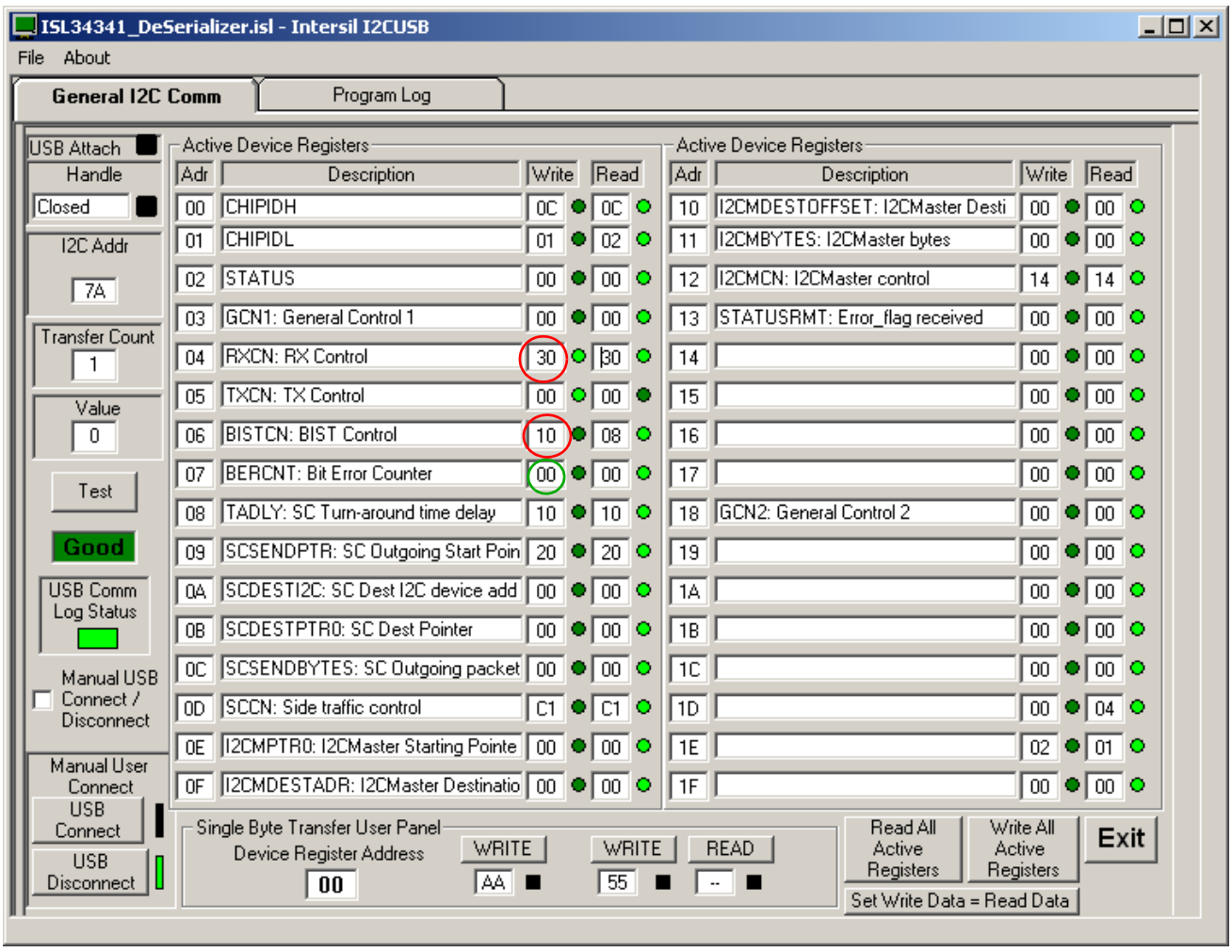


FIGURE 9. DESERIALIZER CONFIGURATION

It is important to monitor the clock output and status pin on the deserializer in addition to the error count in 0x07. This ensures that valid data is being received. If the deserializer loses lock, from for example a sudden change of frequency, the error count may continue to report zero errors when no data is being received. With a stable clock driving both the serializer and deserializer, this is never a problem.

To return to normal video you can program the register values back to their previous values or simply do a reset of both chips. When the PRBS is running the side channel is automatically disabled so the user is not able to send configuration data to the remote side of the link. This is not an issue when in the standard eval configuration (shown in figure 4) since both chips are connected to the USB hub.