ISL55110_11EVAL1Z, ISL55110_11EVAL2Z

Evaluation Board User's Manual

AN1283
Rev 0.00
February 13, 2007

Before Getting Started

This document supplements the ISL55110, ISL55111 Specification **FN6228**. Evaluation board users should review that document to obtain information on the parts' basic functionality and power requirements. A most important note is **before powering up the board, review the Power Up Sequence in that specification.** There are two DC sources utilized, so a user may inadvertently mis-apply the power sources causing damage to the part.

Take time to review the ISL55110, ISL55111 Data Sheet (FN6228) and become familiar with the part's basic functions and power options. Note also that FN6228 supersedes this document with respect to updates and modifications. Always refer to that document if discrepancies occur.

All ISL55110, ISL55111 QFN and TSSOP boards are designed essentially in the same fashion. This document provides the user with the information regarding the evaluation board design, circuitry layout and driver load options.

Scope Probe Connections

Another topic to cover before getting started is the evaluation board physical connections for waveform observations. On each schematic version you will see a component with pins designated as DIF+ and DIF-. This is not an active component but a dual pin header physically designed to accommodate leadless connection of active differential or FET Probes. This will minimize ground lead inductance and capacitive loading while making waveform observations. However, the user must also be mindful of max voltage limitations when using these types of probes. The ISL55110, ISL55111 drivers cover a large voltage range, so double check the probe's specifications.

Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

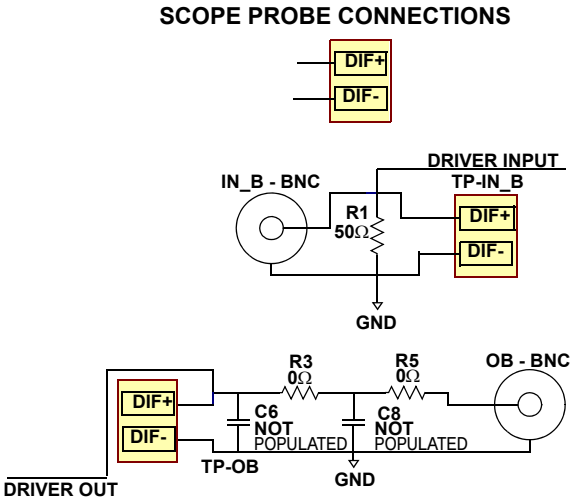

FIGURE 1. DUAL.1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

BNC Connections

This series of evaluation boards also provides BNC connections for Input and Output signals. A key point to remember is the ISL55110, ISL55111 Driver Outputs (OA/OB) operate with the VH voltage as a High and Ground as a Low. These connectors are laid out to accommodate SMD connectors as well as BNC's. Also note that the Driver Inputs have 50Ω terminations that you may need to remove for your application.

Power Down Feature

All boards provide the same capability for testing the Power Down Feature. A SPDT- Center OFF switch is provided for manual testing of the feature. In one position the PD input is connected to VDD (Power Down Enabled). In the other position the PD Input is connected to Ground.

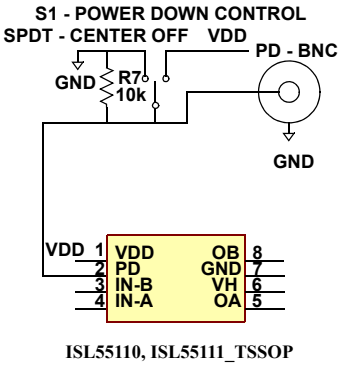

FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

Finally the center off position provides a means of connecting a repetitive signal source to the PD input. This is so that the user can observe Power Down Enable/Disable timing. An important note to remember when using the PD - BNC: 1) Place the switch in Center-Off position. 2) The PD input is referenced to VDD and ground.

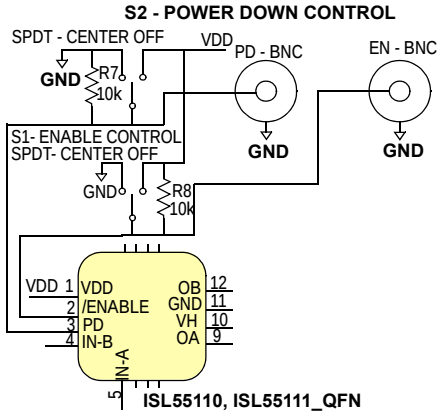

FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

Initial Power Up

Please refer to the device specification for power up sequencing and current requirements. Also note that the frequency of operation of each driver will determine the current needed. There are graphs in the specification regarding current characteristics.

When first powering up the device, set all power bus inputs to minimum current levels needed for quiescent operation. Check the device out statically with DC inputs on the IN_A/IN_B pins and observe that the OA/OB outputs toggle when the Input pins rise above and below the logic thresholds. Please note that these inputs are intended for use by high speed logic. Avoid slow DC ramps.

VDD current should be ~3.6mA and VH should be less then 100µAmps with no DC loads on the outputs.

Once static observations check out, you can then increase power current limits for VCC/VH and apply higher frequency inputs to the IN_A/IN_B pins.

Layout Information

All evaluation boards have complete silk-screen information regarding Test points, Jumpers and Component placements.

Schematic Information

Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

Included below are two schematics. ISL55110, ISL55111: TSSOP dual driver device and ISL55110, ISL55111 QFN dual driver. Both packages have the Power Down Control, while the QFN has both Power Down and $\overline{\text{Enable}}$ inputs.

Driver Loads

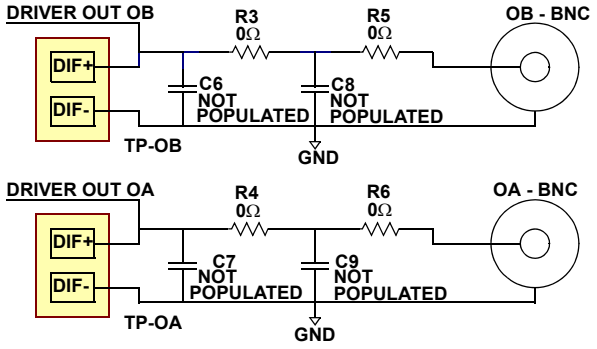

FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

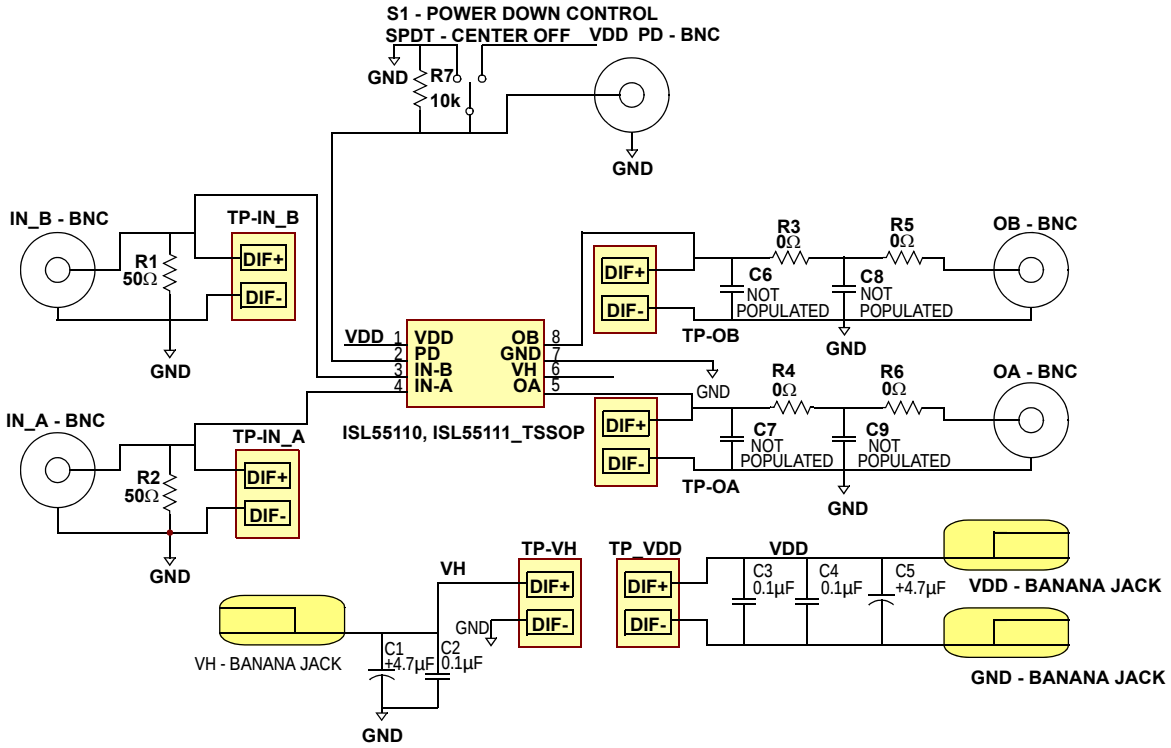

FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

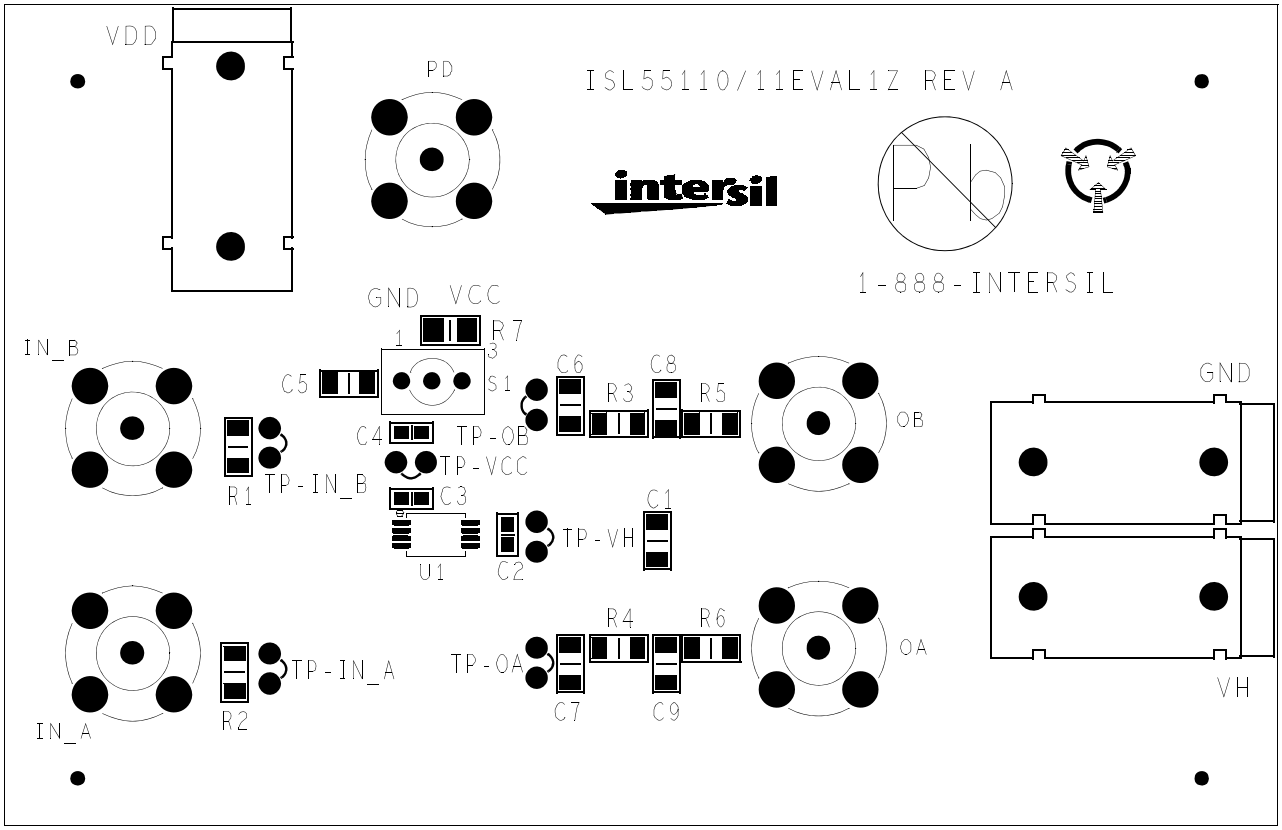

FIGURE 6. TSSOP LAYOUT

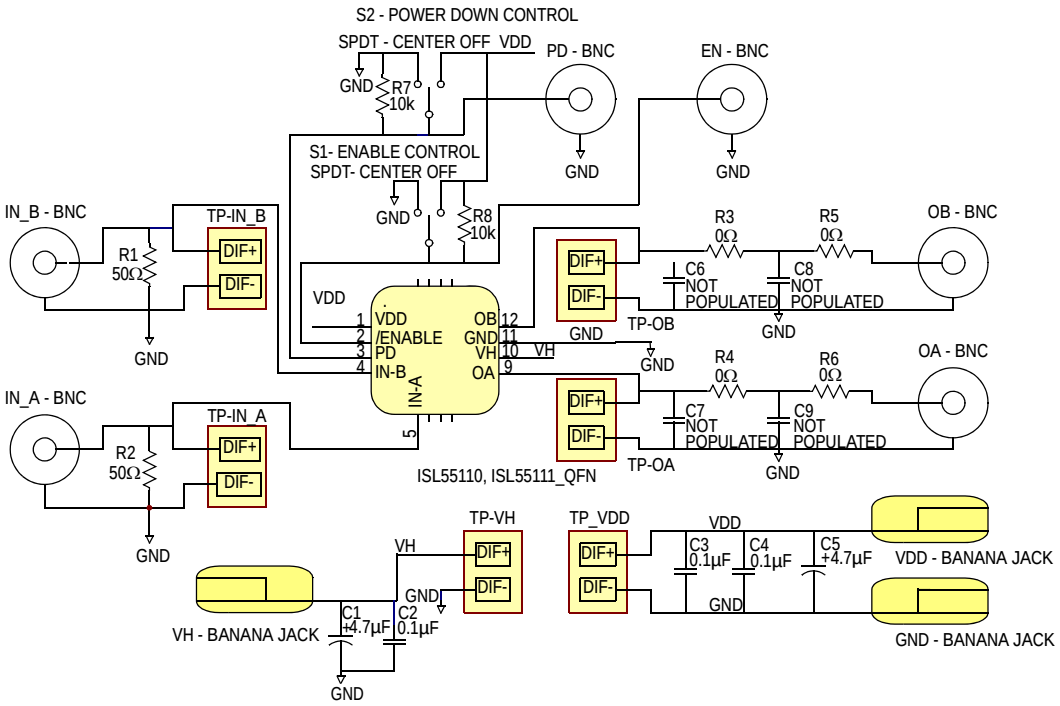

FIGURE 7. QFN EVALUATION BOARD SCHEMATIC

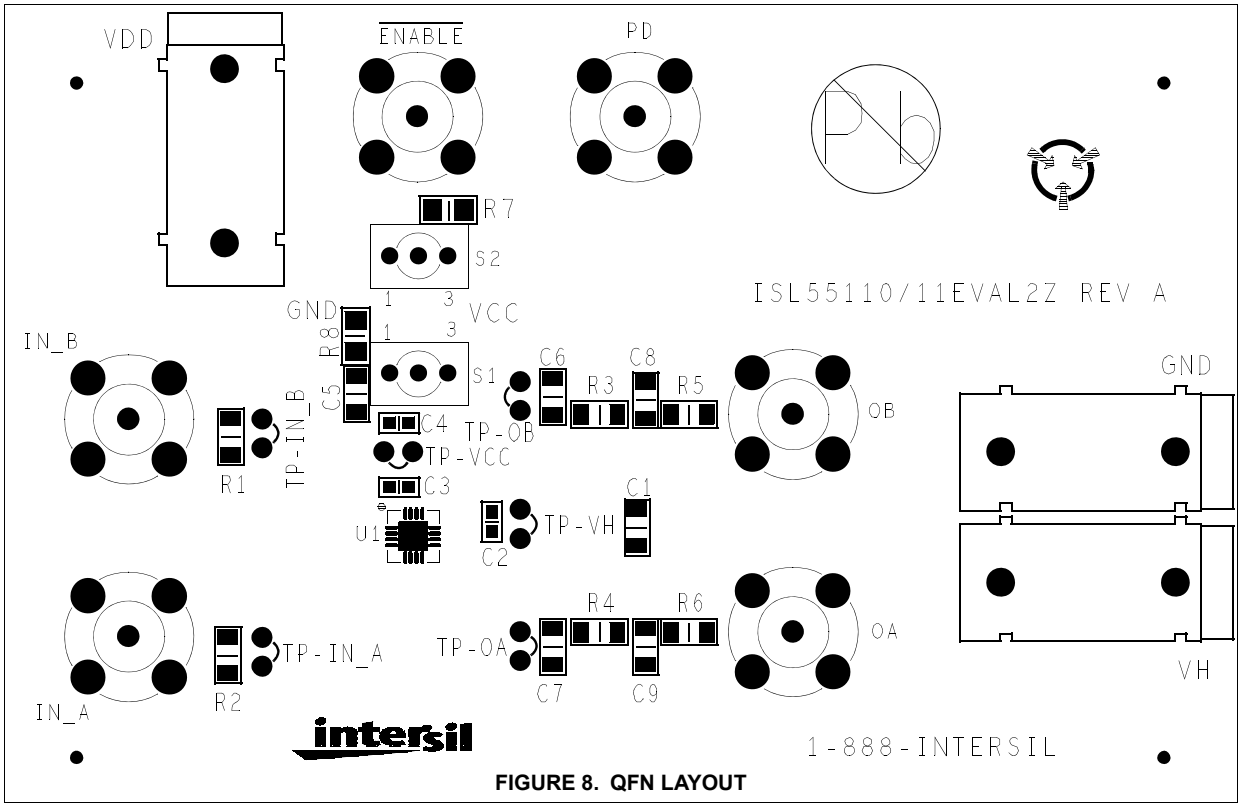

FIGURE 8. QFN LAYOUT

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0

ISL55110_11EVAL1Z, ISL55110_11EVAL2Z

Evaluation Board User's Manual

AN1283
Rev 0.00
February 13, 2007

Before Getting Started

This document supplements the ISL55110, ISL55111 Specification **FN6228**. Evaluation board users should review that document to obtain information on the parts' basic functionality and power requirements. A most important note is **before powering up the board, review the Power Up Sequence in that specification.** There are two DC sources utilized, so a user may inadvertently mis-apply the power sources causing damage to the part.

Take time to review the ISL55110, ISL55111 Data Sheet (FN6228) and become familiar with the part's basic functions and power options. Note also that FN6228 supersedes this document with respect to updates and modifications. Always refer to that document if discrepancies occur.

All ISL55110, ISL55111 QFN and TSSOP boards are designed essentially in the same fashion. This document provides the user with the information regarding the evaluation board design, circuitry layout and driver load options.

Scope Probe Connections

Another topic to cover before getting started is the evaluation board physical connections for waveform observations. On each schematic version you will see a component with pins designated as DIF+ and DIF-. This is not an active component but a dual pin header physically designed to accommodate leadless connection of active differential or FET Probes. This will minimize ground lead inductance and capacitive loading while making waveform observations. However, the user must also be mindful of max voltage limitations when using these types of probes. The ISL55110, ISL55111 drivers cover a large voltage range, so double check the probe's specifications.

Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

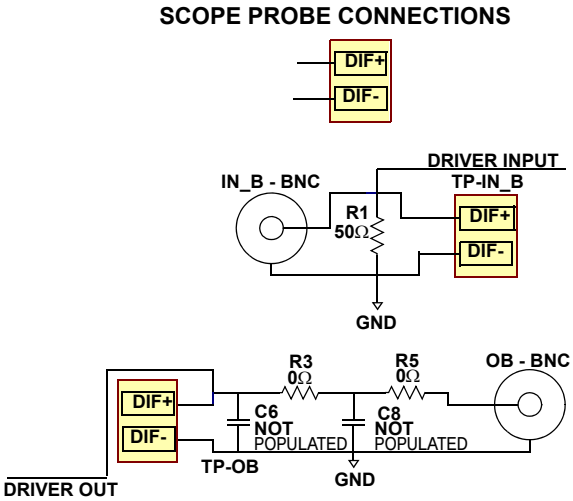

FIGURE 1. DUAL.1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

BNC Connections

This series of evaluation boards also provides BNC connections for Input and Output signals. A key point to remember is the ISL55110, ISL55111 Driver Outputs (OA/OB) operate with the VH voltage as a High and Ground as a Low. These connectors are laid out to accommodate SMD connectors as well as BNC's. Also note that the Driver Inputs have 50Ω terminations that you may need to remove for your application.

Power Down Feature

All boards provide the same capability for testing the Power Down Feature. A SPDT- Center OFF switch is provided for manual testing of the feature. In one position the PD input is connected to VDD (Power Down Enabled). In the other position the PD Input is connected to Ground.

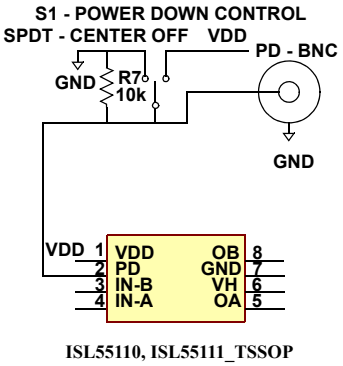

FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

Finally the center off position provides a means of connecting a repetitive signal source to the PD input. This is so that the user can observe Power Down Enable/Disable timing. An important note to remember when using the PD - BNC: 1) Place the switch in Center-Off position. 2) The PD input is referenced to VDD and ground.

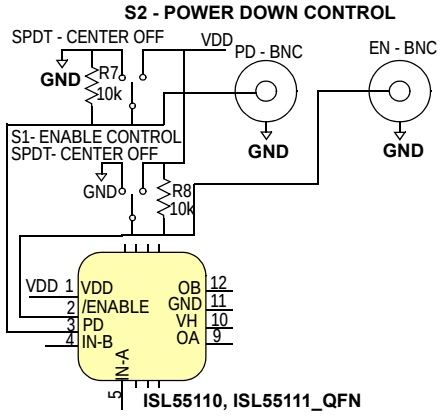

FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

Initial Power Up

Please refer to the device specification for power up sequencing and current requirements. Also note that the frequency of operation of each driver will determine the current needed. There are graphs in the specification regarding current characteristics.

When first powering up the device, set all power bus inputs to minimum current levels needed for quiescent operation. Check the device out statically with DC inputs on the IN_A/IN_B pins and observe that the OA/OB outputs toggle when the Input pins rise above and below the logic thresholds. Please note that these inputs are intended for use by high speed logic. Avoid slow DC ramps.

VDD current should be ~3.6mA and VH should be less then 100µAmps with no DC loads on the outputs.

Once static observations check out, you can then increase power current limits for VCC/VH and apply higher frequency inputs to the IN_A/IN_B pins.

Layout Information

All evaluation boards have complete silk-screen information regarding Test points, Jumpers and Component placements.

Schematic Information

Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

Included below are two schematics. ISL55110, ISL55111: TSSOP dual driver device and ISL55110, ISL55111 QFN dual driver. Both packages have the Power Down Control, while the QFN has both Power Down and $\overline{\text{Enable}}$ inputs.

Driver Loads

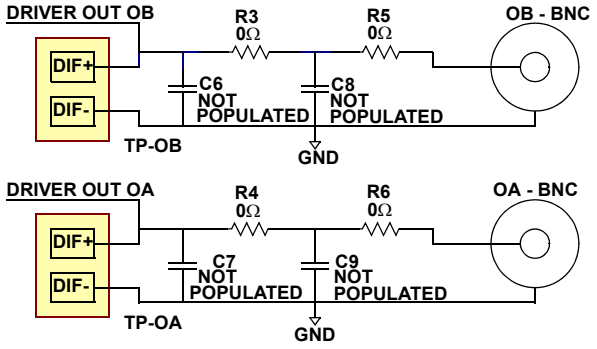

FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

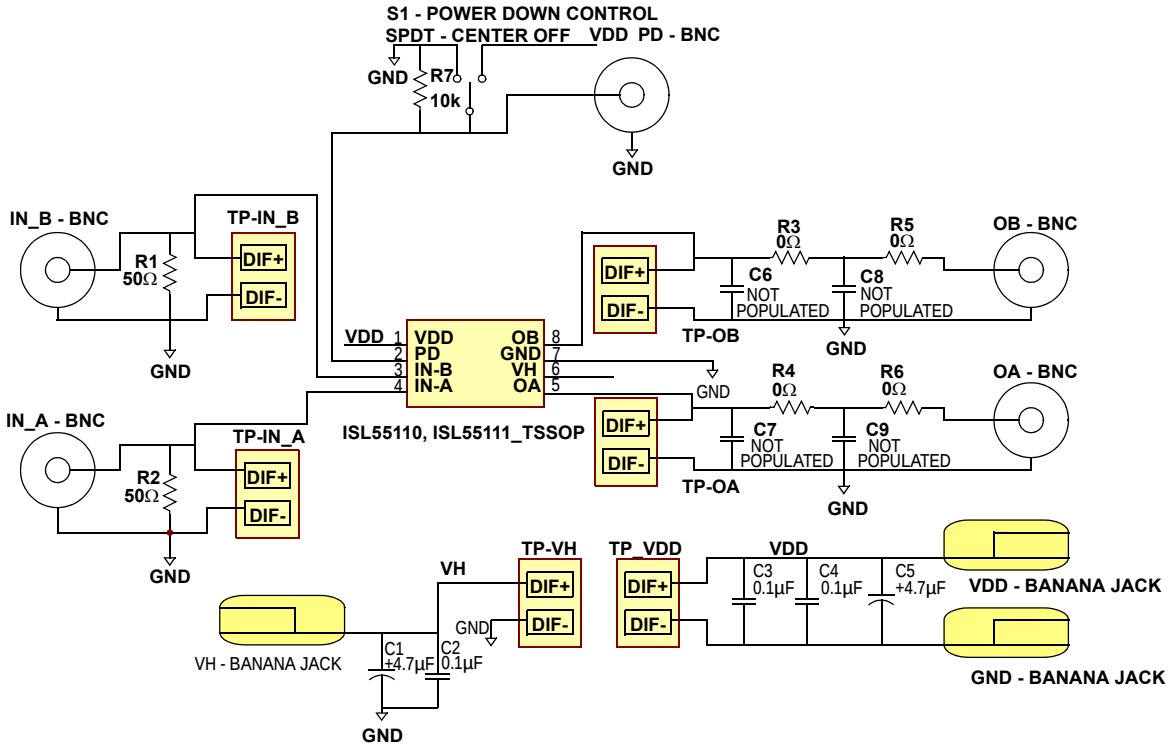

FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

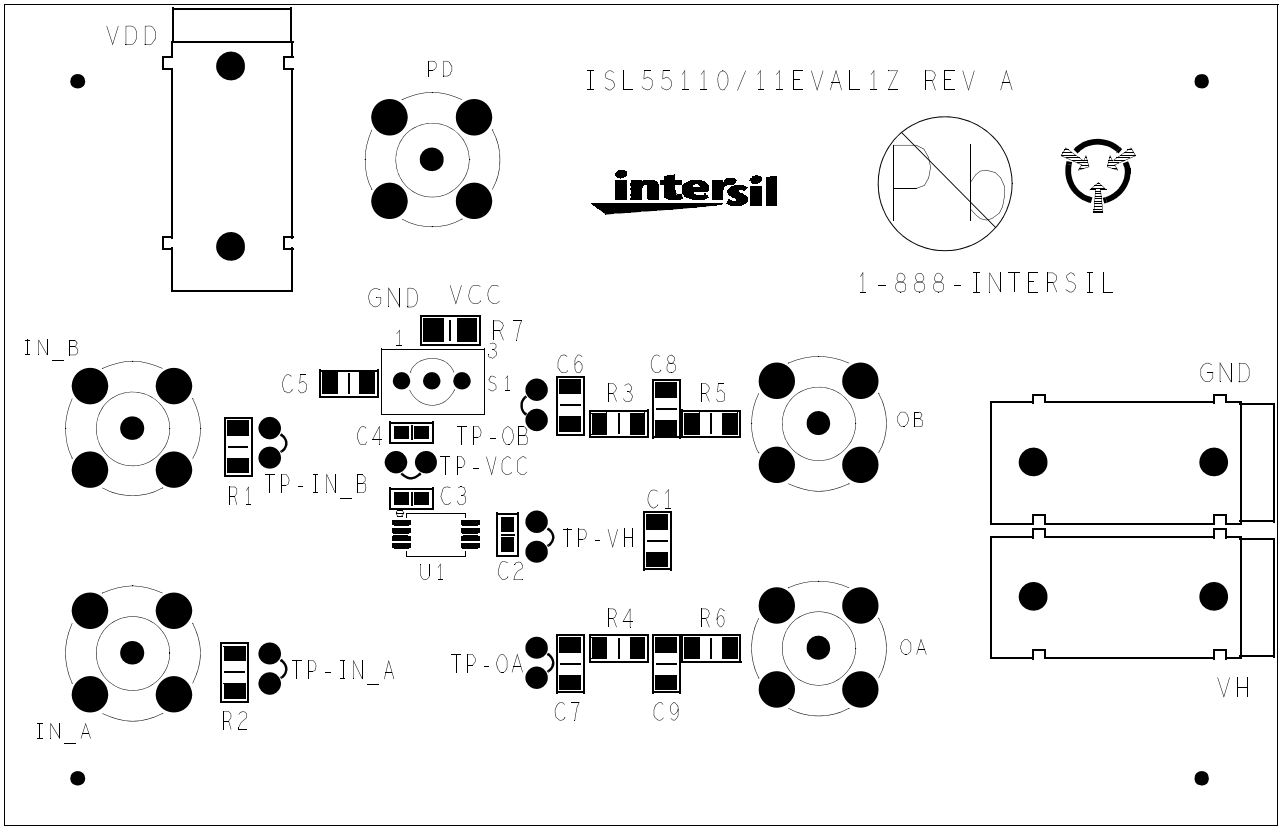

FIGURE 6. TSSOP LAYOUT

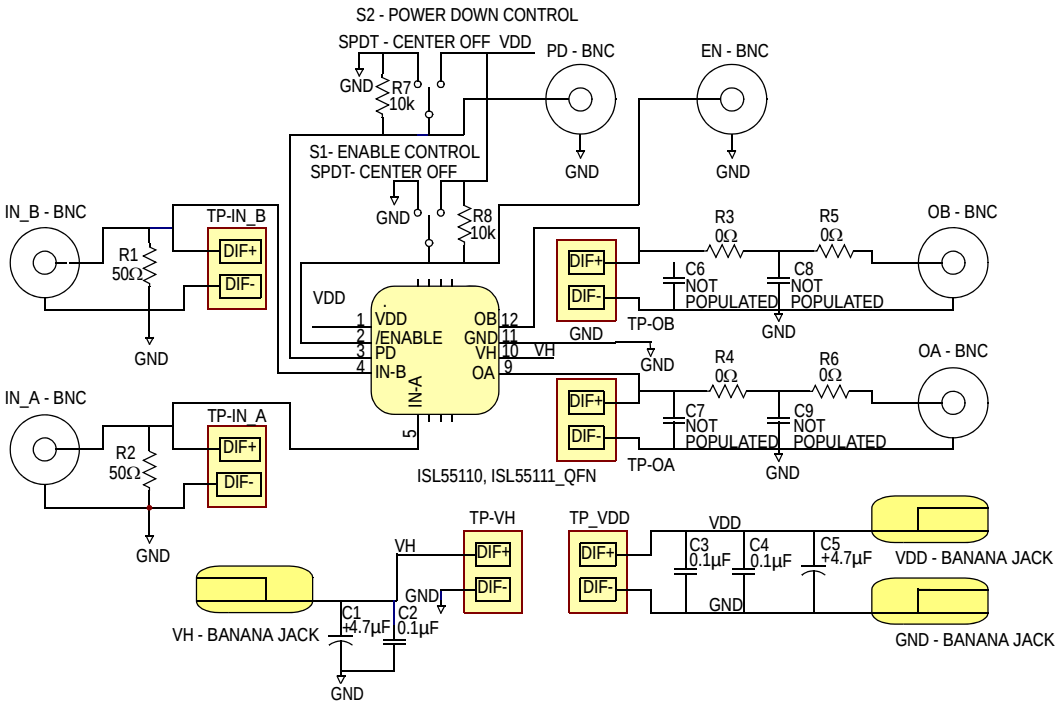

FIGURE 7. QFN EVALUATION BOARD SCHEMATIC

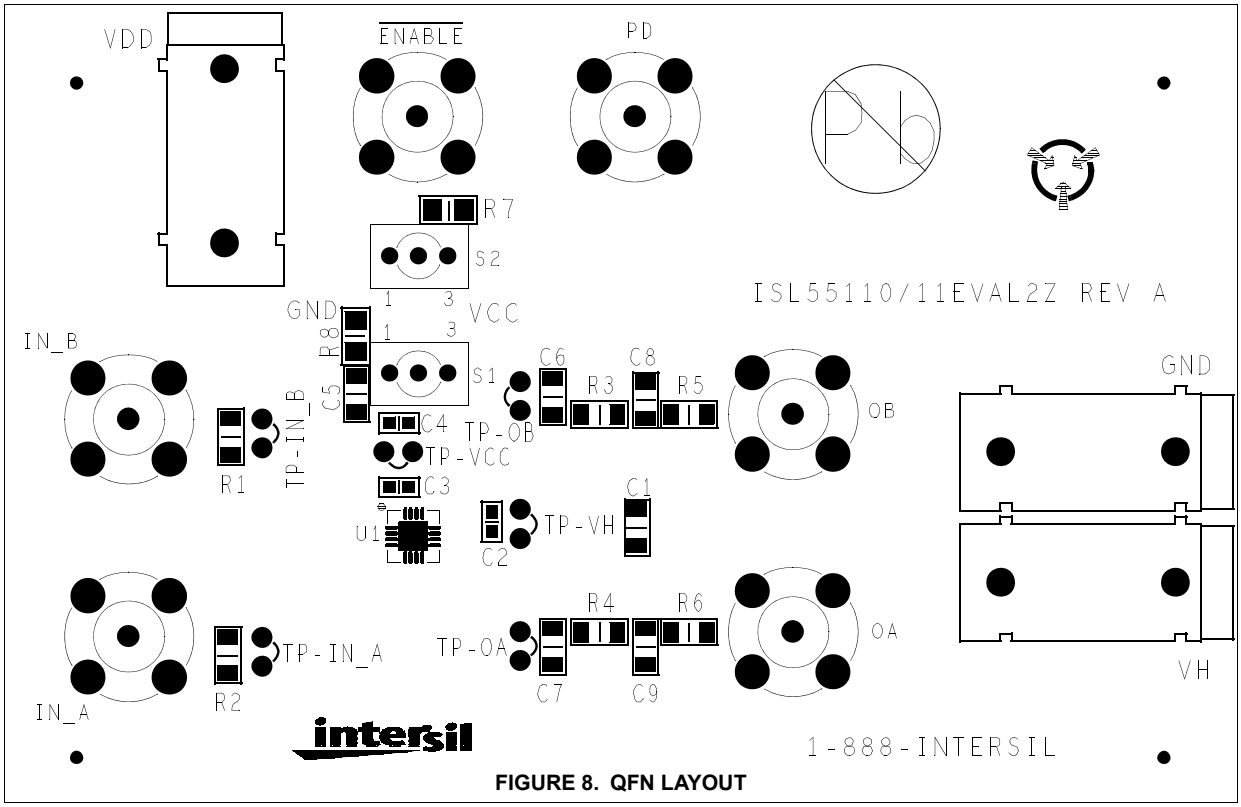

FIGURE 8. QFN LAYOUT