

Before Getting Started

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Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

SCOPE PROBE CONNECTIONS

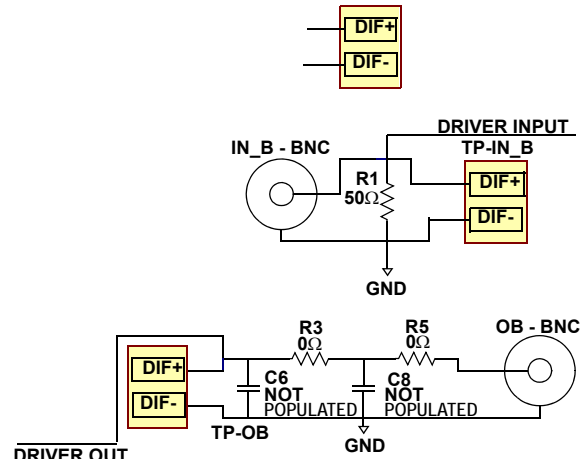


FIGURE 1. DUAL .1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

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This series of evaluation boards also provides BNC connections for Input and Output signals. A key point to remember is the ISL55110, ISL55111 Driver Outputs (OA/OB) operate with the VH voltage as a High and Ground as a Low. These connectors are laid out to accommodate SMD connectors as well as BNC's. Also note that the Driver Inputs have 50Ω terminations that you may need to remove for your application.

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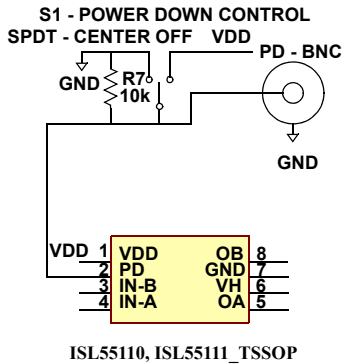


FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

Finally the center off position provides a means of connecting a repetitive signal source to the PD input. This is so that the user can observe Power Down Enable/Disable timing. An important note to remember when using the PD - BNC: 1) Place the switch in Center-Off position. 2) The PD input is referenced to VDD and ground.

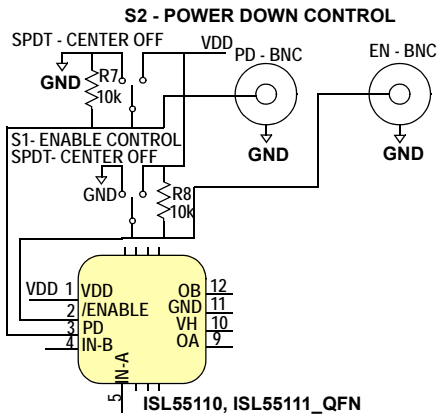


FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

Initial Power Up

Please refer to the device specification for power up sequencing and current requirements. Also note that the frequency of operation of each driver will determine the current needed. There are graphs in the specification regarding current characteristics.

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Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

Included below are two schematics. ISL55110, ISL55111: TSSOP dual driver device and ISL55110, ISL55111 QFN dual driver. Both packages have the Power Down Control, while the QFN has both Power Down and Enable inputs.

Driver Loads

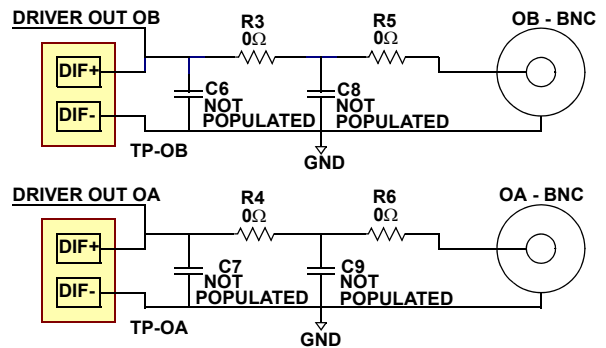


FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

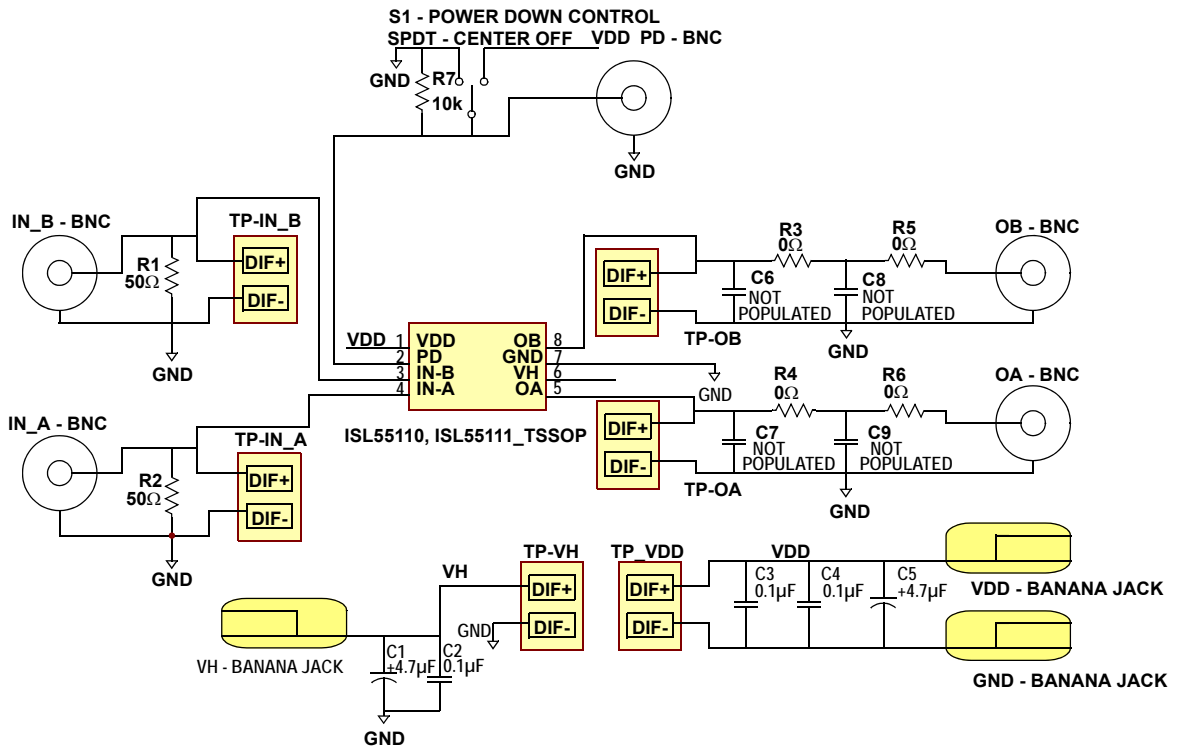


FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

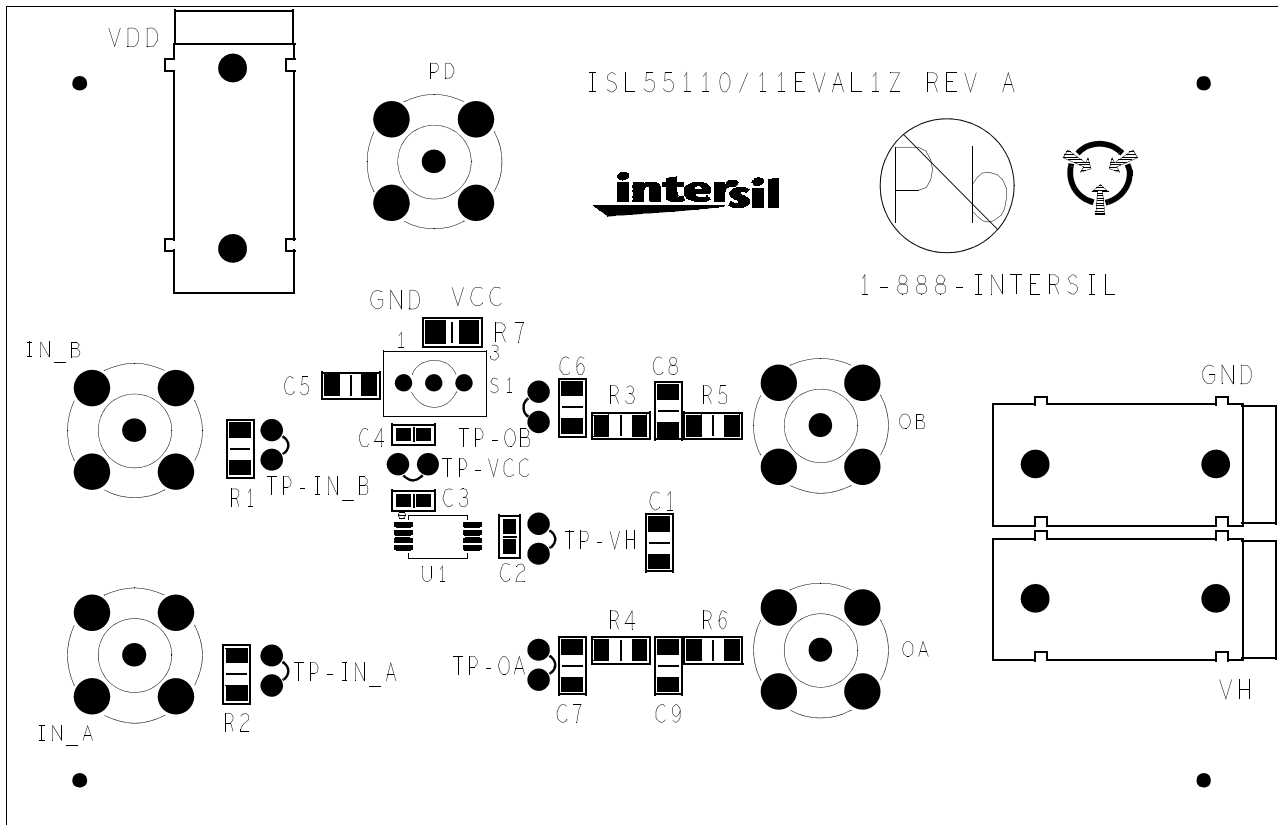


FIGURE 6. TSSOP LAYOUT

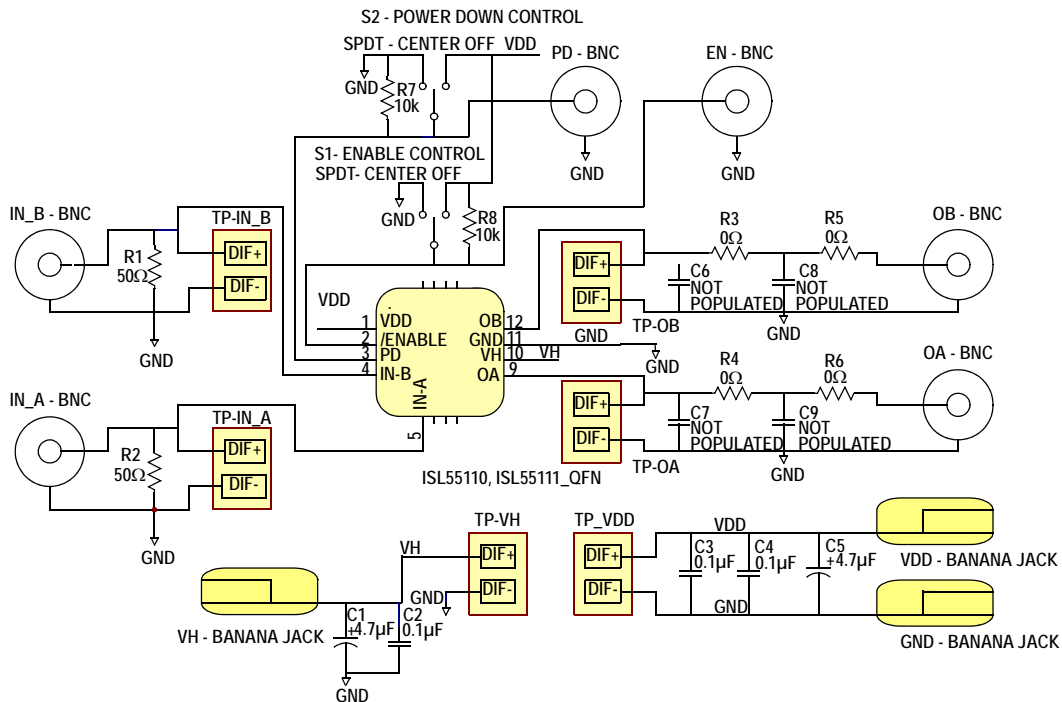


FIGURE 7. QFN EVALUATION BOARD SCHEMATIC

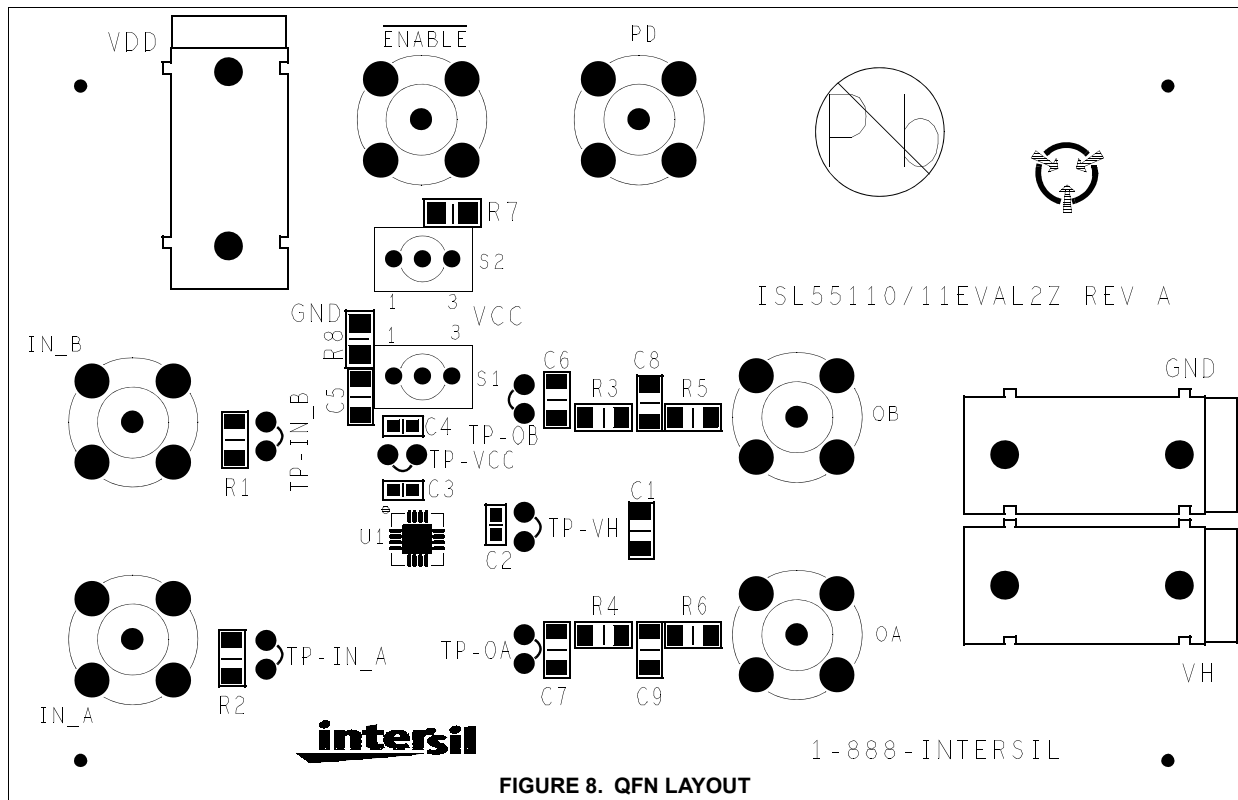


FIGURE 8. QFN LAYOUT

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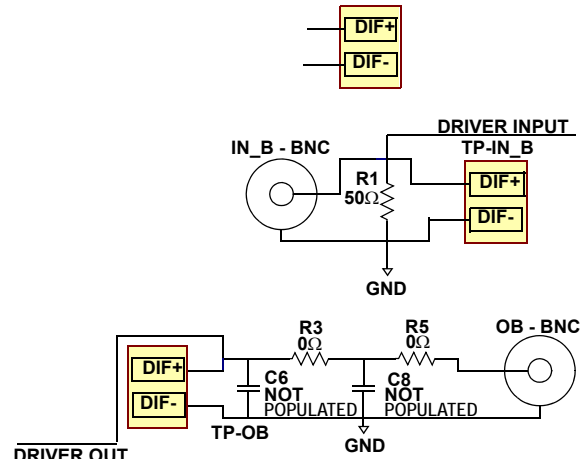


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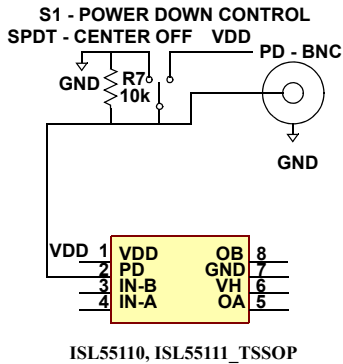


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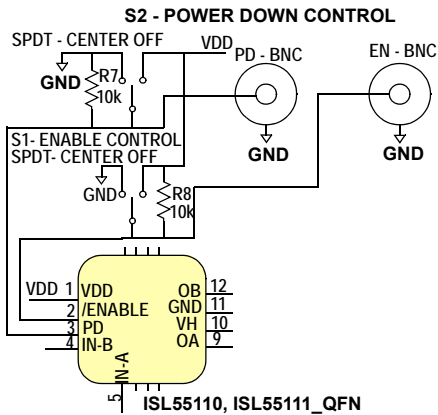


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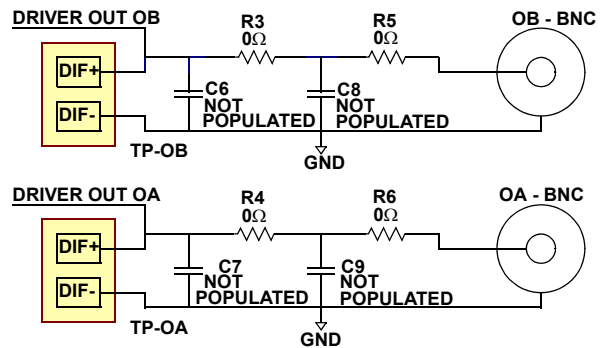


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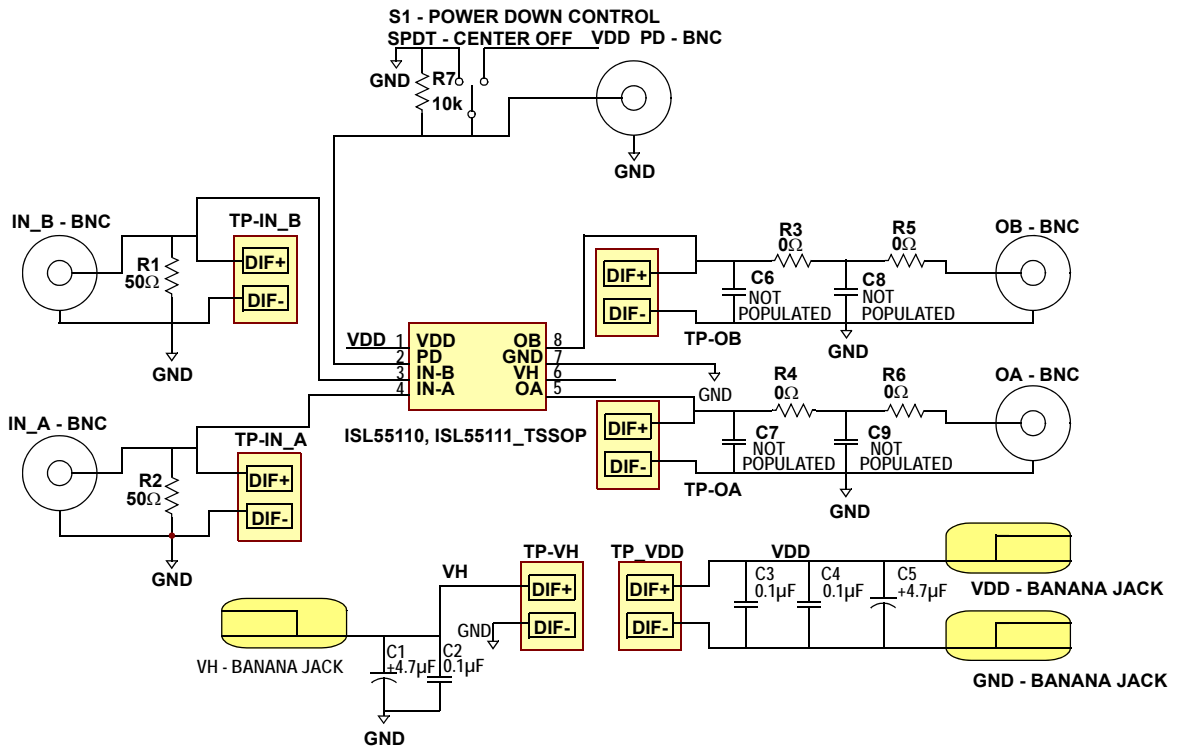


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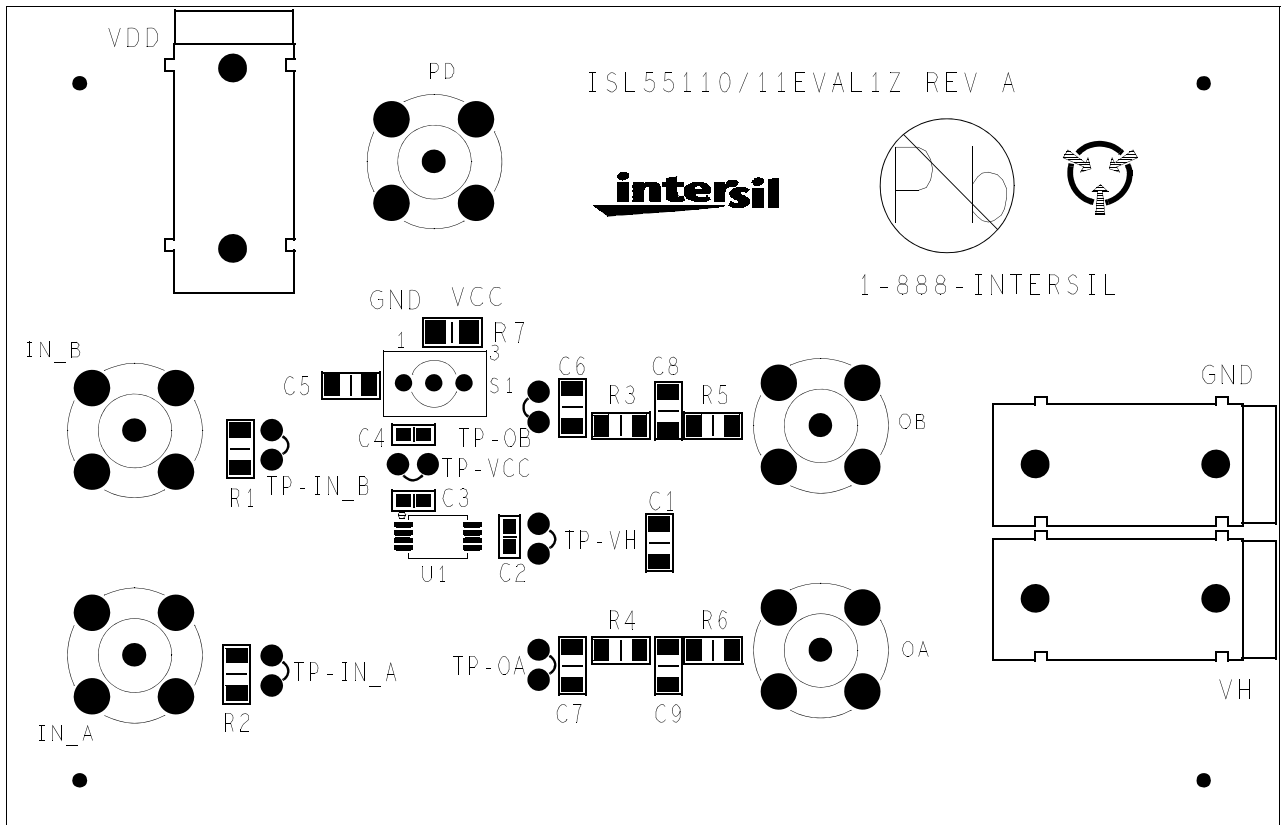


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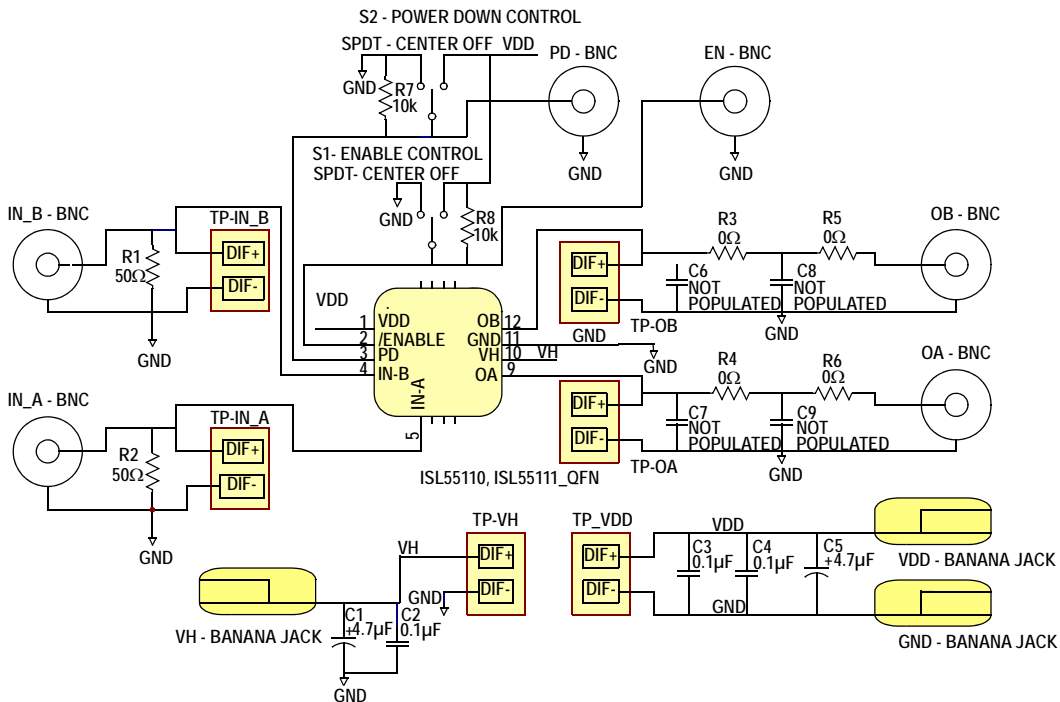


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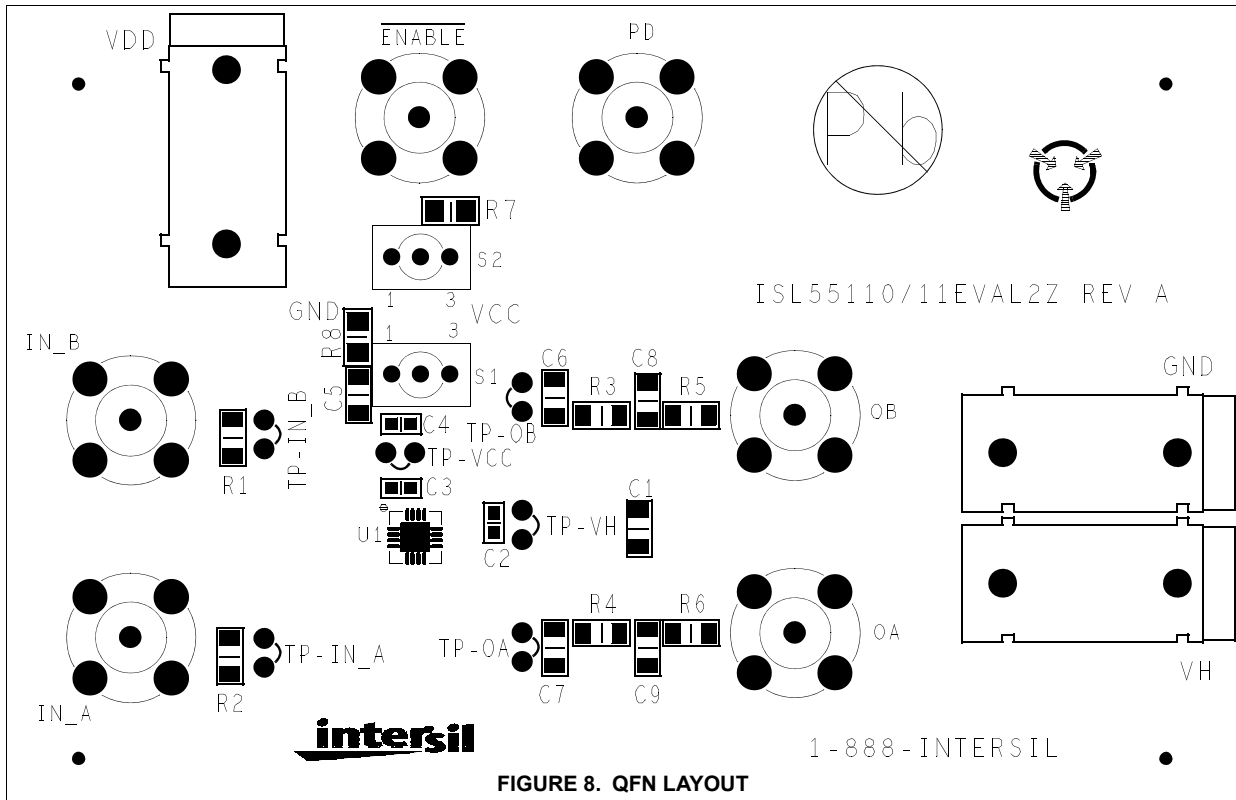


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