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Scope Probe Test Points (TP) are provisioned across all inputs, outputs and VDD/VH to ground.

SCOPE PROBE CONNECTIONS

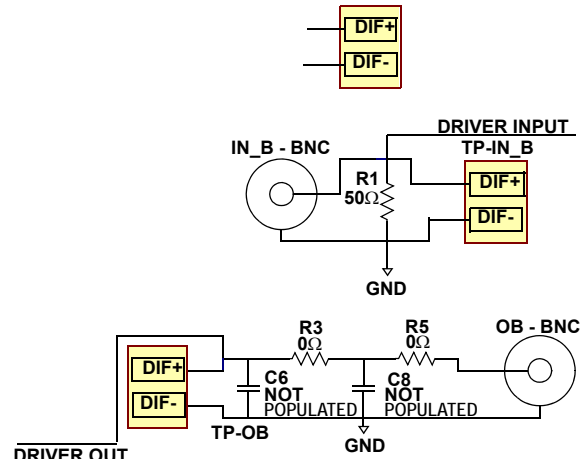


FIGURE 1. DUAL .1" SPACED PINS ARE PLACED ON THE EVALUATIONS BOARDS FOR LEADLESS ACTIVE PROBE CONNECTIONS

BNC Connections

This series of evaluation boards also provides BNC connections for Input and Output signals. A key point to remember is the ISL55110, ISL55111 Driver Outputs (OA/OB) operate with the VH voltage as a High and Ground as a Low. These connectors are laid out to accommodate SMD connectors as well as BNC's. Also note that the Driver Inputs have 50Ω terminations that you may need to remove for your application.

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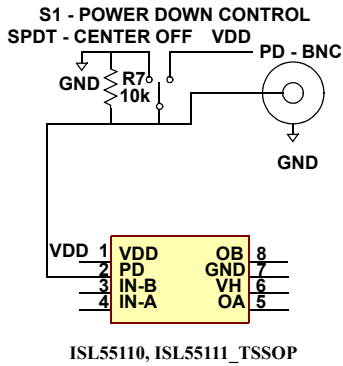


FIGURE 2. TSSOP AND QFN EVALUATION BOARDS HAVE THE SAME POWER DOWN CIRCUITRY

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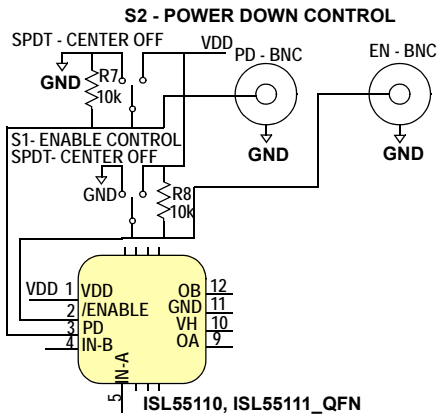


FIGURE 3. QFN PACKAGES HAVE BOTH POWER DOWN AND OUTPUT ENABLE DIGITAL INPUTS

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Schematics are drawn with physical location in mind. Any changes in electrical circuitry will be updated in this document as needed.

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Driver Loads

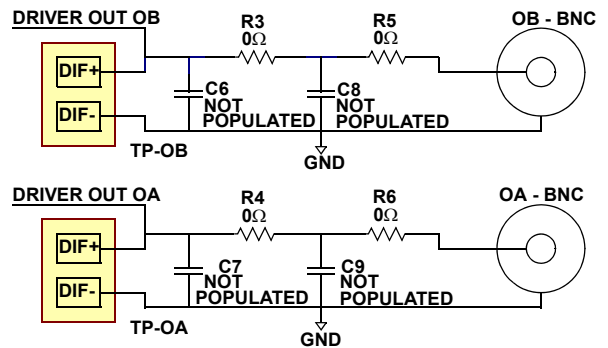


FIGURE 4. CUSTOM LOAD COMPONENTS

Component locations C6 to C7 and R3 to R6 are surface mount locations provided so the user can experiment with various load configurations.

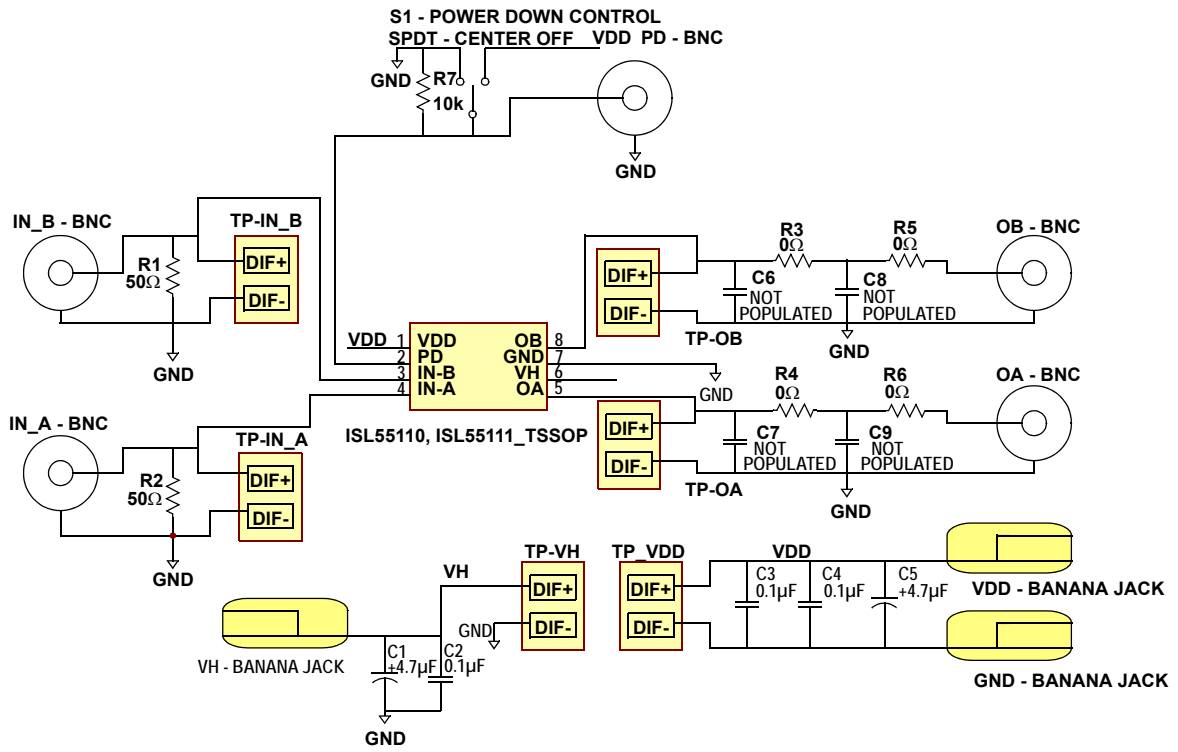


FIGURE 5. TSSOP EVALUATION BOARD SCHEMATIC

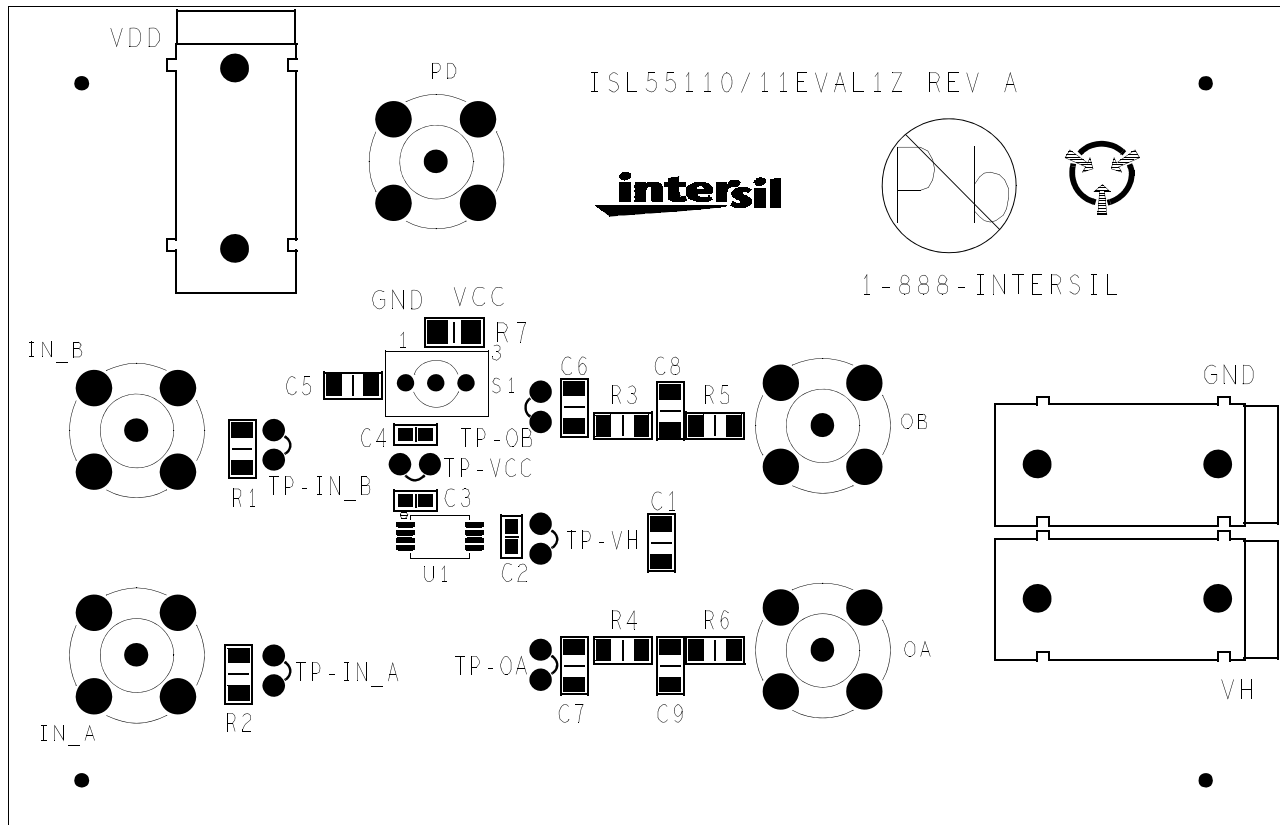


FIGURE 6. TSSOP LAYOUT

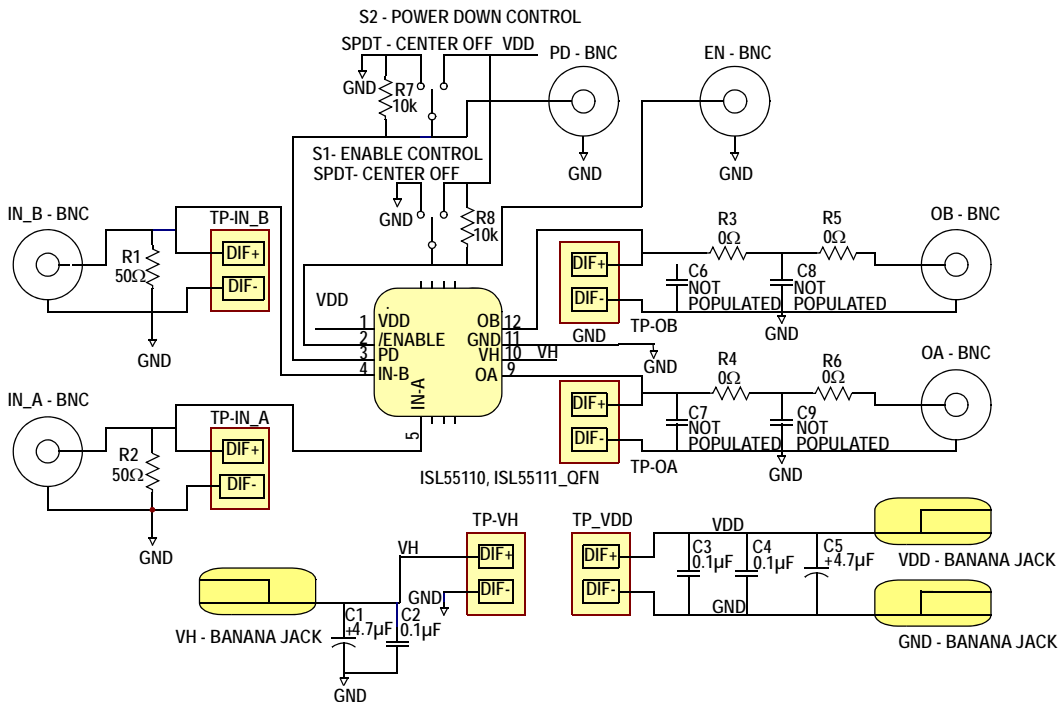


FIGURE 7. QFN EVALUATION BOARD SCHEMATIC

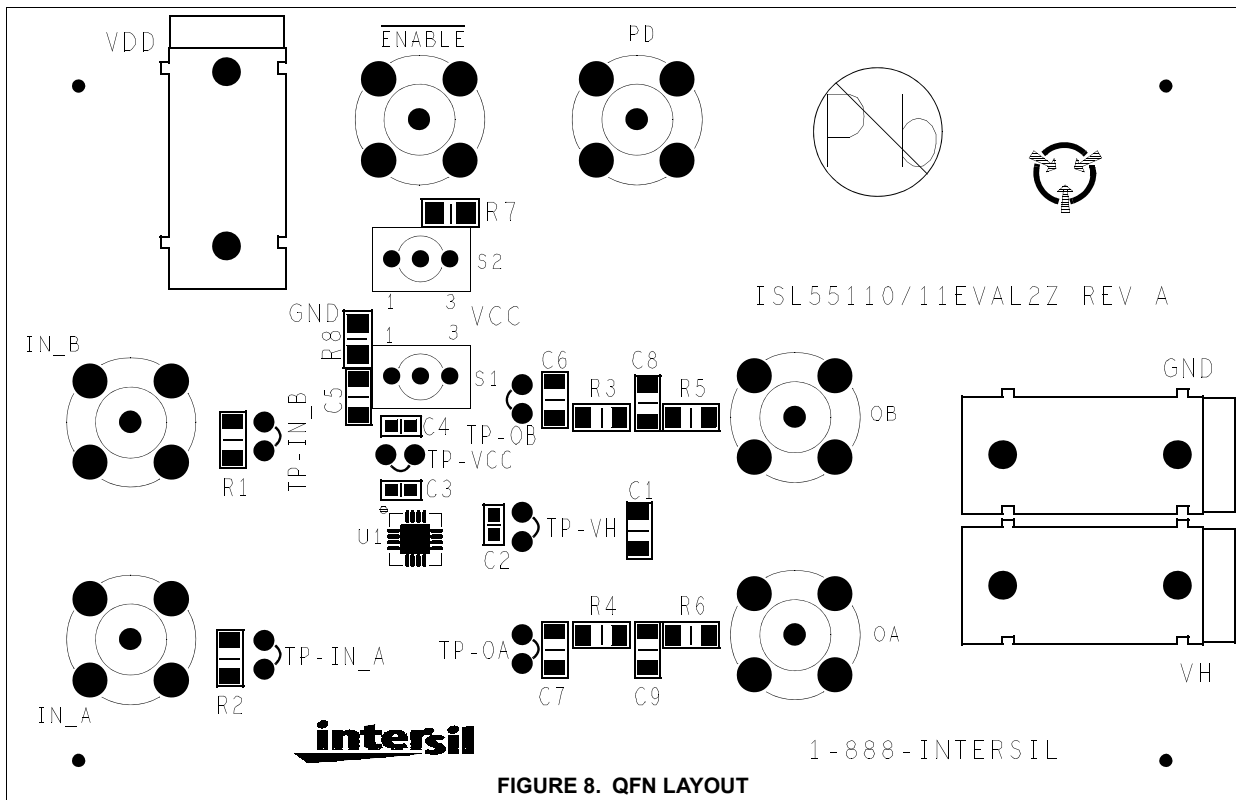


FIGURE 8. QFN LAYOUT

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(Rev.4.0-1 November 2017)



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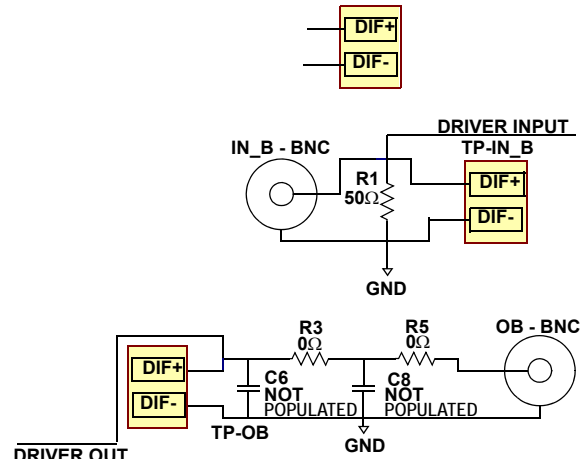


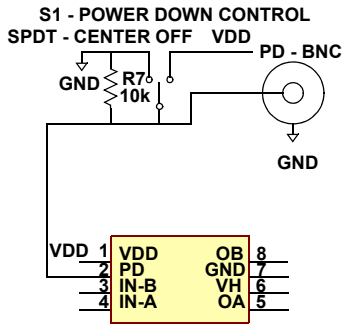
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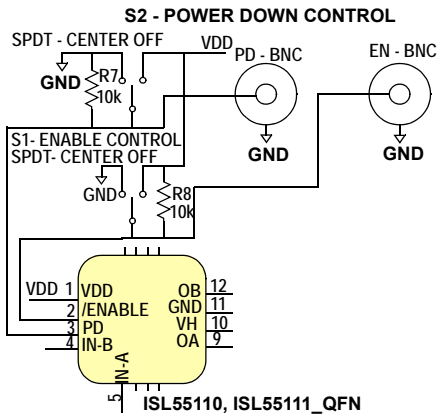
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ISL55110, ISL55111_TSSOP

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ISL55110, ISL55111_QFN

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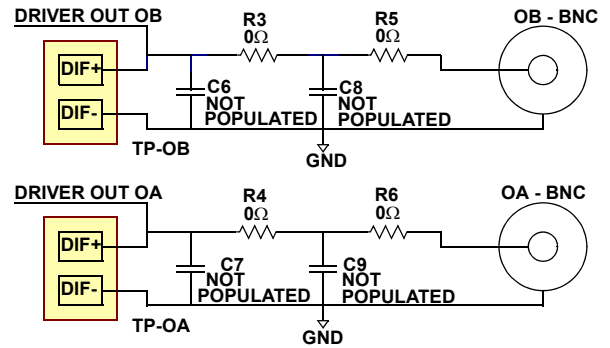


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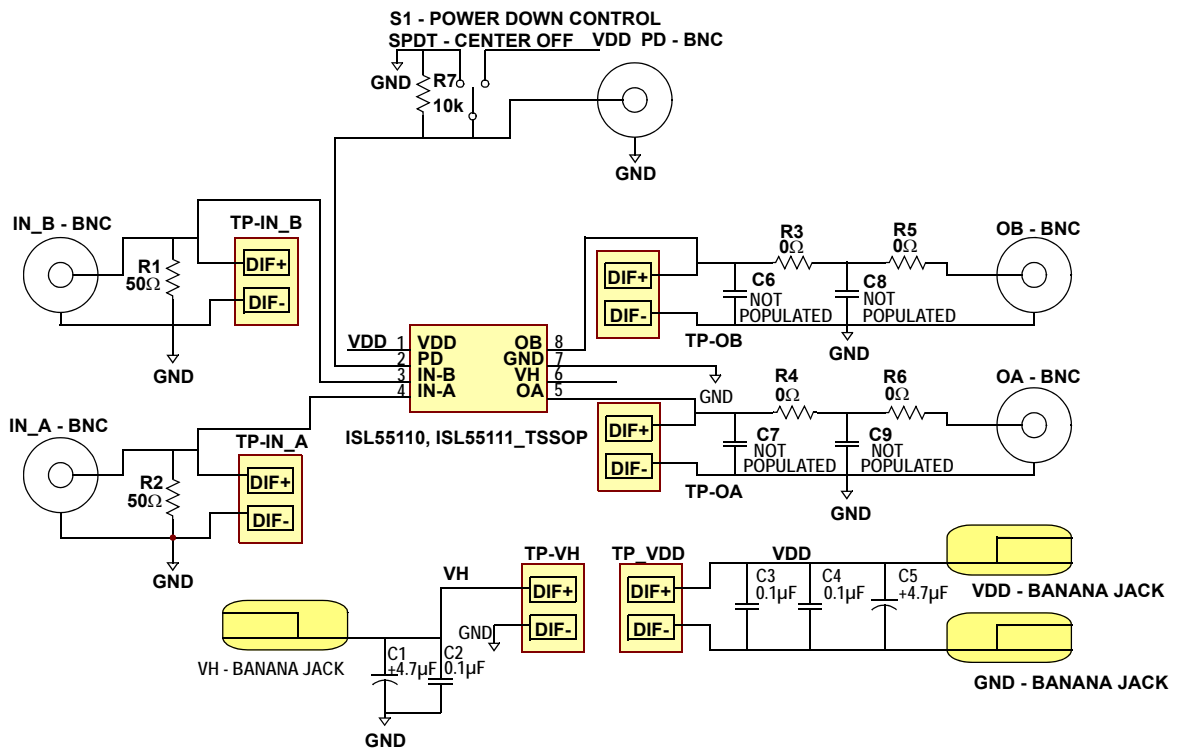


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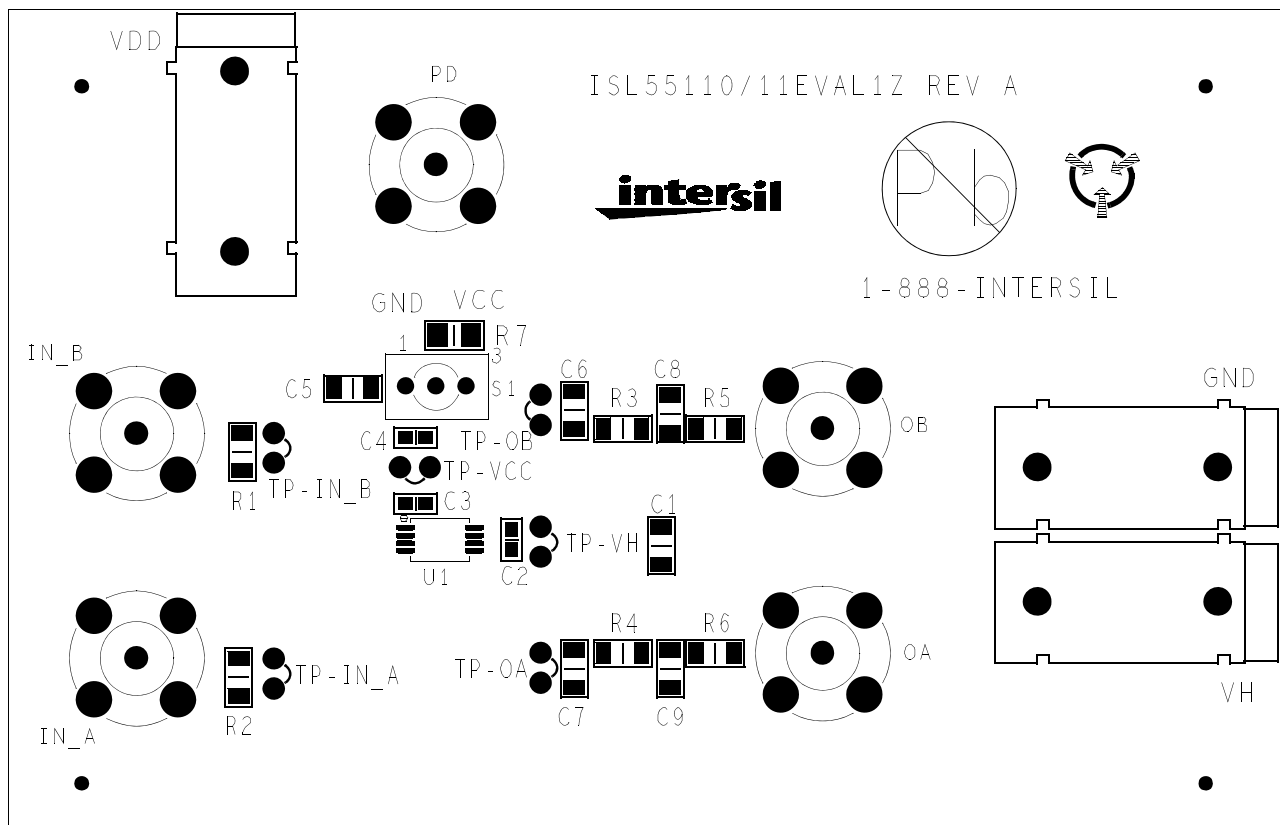


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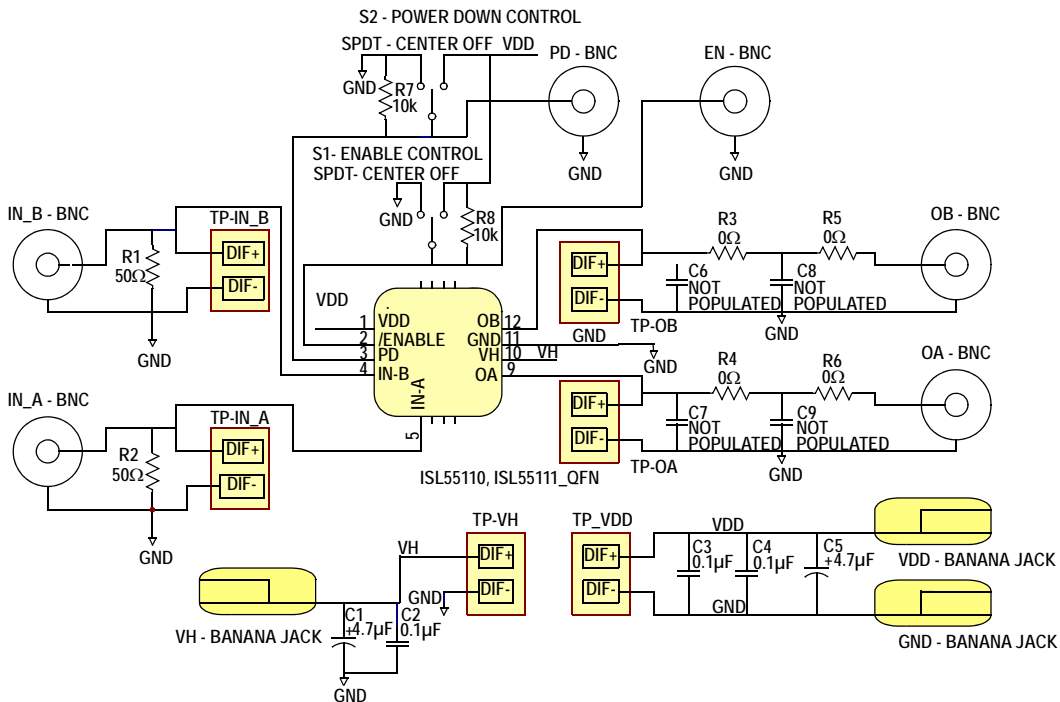


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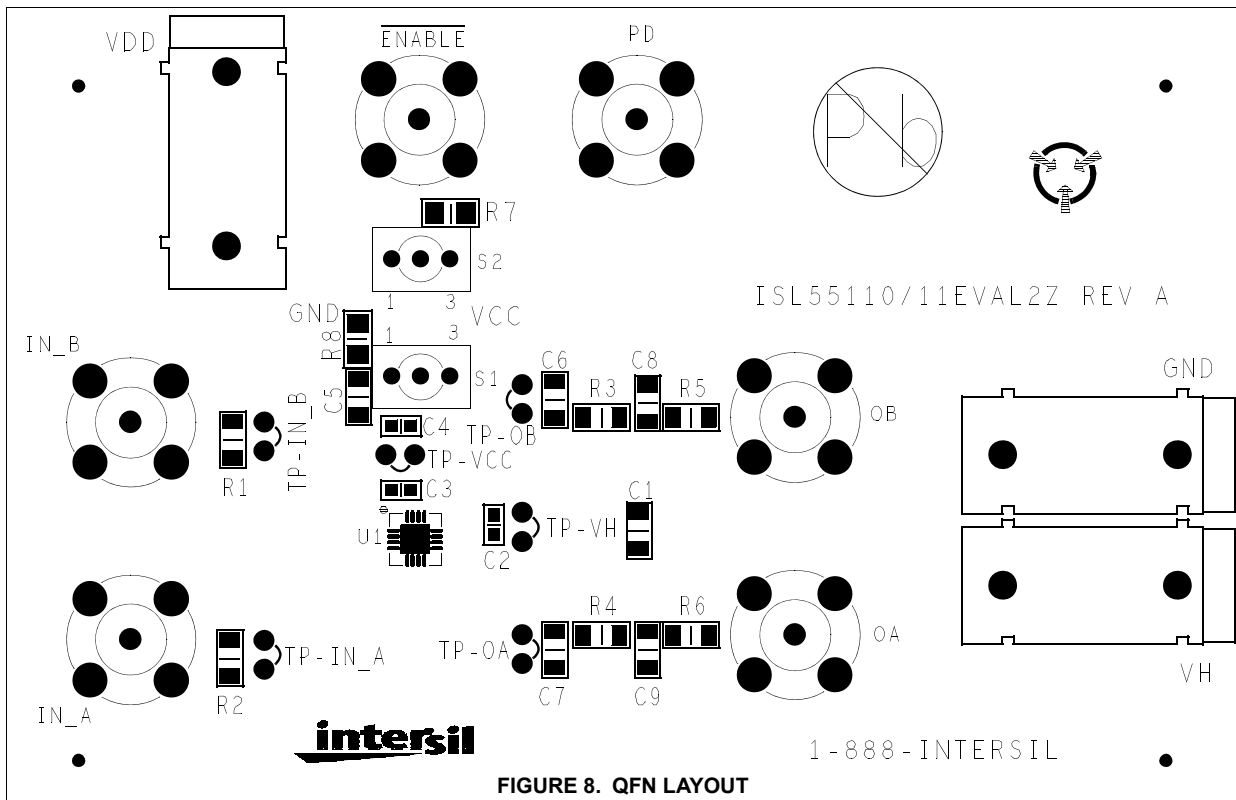


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