

ISL6255EVAL2Z

Evaluation Board

AN1297
Rev 0.00
April 10, 2007

General Description

The ISL6255EVAL2Z REV B EV kit includes all the circuitry needed to demonstrate the capabilities of the ISL6255 Lithium-Ion battery-charger with integrated AC adapter current limit. The user can experiment with an extensive matrix of battery charge parameters, AC adapter current limit, monitor functions, and load switching.

The ISL6255, ISL6255A is a highly integrated battery charger controller for Li-Ion/Li-Ion polymer batteries. High Efficiency is achieved by a synchronous buck topology and the use of a MOSFET, instead of a diode, for selecting power from the adapter or battery. The low side MOSFET emulates a diode at light loads to improve the light load efficiency and prevent system bus boosting.

The constant output voltage can be selected for 2, 3 and 4 series Li-Ion cells with 0.5% accuracy over-temperature. It can also be programmed between 4.2V + 5%/cell and 4.2V - 5%/cell to optimize battery capacity. When supplying the load and battery charger simultaneously, the input current limit for the AC adapter is programmable to within 3% accuracy to avoid overloading the AC adapter and to allow the system to make efficient use of available adapter power for charging. It also has a wide range of programmable charging current. The ISL6255, ISL6255A provides outputs that are used to monitor the current drawn from the AC adapter, and monitor for the presence of an AC adapter. The ISL6255, ISL6255A automatically transitions from regulating current mode to regulating voltage mode.

ISL6255, ISL6255A has a feature for automatic power source selection by switching to the battery when the AC adapter is removed or switching to the AC adapter when the AC adapter is available. It also provides a DC adapter monitor to support aircraft power applications with the option of no battery charging.

Features

- ±0.5% Charge Voltage Accuracy (-10°C to +100°C)
- ±3% Accurate Input Current Limit
- ±3% Accurate Battery Charge Current Limit
- ±25% Accurate Battery Trickle Charge Current Limit (ISL6255A)
- Programmable Charge Current Limit, Adapter Current Limit and Charge Voltage
- Fixed 300kHz PWM Synchronous Buck Controller with Diode Emulation at Light Load
- Output for Current Drawn from AC Adapter
- AC Adapter Present Indicator
- Fast Input Current Limit Response
- Input Voltage Range 7V to 25V
- Support 2, 3 and 4 Cells Battery Pack
- Up to 17.64V Battery-Voltage Set Point
- Control Adapter Power Source Select MOSFET
- Thermal Shutdown
- Aircraft Power Capable
- DC Adapter Present Indicator
- Battery Discharge MOSFET Control
- Less than 10µA Battery Leakage Current
- Support Pulse Charging
- Charge Any Battery Chemistry: Li-Ion, NiCd, NiMH, etc.
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Notebook, Desknote and Sub-notebook Computers
- Personal Digital Assistant

Ordering Information

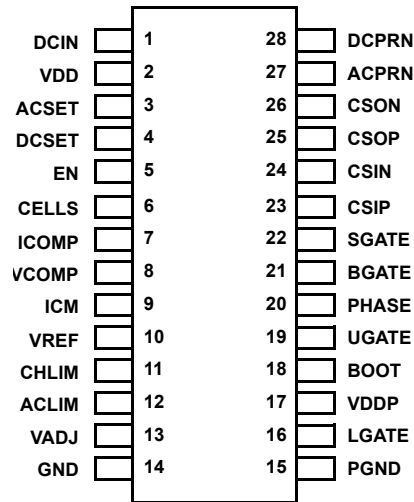
PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6255HRZ	ISL 6255HRZ	-10 to +100	28 Ld 5x5 QFN	L28.5x5
ISL6255HAZ	ISL 6255HAZ	-10 to +100	28 Ld QSOP	M28.15
ISL6255AHRZ	ISL6255 AHRZ	-10 to +100	28 Ld 5x5 QFN	L28.5x5
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NOTES:

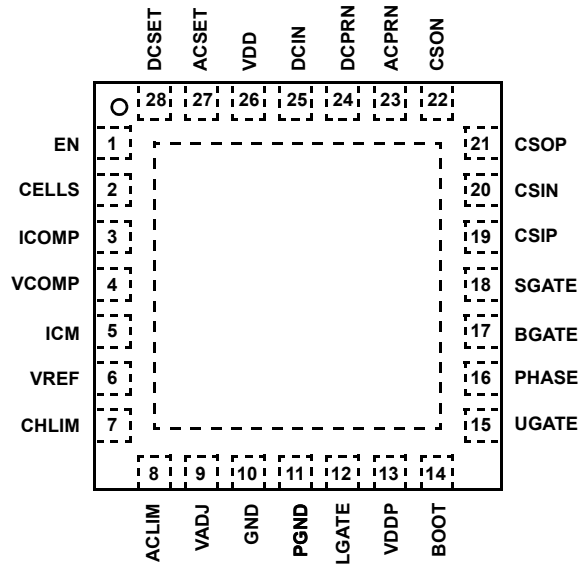
1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-T" for Tape and Reel.

Pinouts

ISL6255, ISL6255A
(28 LD QSOP)
 TOP VIEW



ISL6255, ISL6255A
(28 LD QFN)
 TOP VIEW



What's Inside

This Evaluation Board Kit contains the following materials:

- Qty(1) ISL625x EVAL2Z Evaluation Board
- Qty(1) ISL6255EVAL2Z Setup Procedure

What is Needed

The following materials are recommended to perform testing:

- One adjustable 25V 6A power supply
- Two adjustable 6A constant current electronic loads
- Two DVMs
- One 500MHz four channel oscilloscope
- Four passive oscilloscope voltage probes
- Two 10ADC Current Probes
- One Signal generator

Jumper Selection Guide

Step 1: Select the Number of Cells (Table 1)

The CELLS pin chooses the correct output voltage clamp for a given number of cells series-connected in the battery pack. Select the output voltage by placing a shunt jumper across the appropriate pins of JP1.

TABLE 1. JUMPER JP1 FUNCTIONS

SHUNT JUMPER LOCATION	CELLS PIN CONNECTED TO:	NUMBER OF CELLS CONNECTED IN SERIES	100% CONSTANT OUTPUT VOLTAGE
1 to 2	VDD	4	16.8
2 to 3	GND	3	12.6
Removed	Floating	2	8.4

Step 2: Select the Cell Trim Voltage (Table 2)

The VADJ pin trims the battery charger output voltage limit. Preset battery charger output voltage limits are selected by placing a shunt jumper across the appropriate pins of JP6. For other battery charger output voltage limits, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₄ to VADJ. Potentiometer R₂₄ may be removed and replaced with resistors R₁₉ and R₂₁. Resistor R₂₀ limits the trim increase to 1%. Shorting R₂₀ allows the trim to increase 5%. Decreasing trim range is unaffected.

TABLE 2. JUMPER JP6 FUNCTIONS

SHUNT LOCATION	VADJ PIN	BATTERY VOLTAGE CHANGE PER CELL
1 to 3	Through R ₂₀ to VREF	+5%
3 to 5	To GND	-5%
5 to 6	Floating	None
3 to 4	R ₂₄ Wiper or R ₁₉ /R ₂₁	Adjustable between -5% to +5%

Step 3: Select the Battery Charger Current Limit (Table 3)

The CHLIM pin chooses the desired battery charger current limit threshold. Preset battery charger current limit thresholds are selected by placing a shunt jumper across the appropriate pins of JP4. For other battery charger current limit thresholds, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₂ to CHLIM. Potentiometer R₂₂ may be removed and replaced with resistors R₆ and R₇.

TABLE 3. JUMPER JP4 FUNCTIONS

SHUNT JUMPER LOCATION	CHLIM PIN CONNECTED TO:	100% CURRENT FEEDBACK CSOP TO CSON	100% CONSTANT CURRENT
1 to 3	VREF	120mV	4.80A
Removed	Floating	0V	0A
3 to 5	GND	0V	0A
3 to 4	R ₂₂ or R ₆ /R ₇	0mV to 120mV	0A to 4.8A

Step 4: Select the AC Adapter Current Limit (Table 4)

The ACLIM pin chooses the desired AC adapter current limit threshold. Preset AC adapter current limit thresholds are selected by placing a shunt jumper across the appropriate pins of JP5. For other AC adapter current limit thresholds, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₃ to ACLIM. Potentiometer R₂₃ may be removed and replaced with resistors R₁₇ and R₁₈.

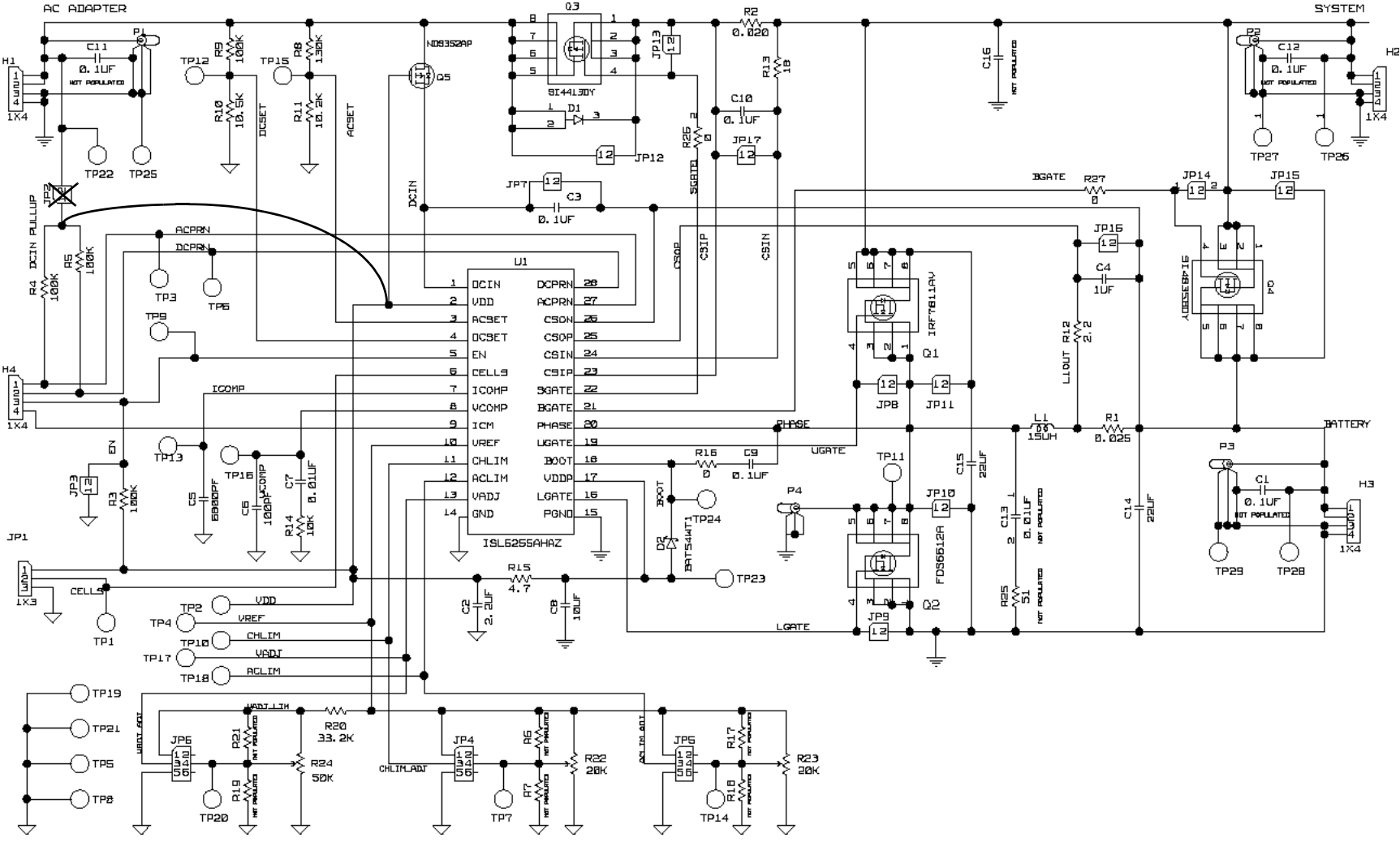
TABLE 4. JUMPER JP5 FUNCTIONS

SHUNT JUMPER LOCATION	ACLIM PIN CONNECTED TO:	100% CURRENT FEEDBACK CSIP TO CSIN	100% ADAPTER CURRENT
1 to 3	VREF	100mV	5.15A
Removed	Floating	75mV	3.90A
3 to 5	GND	50mV	2.65A
3 to 4	R ₂₃ or R ₁₇ /R ₁₈	50mV to 100mV	2.65A to 5.15A

Interface Connections

TABLE 5.

HEADER	PIN#	CONNECT TO
H1 INPUT POWER	1	"+" INPUT POWER
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" INPUT POWER
H2 SYSTEMLOAD OUTPUT	1	"+" SYSTEM LOAD OUTPUT
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" SYSTEM LOAD OUTPUT
H3 BATTERY CHARGER OUTPUT	1	"+" BATTERY CHARGER OUTPUT
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" BATTERY CHARGER OUTPUT



ISL6255EVAL2Z Schematic

TABLE 6. BILL OF MATERIALS

QTY	REF DES	DESCRIPTION	MFG NAME	PART NUMBER
1	C6	Capacitor, SMD, 0603, 100pF, 50V, 5%, COG	TDK	C1608COG1H101J
1	C7	Capacitor, SMD, 0805, 0.01 μ F, 50V, 5%, COG	TDK	C2012COG1H103J
1	C5	Capacitor, SMD, 0805, 6800pF, 50V, 5%, COG	TDK	C2012COG1H682J
3	C2, C4, C8	Capacitor, SMD, 0805, 1.0 μ F, 16V, 20%, X7R	TDK	C2012X7R1C105M
3	C3, C9, C10	Capacitor, SMD, 0805, 0.1 μ F, 50V, 10%, X7R	TDK	C2012X7R1H104K
2	C14, C15	Capacitor, SMD, 1812, 22 μ F, 25V, 20%, X5R	TDK	C4532X5R1E226M
1	L1	Choke, SMD, 8mm, 15 μ H, 20%, 5.65A, Shielded	Sumida	CDRH127/LD-150NC
1	U1	IC, Battery Charger, 24 Ld QSOP, -10°C to +100°C	Intersil	ISL6251HAZ
1	Q2	MOSFET, N-CH, 8P, SOIC, 30V, 8.4A, 0.022 Ω	Fairchild	FDS6612A
1	Q1	MOSFET, N-CH, 8P, SOIC, 30V, 10.8A, 0.011 Ω	IR	IRF7811AV
1	Q3	MOSFET, P-CH, SOIC, 30V, 13A, 0.014 Ω	Siliconix	SI4413DY
1	Q4	MOSFET, P-CH, SOIC, 30V, 6A, 0.033 Ω	Siliconix	SI4835BDY
1	Q5	MOSFET, P-CH, 3P, SOT23, -30V, -0.9A, 0.5 Ω	Fairchild	NDS352AP
1	D1	DIODE SCHOTTKY 40V 10A POWERDI5	Diodes Inc.	PDS1040-13
1	D2	SURFACE MOUNT SCHOTTKY BARRIER DIODE	Diodes Inc	BAT54WT1
1	R2	Resistor, Shunt, SMD, 2010, 0.020 Ω , 1W, 1%	IRC	LRC-LRF2010-01-R020-F
1	R1	Resistor, Shunt, SMD, 2010, 0.025 Ω , 1W, 1%	IRC	LRC-LRF2010-01-R025-F
1	R13	Resistor, SMD, 0805, 18 Ω , 0.125W, 5%	KOA	RK73B2AT180J
1	R12	Resistor, SMD, 0805, 2.2 Ω , 0.125W, 5%	KOA	RK73B2AT2R2J
1	R15	Resistor, SMD, 0805, 4.7 Ω , 0.125W, 5%	KOA	RK73B2AT4R7J
1	R14	Resistor, SMD, 0805, 10k Ω , 0.125W, 1%	KOA	RK73H2AT1002F
1	R11	Resistor, SMD, 0805, 7.87k Ω , 0.125W, 1%	KOA	RK73H2AT7871F
3	R3, R4, R8	Resistor, SMD, 0805, 100k Ω , 0.125W, 1%	KOA	RK73H2AT1003F
1	R20	Resistor, SMD, 0805, 33.2k Ω , 0.125W, 1%	KOA	RK73H2AT3322F
1	R16	Resistor, SMD, 0805, 0 Ω , 2A, 50m Ω Max	KOA	RK73Z2AT

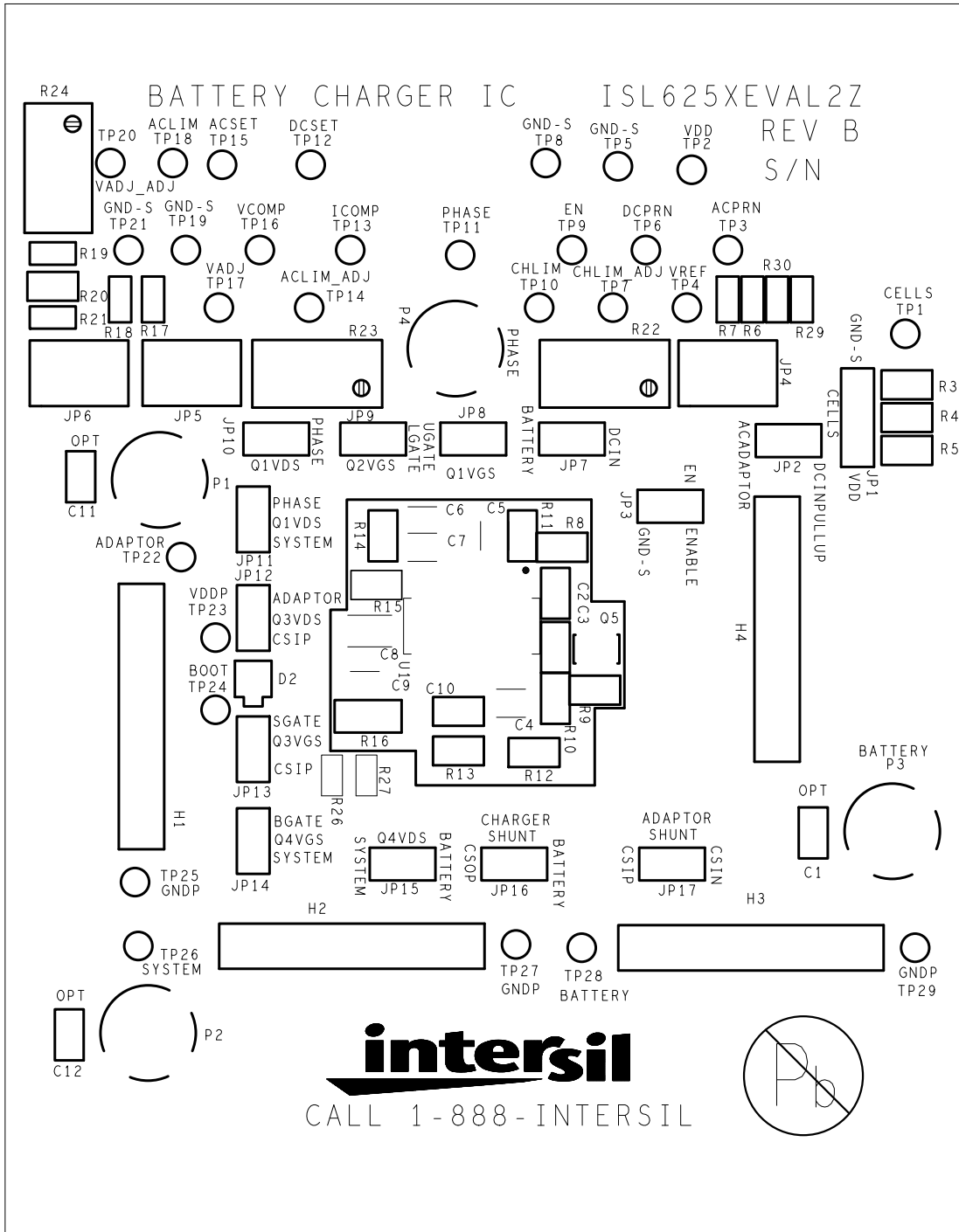


FIGURE 1. TOP SILK

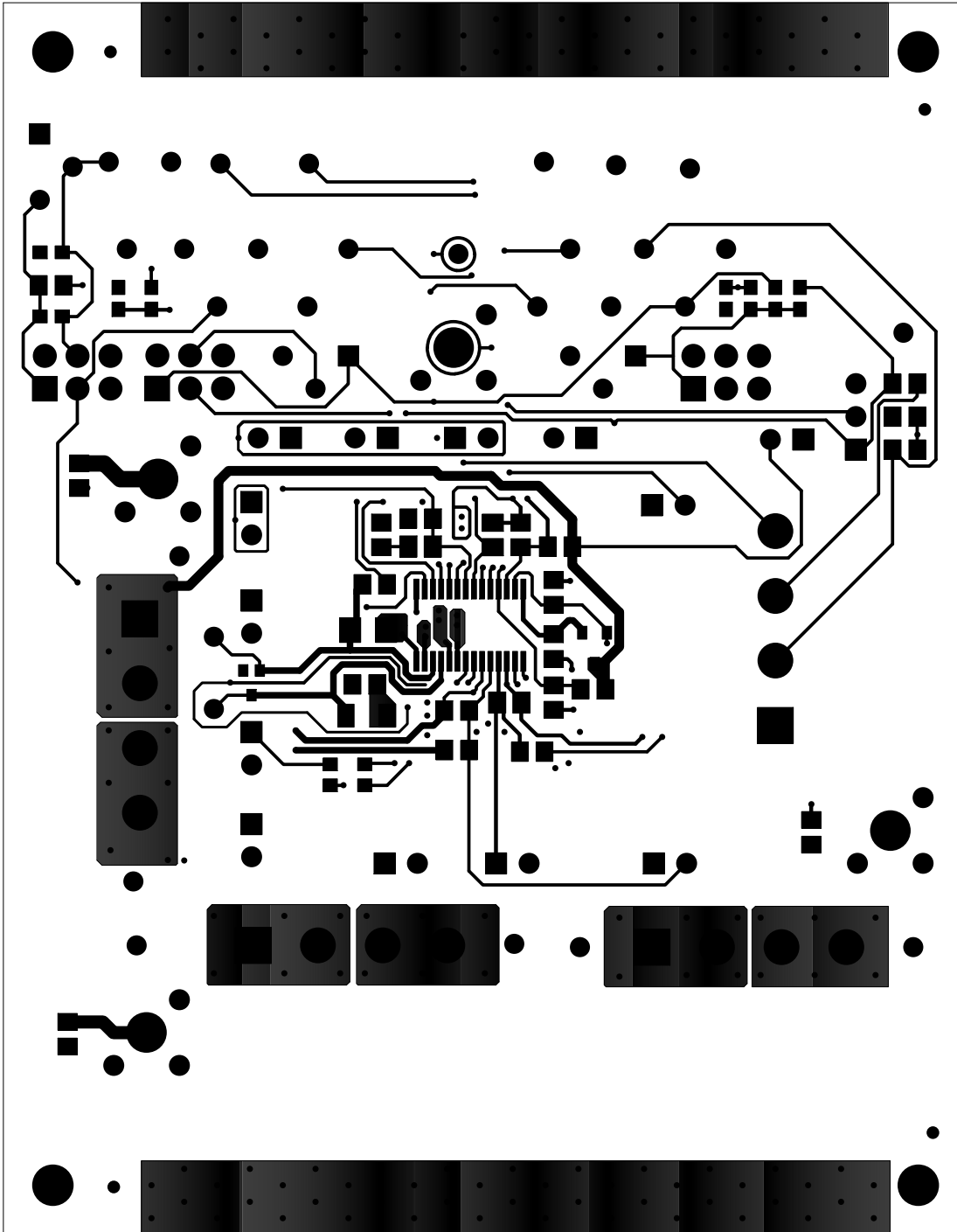


FIGURE 2. TOP LAYER

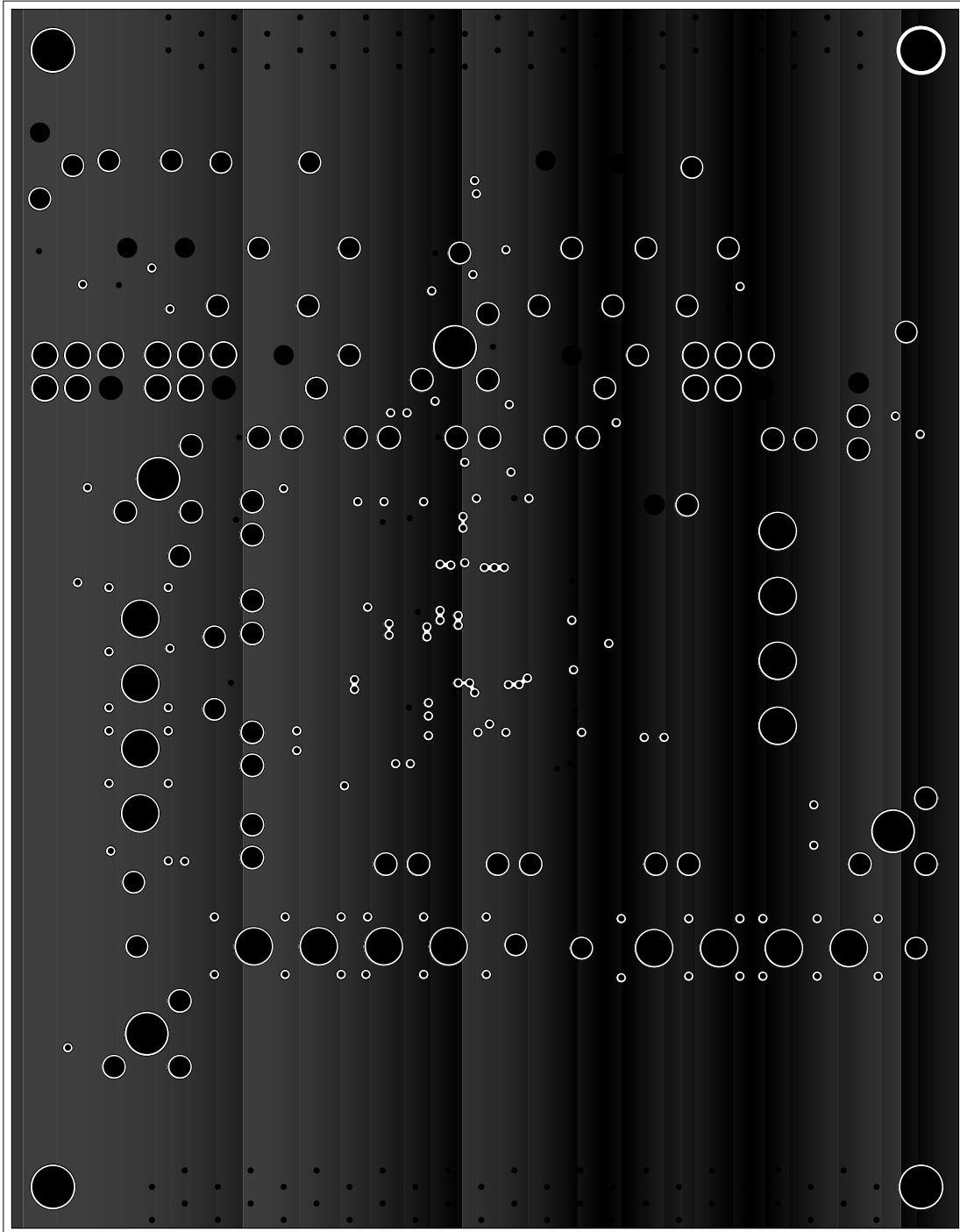


FIGURE 3. LAYER 2 GROUND

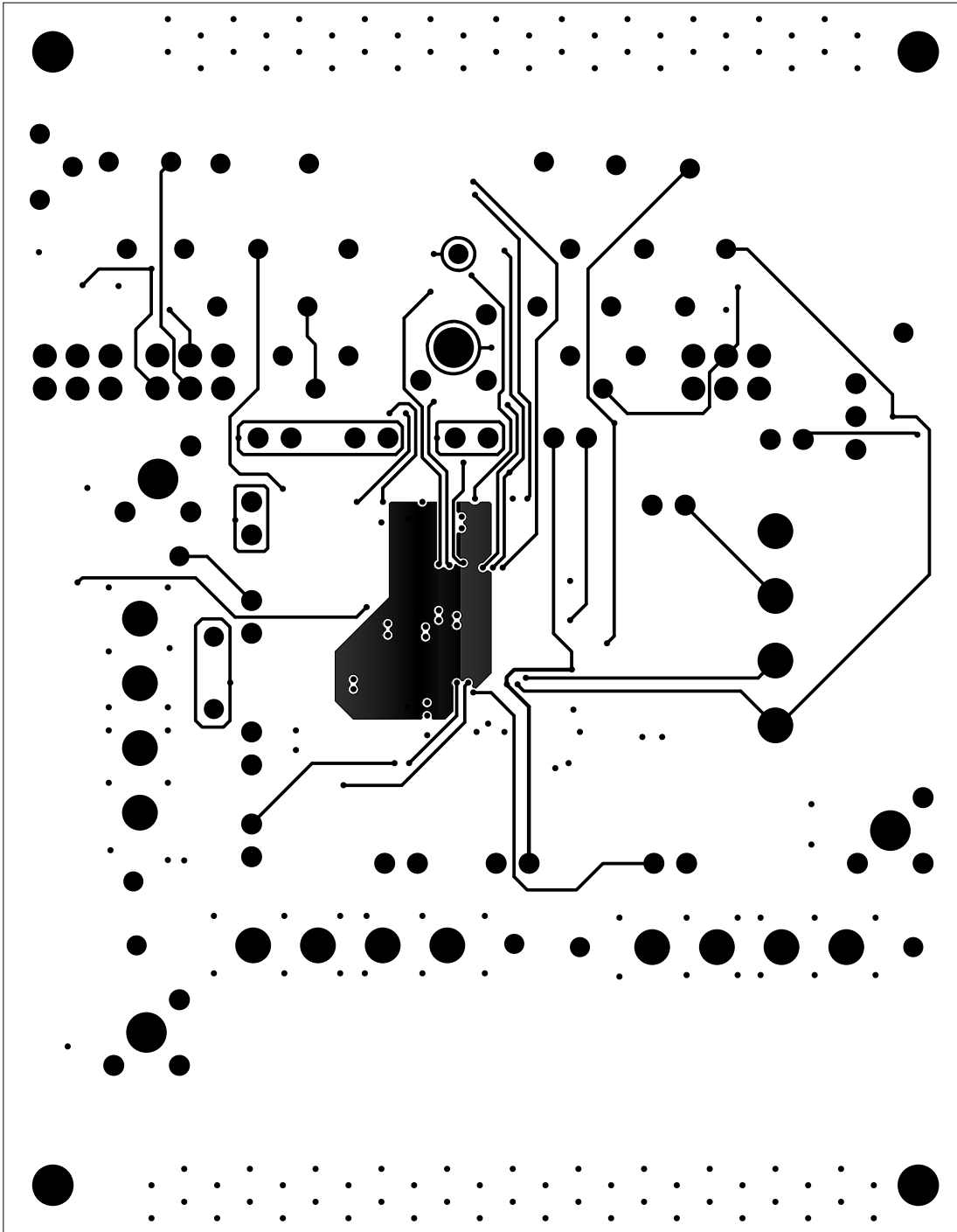


FIGURE 4. LAYER 3 SIGNAL

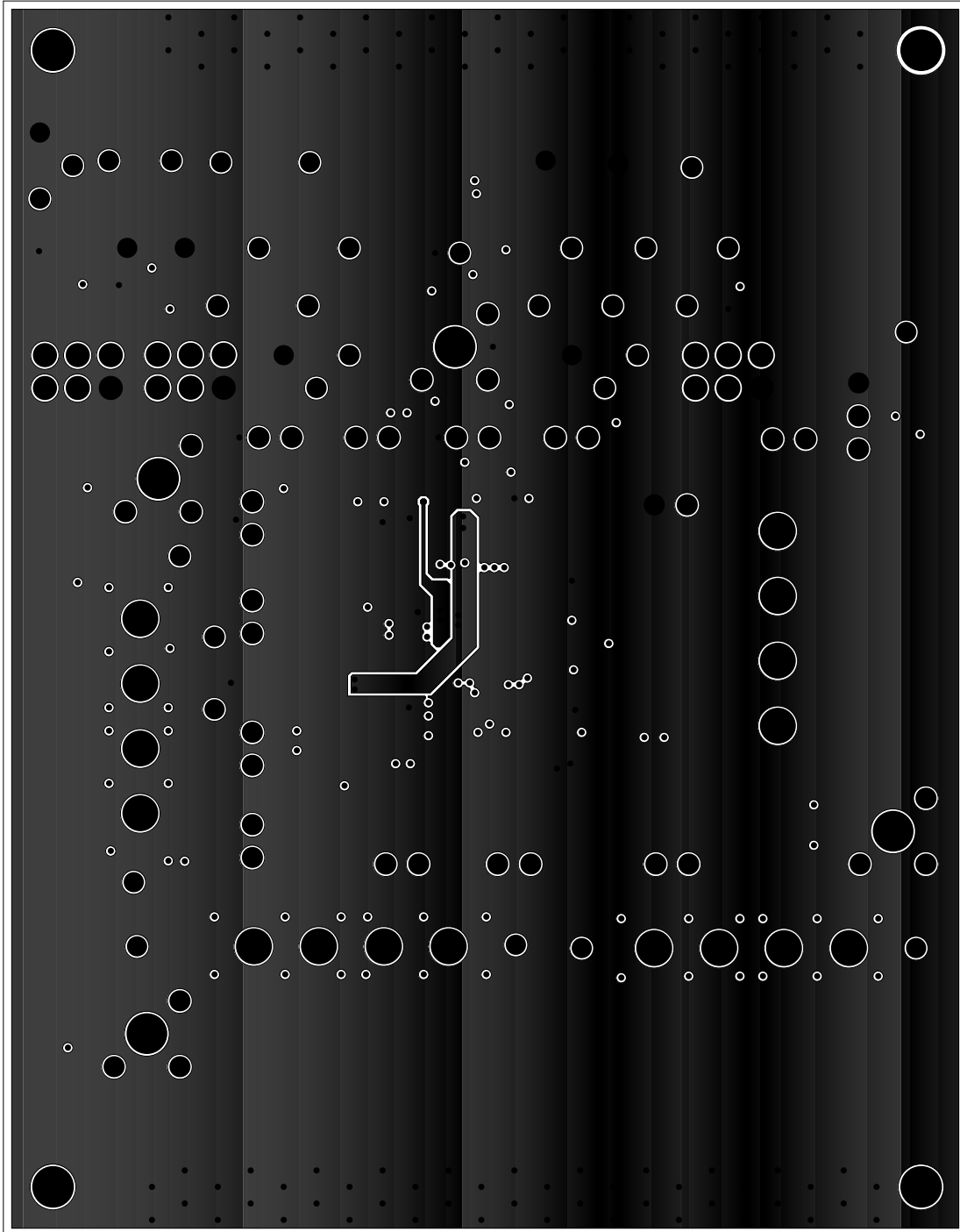


FIGURE 5. LAYER 4 GROUND

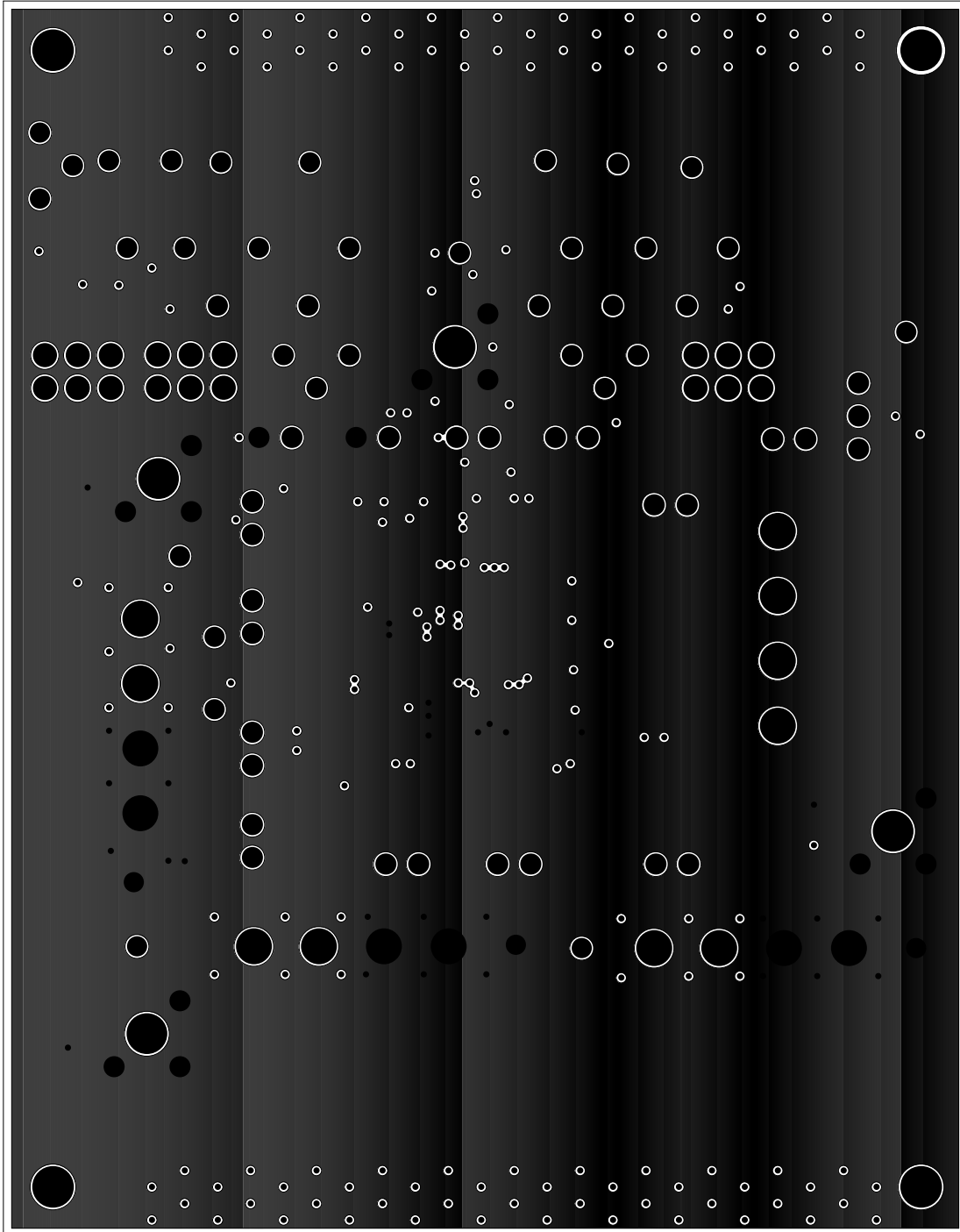


FIGURE 6. LAYER 5 GROUND

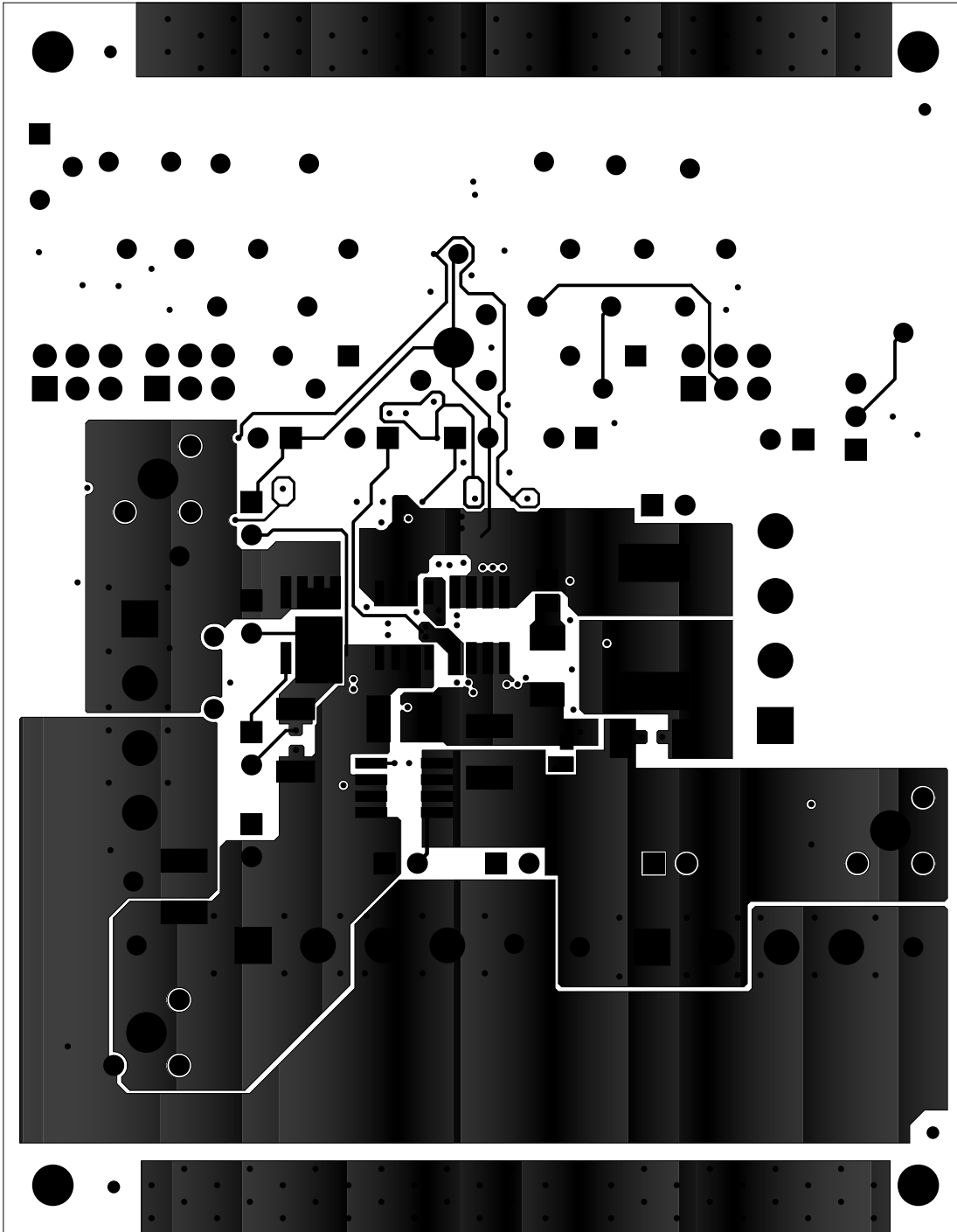


FIGURE 7. BOTTOM COPPER

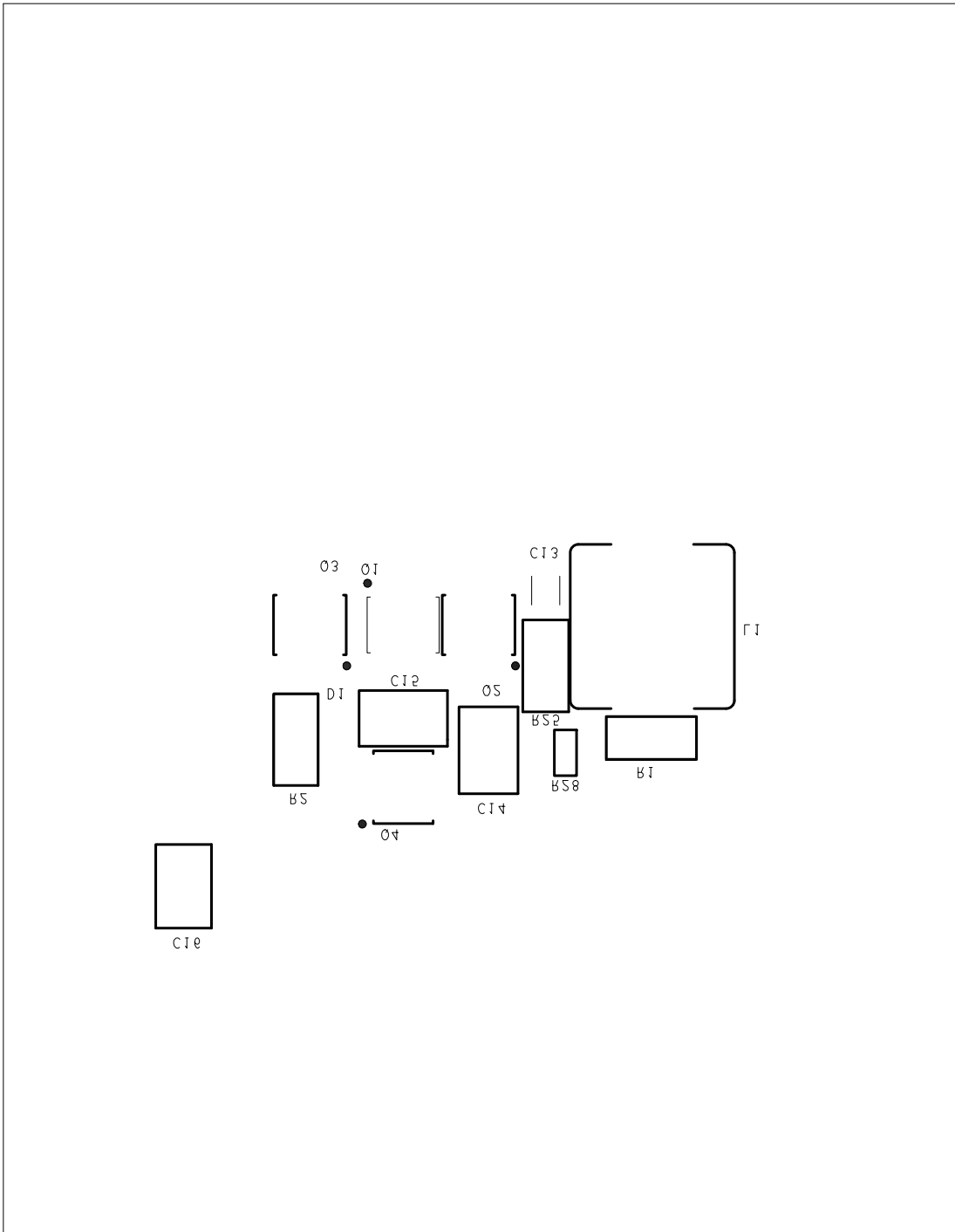


FIGURE 8. BOTTOM SILK

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(Rev.4.0-1 November 2017)



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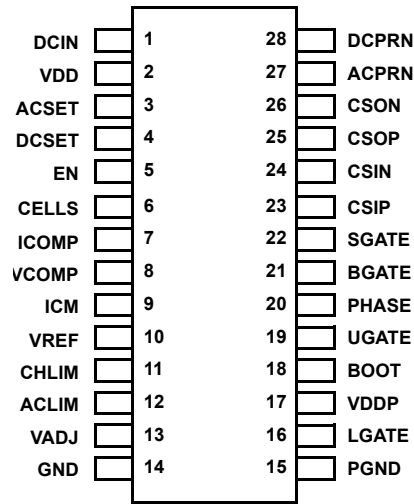
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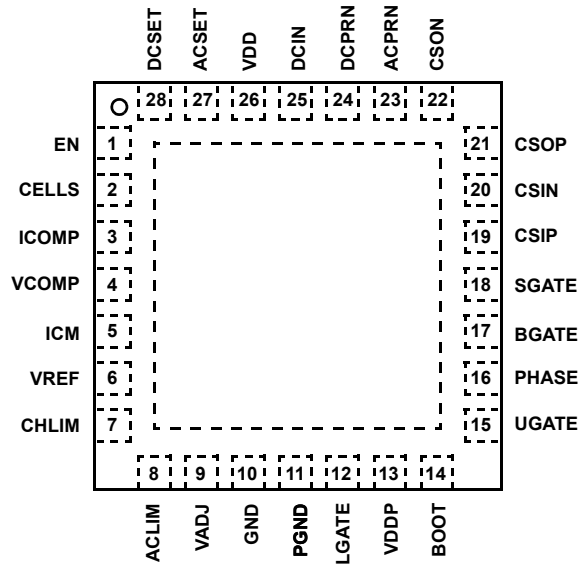
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 TOP VIEW



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Removed	Floating	2	8.4

Step 2: Select the Cell Trim Voltage (Table 2)

The VADJ pin trims the battery charger output voltage limit. Preset battery charger output voltage limits are selected by placing a shunt jumper across the appropriate pins of JP6. For other battery charger output voltage limits, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₄ to VADJ. Potentiometer R₂₄ may be removed and replaced with resistors R₁₉ and R₂₁. Resistor R₂₀ limits the trim increase to 1%. Shorting R₂₀ allows the trim to increase 5%. Decreasing trim range is unaffected.

TABLE 2. JUMPER JP6 FUNCTIONS

SHUNT LOCATION	VADJ PIN	BATTERY VOLTAGE CHANGE PER CELL
1 to 3	Through R ₂₀ to VREF	+5%
3 to 5	To GND	-5%
5 to 6	Floating	None
3 to 4	R ₂₄ Wiper or R ₁₉ /R ₂₁	Adjustable between -5% to +5%

Step 3: Select the Battery Charger Current Limit (Table 3)

The CHLIM pin chooses the desired battery charger current limit threshold. Preset battery charger current limit thresholds are selected by placing a shunt jumper across the appropriate pins of JP4. For other battery charger current limit thresholds, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₂ to CHLIM. Potentiometer R₂₂ may be removed and replaced with resistors R₆ and R₇.

TABLE 3. JUMPER JP4 FUNCTIONS

SHUNT JUMPER LOCATION	CHLIM PIN CONNECTED TO:	100% CURRENT FEEDBACK CSOP TO CSON	100% CONSTANT CURRENT
1 to 3	VREF	120mV	4.80A
Removed	Floating	0V	0A
3 to 5	GND	0V	0A
3 to 4	R ₂₂ or R ₆ /R ₇	0mV to 120mV	0A to 4.8A

Step 4: Select the AC Adapter Current Limit (Table 4)

The ACLIM pin chooses the desired AC adapter current limit threshold. Preset AC adapter current limit thresholds are selected by placing a shunt jumper across the appropriate pins of JP5. For other AC adapter current limit thresholds, install a shunt jumper across pins 3 and 4, which connects the wiper of potentiometer R₂₃ to ACLIM. Potentiometer R₂₃ may be removed and replaced with resistors R₁₇ and R₁₈.

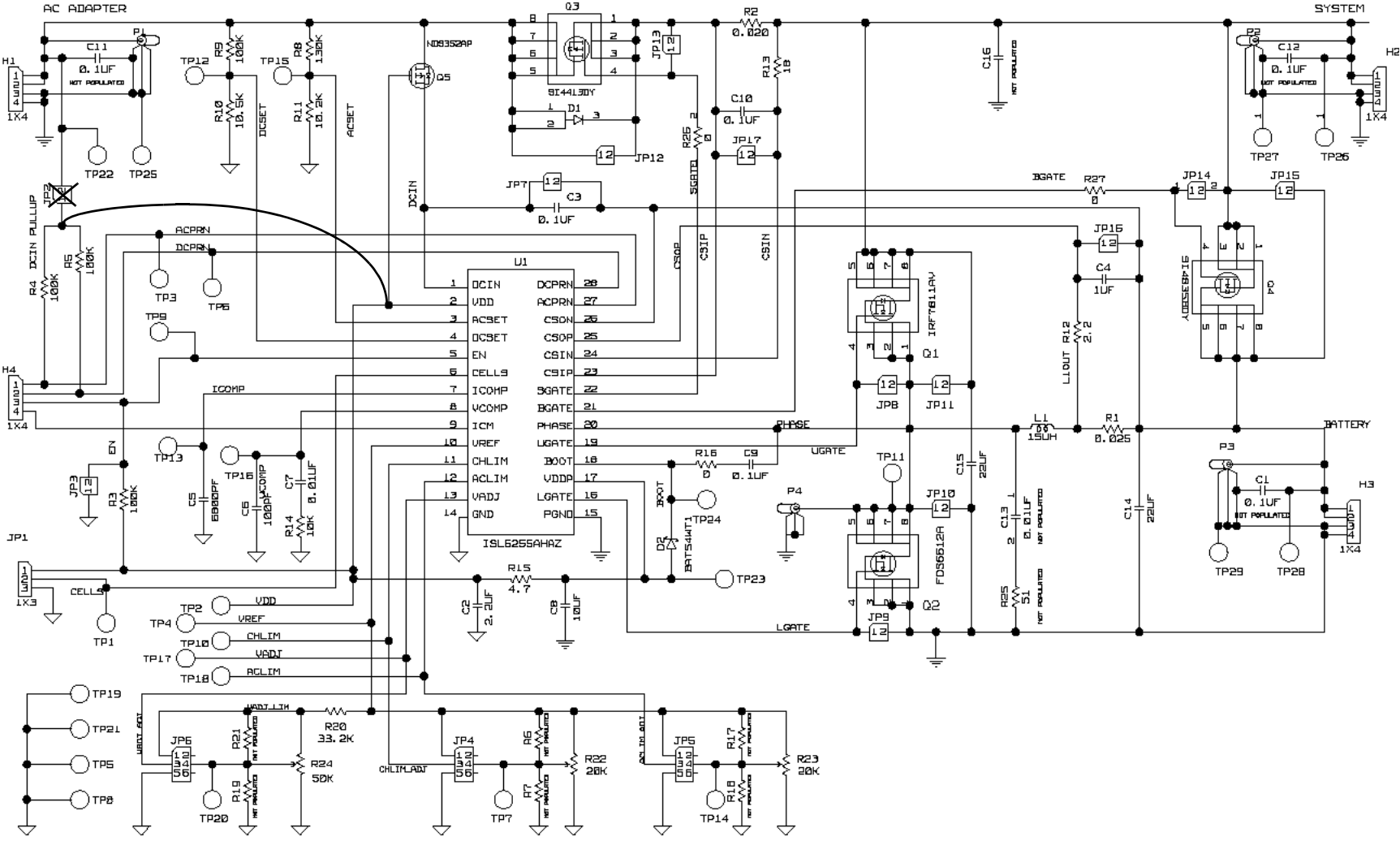
TABLE 4. JUMPER JP5 FUNCTIONS

SHUNT JUMPER LOCATION	ACLIM PIN CONNECTED TO:	100% CURRENT FEEDBACK CSIP TO CSIN	100% ADAPTER CURRENT
1 to 3	VREF	100mV	5.15A
Removed	Floating	75mV	3.90A
3 to 5	GND	50mV	2.65A
3 to 4	R ₂₃ or R ₁₇ /R ₁₈	50mV to 100mV	2.65A to 5.15A

Interface Connections

TABLE 5.

HEADER	PIN#	CONNECT TO
H1 INPUT POWER	1	"+" INPUT POWER
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" INPUT POWER
H2 SYSTEMLOAD OUTPUT	1	"+" SYSTEM LOAD OUTPUT
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" SYSTEM LOAD OUTPUT
H3 BATTERY CHARGER OUTPUT	1	"+" BATTERY CHARGER OUTPUT
	2	"+" SENSE (if used)
	3	"-" SENSE (if used)
	4	"-" BATTERY CHARGER OUTPUT



ISL6255EVAL2Z Schematic



TABLE 6. BILL OF MATERIALS

QTY	REF DES	DESCRIPTION	MFG NAME	PART NUMBER
1	C6	Capacitor, SMD, 0603, 100pF, 50V, 5%, COG	TDK	C1608COG1H101J
1	C7	Capacitor, SMD, 0805, 0.01 μ F, 50V, 5%, COG	TDK	C2012COG1H103J
1	C5	Capacitor, SMD, 0805, 6800pF, 50V, 5%, COG	TDK	C2012COG1H682J
3	C2, C4, C8	Capacitor, SMD, 0805, 1.0 μ F, 16V, 20%, X7R	TDK	C2012X7R1C105M
3	C3, C9, C10	Capacitor, SMD, 0805, 0.1 μ F, 50V, 10%, X7R	TDK	C2012X7R1H104K
2	C14, C15	Capacitor, SMD, 1812, 22 μ F, 25V, 20%, X5R	TDK	C4532X5R1E226M
1	L1	Choke, SMD, 8mm, 15 μ H, 20%, 5.65A, Shielded	Sumida	CDRH127/LD-150NC
1	U1	IC, Battery Charger, 24 Ld QSOP, -10°C to +100°C	Intersil	ISL6251HAZ
1	Q2	MOSFET, N-CH, 8P, SOIC, 30V, 8.4A, 0.022 Ω	Fairchild	FDS6612A
1	Q1	MOSFET, N-CH, 8P, SOIC, 30V, 10.8A, 0.011 Ω	IR	IRF7811AV
1	Q3	MOSFET, P-CH, SOIC, 30V, 13A, 0.014 Ω	Siliconix	SI4413DY
1	Q4	MOSFET, P-CH, SOIC, 30V, 6A, 0.033 Ω	Siliconix	SI4835BDY
1	Q5	MOSFET, P-CH, 3P, SOT23, -30V, -0.9A, 0.5 Ω	Fairchild	NDS352AP
1	D1	DIODE SCHOTTKY 40V 10A POWERDI5	Diodes Inc.	PDS1040-13
1	D2	SURFACE MOUNT SCHOTTKY BARRIER DIODE	Diodes Inc	BAT54WT1
1	R2	Resistor, Shunt, SMD, 2010, 0.020 Ω , 1W, 1%	IRC	LRC-LRF2010-01-R020-F
1	R1	Resistor, Shunt, SMD, 2010, 0.025 Ω , 1W, 1%	IRC	LRC-LRF2010-01-R025-F
1	R13	Resistor, SMD, 0805, 18 Ω , 0.125W, 5%	KOA	RK73B2AT180J
1	R12	Resistor, SMD, 0805, 2.2 Ω , 0.125W, 5%	KOA	RK73B2AT2R2J
1	R15	Resistor, SMD, 0805, 4.7 Ω , 0.125W, 5%	KOA	RK73B2AT4R7J
1	R14	Resistor, SMD, 0805, 10k Ω , 0.125W, 1%	KOA	RK73H2AT1002F
1	R11	Resistor, SMD, 0805, 7.87k Ω , 0.125W, 1%	KOA	RK73H2AT7871F
3	R3, R4, R8	Resistor, SMD, 0805, 100k Ω , 0.125W, 1%	KOA	RK73H2AT1003F
1	R20	Resistor, SMD, 0805, 33.2k Ω , 0.125W, 1%	KOA	RK73H2AT3322F
1	R16	Resistor, SMD, 0805, 0 Ω , 2A, 50m Ω Max	KOA	RK73Z2AT

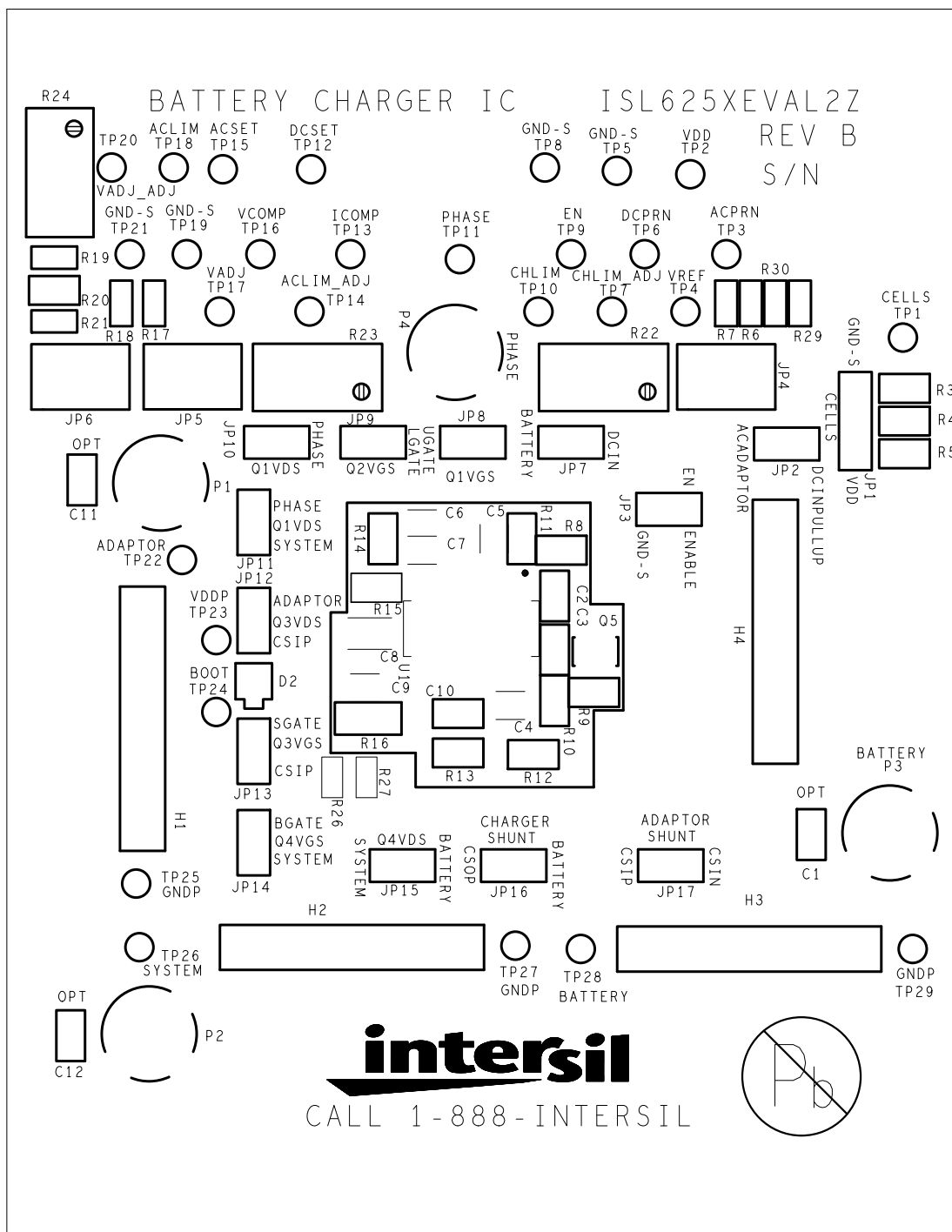


FIGURE 1. TOP SILK

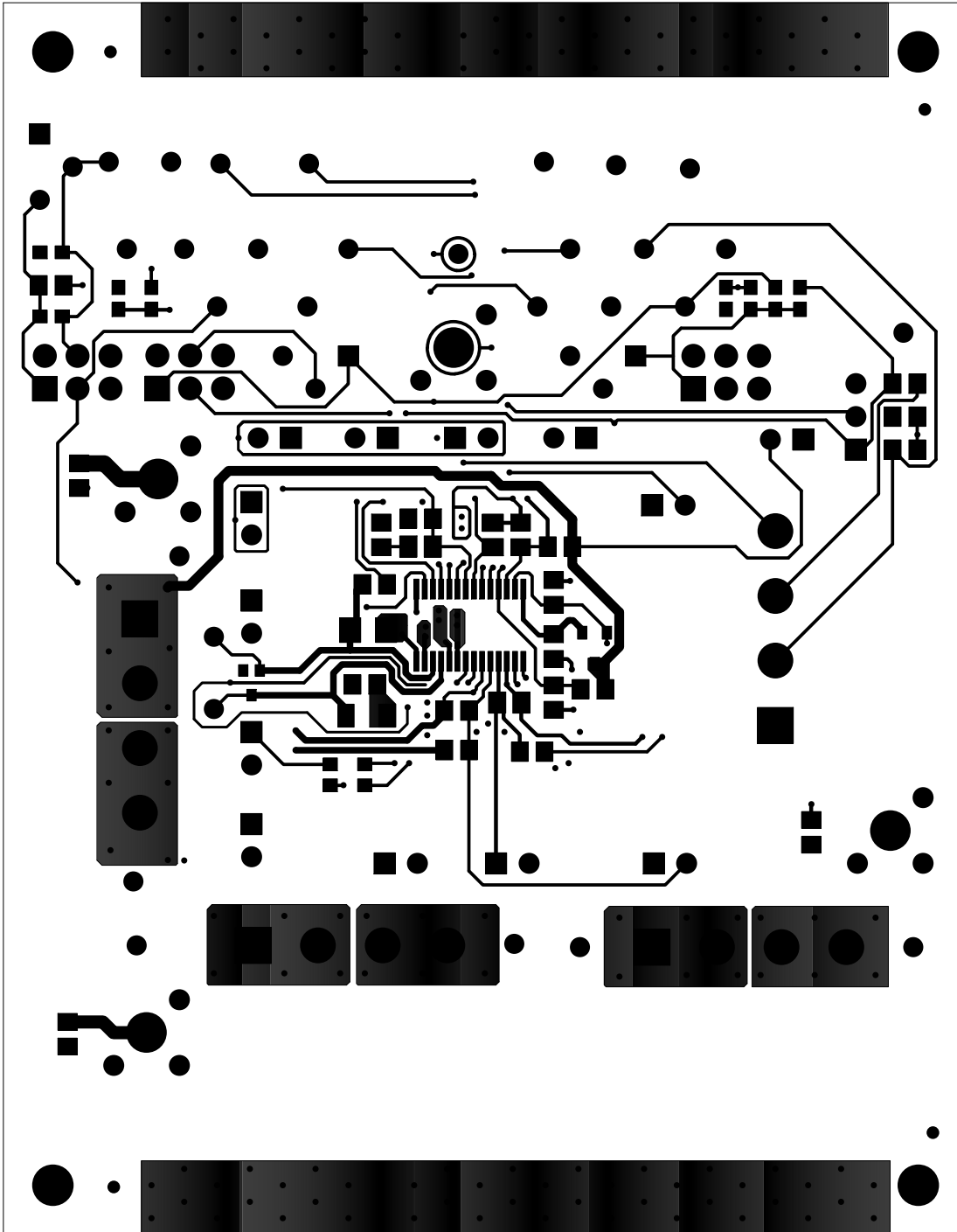


FIGURE 2. TOP LAYER

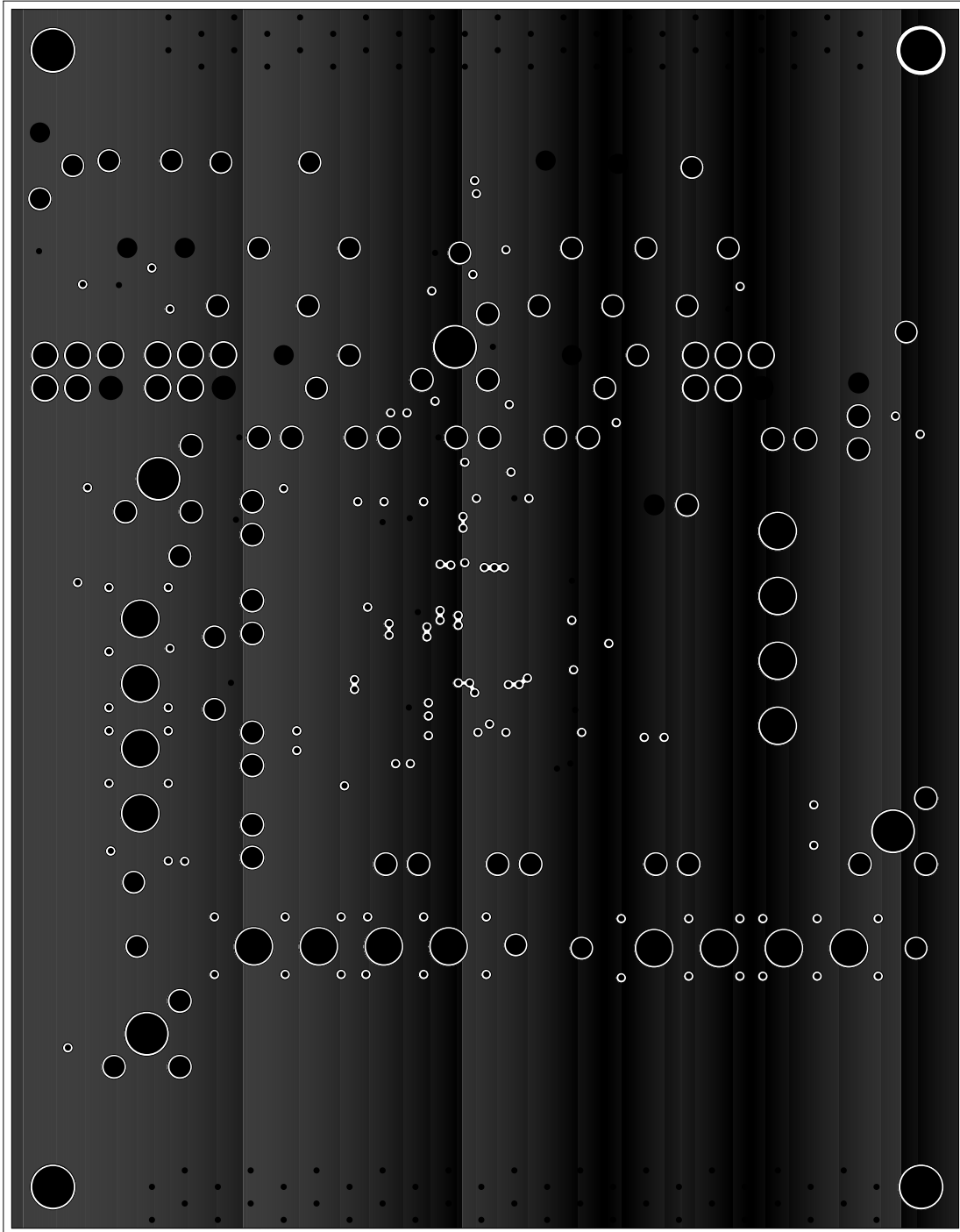


FIGURE 3. LAYER 2 GROUND

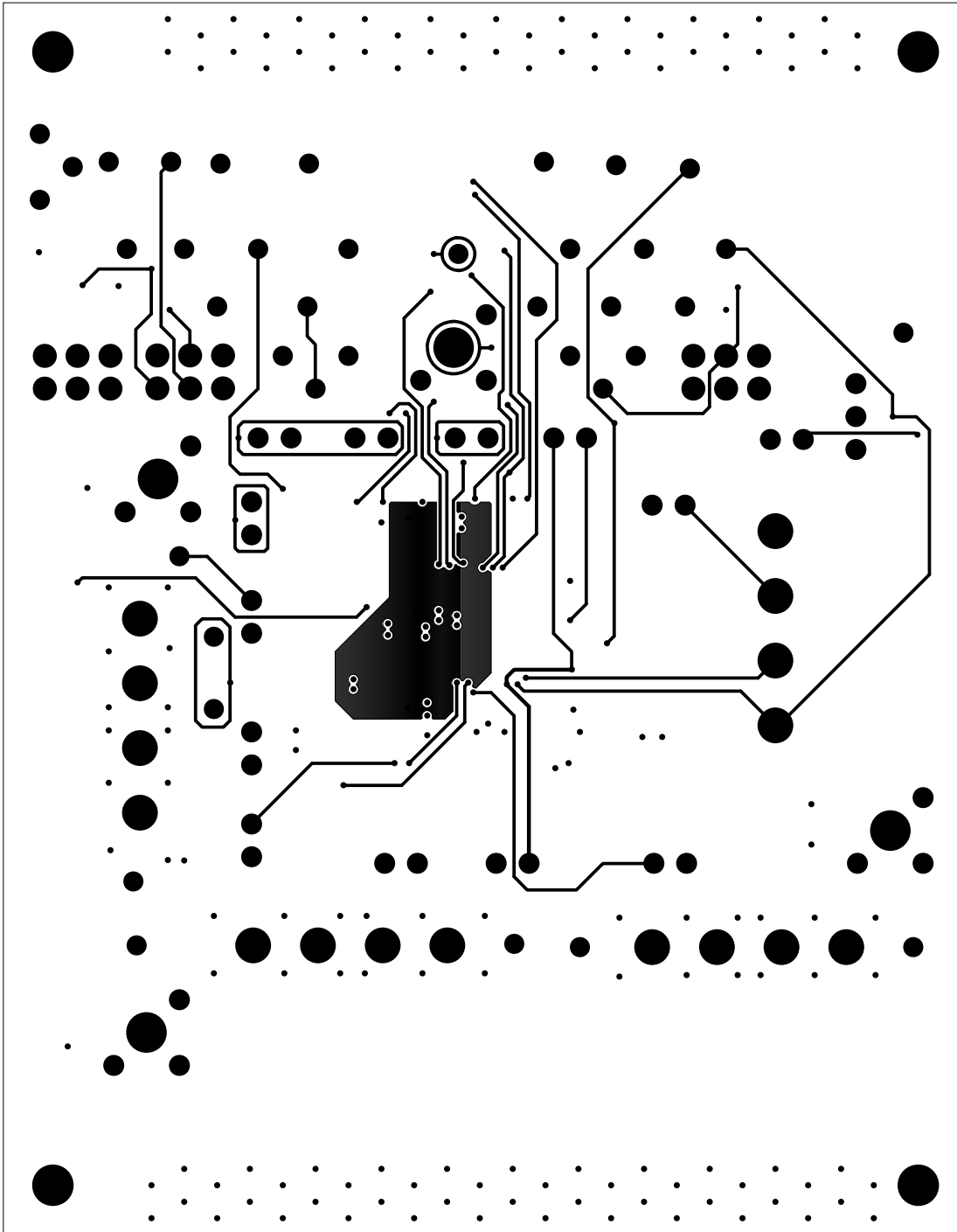


FIGURE 4. LAYER 3 SIGNAL

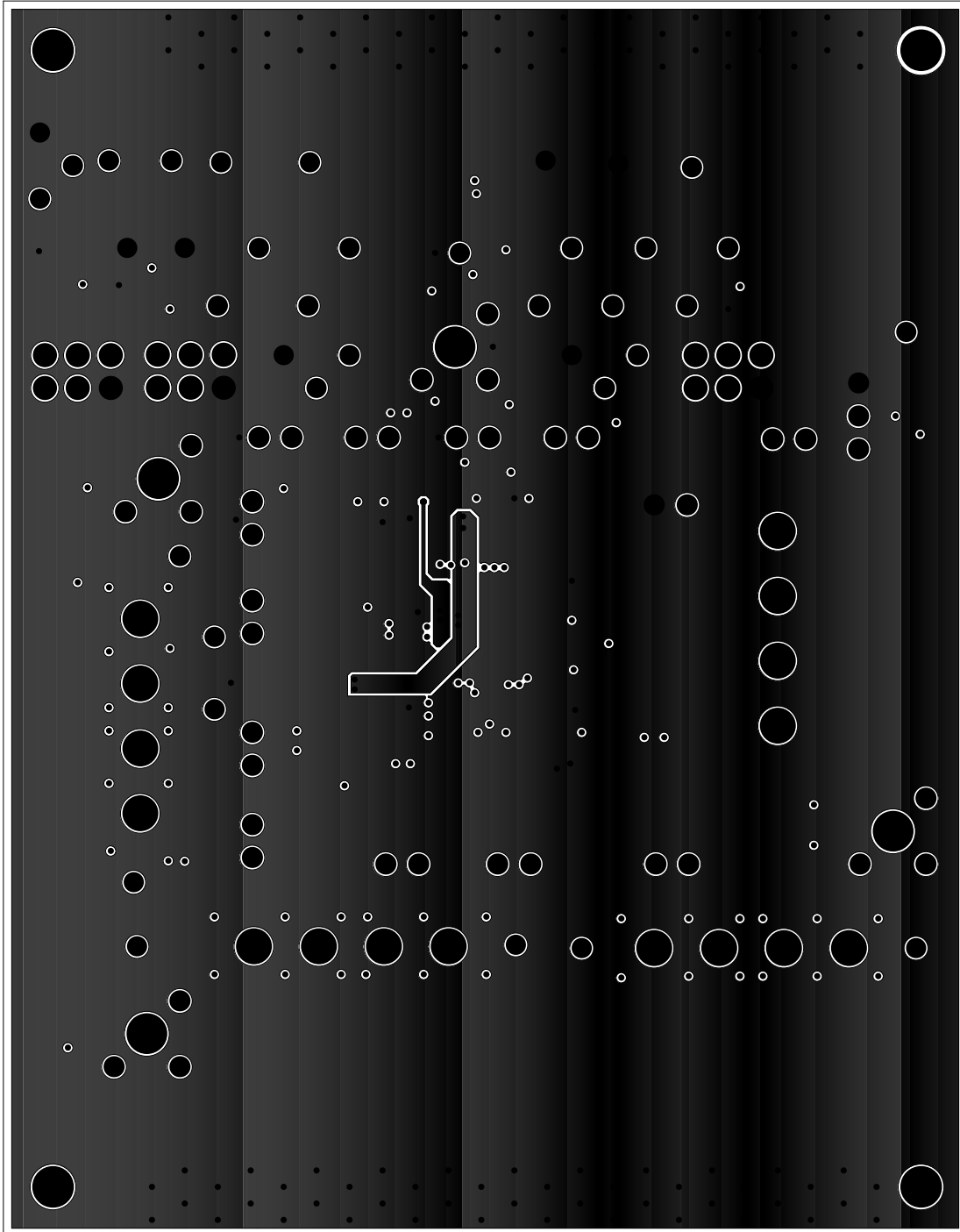


FIGURE 5. LAYER 4 GROUND

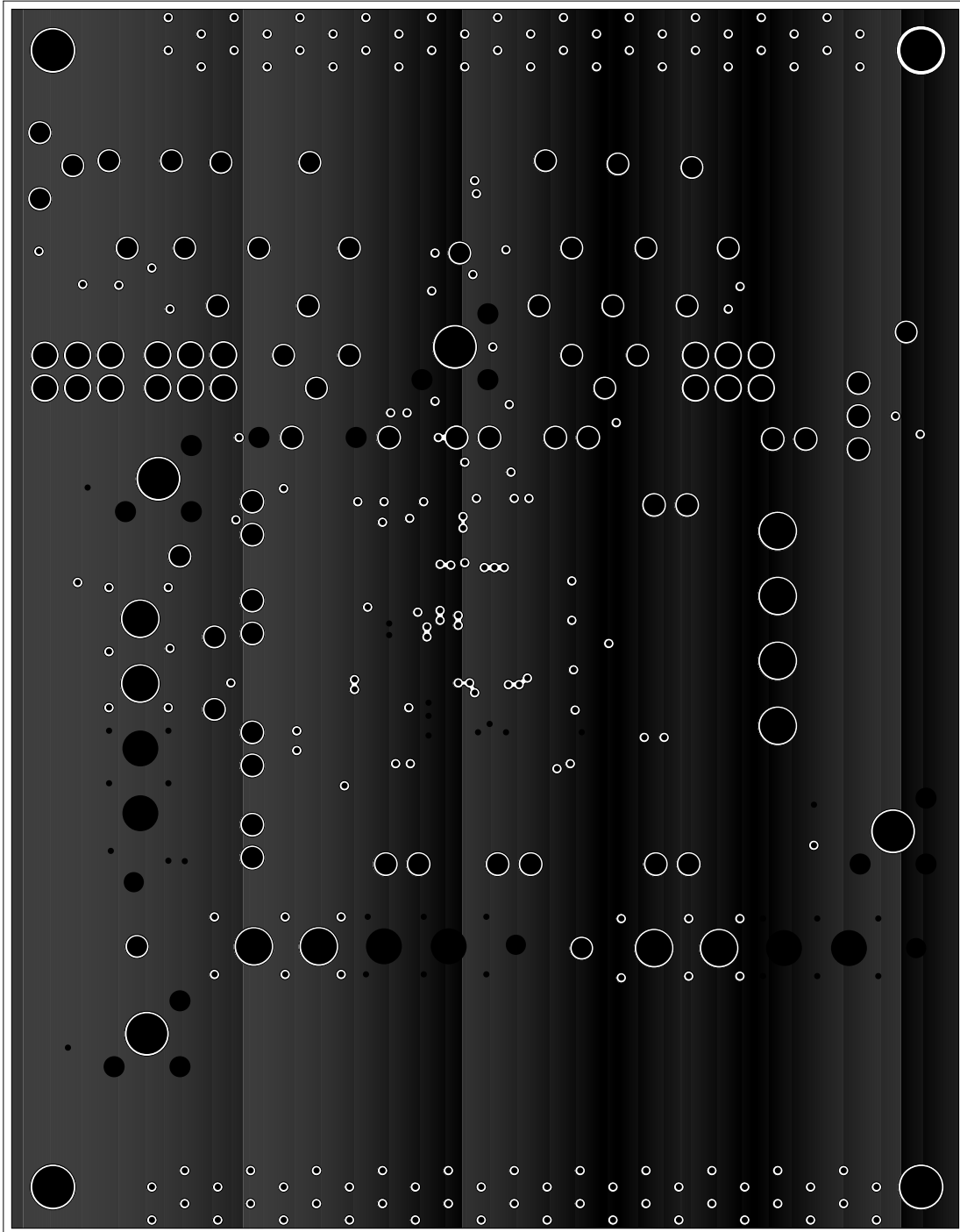


FIGURE 6. LAYER 5 GROUND

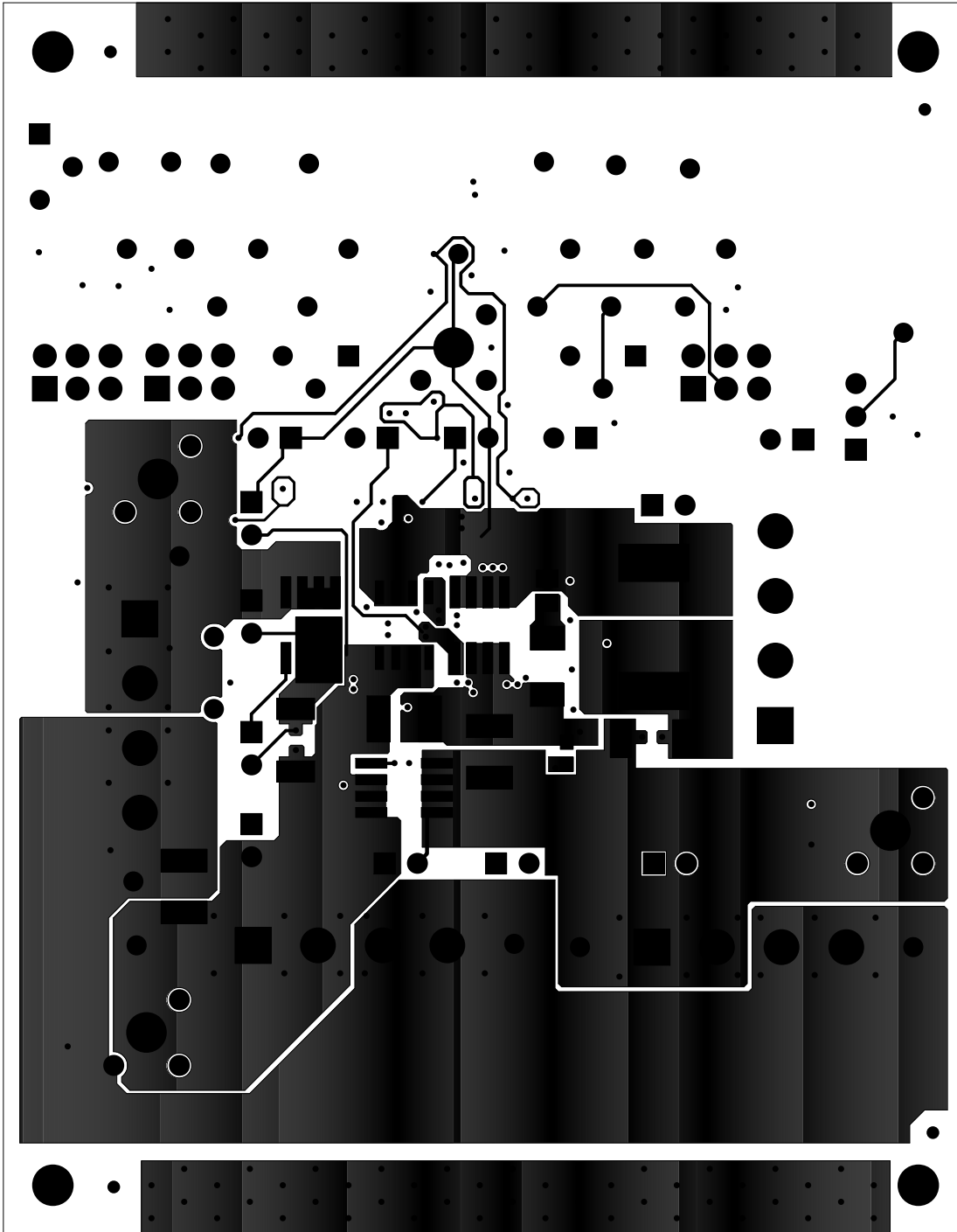


FIGURE 7. BOTTOM COPPER

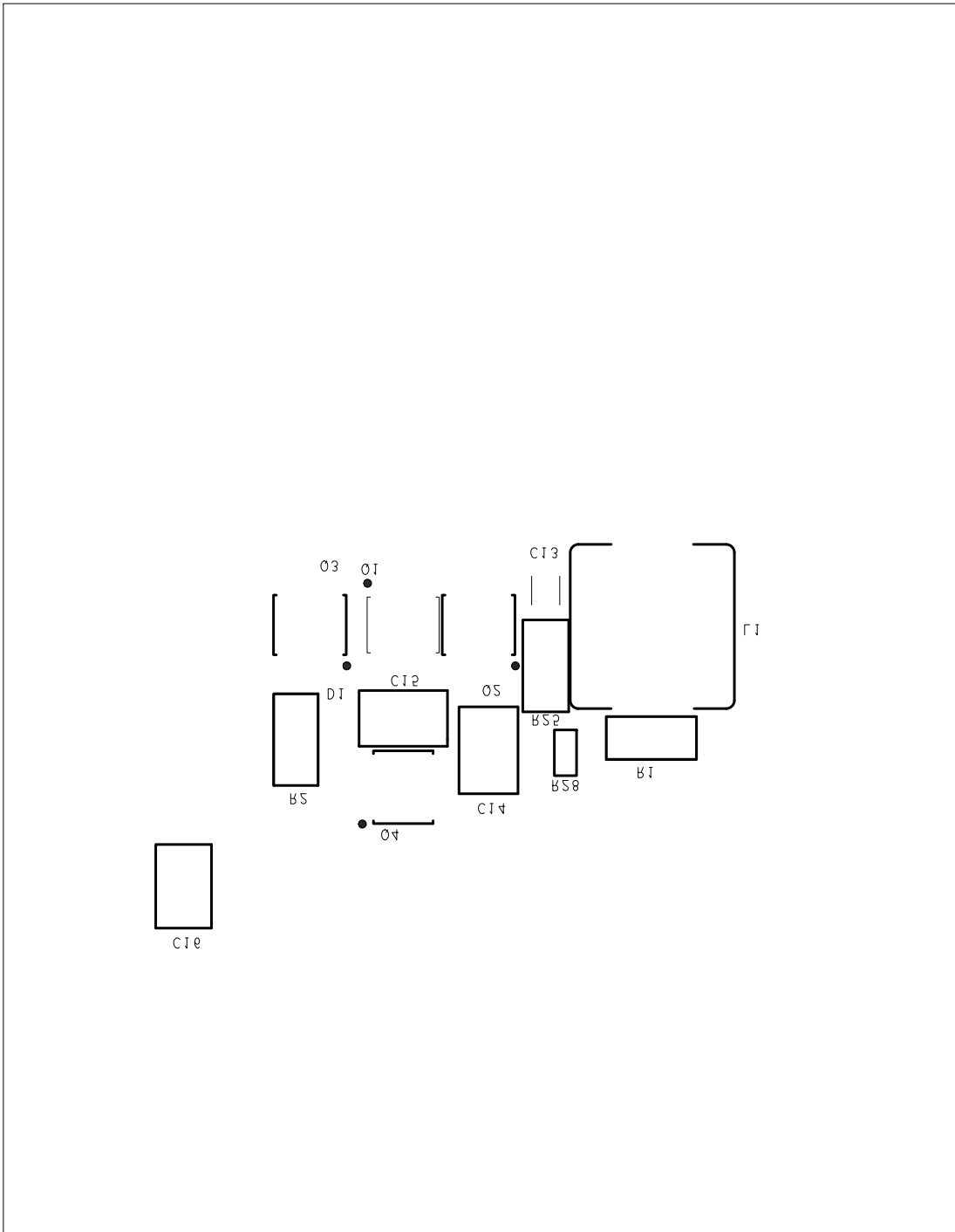


FIGURE 8. BOTTOM SILK