ISL6440

Using the ISL6440 Evaluation Board

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Description

The ISL6440 is a high performance triple-output controller offering control and protection features for two synchronous buck PWMs.

The ISL6440EVAL1Z evaluation board highlights the operation of the IC in an embedded DC/DC converter application. Table Ordering Information shows the available evaluation board.

Ordering Information

PART NUMBER	DESCRIPTION
ISL6440EVAL1Z	Evaluation board for the ISL6440IAZ

Related Literature

- For a full list of related documents please visit our website
  - ISL6440 product page

Specifications

This board has been configured and optimized for the following operating conditions:

- Input Voltage Range . . . . . 5.6V to 24V
- Output
  - V_{OUT1} 3.3V/2A
  - V_{OUT2} 1.8V/2A
- F_{OSC} = 300k fixed
- Overcurrent Threshold . . . . . >2A

Recommended Test Equipment

- A 12V, 5A capable power supply
- An electronic load
- Four channel oscilloscope with probes
- Precision digital multimeters

Power and Load Connections

Input Voltage - To connect a +12V power supply to the evaluation board, connect the positive lead of the power supply to VIN (P1) post and the ground lead of the supply to the GND (P2) post.

Output Adjustment

Change the respective output voltage feedback resistors to modify the output voltage:

$$V_{OUT1} = 0.8 \cdot \left(1 + \frac{R_5}{R_6}\right) \qquad V_{OUT2} = 0.8 \cdot \left(1 + \frac{R_7}{R_8}\right)$$

(EQ. 1)

Soft-Start and Shutdown

The soft-start capacitors can be adjusted for sequencing of the output voltages, PWM start-up tracking, and/or to adjust the start-up current required to charge the output capacitors.

$$t_{SS(PWM1)} = C_5 \cdot \frac{0.8V}{5\mu A} \qquad t_{SS(PWM2)} = C_3 \cdot \frac{0.8V}{5\mu A}$$

(EQ. 2)

To independently shutdown the PWMs, the SD1 or SD2 pin can be pulled to GND using the on board posts, P7 and P8 respectively.

Power Good

When both PWMs are within ±10% of their set value, the PGOOD signal will go high. The open-drain PGOOD pin is pulled HIGH to VCC_5V on the board. The PGOOD circuitry monitors the FBx pin of each regulated output to determine if the outputs are in regulation. PGOOD can be monitored at post P9.

Overcurrent Protection

The overcurrent thresholds can be adjusted on the ISL6440 evaluation board. The current sense resistors, I_{SENSE}, are set at 1.0k. The overcurrent set resistor is 95.3k. The overcurrent trip point can be adjusted by modifying R_{OCSET}, R_3 and R_4:

$$R_{OCSET} = \frac{7 \cdot R_{CS}}{I_{OC} \cdot r_{DS(ON)}}$$

(EQ. 3)

R_{OCSET} is the overcurrent set resistor, R_{CS} is the current sense resistor, I_{OC} is the desired overcurrent trip point, and $r_{DS(ON)}$ is the on-resistance of the respective PWM's lower MOSFET. Refer to the ISL6440 datasheet for more information on how to select the current sense and overcurrent select resistors.

ISL6440EVAL1Z Schematic

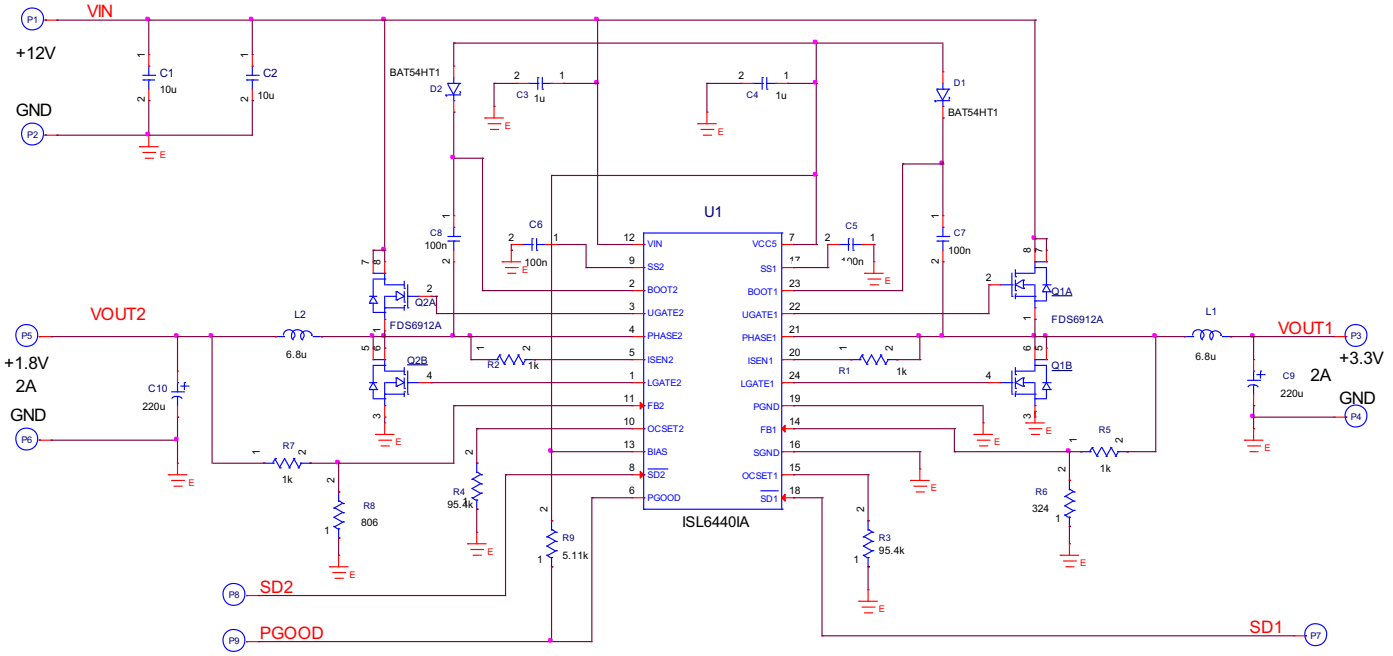

FIGURE 1. SCHEMATIC

ISL6440EVAL1Z Bill of Materials

ITEM	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	VENDOR
1	P1-P9	9	1514-2	Test Point	Turret 0.281 Height	Keystone
2	D1, D2	2	BAT54HT1G	Diode, Schottky	30V, 200mA	On Semi
3	C4	1	ECJ1VB0J105K	Cap, Ceramic, X5R	1µF, 10V, 0603, X5R	Panasonic
4	C9, C10	2	10TPB220M	Cap, POSCAP	220µF, 10V	Sanyo
5	C1, C2	2	C3225X7R1E106	Cap, Ceramic, 1210	10µF, 10%, 25V, 1210, X7R	TDK
6	L1, L2	2	DO3316P-682ML	SMT Power Inductor	6.8µH, ±20%, 4.6A, 27mΩ	Coilcraft
7	C3	1	GRM188R61C105KA12D	Capacitor, Ceramic	1µF, 20%, 16V, Y5V, 0603	MURATA
8	Q1, Q2	2	FDS6912A	Dual NFET	6A, 30V, Dual NFET, SO8	Fairchild
9	C5, C6, C7, C8	4	GRM188R71E104KA01D	Cap, Ceramic, 0603	0.1µF, 10%, 6.3V	MURATA/Generic
10	R1, R2, R5, R7	5		Resistor, Film	1kΩ, 0603, 1%, 1/16W	Any
11	R6	1		Resistor, Film	324Ω, 0603, 1%, 1/16W	Any
12	R3, R4	1		Resistor, Film	95.3kΩ, 0603, 1%, 1/16W	Any
13	R9	1		Resistor, Film	5.11kΩ, 0603, 1%, 1/16W	Any
14	R8	1		Resistor, Film	806Ω, 0603, 1%, 1/16W	Any
15	U1	1	ISL6440IAZ	300kHz, Dual PWM Controller		Intersil

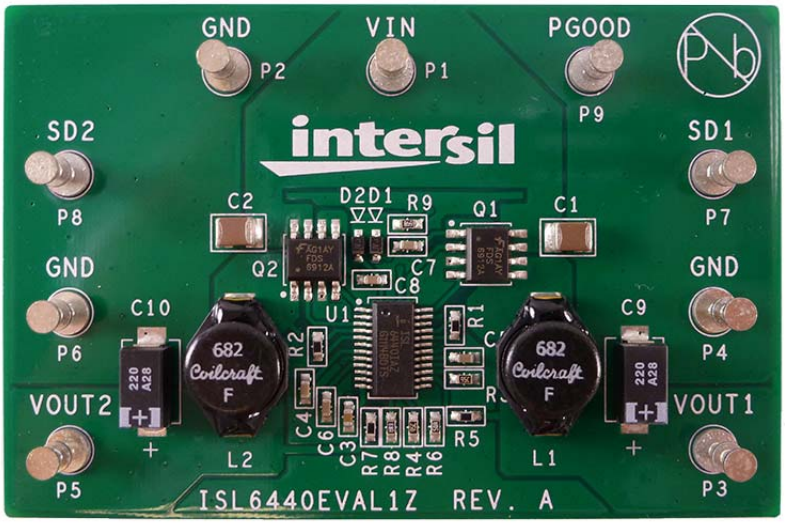

FIGURE 2. TOP OF BOARD

ISL6440EVAL1Z Layout

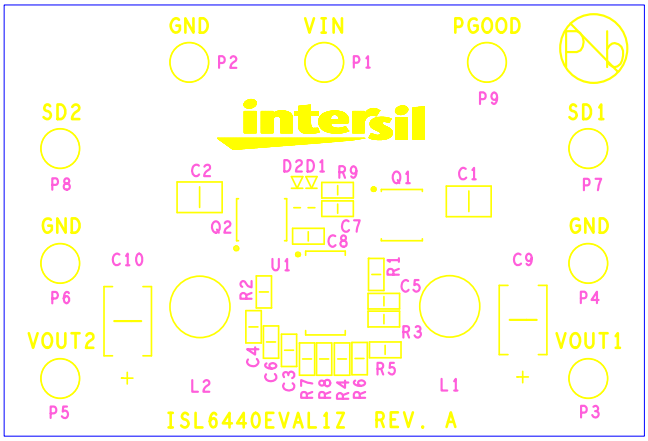

FIGURE 3. TOP SILK

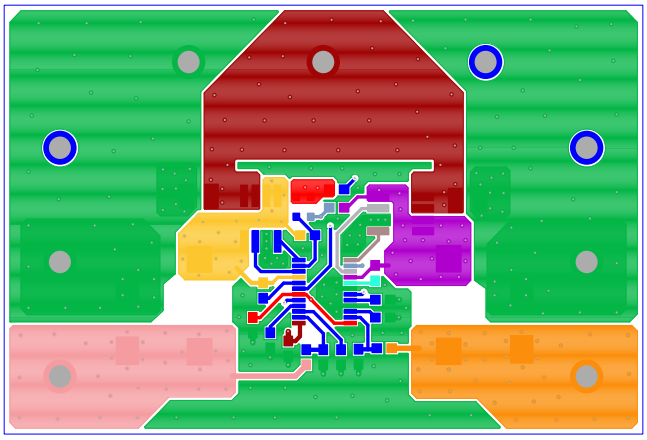

FIGURE 4. LAYER 1

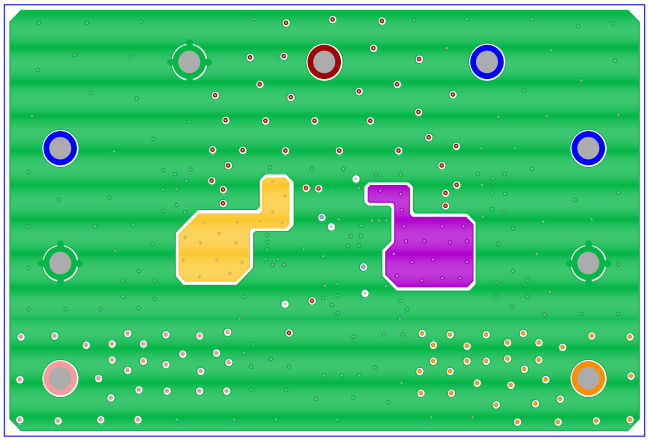

FIGURE 5. LAYER 2

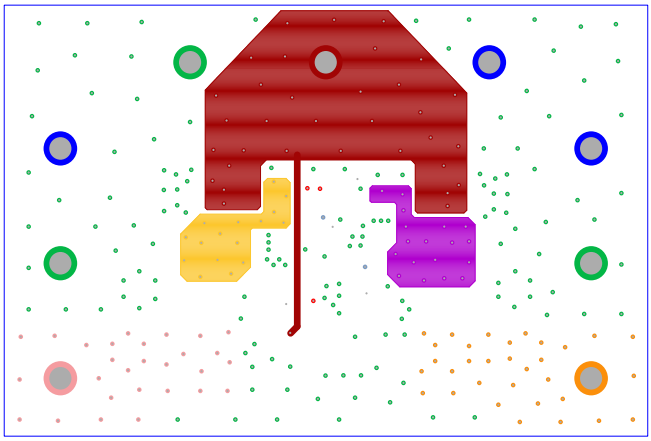

FIGURE 6. LAYER 3

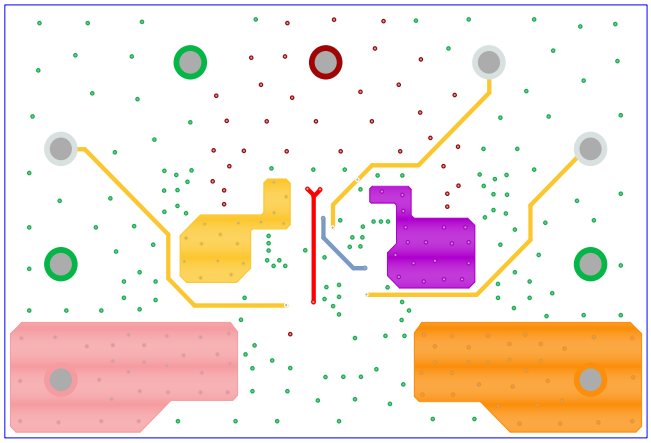

FIGURE 7. LAYER 4

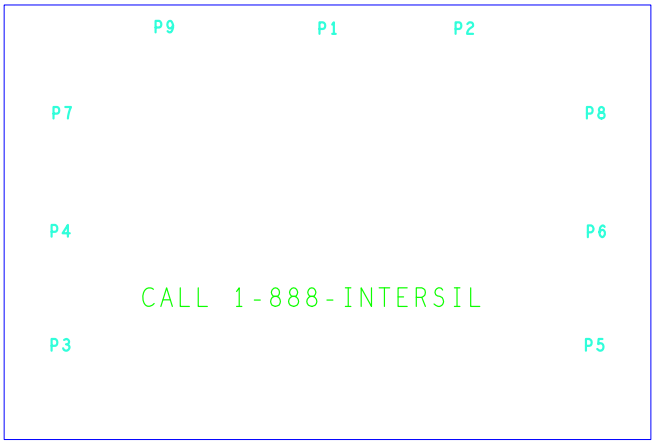

FIGURE 8. BOTTOM SILK