ISL6617

PWM Doubler with Phase Shedding Function and Output Monitoring Feature

FN7564
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The ISL6617 utilizes Intersil's proprietary Phase Doubler scheme to modulate two-phase power trains with single PWM input. It doubles the number of phases that Intersil's multi-phase controllers ISL63xx can support. When the enable pin (EN_PH_SYNC) is pulled low, the PWM input is pulled high. This simplifies the phase shedding implementation for some Intersil controllers (VR10, VR11, VR11.1, and VR12 family) that can disable the respective and higher phase(s) by pulling the respective PWM line high.

The ISL6617 is designed to minimize the number of analog signals that interface between the controller and drivers in high phase count scalable applications. The common COMP signal, which is usually seen in conventional cascaded configuration, is not required; this improves noise immunity and simplifies the layout. Furthermore, the ISL6617 provides low part count and low cost advantage over the conventional cascaded technique.

By cascading the ISL6617 with another ISL6617 or ISL6611A, it can quadruple the number of phases that Intersil's multi-phase controllers ISL63xx can support.

The ISL6617 also features Tri-State input and outputs that recognize a high-impedance state, working together with Intersil multiphase PWM controllers and driver stages to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the schottky diode that may be utilized in a power system to protect the load from excessive negative output voltage damage.

Applications

- High Current Low Voltage DC/DC Converters
- High Frequency and High Efficiency VRM and VRD
- High Phase Count and Phase Shedding Applications
- 5V PWM Input Integrated Power Stage or DrMOS

Features

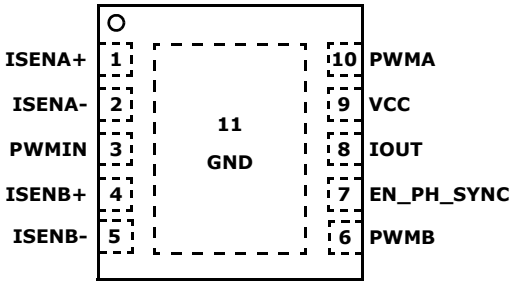
- Proprietary Phase Doubler scheme with Phase Shedding Function ***(Patent Pending)***
- Enhanced Light to Full Load Efficiency
- Double or Quadruple Phase Count
- Patented Current Balancing with DCR Current Sensing and Adjustable Gain
- Current Monitoring Output (IOUT) to Simplify System Interface and Layout
- Triple-Level Enable Input for Mode Selection
- Dual PWM Output Drives for Two Synchronous Rectified Bridges with Single PWM Input
- Channel Synchronization and Two Interleaving Options
- Tri-State PWM Input and Outputs for Output Stage Shutdown
- Phase Enable Input and PWM Forced High Output to Interface with Intersil's Controller for Phase Shedding
- Overvoltage Protection
- Dual Flat No-Lead (DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Utilization, Thinner Profile
  - Pb-Free (RoHS Compliant)

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Pin Configuration

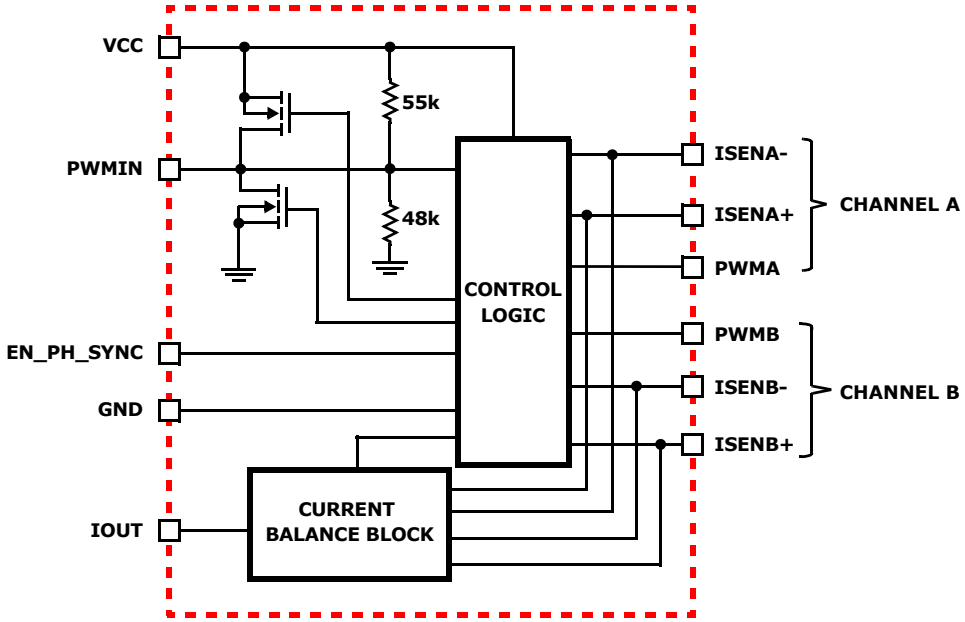
ISL6617
(10 LD DFN)
TOP VIEW



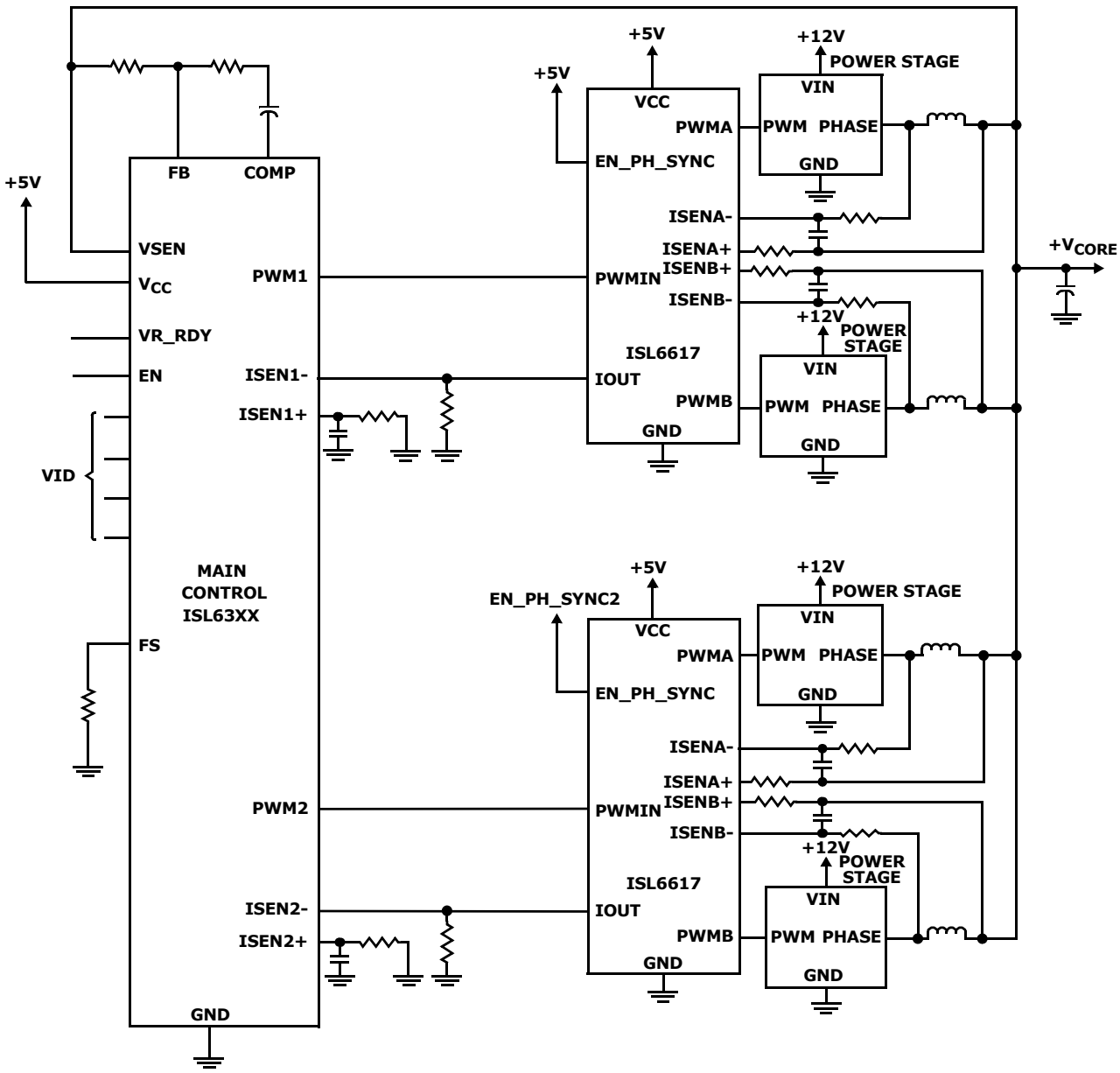
Functional Pin Descriptions

PIN #	PIN SYMBOL	FUNCTION
1	ISENA+	Output of the differential amplifier for Channel A. Connect a resistor on this pin to the negative rail of the sensed voltage to set the current gain.
2	ISENA-	Input of the differential amplifier for Channel A. Typically, the positive rail of sensed voltage via DCR sensing network connects to this node.
3	PWMIN	The PWM input signal triggers the J-K flip flop and alternates its input to channel A and B. Both channels are effectively modulated. The PWM signal can enter three distinct states during operation, see Operation section for further details. Connect this pin to the PWM output of the controller. The pin is pulled to VCC when EN_PH_SYNC is low.
4	ISENB+	Output of the differential amplifier for Channel B. Connect a resistor on this pin to the negative rail of the sensed voltage to set the current gain.
5	ISENB-	Input of the differential amplifier for Channel B. Typically, the positive rail of sensed voltage via DCR sensing network connects to this node.
6	PWMB	PWM output of Channel B with Tri-state feature.
7	EN_PH_SYNC	Driver Enable and Mode Selection Input. See Enable and Mode Operation for more details.
8	IOUT	Current monitoring Output. It sources out the average current of both Channel A and B.
9	VCC	Connect this pin to a +5V bias supply. It supplies power to internal analog circuits. Place a high quality low ESR ceramic capacitor from this pin to GND.
10	PWMA	PWM output of Channel A with Tri-state feature.
11	GND	Bias and reference ground. All signals are referenced to this node. Place a high quality low ESR ceramic capacitor from this pin to VCC. Connect this pad to the power ground plane (GND) via thermally enhanced connection.

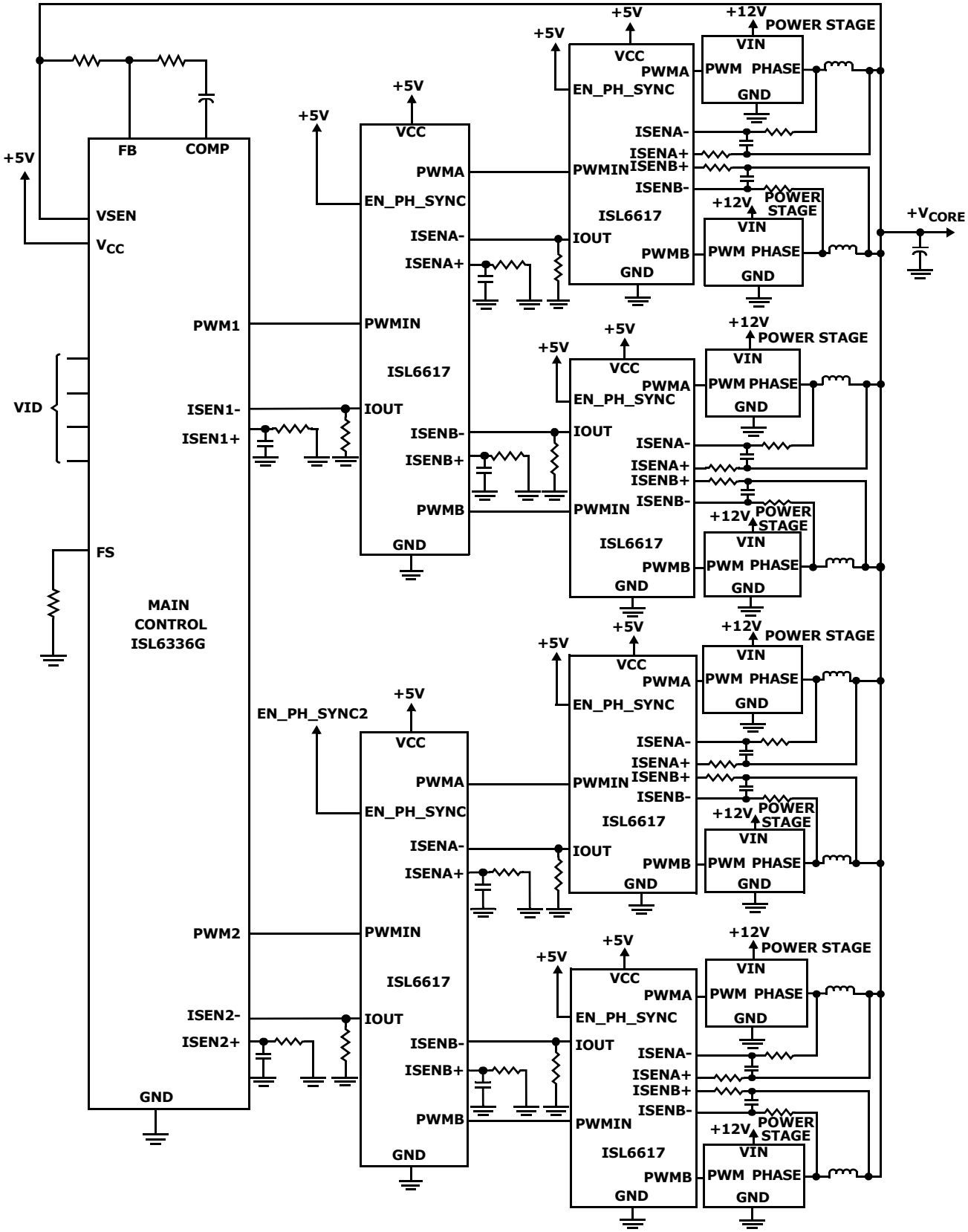
Block Diagram



Typical Application (2 Phase Controller for 4 Phase Operation)



Typical Application II (2-Phase Controller to 8-Phase Operation)



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6617CRZ	617C	0 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6617IRZ	617I	-40 to +85	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6617. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 6.7V
Input Voltage (V_{ENx}, V_{PWMIN}, I_{SENx}) . . -0.3V to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C
ESD Rating
Human Body Model (JEDEC Class 2) 2kV
Machine Model (JEDEC Class B). 200V
Charged Device Model (JEDEC Class IV). 2kV
Latch Up (JEDEC Class II) . . . . . +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
10 Ld DFN (Notes 4, 5)	48	7

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature
ISL6617CRZ . . . . . 0°C to +70°C
ISL6617IRZ. . . . . -40°C to +85°C
Maximum Operating Junction Temperature. . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
5. θ_{JC}, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

Electrical Specifications

These specifications apply for recommended ambient temperature, unless otherwise noted. **Boldface limits apply over the operating temperature range.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
SUPPLY CURRENT						
Bias Supply Current	I_{VCC}	PWM pin floating, V_{VCC} = 5V, EN_PH = 5V		5	6.5	mA
		PWM pin floating, V_{VCC} = 5V, EN_PH = 0V		5	6.5	mA
		F_{PWM} = 600kHz, V_{VCC} = 5V, EN_PH_SYNC = 5V		6	7.5	mA
		F_{PWM} = 600kHz, V_{VCC} = 5V, EN_PH_SYNC = 4.25V		6	7.5	mA
		F_{PWM} = 300kHz, V_{VCC} = 5V, EN_PH_SYNC = 3.25V		6	7.5	mA
POWER-ON RESET						
POR Rising				3.4	4.2	V
POR Falling			2.3	3.0		V
Hysteresis				350		mV
EN_PH_SYNC INPUT						
ENx Minimum LOW Threshold	V_{ENx}				0.8	V
ENx Maximum HIGH Threshold	V_{ENx}		2.0			V
SYNC AND INTERLEAVING MODE						
Interleaving Mode 1 Window	V_{ENx}		97%			VCC
Interleaving Mode 2 Window	V_{ENx}		78%		85%	VCC
Synchronous Mode Window	V_{ENx}		54%		64%	VCC
Typical Threshold Hysteresis				-5%		VCC
Minimum SYNC Pulse					40	ns
Maximum Synchronization Delay			50			ns
Interleaving Mode Phase Shift		SYNC = 5V, PWM = 300kHz, 10% Width		180		°

Electrical Specifications These specifications apply for recommended ambient temperature, unless otherwise noted. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Synchronization Mode Phase Shift		SYNC = 0V, PWM = 300kHz, 10% Width		0		°
PWM INPUT (PWMIN)						
Sinking Impedance	R_{PWM_SNK}			55		kΩ
Source Impedance	R_{PWM_SRC}			48		kΩ
Minimum Pull-Up Current	I_{PWM_SRC}	EN_PH_SYNC = LOW	40			mA
Tri-State Rising Threshold		V_{VCC} = 5V (250mV Hysteresis)	0.95	1.20	1.45	V
Tri-State Falling Threshold		V_{VCC} = 5V (300mV Hysteresis)	3.00	3.40	3.7	V
PWM Pulled High Threshold		EN_PH = LOW, Ramping PWM low		3.4		V
CURRENT SENSE (ISENA±, ISENB±, IOUT) AND PROTECTION (IOUT)						
Sensed Current Tolerance	I_{OUT}	ISENA = ISENB = 0µA	-6	0	6	µA
		ISENA = ISENB = 20µA	14	20	26	µA
		ISENA = ISENB = 50µA	43	50	57	µA
		ISENA = ISENB = 100µA	90	100	110	µA
Un-Tri State Trip For OVP	I_{OUT}	ENx = LOW TO HIGH, PWM = LOW	40	60	90	µA
PWM OUTPUT (PWMA AND PWMB)						
Sourcing Impedance	R_{PWM_SRC}	VCC = 5V	45	100	200	Ω
Sink Impedance	R_{PWM_SNK}	VCC = 5V	45	100	125	Ω
Tri-State Level	$V_{PWMA/B}$	VCC = 5V, EN_PH = LOW	1.65	2.00	2.6	V
SWITCHING TIME (See Figure 1 on Page 8)						
PWMA/B Low to High Rise Time	t_{R1}	Unloaded, 10% to 90%		4.5		ns
PWMA/B Tri-State to High Rise Time	t_{R2}	Unloaded, 10% to 90%		4.5		ns
PWMA/B High to Low Fall Time	t_{F1}	Unloaded, 90% to 10%		4.0		ns
PWMA/B High to Tri-State Fall Time	t_{F2}	100% to 60% (3V), Assume Equavilent Loading of RC = 50kΩ*10pF = 500ns		255		ns
PWMA/B Turn-On Propagation Delay	t_{PDH}	Outputs Unloaded		35		ns
PWMA/B Turn-Off Propagation Delay	t_{PDL}	Outputs Unloaded, excluding extension		35		ns
PWMA/B Extension	t_{EXT}	ENx = VCC, $I_{PWMA} > I_{PWMB}$		70		ns
		ENx = VCC, $I_{PWMA} < I_{PWMB}$		70		ns
		ENx = 80%*VCC, $I_{PWMA} > I_{PWMB}$		190		ns
		ENx = 80%*VCC, $I_{PWMA} < I_{PWMB}$		190		ns
Tri-State to High or Low Propagation Delay	t_{PTS}	Outputs Unloaded, excluding extension		10		ns
Tri-State Shutdown Holdoff Time	t_{TSSHD}	Including Propagation Delay		65		ns

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagram

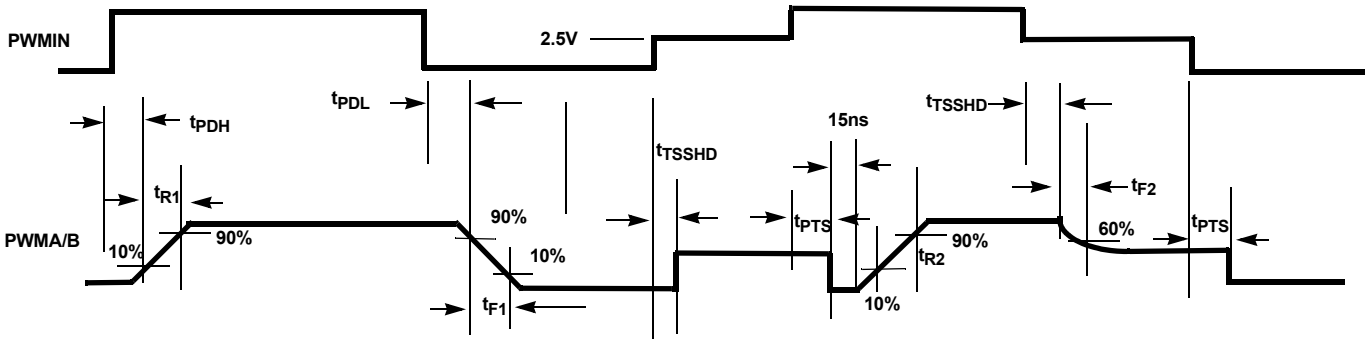


FIGURE 1. TIMING DIAGRAM

Operation

Designed for high phase count and phase shedding applications, the ISL6617 driverless phase doubler is meant to double or quadruple (cascaded option using two ISL6617s) the number of phases that Intersil's multi-phase controllers ISL63xx can support. Further, the PWM line can be pulled high to disable the respective phase and higher phase(s) when the enable pin (EN_PH_SYNC) is pulled low. This simplifies the phase shedding implementation for the controller that can disable the respective and higher phase(s) by pulling the respective PWM input high.

A rising transition on PWMIN initiates the turn-on of the PWMA/B (see Figure 1). After a short propagation delay [t_{PDH}], the PWMA/B begins to rise. Typical rise times [t_{R1}] are provided in the "Electrical Specifications" table on page 7.

A falling transition on PWMIN indicates the turn-off of the PWMA/B. The PWMA/B begins to fall [t_{F1}] after a propagation delay [t_{PDL}], which is modulated by the current balance circuits.

When the PWMIN stays in the tri-state window for longer than [t_{TSSHD}], both PWMA/B will pull to ~2V so that the cascaded 5V PWM input MOSFET driver or integrated power stage can recognize tri-state.

EN_PH_SYNC Operation

The EN_PH_SYNC pin features multiple functions. It is the enable input of the device and the input to select various operational modes.

A. ENABLE OPERATION

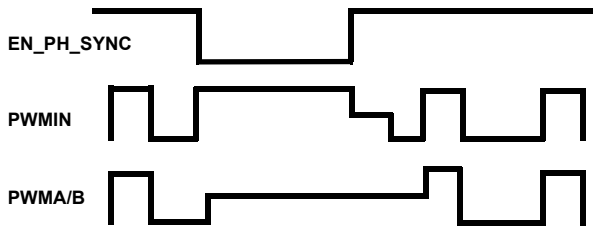


FIGURE 2. TYPICAL ENABLE OPERATION TIMING DIAGRAM

As shown in Figure 2, the ISL6617 disables the doubler operation when the EN_PH_SYNC pin is pulled to ground, while the PWMIN pin is pulled to VCC. With the PWM line pulled high, some Intersil controllers such as VR10, VR11, VR11.1 and VR12 family can disable the respective and higher phase(s). When the EN_PH_SYNC returns high, the phase doubler will pull the PWM line into tri-state window, and then will be enabled only at the leading edge of PWM input. Prior to the first PWMin rising edge, both the PWMA and PWMB output will remain in tri-state unless an overvoltage fault is detected. This fault is defined as when a phase is detected to have more than 60% of the maximum I_{OUT} current. This provides additonal protection to the load if the upper MOSFET experiences a short while the doubler is enabled.

The EN_PH_SYNC pin should remain high if driving the PWM line high is prohibited for the associated controller. For proper system interface, please refer to the device data sheets.

B. SYNCHRONOUS OPERATION

The ISL6617 can be set in interleaving mode or synchronous mode by pulling the EN_PH_SYNC pin to the respective level, shown in Table 1. A synchronous pulse can be sent to the phase doubler during the load application to improve the voltage droop and current balance while still maintaining interleaving operation at DC load conditions. However, excessive ringback can occur; hence, the synchronous mode operation should be carefully investigated. Figure 3 shows how to generate a synchronous pulse when a transient load is applied. The comparator should be a fast comparator with a minimum delay.

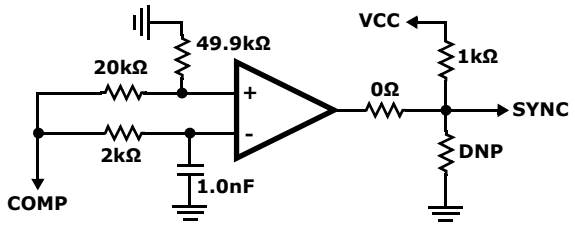


FIGURE 3. TYPICAL SYNC PULSE GENERATOR

C. VARIOUS OPERATIONAL MODES

The ISL6617 has three distinct operating modes depending upon the voltage level of the EN_PH_SYNC pin. To ensure that the ISL6617 is in operation, the pin must be above 2V. When the EN_PH_SYNC pin is set to above 97% of V_{CC}, the ISL6617 will operate in interleaving mode with a maximum extension of 70ns. When V_{CC} is between 78% and 85% of V_{CC}, the ISL6617 operates in interleaving mode with a fixed extension of 120ns and a variable extension of up to 70ns. This results in a minimum extension of 120ns and a max of 190ns. To enter this 2nd interleaving mode, the pin must remain in the 78% to 85% range for at least 4 cycles. Between 54% and 64% of V_{CC}, the device operates in synchronous mode. Figures 4 and 5 show simplified synchronous and interleaving modes' operational waveforms, respectively.

TABLE 1. ISL6617 OPERATIONAL MODES

MODE	MIN	TYP	MAX	EXTENSION
Enable Low			0.8V	
Enable High	2V			
Interleaving#1	97%*VCC		VCC	0ns to 70ns
Interleaving#2	78%*VCC	81%*VCC	85%*VCC	120ns + (0ns to 70ns)
Synchronous	54%*VCC	60%*VCC	64%*VCC	0ns to 70ns
Not Used	From 0.8V to 2V or 54% of VCC is not recommended Region.			

To transition between two different modes, the EN_PH_SYNC pin voltage level needs to be set accordingly. Figures 6 and 7 show an example of external circuits for mode transition between synchronous mode and interleaving #1 or #2 mode, respectively. The R should be less than 50kΩ to improve transition time.

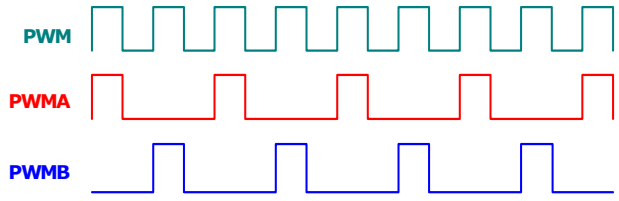


FIGURE 4. INTERLEAVING MODE'S OPERATIONAL WAVEFORMS (ENx = VCC, OR 81%*VCC)

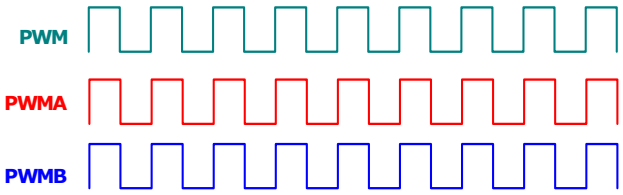


FIGURE 5. SYNCHRONOUS MODE'S OPERATIONAL WAVEFORMS (EN_PH_SYNC = 60%*VCC)

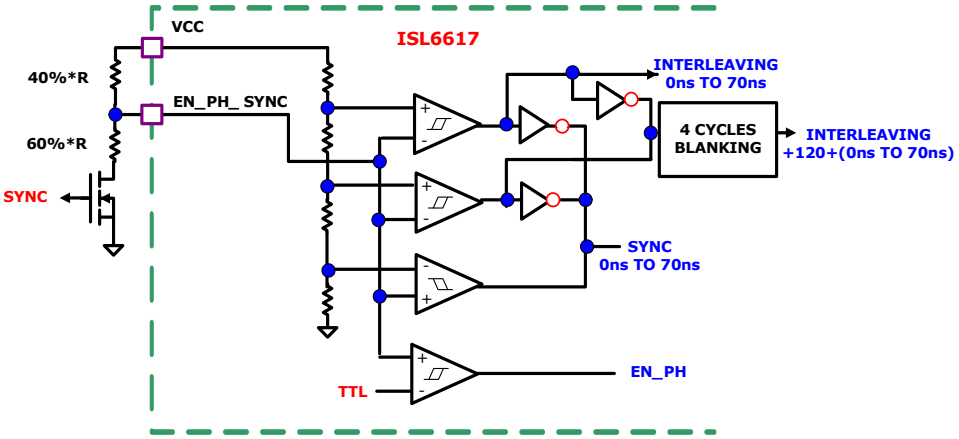


FIGURE 6. CONFIGURATION FOR TRANSITION BETWEEN SYNCHRONOUS AND INTERLEAVING #1 MODES

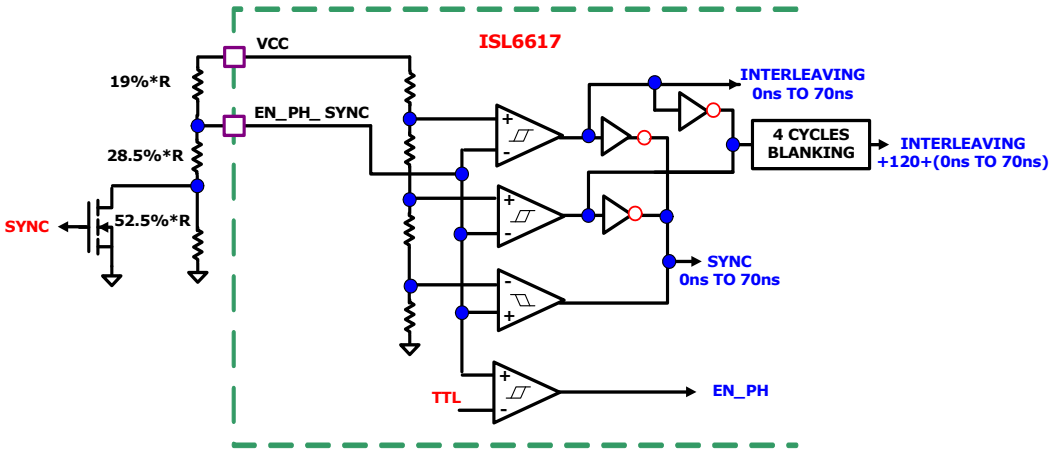


FIGURE 7. CONFIGURATION FOR TRANSITION BETWEEN SYNCHRONOUS AND INTERLEAVING #2 MODES

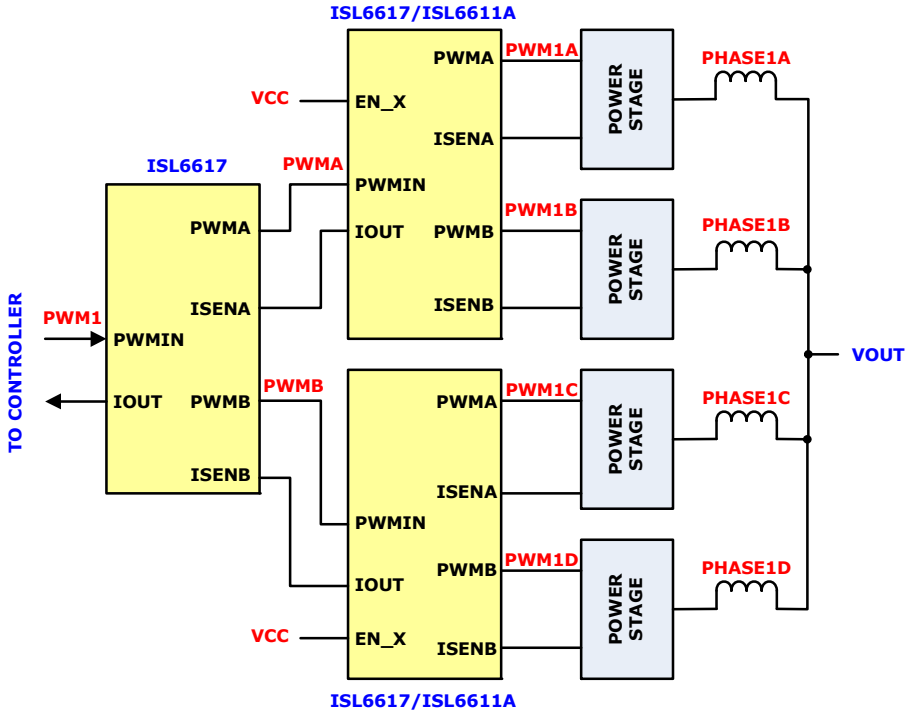


FIGURE 8. CASCADED PHASE DOUBLER SIMPLIFIED DIAGRAM

The ISL6617 can further be cascaded with itself or ISL6611A (phase doubler with integrated 5V drivers), as shown in Figure 8. This can quadruple the number of phase each PWM line can support. Figure 9 shows the operational waveforms of the cascaded doublers. The PWMIN pin will be pulled to VCC when the doubler is disabled (EN_x = Low). To avoid driving the PWM outputs of the 1st stage ISL6617 by the 2nd stage's PWMIN, the 2nd stage doubler's enable input should remain high, i.e, tied to VCC, as shown in Figure 8.

To operate each phase at the switching frequency of F_{SW}, the operational frequency of the controller needs to be scaled accordingly for different modes, as shown in Table 2.

TABLE 2. CONTROLLER FREQUENCY AND MAXIMUM DUTY CYCLE

OPERATIONAL MODES	$F_{CONTROLLER}$	ISL6617 MAXIMUM DUTY CYCLE PER PHASE	D_{MAX} WITH ISL6336G
Interleaving	2 x F_{SW}	50%	45%
Synchronous	F_{SW}	100%	90%
Cascaded Interleaving	4 x Fsw	25%	22.5%

When the doubler operates in interleaving mode, the PWM controller frequency should be set at two times the desired phase frequency (F_{SW}). Since the input PWM pulse is divided into half to feed into each phase of the doubler, the operational duty cycle of each phase should be less than 50%. In synchronous mode, the PWM controller should be operated at the same frequency as the desired phase frequency. In this mode, the allowable duty cycle is up to 100%. For cascaded interleaving, the controller switching frequency needs to be set at four times the phase frequency. During cascaded operation, the maximum allowable duty cycle will be less than 25%. All of the maximum allowable duty cycle numbers referenced assume that the PWM controller can send out a 100% duty cycle pulse. In many cases, this is not achievable because the controller needs time to reset it's internal sawtooth ramp or internal max duty limit. However, the fixed 120ns extension of interleaving mode 2 helps recover the typical 1% duty cycle loss associated with the ramp reset time. In addition, Intersil has developed a dedicated controller, the ISL6336G with 90% duty cycle, to work with the ISL6617 for high-phase count and overclocking applications.

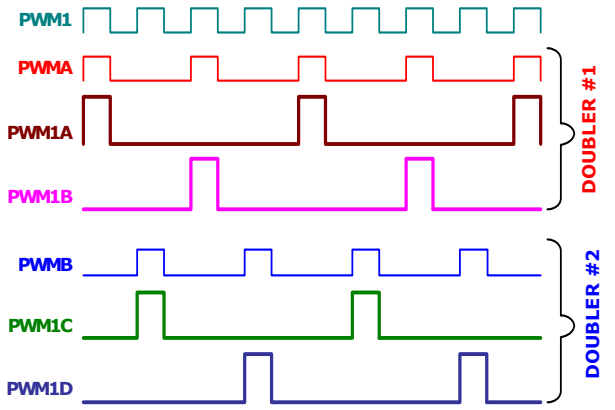


FIGURE 9. CASCADED DOUBLER OPERATIONAL WAVEFORMS

To properly compensate the system that uses phase doublers, the effective system sawtooth to calculate the modulator gain should factor in the duty cycle limitation (D_{MAX}) as Equation 1. For instance, when using ISL6336G and ISL6617s in cascaded interleaving mode, the effective sawtooth amplitude should be scaled as 3V/22.5% = 13.33V.

$$V_{RAMP\_EFFECTIVE} = \frac{V_{RAMP}}{D_{MAX}} \quad \text{(EQ. 1)}$$

Current Sensing

The ISL6617 senses current continuously for fast response. The ISL6617 supports inductor DCR sensing, or resistive sensing techniques. The associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. The sensed current, I_{SEN}, is proportional to the inductor current. The sensed current is used for current balance and load-line regulation.

The internal circuitry, shown in Figures 10 and 11, represents one channel. This circuitry is repeated for each channel in the doubler. The input bias current of the current sensing amplifier is typically 60nA; less than 5kΩ input impedance is preferred to minimize the offset error. In addition, the common mode input voltage to the amplifier should be less than VCC-3V.

A. INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 10.

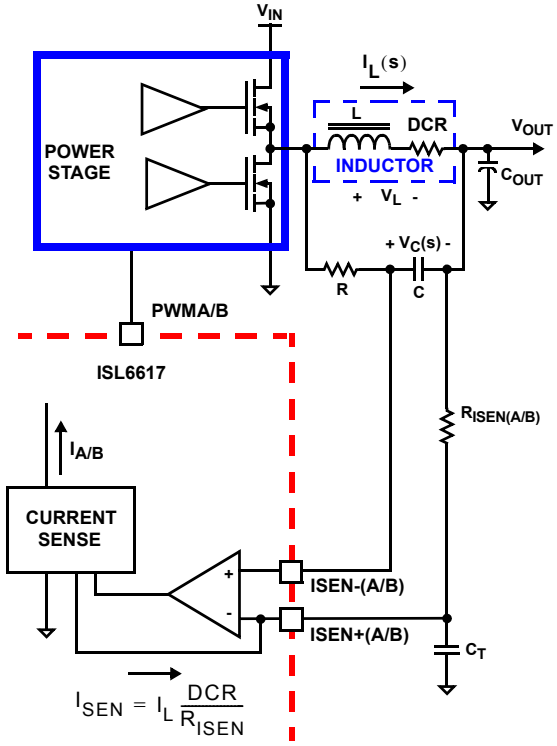


FIGURE 10. DCR SENSING CONFIGURATION

The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 2 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 2)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 10.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L. See Equation 3.

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 3)}$$

If the R-C network components are selected such that the RC time constant matches the inductor time constant (RC = L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR, i.e., proportional to the channel current.

With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense

resistor R_{ISEN}. Therefore, the current out of ISEN+ pin, I_{SEN}, is proportional to the inductor current.

Because of the internal filter at ISEN- pin, one capacitor, C_T, is needed to match the time delay between the ISEN- and ISEN+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.

Equation 4 shows that the ratio of the channel current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 4)}$$

B. RESISTIVE SENSING

For more accurate current sensing, a dedicated resistor R_{SENSE} in series with each output inductor can serve as the current sense element (see Figure 11). This technique reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

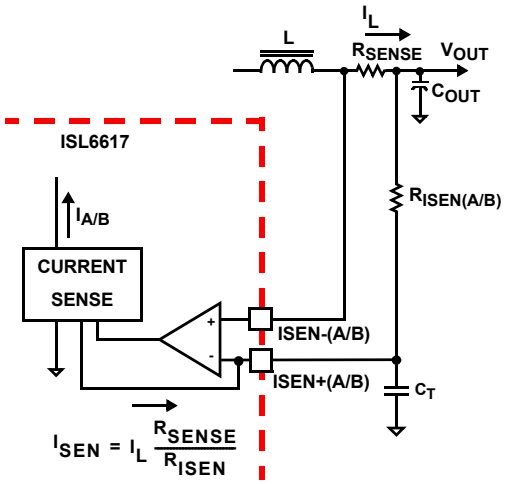


FIGURE 11. SENSE RESISTOR IN SERIES WITH INDUCTORS

The same capacitor C_T is needed to match the time delay between ISEN- and ISEN+ signals. Select the proper C_T to keep the time constant of R_{ISEN} and C_T (R_{ISEN} x C_T) close to 27ns.

Equation 5 shows the ratio of the channel current to the sensed current I_{SEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SENSE}}{R_{ISEN}} \quad \text{(EQ. 5)}$$

Current Balance and Current Monitoring

The sensed currents I_A and I_B from each respective channel are summed together and divided by 2. The resulting average current I_{AVG} provides a measure of the total load current. Channel current balance is achieved by comparing the sensed current of each channel to the average current to make an appropriate adjustment to the PWMA and PWMB duty cycle with Intersil's patented current-balance method.

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

The resulting average current I_{AVG} also goes out from the IOUT pin for current monitoring and can also be fed back to the controller's ISEN lines for current balance, load-line regulation, and overcurrent protection. For fast response to the current information, the IOUT pin should have minimum decoupling; no more than 50ns filter is recommended. The full scale of IOUT is 100µA; it typically should set resistor gain around 50µA to 80µA at the full load to ensure that it will not hit the full scale prior to the overcurrent trip point. At the same time, the current signal accuracy is maximized.

Benefits of a High Phase Count System

At heavy load condition, efficiency can be improved by spreading the load across many phases. This is primarily because the resistive loss becomes the dominant component of total loss budget at high current levels.

Since the load is carried by more phases, each power device handles less current. In addition, the devices are likely to be spread over a larger area on the Printed Circuit Board (PCB). Both these factors result in improved heat dissipation for higher phase count systems. By reducing the system's operating temperature, components reliability is improved.

Furthermore, increasing the phase count also reduces the size of ripple on both the input and output currents. It reduces EMI and improves the efficiency. Figures 12 and 13 show the ripple values for a 24-Phase voltage regulator with the following parameters:

- Input voltage: 12V
- Output voltage: 1.6V
- Duty cycle: 13.3%
- Load current: 200A
- Output Phase Inductor: 500nH
- Phase switching frequency: 200kHz

In this example, the 24-phase voltage regulator (VR) can run in 6-phase, 8-phase, 12-phase, 24-phase interleaving mode. In 6-phase interleaving mode, every 4 phases runs synchronously, which yields 18.73A and 12.93A input and output ripple currents, respectively. The 24-phase interleaving regulator significantly drops these values to 4.05A and 0.78A, respectively. As shown in Table 3, both input and output ripple currents are reduced when more phases are running in interleaving mode. Note that the 8-phase VR has lower output ripple current than the 12-phase VR since the 8-phase VR has better output ripple cancellation factor close to the duty cycle of 1/8.

TABLE 3. RIPPLE CURRENT (UNIT: A)

INTERLEAVED PHASES	6	8	12	24
Input Ripple Current	18.73	11.64	8.79	4.05
Output Ripple Current	12.93	2.70	4.83	0.78

Figure 14 shows the efficiency of a 12-phase VR design, which runs the doubler in interleaving and synchronous modes. For comparison, a 6-phase VR with the same number of MOSFETs and inductors is also plotted, clearly demonstrating the efficiency improvement of a high-phase count system and interleaving mode over synchronous mode resulting from the better ripple cancellation.

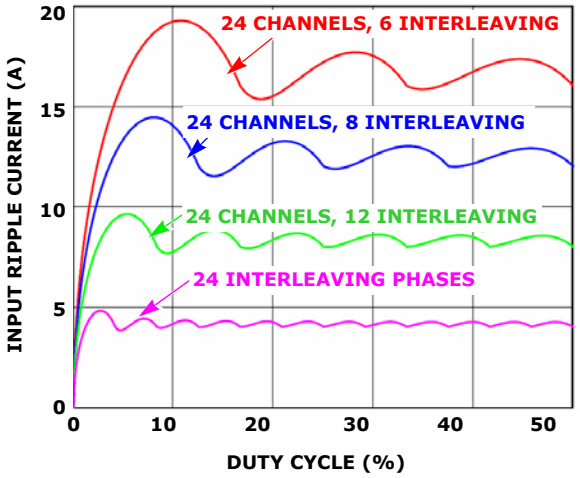


FIGURE 12. INPUT CURRENT RIPPLE VS DUTY CYCLE, PHASE COUNT

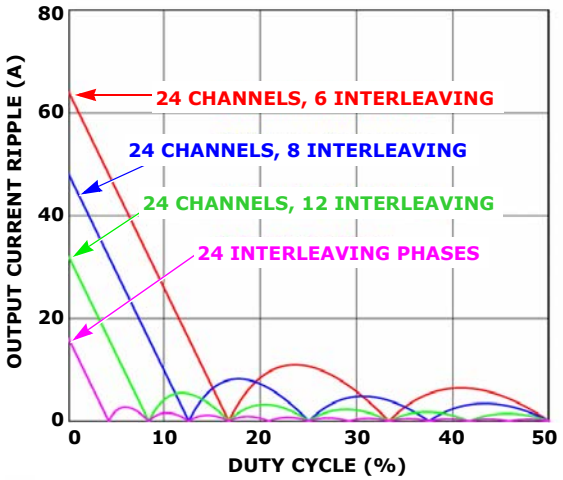


FIGURE 13. OUTPUT CURRENT RIPPLE VS DUTY CYCLE, PHASE COUNT

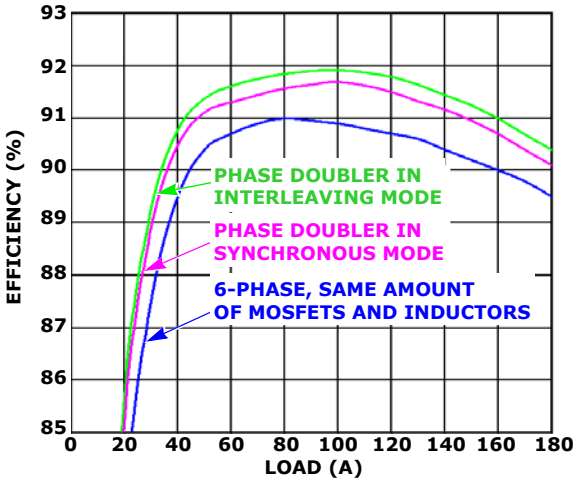


FIGURE 14. EFFICIENCY COMPARISON IN 12-PHASE DESIGN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
2/4/10	FN7564.0	Initial release.

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