ISL6721A

Flexible Single-Ended Current Mode PWM Controller

FN6797
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The ISL6721A is a low power, single-ended Pulse-Width Modulating (PWM) current mode controller designed for a wide range of DC/DC conversion applications including Boost, Flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection. Other features include a low power mode in which the supply current drops to less than 200µA during overvoltage and overcurrent shutdown faults. The ISL6721A differs from the ISL6721 in that the UVLO and UV thresholds have been modified.

This advanced BiCMOS design features low operating current, adjustable operating frequency up to 1MHz, adjustable soft-start, and a bidirectional SYNC signal that allows the oscillator to be locked to an external clock for noise sensitive applications.

Related Literature

For a full list of related documents, visit our website

- ISL6721A product page

Features

- 1A MOSFET gate driver
- 100µA startup current
- Fast transient response with Peak Current Mode control
- Adjustable switching frequency up to 1MHz
- Bidirectional synchronization
- Low Power Disable mode
- Delayed restart from OV and OC shutdown faults
- Adjustable slope compensation
- Adjustable soft-start
- Adjustable overcurrent shutdown threshold
- Adjustable UV and OV monitors
- Leading edge blanking
- Integrated thermal shutdown
- 1% tolerance voltage reference
- Pb-Free (RoHS compliant)

Applications

- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- Isolated buck and flyback regulators
- Boost regulators

Contents

1. Overview

1.1 Typical Applications

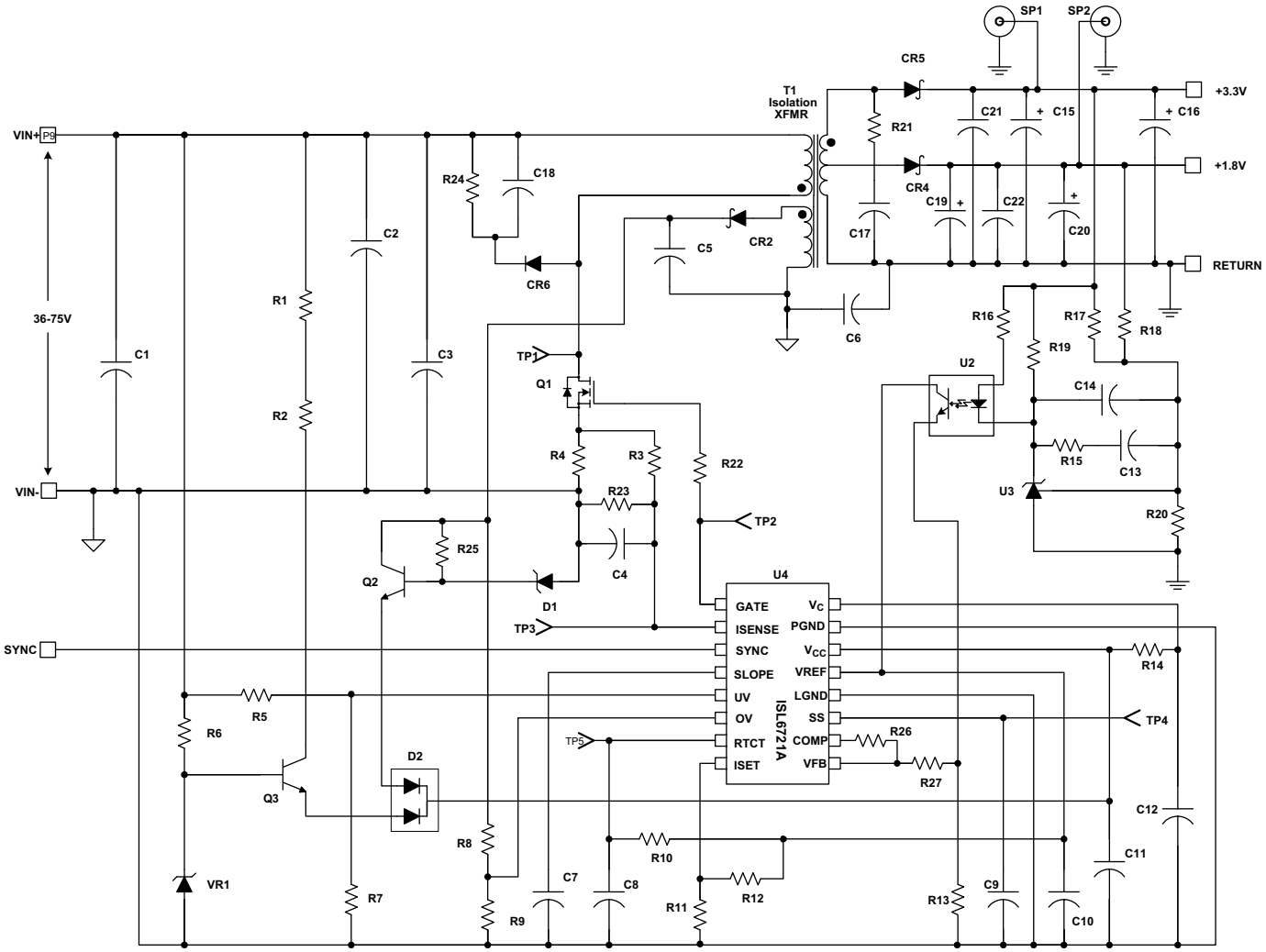


Figure 1. Typical Application, 48V Input Dual Output Flyback, 3.3V at 2.5A, 1.8V at 1.0A

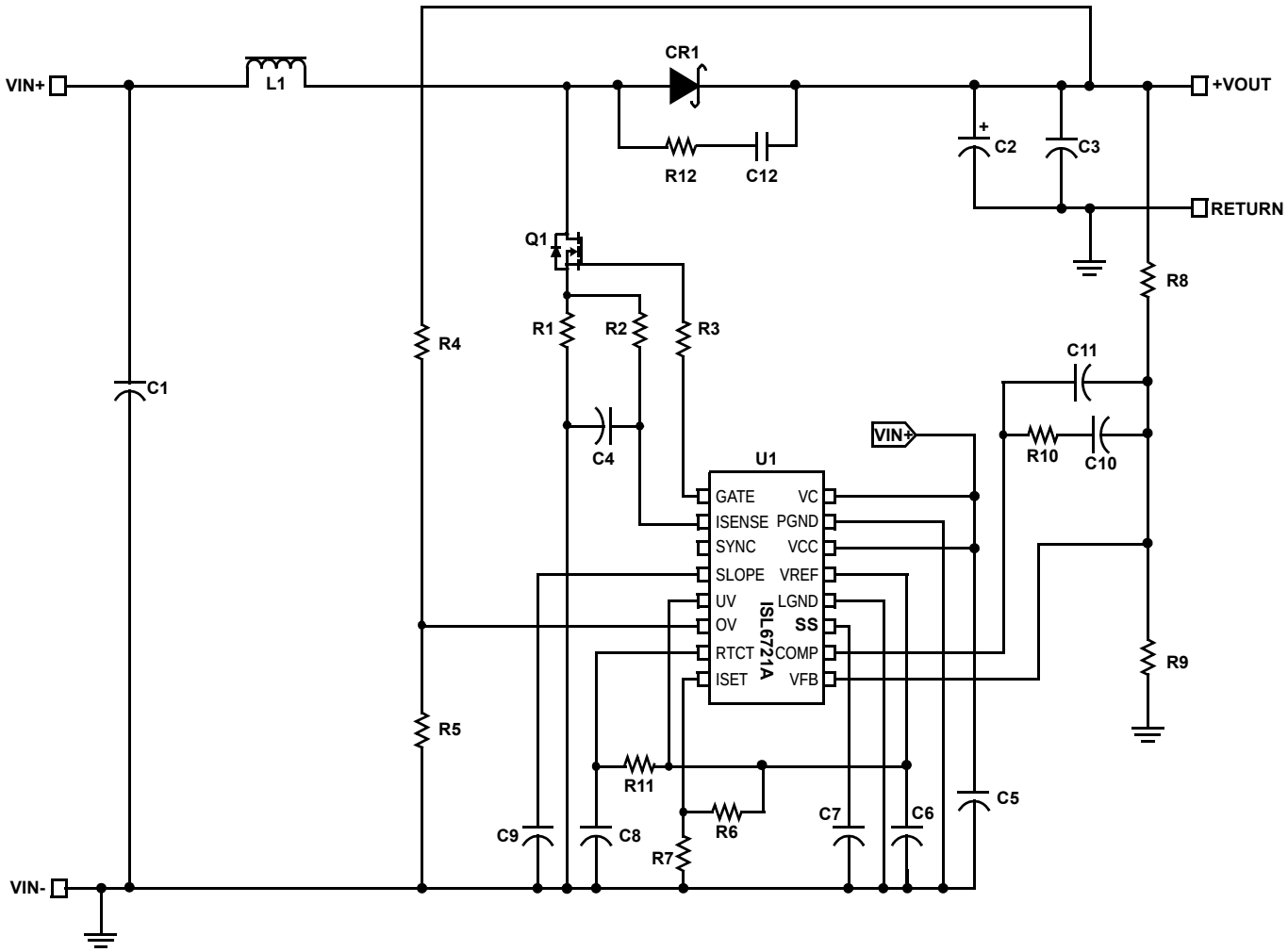
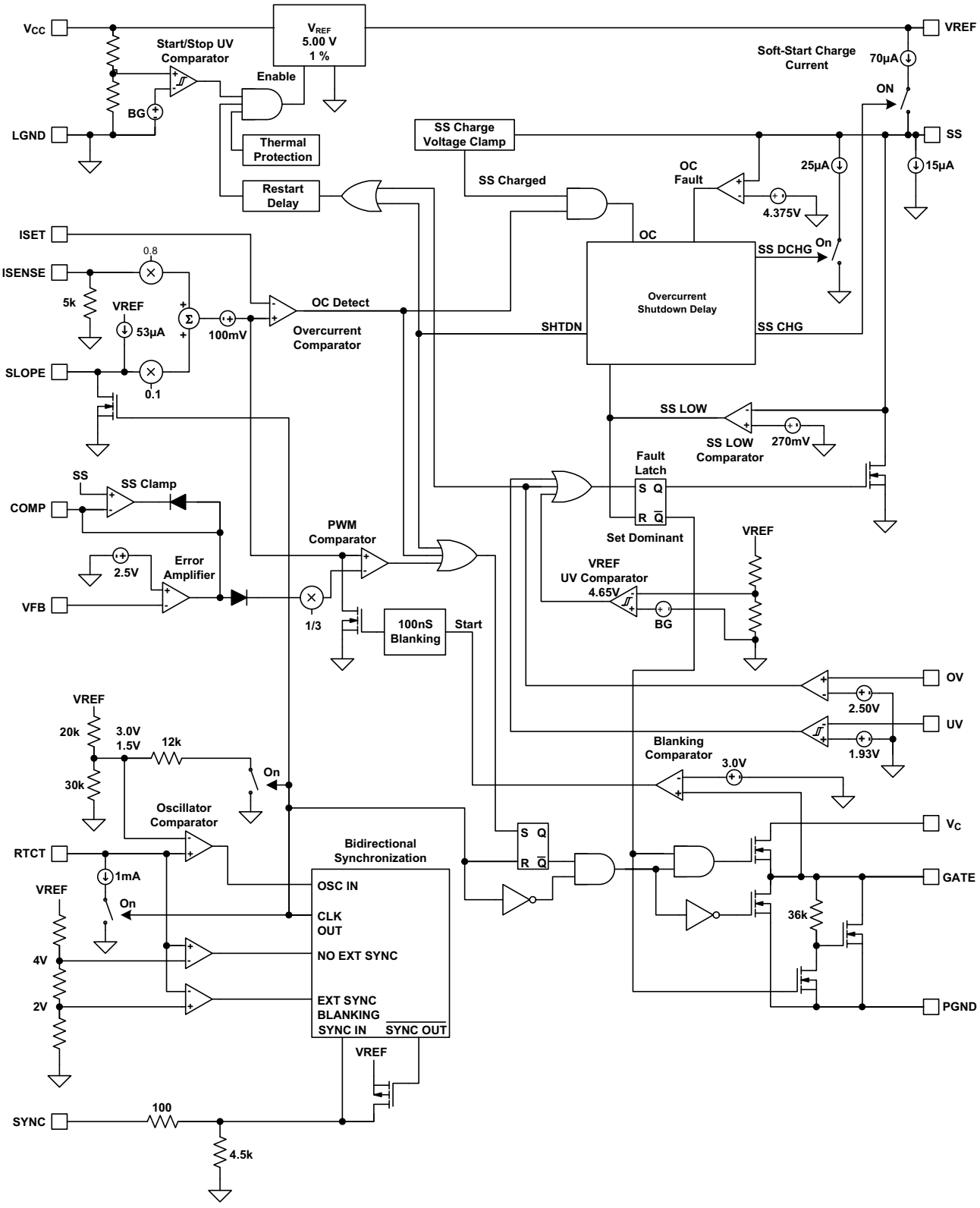


Figure 2. Typical Boost Converter Application Schematic

1.2 Block Diagram



1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL6721AARZ	21AZ	-40 to +105	-	16 Ld QFN	L16.3x3B
ISL6721AARZ-T	21AZ	-40 to +105	6k	16 Ld QFN	L16.3x3B
ISL6721AAVZ	6721A AVZ	-40 to +105	-	16 Ld TSSOP	M16.173
ISL6721AAVZ-T	6721A AVZ	-40 to +105	2.5k	16 Ld TSSOP	M16.173

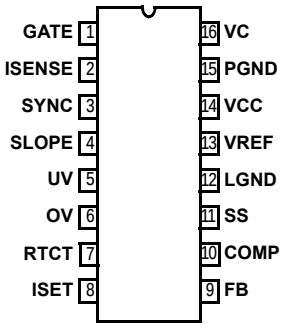
Notes:
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL6721A device information page. For more information about MSL, refer to TB363.

Table 1. Key Differences Between Family of Parts

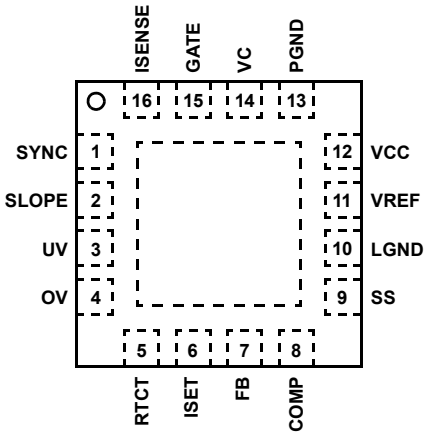
Part Number	ISL6721A	ISL6721
UVLO thresholds (start/stop) (V)	6.80/6.20	8.25/7.7
UV threshold (V)	1.93	1.45

1.4 Pin Configurations

16 Ld TSSOP
Top View



16 Ld QFN
Top View



1.5 Pin Descriptions

Pin Number (16 Ld TSSOP)	Pin Number (16 Ld QFN)	Pin Name	Description
1	15	GATE	Device output. This high current power driver is capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{CC} is below the UVLO threshold. The output high voltage is held to ~13.5V. Do not apply voltages exceeding this clamp value to the GATE pin. The output stage provides very low impedance to overshoot and undershoot.
2	16	ISENSE	Input to the current sense comparators. The IC has two current sensing comparators: a PWM comparator for peak current mode control and an overcurrent protection comparator. The overcurrent comparator threshold is adjustable through the ISET pin. Exceeding the overcurrent threshold starts a delayed shutdown sequence. When an overcurrent condition is detected, the soft-start charge current source is disabled and a discharge current source is enabled. The soft-start capacitor begins discharging, and if it discharges to less than 4.375V (sustained overcurrent threshold), a shutdown condition occurs and the GATE output is forced low. Refer to "Overcurrent Operation" on page 17 for more details. The GATE output remains low until the reset threshold is attained. At this point, a soft-start cycle begins. If the overcurrent condition ceases and an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs and the soft-start voltage is allowed to recharge.
3	1	SYNC	This bidirectional synchronization signal coordinates the switching frequency of multiple units. Units can be synchronized by connecting the SYNC signal of each unit together or by using an external master clock signal. The oscillator timing capacitor, C_T, is still required even if an external clock is used. The first unit to assert this signal assumes control. The SYNC frequency can be either higher or lower than the free running oscillator frequency.
4	2	SLOPE	Method by which the ISENSE ramp slope can be increased for improved noise immunity or improved control loop stability for duty cycles greater than 50%. An internal current source charges an external capacitor to GND during each switching cycle. The resulting ramp is scaled and added to the ISENSE signal.
5	3	UV	Undervoltage monitor input pin. This signal is compared to an internal 1.93V reference to detect an undervoltage condition.
6	4	OV	Overvoltage monitor input pin. This signal is compared to an internal 2.5V reference to detect an overvoltage condition.
7	5	RTCT	Oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, R_T, between V_{REF} and this pin and a timing capacitor, C_T, from this pin to LGND. The oscillator produces a sawtooth waveform with a programmable frequency range of 100kHz to 1.0MHz. The charge time, t_C; the discharge time, t_D; the switching frequency, f_{SW}; and the maximum duty cycle, Dmax, can be calculated from Equations 1, 2, 3, and 4: (EQ. 1) $t_C \approx 0.655 \bullet R_T \bullet C_T$ s (EQ. 2) $t_D \approx -R_T \bullet C_T \bullet LN\left(\frac{0.001 \bullet R_T - 3.6}{0.001 \bullet R_T - 1.9}\right)$ s (EQ. 3) $f_{sw} = \frac{1}{t_D + t_C}$ Hz (EQ. 4) $Dmax = t_C \bullet f_{SW}$ Use Figure 4 on page 14 as a guideline for selecting the capacitor and resistor values required for a given frequency.

Pin Number (16 Ld TSSOP)	Pin Number (16 Ld QFN)	Pin Name	Description
8	6	ISET	Sets the pulse-by-pulse overcurrent threshold by applying a DC voltage between 0.35V and 1.2V to this input. When overcurrent inception occurs, the SS capacitor begins to discharge and starts the overcurrent delayed shutdown cycle.
9	7	FB	Feedback voltage input connected to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally tied to a reference voltage. Current sense leading edge blanking is disabled when the FB input is less than 2.0V.
10	8	COMP	Error amplifier output and the PWM comparator input. The control loop frequency compensation network is connected between the COMP and FB pins. The ISL6721A features a built-in full cycle soft-start. Soft-start is implemented as a clamp on the maximum COMP voltage.
11	9	SS	Connect the soft-start capacitor between this pin and LGND to control the duration of soft-start. The value of the capacitor determines both the rate of increase of the duty cycle during start-up and controls the overcurrent shutdown delay.
12	10	LGND	A small signal reference ground for all analog functions on this device.
13	11	VREF	The 5V reference voltage output. Bypass to LGND with a 0.01µF or larger capacitor to filter this output as needed. Using capacitance less than this value may cause unstable operation.
14	12	VCC	Power connection for the device. Although quiescent current, I_{CC}, is low, it is dependent on the frequency of operation. To optimize noise immunity, bypass VCC to LGND with a ceramic capacitor as close to the VCC and LGND pins as possible. The total supply current (I_C plus I_{CC}) will be higher, depending on the load applied to GATE. Total current is the sum of the quiescent current and the average gate current. Knowing the operating frequency, f_{sw}, and the MOSFET gate charge, Qg, the average GATE output current can be calculated in Equation 5: (EQ. 5) $Igate = Qg \bullet f_{SW}$ A
15	13	PGND	Provides a dedicated ground for the output gate driver. Connect the LGND and PGND pins externally using a short printed circuit board trace close to the IC. This is imperative to prevent large, high frequency switching currents flowing through the ground metallization inside the IC (decouple V_C to PGND with a low ESR 0.1µF or larger capacitor).
16	14	VC	A separate collector supply to the output gate drive. Separating VC and PGND helps decouple the IC's analog circuitry from the high power gate drive noise (decouple VC to PGND with a low ESR 0.1µF or larger capacitor).
N/A	Thermal Pad	Thermal Pad	The thermal pad located on the bottom of the QFN package is electrically isolated. Renesas recommends connecting it to signal ground.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{CC}, V_C	GND - 0.3	+20.0	V
GATE	GND - 0.3	Gate Output Limit Voltage	V
PGND to LGND	-0.3	+0.3	V
VREF	GND - 0.3	5.3V	V
Signal Pins	GND - 0.3	VREF	V
Peak GATE Current		1	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN (Notes 4, 5)	44	4
16 Ld TSSOP (Notes 6, 7)	105	33

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	Refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-40	+105	°C
Supply Voltage Range (Typical, Note 8)	9	18	VDC

Note:

8. All voltages are measured with respect to GND.

2.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Block Diagram" on page 6 and the Typical Application schematics on page 4 and page 5. 9V < V_{CC} = V_C < 20V, RT = 11kΩ, CT = 330 pF. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

Parameter	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Units
Undervoltage Lockout					
START Threshold		**6.40**	6.80	**6.90**	V
STOP Threshold		**5.85**	6.20	**6.30**	V
Hysteresis		**0.50**	0.60	**1.00**	V
Start-Up Current, I_{CC}	V_{CC} < START Threshold	-	100	**175**	µA
OC/OV Fault Operating Current, I_{CC}		-	200	**300**	µA
Operating Current, I_{CC}	(Note 11)	-	4.5	**10.0**	mA
Operating Supply Current, I_C	Includes 1nF GATE loading	-	8.0	**12.0**	mA
Reference Voltage					
Overall Accuracy	Line, load, 0°C to +105°C	4.95	5.00	5.05	V
	Line, load, -40°C to +105°C	**4.90**	5.00	**5.05**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 10)	**-**	5	**-**	mV
Fault Voltage		**4.50**	4.65	**4.75**	V
VREF Good Voltage		**4.65**	4.80	**4.95**	V
Hysteresis		**75**	165	**250**	mV
Operational Current		**-10**	-	**-**	mA
Current Limit		**-20**	-	**-**	mA
Current Sense					
Input Impedance		-	5	-	kΩ
Offset Voltage		**0.08**	0.10	**0.11**	V
Input Voltage Range		**0**	-	**1.5**	V
Blanking Time	(Note 10)	**30**	60	**100**	ns
Gain, A_{CS}	V_{SLOPE} = 0V, V_{FB} = 2.3V, V_{ISET} = 0.35V, 1.5V A_{CS} = ΔISET/ΔISENSE	**0.77**	0.79	**0.81**	V/V
Error Amplifier					
Open Loop Voltage Gain	(Note 10)	**60**	90	-	dB
Gain-Bandwidth Product	(Note 10)	-	**15**	-	MHz
Reference Voltage Initial Accuracy	V_{FB} = COMP, T_A = +25°C (Note 10)	2.465	2.515	2.565	V
Reference Voltage	V_{FB} = COMP	**2.44**	2.515	**2.590**	V
COMP to PWM Gain, A_{COMP}	COMP = 4V, T_A = +25°C	0.31	0.33	0.35	V/V
COMP to PWM Offset	COMP = 4V (Note 10)	**0.51**	0.75	**0.88**	V
FB Input Bias Current	V_{FB} = 0V	**-2**	0.1	2	µA
COMP Sink Current	COMP = 1.5V, V_{FB} = 2.7V	**2**	6	-	mA
COMP Source Current	COMP = 1.5V, V_{FB} = 2.3V	**-0.25**	-0.5	-	mA
COMP VOH	V_{FB} = 2.3V	**4.25**	4.4	**5.0**	V
COMP VOL	V_{FB} = 2.7V	**0.4**	0.8	**1.2**	V

Recommended operating conditions unless otherwise noted. Refer to "Block Diagram" on page 6 and the Typical Application schematics on page 4 and page 5. 9V < V_{CC} = V_C < 20V, RT = 11kΩ, CT = 330 pF. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

Parameter	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Units
PSRR	Frequency = 120Hz (Note 10)	**60**	80	-	dB
SS Clamp, V_{COMP}	SS = 2.5V, V_{FB} = 0V, ISET = 2V	**2.4**	2.5	**2.6**	V
Oscillator					
Frequency Accuracy		**289**	318	**347**	kHz
Frequency Variation with V_{CC}	T = +105°C (f_{20V} - f_{9V})/f_{9V}	-	2	3	%
	T = -40°C (f_{20V} -f_{9V})/f_{9V}	-	2	3	%
Temperature Stability	(Note 10)	-	8	-	%
Maximum Duty Cycle	(Note 12)	**68**	75	**81**	%
Comparator High Threshold - Free Running		-	3.00	-	V
Comparator High Threshold - with External SYNC	(Note 10)	-	4.00	-	V
Comparator Low Threshold		-	1.50	-	V
Discharge Current	0°C to +105°C	0.75	1.0	1.2	mA
	-40°C to +105°C	**0.70**	1.0	**1.2**	mA
Synchronization					
Input High Threshold		-	-	2.5	V
Input Pulse Width		**25**	-	-	ns
Input Frequency Range	(Note 10)	**0.65 x Free Running**	**-**	**1.0**	MHz
Input Impedance		-	4.5	-	kΩ
VOH	R_{LOAD} = 4.5kΩ	**2.5**	-	-	V
VOL	R_{LOAD} = open	-	-	**0.1**	V
SYNC Advance	SYNC rising edge to GATE falling edge, C_{GATE} = C_{SYNC} = 100pF	-	25	**55**	ns
Output Pulse Width	C_{SYNC} = 100pF	**50**	-	-	ns
Soft-Start					
Charging Current	SS = 2V	**-40**	-55	**-70**	µA
Charged Threshold Voltage		**4.26**	4.50	**4.74**	V
Initial Overcurrent Discharge Current	Sustained OC Threshold < SS < Charged Threshold	**30**	40	**55**	µA
Overcurrent Shutdown Threshold Voltage	Charged Threshold minus, T_A = +25°C	0.095	0.125	0.155	V
Fault Discharge Current	SS = 2V	**0.25**	1.0	-	mA
Reset Threshold Voltage	T_A = +25°C	0.22	0.27	0.31	V
Slope Compensation					
Charge Current	SLOPE = 2V, 0°C to +105°C	-45	-53	-65	µA
	-40°C to +105°C	**-41**	-53	**-65**	µA
Slope Compensation Gain	Fraction of slope voltage added to I_{SENSE}, T_A = +25°C	0.097	-	0.103	V/V
	Fraction of slope voltage added to I_{SENSE}	**0.082**	**-**	**0.118**	V/V

Recommended operating conditions unless otherwise noted. Refer to "Block Diagram" on page 6 and the Typical Application schematics on page 4 and page 5. 9V < V_{CC} = V_C < 20V, RT = 11kΩ, CT = 330 pF. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

Parameter	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Units
Discharge Voltage	V_{RTCT} = 4.5V	-	0.1	**0.2**	V
Gate Output					
Gate Output Limit Voltage	V_C = 20V, C_{GATE} = 1nF, I_{OUT} = 0mA	**11.0**	13.5	**16.0**	V
Gate VOH	V_C - GATE, V_C = 10V, I_{OUT} = 150mA	-	1.5	**2.2**	V
Gate VOL	GATE - PGND, IOUT = 150mA	-	1.2	**1.5**	V
	IOUT = 10mA	-	0.6	**0.8**	V
Peak Output Current	V_C = 20V, C_{GATE} = 1nF (Note 10)	-	1.0	-	A
Output "Faulted" Leakage	V_C = 20V, UV = 0V, GATE = 2V	**1.2**	2.6	-	mA
Rise Time	V_C = 20V, C_{GATE} = 1nF 1V < GATE < 9V	-	60	**100**	ns
Fall Time	V_C = 20V, C_{GATE} = 1nF 1V < GATE < 9V	-	15	**40**	ns
Minimum ON time	ISET = 0.5V; V_{FB} = 0V; VC = 11V ISENSE to GATE w/10:1 Divider RTCT = 4.75V through 1kΩ (Note 10)	-	-	**110**	ns
Overcurrent Protection					
Minimum ISET Voltage		-	-	**0.35**	V
Maximum ISET Voltage		**1.2**	-	-	V
ISET Bias Current	V_{ISET} = 1.00V	**-1.0**	-	**1.0**	µA
Restart Delay	T_A = +25°C	150	295	445	ms
OV and UV Voltage Monitor					
Overvoltage Threshold		**2.4**	2.5	**2.6**	V
Undervoltage Fault Threshold		**1.89**	1.93	**2.00**	V
Undervoltage Clear Threshold		**1.96**	2.01	**2.10**	V
Undervoltage Hysteresis Voltage		**20**	50	**100**	mV
UV Bias Current	V_{UV} = 2.10 V	**-1.0**	-	**1.0**	µA
OV Bias Current	V_{OV} = 2.00 V	**-1.0**	-	**1.0**	µA
Thermal Protection					
Thermal Shutdown	(Note 10)	120	130	140	°C
Thermal Shutdown Clear	(Note 10)	105	120	135	°C
Hysteresis	(Note 10)	-	10	-	°C

Notes:

9. Parameters with MIN and/or MAX limits are 100% tested at 25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. This parameter, although guaranteed by characterization or correlation testing, is not 100% tested in production.
11. This is the V_{CC} current consumed when the device is active but not switching. Does not include gate drive current.
12. This is the maximum duty cycle achievable using the specified values of RT and CT. Larger or smaller maximum duty cycles may be obtained using other values for RT and CT. See Equations 1, 2, 3, and 4.

3. Typical Performance Curves

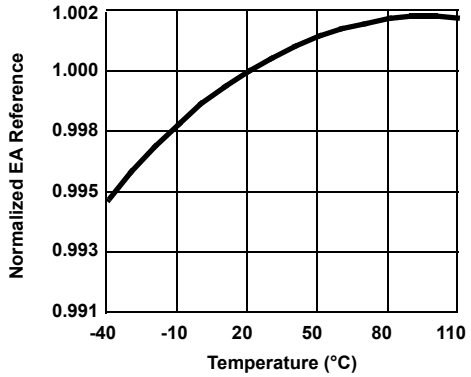


Figure 3. EA Reference Voltage vs Temperature

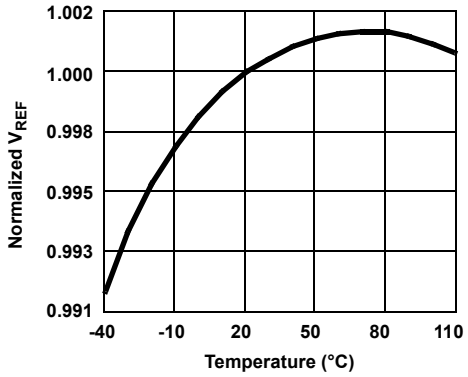


Figure 4. VREF Reference Voltage vs Temperature

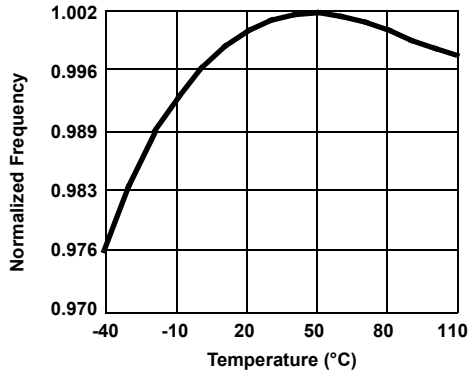


Figure 5. Oscillator Frequency vs Temperature

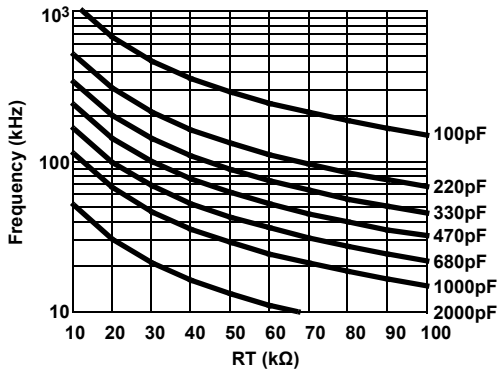


Figure 6. Resistance for CT Capacitor Values Given

4. Functional Description

4.1 Features

The ISL6721A current mode PWM is an ideal choice for low-cost Flyback and Forward topology applications requiring enhanced control and supervisory capability. With adjustable overvoltage and undervoltage thresholds, overcurrent threshold, and hiccup delay, a highly flexible design with minimal external components is possible. Other features include peak current mode control, adjustable soft-start, slope compensation, adjustable oscillator frequency, and a bidirectional synchronization clock input.

4.2 Oscillator

The ISL6721A has a sawtooth oscillator with a programmable frequency range to 1MHz, which can be programmed with a resistor and capacitor on the RTCT pin. Refer to Figure 6 for the resistance and capacitance required for a given frequency.

4.3 Implementing Synchronization

Synchronize the oscillator to an external clock applied at the SYNC pin or by connecting the SYNC pins of multiple ICs together. If using an external master clock signal, it must be at least 65% of the free-running frequency of the oscillator for proper synchronization. The external master clock signal should have a pulse width greater than 20ns. If no master clock is used, the first device to assert SYNC assumes control of the SYNC signal. An external SYNC pulse is ignored if it occurs during the first 1/3 of the switching cycle.

During normal operation, the RTCT voltage charges from 1.5V to 3.0V and back during each cycle. Clock and SYNC signals are generated when the 3.0V threshold is reached. If an external clock signal is detected during the latter 2/3 of the charging cycle, the oscillator switches to external synchronization mode and relies on the external SYNC signal to terminate the oscillator cycle. The generation of a SYNC signal is inhibited in this mode. If the RTCT voltage exceeds 4.0V (no external SYNC signal terminates the cycle), the oscillator reverts to the internal clock mode and a SYNC signal is generated.

4.4 Soft-Start Operation

The ISL6721A features soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces voltage stresses and surge currents during start-up.

At start-up, the soft-start circuitry clamps the error amplifier output (COMP pin) to a value proportional to the soft-start voltage. The error amplifier output rises as the soft-start capacitor voltage rises. This increases the output pulse width from zero to the steady state operating duty cycle during the soft-start period. When the soft-start voltage exceeds the error amplifier voltage, soft-start is complete. Soft-start forces a controlled output voltage rise. Soft-start occurs during start-up and after recovery from a fault condition or overcurrent shutdown. The soft-start voltage is clamped to 4.5V.

4.5 Gate Drive

The ISL6721A can source and sink 1A peak current. Separate collector supply (V_C) and power ground (PGnd) pins help isolate the IC's analog circuitry from the high power gate drive noise. To limit the peak current through the IC, place an external resistor between the IC totem-pole output (GATE pin) and the MOSFET gate. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

4.6 Slope Compensation

Use slope compensation to improve noise immunity in applications in which the maximum duty cycle is less than 50%, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. Slope compensation is required to prevent instability in applications in which the duty cycle is greater than 50%. Slope compensation is a technique in

which the current feedback signal is modified by adding additional slope to it. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. However, adding excessive slope compensation results in a control loop that behaves more as a voltage mode controller than as current mode controller (Figure 7).

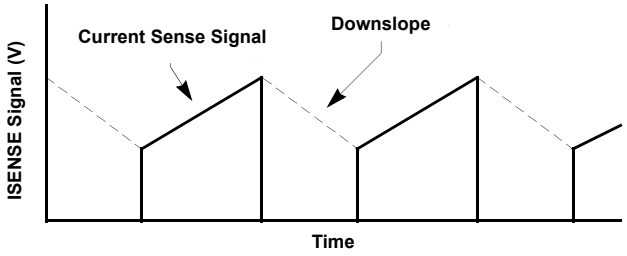


Figure 7. Slope Compensation

The minimum amount of capacitance to place at the SLOPE pin is calculated in Equation 6:

$$C_{SLOPE} = 4.24\times10^{-6} \bullet \frac{t_{ON}}{V_{SLOPE}} \quad F \tag{EQ. 6}$$

where t_{ON} is the On time and V_{SLOPE} is the amount of voltage to be added as slope compensation to the current feedback signal. In general, the amount of slope compensation added is two to three times the minimum required.

Example:

Assume the inductor current signal presented at the ISENSE pin decreases 125mV during the Off period, and:

Switching Frequency, f_{SW} = 250kHz

Duty Cycle, D = 60%

$t_{ON} = D/f_{SW} = 0.6/250E3 = 2.4\mu s$

$t_{OFF} = (1 - D)/f_{SW} = 1.6\mu s$

Determine the downslope:

Downslope = 0.125V/1.6µs = 78mV/µs. Now determine the amount of voltage that must be added to the current sense signal by the end of the On time (Equation 7).

$$V_{SLOPE} = \frac{1}{2} \bullet 0.078 \bullet 2.4 = 94mV \tag{EQ. 7}$$

Therefore (Equation 8),

$$C_{SLOPE(MIN)} = 4.24\times10^{-6} \bullet \frac{2.4\times10^{-6}}{0.094} \approx 110pF \tag{EQ. 8}$$

An appropriate slope compensation capacitance for this example would be 1/2 to 1/3 the calculated value, or between 68pF and 33pF.

4.7 Overvoltage and Undervoltage Monitor

The OV and UV signals are inputs to a window comparator that monitors the input voltage level to the converter. If the voltage falls outside of the user designated operating range, a shutdown fault occurs. For OV faults, the supply current, I_{CC}, is reduced to 200µA for ~295ms, at which time recovery is attempted. If the fault is cleared, a soft-start cycle begins. If the fault is not cleared, another shutdown cycle occurs. A UV condition also results in a shutdown fault, but the device does not enter Low Power mode and no restart delay occurs when the fault clears.

A resistor divider between V_{IN} and LGND to each input determines the operational thresholds. The UV threshold has a fixed hysteresis of 75mV nominal.

4.8 Overcurrent Operation

The overcurrent threshold level is set by the voltage applied at the ISET pin. Set the overcurrent level by using a resistor divider network from VREF to LGND. Set the ISET threshold at a level that corresponds to the desired peak output inductor current plus the additive effects of slope compensation.

Overcurrent delayed shutdown is enabled when the soft-start cycle is complete. If an overcurrent condition is detected, the soft-start charging current source is disabled and the discharging current source is enabled. The soft-start capacitor is discharged at a rate of 40µA. At the same time, a 50µs retriggerable one-shot timer is activated and remains active for 50µs after the overcurrent condition stops. The soft-start discharge cycle cannot be reset until the one-shot timer becomes inactive. If the soft-start capacitor discharges by more than 0.125V to 4.375V, the output is disabled and the soft-start capacitor is discharged. The output remains disabled and I_{CC} drops to 200µA for approximately 295ms. A new soft-start cycle is then initiated. The OC protection shutdown and restart behavior is often referred to as hiccup operation due to its repetitive start-up and shutdown characteristics.

If the overcurrent condition stops at least 50µs before the soft-start voltage reaches 4.375V, the soft-start charging and discharging currents revert to normal operation and the soft-start voltage is allowed to recover.

Hiccup OC protection may be defeated by setting ISET to a voltage that exceeds the Error Amplifier current control voltage, or about 1.5V.

4.9 Leading Edge Blanking

The leading edge blanking circuitry removes the initial 100ns of the current feedback signal input at ISENSE. The blanking period begins when the GATE output leading edge exceeds 3.0V. Leading edge blanking prevents current spikes from parasitic elements in the power supply from causing false trips of the PWM comparator and the overcurrent comparator.

4.10 Fault Conditions

A fault condition occurs if VREF falls below 4.65V, the OV input exceeds 2.50V, the UV input falls below 1.93V, or the junction temperature of the die exceeds ~+130°C. When a Fault is detected, the GATE output is disabled and the soft-start capacitor is quickly discharged. A soft-start cycle begins when the Fault condition clears and the soft-start voltage is below the reset threshold.

4.11 Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. Power ground (PGND) can be separated from the logic ground (LGND) and connected at a single point. Bypass V_C directly to PGND with good high frequency capacitors. Connect the return connection for input power and the bulk input capacitor to the PGND ground plane.

5. Reference Design

The typical boost converter application schematic (Figure 2 on page 5) features the ISL6721A in a conventional dual output 10W discontinuous mode Flyback DC/DC converter. The ISL6721EVAL1Z demonstration board implements this design and is available for evaluation.

The input voltage range is from 36VDC to 75VDC, and the two outputs are 3.3V at 2.5A and 1.8V at 1.0A. Use the weighted sum of the two outputs for cross regulation.

5.1 Circuit Element Descriptions

The converter design consists of the following functional blocks:

Input Storage and Filtering Capacitors: C_1, C_2, C_3

Isolation Transformer: T1

Primary voltage Clamp: C_{R6}, R_{24}, C_{18}

Start Bias Regulator: R_1, R_2, R_6, Q_3, V_{R1}

Operating Bias and Regulator: R_{25}, Q_2, D_1, C_5, C_{R2}, D_2

Main MOSFET Power Switch: Q_1

Current Sense Network: R_4, R_3, R_{23}, C_4

Feedback Network: R_{13}, R_{15}, R_{16}, R_{17}, R_{18}, R_{19}, R_{20}, R_{26}, R_{27}, C_{13}, C_{14}, U_2, U_3

Control Circuit: C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, R_5, R_6, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{14}, R_{22}

Output Rectification and Filtering: C_{R4}, C_{R5}, C_{15}, C_{16}, C_{19}, C_{20}, C_{21}, C_{22}

Secondary Snubber: R_{21}, C_{17}

5.2 Design Criteria

The following design requirements were selected:

Switching frequency, f_{SW}: 200kHz

V_{IN}: 36V to 75V

$V_{OUT(1)}$: 3.3V at 2.5A

$V_{OUT(2)}$: 1.8V at 1.0A

$V_{OUT(BIAS)}$: 12V at 50mA

P_{OUT}: 10W

Efficiency: 70%

Maximum duty cycle, D_{MAX}: 0.45

5.3 Transformer Design

Flyback transformer design is an iterative process that requires a great deal of experience to achieve the desired result. It is a process of many compromises, and even experienced designers will produce different designs when presented with identical requirements. The iterative design process is not presented here for clarity.

The abbreviated design process is as follows:

- Select a core geometry suitable for the application. Constraints of height, footprint, mounting preference, and operating environment will affect the choice.
- Select suitable core material(s).
- Select the maximum flux density desired for operation.

- Select the core size. Core size is determined by the ability of the core structure to store the required energy, the number of turns that have to be wound, and the wire gauge needed. Often, the window area (the space used for the windings) and power loss determine the final core size. Flyback transformers' ability to store energy is the critical factor in determining the core size. The cross sectional area of the core and the length of the air gap in the magnetic path determine the energy storage capability.
- Determine the maximum desired flux density. Depending on the frequency of operation, the core material selected, and the operating environment, the allowed flux density must be determined. The allowed flux density is often difficult to determine initially. Usually the highest flux density that produces an acceptable design is used, but the winding geometry often dictates a larger core than is required based on flux density and energy storage calculations.
- Determine the number of primary turns.
- Determine the turns ratio.
- Select the wire gauge for each winding.
- Determine winding order and insulation requirements.
- Verify the design.

Input Power:

P_{OUT}/efficiency = 14.3W (use 15W)

Max ON time: $t_{ON(MAX)} = D_{MAX}/f_{SW} = 2.25\mu s$

Average input current: $I_{AVG(IN)} = P_{IN}/V_{IN(MIN)} = 0.42A$

Peak primary current (Equation 9):

$$I_{PPK} = \frac{2 \bullet I_{AVG(IN)}}{f_{SW} \bullet t_{ON(MAX)}} = 1.87 \quad A \tag{EQ. 9}$$

Maximum primary inductance (Equation 10):

$$Lp(max) = \frac{V_{IN(MIN)} \bullet t_{ON(MAX)}}{I_{PPK}} = 43.3 \quad \mu H \tag{EQ. 10}$$

Select 40µH for the primary inductance.

The core structure must be able to deliver a certain amount of energy to the secondary on each switching cycle in order to maintain the specified output power (Equation 11).

$$\Delta w = P_{OUT} \bullet \frac{\langle V_{OUT} + Vd \rangle}{f_{SW} \bullet V_{OUT}} \quad joules \tag{EQ. 11}$$

where Δw is the amount of energy required to be transferred each cycle and Vd is the drop across the output rectifier.

The capacity of a gapped ferrite core structure to store energy is dependent on the volume of the airgap and can be expressed in Equation 12:

$$Vg = Aeff \bullet lg = \frac{2 \bullet \mu_o \bullet \Delta w}{\Delta B^2} \quad m^3 \tag{EQ. 12}$$

where Aeff is the effective cross sectional area of the core in m^2, lg is the length of the airgap in meters, μ_o is the permeability of free space ($4\pi \bullet 10^{-7}$), and ΔB is the change in flux density in Tesla.

A core structure with less airgap volume than calculated cannot provide the full output power over some portion of its operating range. Conversely, if the length of the airgap becomes large, magnetic field fringing around the gap occurs. This increases the airgap volume. Some fringing is usually acceptable, but excessive fringing can cause increased losses in the windings around the gap, resulting in excessive heating. When a suitable core and gap combination are found, the iterative design cycle begins. Develop the design and check for ease of assembly and thermal performance.

If the core does not allow adequate space for the windings, a core with a larger window area is required. If the transformer runs hot, it may be necessary to lower the flux density (more primary turns, lower operating frequency), select a less lossy core material, change the geometry of the windings (winding order), use heavier gauge wire or multi-filar windings, and/or change the type of wire used (Litz wire, for example).

For simplicity, only the final design is further described.

An EPCOS EFD 20/10/7 core using N87 material gapped to an A_L value of 25nH/N^2 was chosen. It has more than the required air gap volume to store the energy required, but was needed for the window area it provides.

$Aeff = 31 \bullet 10^{-6} \quad m^2$

$lg = 1.56 \bullet 10^{-3} \quad m$

The flux density ΔB is only 0.069T or 690 gauss, a relatively low value.

Because Equation 13 shows the number of primary turns, N_p may be calculated.

(EQ. 13) $$L_p = \frac{\mu_o \bullet N_p^2 \bullet Aeff}{lg} \quad \mu H$$

The result is N_p = 40 turns. The secondary turns may be calculated as follows (Equation 14):

(EQ. 14) $$N_s \leq \frac{lg \bullet \langle Vout + Vd \rangle \bullet tr}{N_p \bullet Ippk \bullet \mu_o \bullet Aeff}$$

where tr is the time required to reset the core. Because discontinuous MMF mode operation is desired, the core must completely reset during the off time. To maintain Discontinuous mode operation, the maximum time allowed to reset the core is t_{sw} - $t_{ON(MAX)}$ where $t_{SW} = 1/f_{SW}$. The minimum time is application dependent and at the designers discretion, knowing that the secondary winding RMS current and ripple current stress in the output capacitors increases with decreasing reset time. The calculation for maximum N_s for the 3.3 V output using $t = t_{SW} - t_{ON\ (MAX)}$ = 2.75µs is 5.52 turns.

The number of secondary turns is also dependent on the number of outputs and the required turns ratios required to generate them. If Schottky output rectifiers are used and we assume a forward voltage drop of 0.45V, the required turns ratio for the two output voltages, 3.3V and 1.8V, is 5:3.

With a turns ratio of 5:3 for the secondary windings, we will use N_{s1} = 5 turns and N_{s2} = 3 turns. Checking the reset time using these values for the number of secondary turns yields a duration of Tr = 2.33µs, or about 47% of the switching period, an acceptable result.

The bias winding turns may be calculated similarly, except a diode forward drop of 0.7V is used. The rounded off result is 17 turns for a 12V bias.

The next step is to determine the wire gauge. Calculate the RMS current in the primary winding using Equation 15:

(EQ. 15) $$I_{P(RMS)} = I_{PPK} \bullet \sqrt{\frac{t_{ON(MAX)}}{3 \bullet t_{SW}}} \quad A$$

Calculate the peak and RMS current values in the remaining windings using Equations 16 and 17:

(EQ. 16) $$I_{SPK} = \frac{2 \bullet I_{OUT} \bullet t_{SW}}{Tr} \quad A$$

(EQ. 17) $$I_{RMS} = 2 \bullet I_{OUT} \bullet \sqrt{\frac{t_{SW}}{3 \bullet Tr}} \quad A$$

The RMS currents are:

• Primary winding: 0.72A

• 3.3V output: 4.23A

• 1.8V output: 1.69A

• Bias winding: 85mA.

To minimize the transformer leakage inductance, the primary winding is split into two sections connected in parallel and positioned so that the other windings are sandwiched between them. The output windings are configured so that the 1.8V winding is a tap off of the 3.3V winding. Tapping the 1.8V output requires that the shared portion of the secondary conduct the combined current of both outputs. The secondary wire gauge must be selected accordingly.

The determination of wire current carrying capacity is a compromise between performance, size, and cost. It is affected by many design constraints such as operating frequency (harmonic content of the waveform) and the winding proximity/geometry. It generally ranges between 250 and 1000 circular mils per ampere. A circular mil is defined as the area of a circle 0.001” (1 mil) in diameter. As the frequency of operation increases, the AC resistance of the wire increases due to skin and proximity effects. Using heavier gauge wire may not alleviate the problem. Instead multiple strands of wire in parallel must be used. In some cases, Litz wire is required.

The winding configuration selected is:

Primary #1: 40T, 2 #30 bifilar

Secondary: 5T, 0.003” (3 mil) copper foil tapped at 3T

Bias: 17T #32

Primary #2: 40T, 2 #30 bifilar

The internal spacing and insulation system is designed for 1500VDC dielectric withstand rating between the primary and secondary windings.

5.4 Selecting Power MOSFETs

Selecting the main switching MOSFET requires consideration of the voltage and current stresses in the application, the power dissipated by the device, its size, and its cost.

The converter’s input voltage range is 36VDC to 75VDC. This suggests a MOSFET with a voltage rating of 150V is required due to the flyback voltage likely to be seen on the primary of the isolation transformer.

The losses associated with MOSFET operation are divided into three categories: conduction, switching, and gate drive.

The conduction losses are due to the MOSFET’s ON-resistance (Equation 18).

$$Pcond = r_{DS(ON)} \bullet Iprms^2 \quad W \tag{EQ. 18}$$

where $r_{DS(ON)}$ is the ON-resistance of the MOSFET and Iprms is the RMS primary current. Determining the conduction losses is complicated by the variation of $r_{DS(ON)}$ with temperature. As junction temperature increases, so does $r_{DS(ON)}$, which increases losses and raises the junction temperature more, and so on. It is possible for the device to enter a thermal runaway situation without proper heatsinking. Generally, doubling the +25°C $r_{DS(ON)}$ specification yields a reasonable value for estimating the conduction losses at +125°C junction temperature.

The switching losses have two components: capacitive switching losses and voltage/current overlap losses. The capacitive losses occur during device turn-on and can be calculated in Equation 19:

$$Pswcap = \frac{1}{2} \bullet Cfet \bullet Vin^2 \bullet f_{SW} \quad W \tag{EQ. 19}$$

where Cfet is the equivalent output capacitance of the MOSFET. Device output capacitance is specified on datasheets as Coss and is non-linear with applied voltage. To find the equivalent discrete capacitance, Cfet, a

charge model is used. Using a known current source, the time required to charge the MOSFET drain to the desired operating voltage is determined and the equivalent capacitance may be calculated in Equation 20:

$$Cfet = \frac{Ichg \bullet t}{V} \quad F \tag{EQ. 20}$$

The other component of the switching loss is due to the overlap of voltage and current during the switching transition. A switching transition occurs when the MOSFET is in the process of either turning on or off. Because the load is inductive, no voltage and current overlap occurs during the turn on transition, so only the turn off transition is of significance. The power dissipation can be estimated using Equation 21:

$$P_{sw} \approx \frac{1}{x} \bullet I_{PPK} \bullet V_{IN} \bullet t_{OL} \bullet f_{SW} \tag{EQ. 21}$$

where t_{OL} is the duration of the overlap period and x ranges from about 3 through 6 in typical applications and depends on where the waveforms intersect. This estimate may predict higher dissipation than is realized because a portion of the turn off drain current is attributable to the charging of the device output capacitance (Coss) and is not dissipative during this portion of the switching cycle (Figure 8).

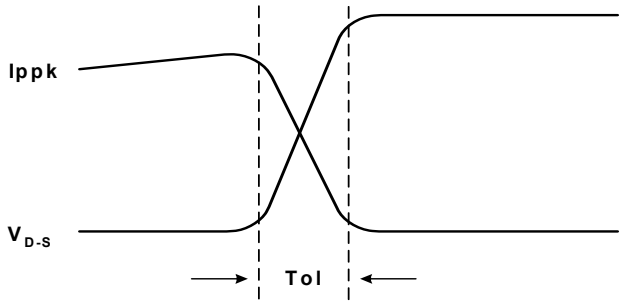


Figure 8. Switching Cycle

The final component of MOSFET loss is caused by the charging of the gate capacitance through the device gate resistance. Depending on the relative value of any external resistance in the gate drive circuit, a portion of this power will be dissipated externally (Equation 22).

$$Pgate = Qg \bullet Vg \bullet f_{SW} \quad W \tag{EQ. 22}$$

When the losses are known, select the device package and design the heatsinking method. Because the design requires a small surface mount part, an 8 Ld SOIC package was selected. A Fairchild FDS2570 MOSFET was selected based on these criteria. The overall losses are estimated at 400mW.

5.5 Output Filter Design

In a Flyback design, the primary concern for the design of the output filter is the capacitor ripple current stress and the ripple and noise specification of the output.

The current flowing in and out of the output capacitors is the difference between the winding current and the output current. The peak secondary current, I_{SPK}, is 10.73A for the 3.3V output and 4.29A for the 1.8V output. The current flowing into the output filter capacitor is the difference between the winding current and the output current. The 3.3V output's peak winding current is I_{SPK} = 10.73A. The capacitor must store this amount minus the output current of 2.5A, or 8.23A. The RMS ripple current in the 3.3V output capacitor is about $3.5A_{RMS}$. The RMS ripple current in the 1.8V output capacitor is about $1.4A_{RMS}$.

Voltage deviation on the output during the switching cycle (ripple and noise) is caused by the change in charge of the output capacitance, the Equivalent Series Resistance (ESR), and Equivalent Series Inductance (ESL). Assign a portion of the total ripple and noise specification to each of these components. The amount to allow for each contributor is dependent on the capacitor technology used.

For purposes of this discussion, assume the following:

3.3V output: 100mV total output ripple and noise

ESR: 60mV

Capacitor ΔQ: 10mV

ESL: 30mV

1.8V output: 50mV total output ripple and noise

ESR: 30mV

Capacitor ΔQ: 5mV

ESL: 15mV

For the 3.3V output (Equation 23):

(EQ. 23) $$ESR \leq \frac{\Delta V}{I_{SPK} - I_{OUT}} = \frac{0.060}{10.73 - 2.5} = 7.3m\Omega$$

The change in voltage due to the change in charge of the output capacitor, ΔQ, determines how much capacitance is required on the output (Equation 24).

(EQ. 24) $$C \geq \frac{(I_{SPK} - I_{OUT}) \bullet tr}{2 \bullet \Delta V} = \frac{(10.73 - 2.5) \bullet 2.33 \times 10^{-6}}{2 \bullet 0.010} = 960\mu F$$

ESL adds to the ripple and noise voltage in proportion to the rate of change of current into the capacitor (V = L • di/dt) (Equation 25).

(EQ. 25) $$L \leq \frac{V \bullet dt}{di} = \frac{0.030 \bullet 200 \times 10^{-9}}{10.73} = 0.56nH$$

High capacitance capacitors usually do not have sufficiently low ESL. High frequency capacitors such as surface mount ceramic or film are connected in parallel with the high capacitance capacitors to address the effects of ESL. A combination of high frequency and high ripple capability capacitors is used to achieve the desired overall performance. The analysis of the 1.8V output is similar to that of the 3.3V output and is omitted for brevity. Two OSCON 4SEP560M (560µF) electrolytic capacitors and a 22µF X5R ceramic 1210 capacitor were selected for both the 3.3 and 1.8V outputs. The 4SEP560M electrolytic capacitors are each rated at 4520mA ripple current and 13mΩ of ESR. The ripple current rating of just one of these capacitors is adequate, but two are needed to meet the minimum ESR and capacitance values.

The bias output is of such low power and current that it places negligible stress on its filter capacitor. A single 0.1µF ceramic capacitor was selected.

5.6 Control Loop Design

The major components of the feedback control loop are a programmable shunt regulator, an opto-coupler, and the ISL6721A's inverting amplifier. The opto-coupler transfers the error signal across the isolation barrier. The opto-coupler is a convenient way to cross the isolation barrier, but it adds complexity to the feedback control loop. It adds a pole at about 10kHz and a significant amount of gain variation due the Current Transfer Ratio (CTR). The of the opto-coupler CTR varies with initial tolerance, temperature, forward current, and age.

Figure 9 shows a block diagram of the feedback control loop.

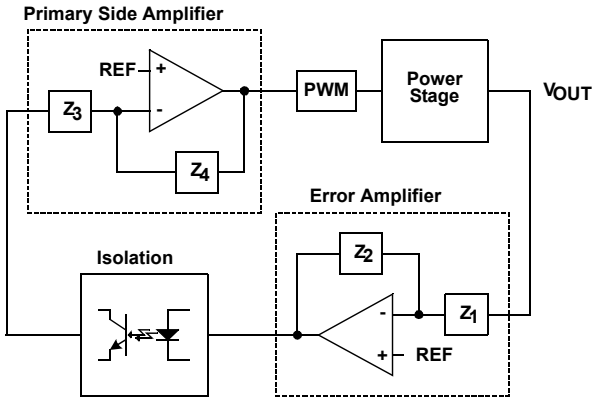


Figure 9. Feedback Control Loop

The loop compensation is placed around the Error Amplifier (EA) on the secondary side of the converter. The primary side amplifier located in the control IC is used as a unity gain inverting amplifier and provides no loop compensation. A Type 2 error amplifier configuration was selected as a precaution if operation in continuous mode occurs at some operating point (Figure 10).

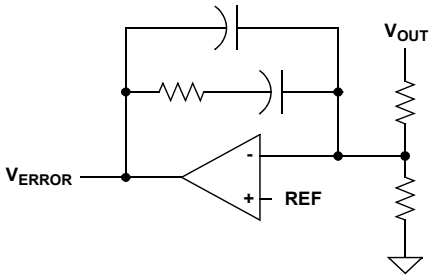


Figure 10. Type 2 Error Amplifier

Development of a small signal model for current mode control is rather complex. The reference method[1] was selected for its ability to accurately predict loop behavior. To further simplify the analysis, the converter will be modeled as a single output supply with all of the output capacitance reflected to the 3.3V output. When the "single" output system is compensated, adjustments to the compensation are required based on actual loop measurements.

The first parameter to determine is the peak current feedback loop gain. Because this application is low power, a resistor in series with the source of the power switching MOSFET is used for the current feedback signal. For higher power applications, a resistor dissipates too much power and a current transformer would be used instead.

Current loop behavior can be difficult to adjust due to the need to provide overcurrent protection. Current limit and current loop gain are determined by the current sense resistor and the ISET threshold. ISET was set at 1.0V, near its maximum, to minimize noise effects. When determining ISET, account for the internal gain and offset of the ISENSE signal in the control IC. The maximum peak primary current was determined earlier to be 1.87A, so a choice of 2.25A peak primary current for current limit is reasonable. A current gain, A_{EXT}, of 0.5V/A was selected to achieve this (Equation 26).

(EQ. 26) $$ISET = 2.25 \bullet 0.8 \bullet 0.5 + 0.100 = 1.00 \quad V$$

Equation 26 represents the control to output transfer function:

(EQ. 27) $$\frac{v_o}{v_c} = K \bullet \sqrt{\frac{R_o \bullet L_s \bullet f_{SW}}{2}} \bullet \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

If we ignore the current feedback sampled-data effects, the value of K can be determined by assuming all of the output power is delivered by the 3.3V output at the threshold of current limit (Equations 28 through 35):

(EQ. 28) $$K = \frac{I_{spk(max)}}{V_{c(max)}}$$

(EQ. 29) R_o = Load Resistance

(EQ. 30) L_s = Secondary Inductance

(EQ. 31) $$\omega_p = \frac{2}{R_o \bullet C_o} \quad \text{or} \quad f_p = \frac{1}{\pi \bullet R_o \bullet C_o}$$

(EQ. 32) $$\omega_z = \frac{1}{R_c \bullet C_o} \quad \text{or} \quad f_z = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_o}$$

(EQ. 33) C_o = Output Capacitance

(EQ. 34) R_c = Output Capacitor ESR

(EQ. 35) $V_{c(max)}$ = Control Voltage Range

The maximum power allowed was determined earlier as 15W, therefore (Equations 36 and 37):

(EQ. 36) $$I_{SPK(max)} = \frac{2 \bullet \frac{P_{OUT}}{V_{OUT}} \bullet t_{SW}}{tr} = \frac{2 \bullet \frac{15}{3.3} \bullet 5 \times 10^{-6}}{2.33 \times 10^{-6}} = 19.5 \quad A$$

(EQ. 37) $$v_{c(max)} = V_{ISENSE} \bullet A_{EXT} \bullet A_{CS} \bullet \frac{1}{A_{COMP}} = 2.93 \quad V$$

where A_{EXT} is the external gain of the current feedback network, A_{CS} is the IC internal gain, and A_{COMP} is the gain between the error amplifier and the PWM comparator.

The Type 2 compensation configuration has two poles and one zero. The first pole is at the origin, and provides the integration characteristic which results in excellent DC regulation. Referring to the typical boost converter application schematic (Figure 2 on page 5), the remaining pole and zero for the compensator are located at (Equations 38 and 39):

(EQ. 38) $$f_{pc} = \frac{C_{13} + C_{14}}{2 \bullet \pi \bullet R_{15} \bullet C_{14} \bullet C_{13}} \approx \frac{1}{2 \bullet \pi \bullet R_{15} \bullet C_{14}}$$

(EQ. 39) $$f_{zc} = \frac{1}{2 \bullet \pi \bullet R_{15} \bullet C_{13}}$$

The ratio of R_{15} to the parallel combination of R_{17} and R_{18} determines the mid band gain of the error amplifier (Equation 40).

(EQ. 40) $$A_{midband} = \frac{R_{15} \bullet (R_{17} + R_{18})}{R_{17} \bullet R_{18}}$$

Equation 27 shows that the control to output transfer function frequency dependence is a function of the output load resistance, the value of output capacitance, and the output capacitor ESR. These variations must be considered when compensating the control loop. The worst case small signal operating point for the converter is at minimum V_{IN}, maximum load, maximum C_{OUT}, and minimum ESR.

The higher the desired bandwidth of the converter, the more difficult it is to create a solution that is stable over the entire operating range. A good standard is to limit the bandwidth to about $f_{SW}/4$. For this example, the bandwidth will

be further limited due to the low GBWP of the LM431-based Error Amplifier (EA) and the opto-coupler. A bandwidth of approximately 5kHz was selected.

For the EA compensation, the first pole is placed at the origin by default (C_{14} is an integrating capacitor). The first zero is placed below the crossover frequency, f_{co}, usually around 1/3 f_{co}. The second pole is placed at the lower of the ESR zero or at one half of the switching frequency. The midband gain is then adjusted to obtain the desired crossover frequency. If the phase margin is not adequate, the crossover frequency may have to be reduced.

Using this technique to determine the compensation, the following values for the EA components were selected.

$R_{17} = R_{18} = R_{15} = 1k\Omega$

R_{20} = open

$C_{13} = 100nF$

$C_{14} = 100pF$

Figures 11 and 12 show a Bode plot of the system at low line and max load.

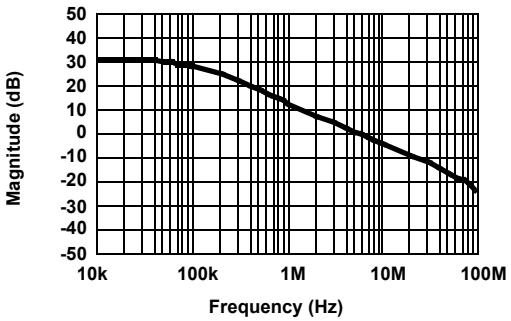


Figure 11. Magnitude

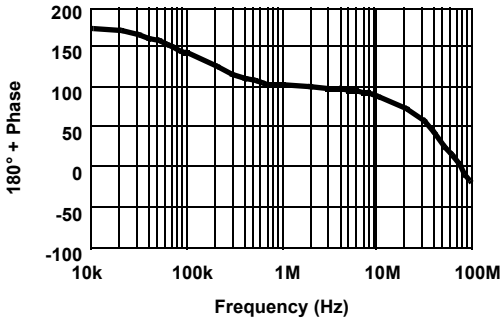


Figure 12. Phase

5.7 Regulation Performance

Table 2. Output Load Regulation, V_{IN} = 48V

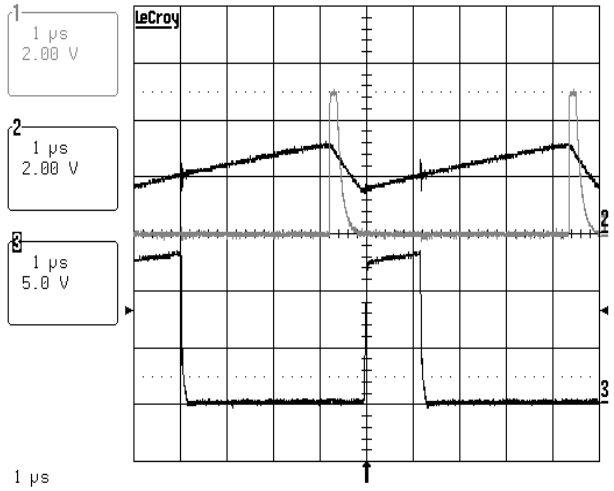
I_{OUT} (A), 3.3V	I_{OUT} (A), 1.8V	V_{OUT} (V), 3.3V	V_{OUT} (V), 1.8V
0	0.030	3.351	1.825
0.39	0.030	3.281	1.956
0.88	0.030	3.251	1.988
1.38	0.030	3.223	2.014
1.87	0.030	3.204	2.029
2.39	0.030	3.185	2.057
2.89	0030	3.168	2.084
3.37	0.030	3.153	2.103
0	0.52	3.471	1.497
0.39	0.52	3.283	1.800
0.88	0.52	3.254	1.836
1.38	0.52	3.233	1.848
1.87	0.52	3.218	1.855
2.39	0.52	3.203	1.859
2.89	0.52	3.191	1.862
0	1.05	3.619	1.347

Table 2. Output Load Regulation, V_{IN} = 48V (Continued)

I_{OUT} (A), 3.3V	I_{OUT} (A), 1.8V	V_{OUT} (V), 3.3V	V_{OUT} (V), 1.8V
0.39	1.05	3.290	1.730
0.88	1.05	3.254	1.785
1.38	1.05	3.235	1.805
1.87	1.05	3.220	1.814
2.39	1.05	3.207	1.820
0	1.55	3.699	1.265
0.39	1.55	3.306	1.682
0.88	1.55	3.260	1.750
1.38	1.55	3.239	1.776
1.87	1.55	3.224	1.789
0	2.07	3.762	1.201
0.39	2.07	3.329	1.645
0.88	2.07	3.270	1.722
1.38	2.07	3.245	1.752
0	2.62	3.819	1.142
0.39	2.62	3.355	1.612
0.88	2.62	3.282	1.697
0	3.14	3.869	1.091
0.39	3.14	3.383	1.581

5.8 Waveforms

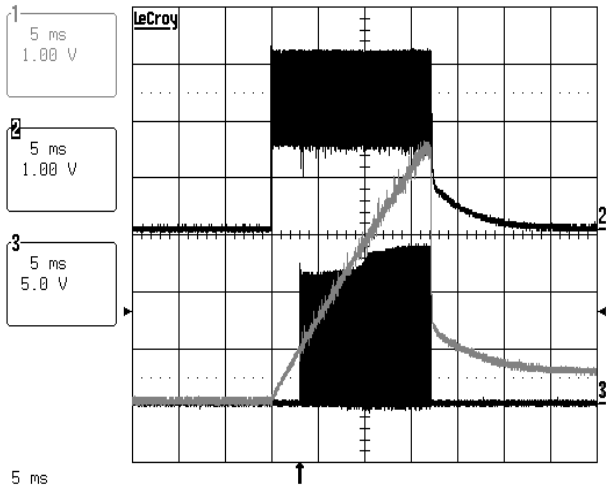
Figures 13 through 15 show typical waveforms. Figure 13 shows the steady state operation of the sawtooth oscillator waveform at RTCT (Trace 2), the SYNC output pulse (Trace 1), and the GATE output to the converter FET (Trace 3).



Note:
Trace 1: SYNC Output
Trace 2: RTCT Sawtooth
Trace 3: GATE Output

Figure 13. Typical Waveforms

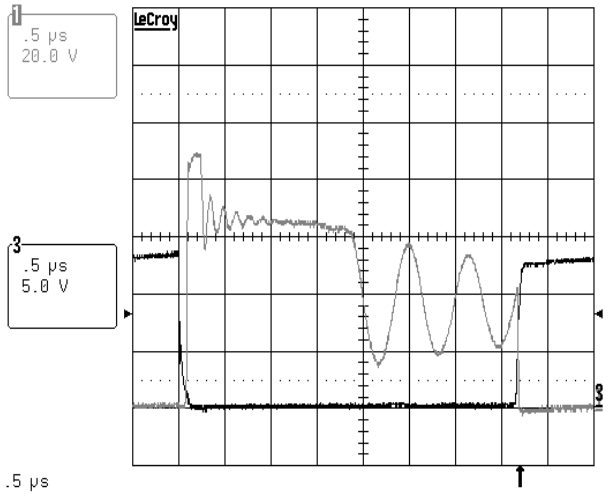
Figure 14 shows the converter behavior while operating in an overcurrent fault condition. Trace 1 is the soft-start voltage, which increases from 0V to 4.5V, at which point the OC fault function is enabled. The OC condition is detected and the soft-start capacitor is discharged to the 4.375V OC fault threshold at which point the IC enters the fault shutdown mode. Trace 2 shows the behavior of the timing capacitor voltage during a shutdown fault. Most of the IC functions, including the oscillator, are de-powered during a fault. During a fault, the IC is turned off until the restart delay has timed out. After the delay, power is restored and the IC resumes normal operation. Trace 3 is the GATE output during the soft-start cycle and OC fault.



Note:
Trace 1: SS
Trace 2: RTCT Sawtooth
Trace 3: GATE Output

Figure 14. Soft-Start with Overcurrent Fault

Figure 15 shows the switching FET waveforms during steady state operation. Trace 1 is drain-source voltage and Trace 2 is gate-source voltage.



Note:
Trace 1: V_{D-S}
Trace 3: V_{G-S}

Figure 15. Gate and Drain-Source Waveforms

5.9 Component List

Reference Designator	Value	Description
C_1, C_2, C_3	1.0µF	Capacitor, 1812, X7R, 100V, 20%
C_5, C_{13}	0.1µF	Capacitor, 0603, X7R, 25V, 10%
C_{15}, C_{16}, C_{19}, C_{20}	560µF	Capacitor, Radial, SANYO 4SEP560M
C_{17}	470pF	Capacitor, 0603, COG, 50V, 5%
C_{18}	0.01µF	Capacitor, 0805, X7R, 50V, 10%
C_{21}, C_{22}	22µF	Capacitor, 1210, X5R, 10V, 20%
C_4, C_{14}	100pF	Capacitor, 0603, COG, 50V, 5%
C_6	1500pF	Capacitor, Disc, Murata DE1E3KX152MA5BA01
C_7		0Ω Jumper, 0603
C_8	330pF	Capacitor, 0603, COG, 50V, 5%
C_9, C_{10}, C_{11}, C_{12}	0.22µF	Capacitor, 0603, X7R, 16V, 10%
C_{R2}, C_{R6}		Diode, Fairchild ES1C
C_{R4}, C_{R5}		Diode, IR 12CWQ03FN
D_1		Zener, 18V, Zetex BZX84C18
D_2		Diode, Schottky, BAT54C
Q_1		FET, Fairchild FDS2570
Q_2		Transistor, Zetex FMMT491A
Q_3		Transistor, ON MJD31C
R_1, R_2	1.00k	Resistor, 1206, 1%
R_{10}	20.0k	Resistor, 0603, 1%

Reference Designator	Value	Description
R_7, R_9, R_{11}, R_{26}, R_{27}	10.0k	Resistor, 0603, 1%
R_{12}	38.3k	Resistor, 0603, 1%
R_{13}, R_{15}, R_{17}, R_{18}, R_{19}, R_{25}	1.00k	Resistor, 0603, 1%
R_{14}	10	Resistor, 0603, 1%
R_{16}	165	Resistor, 0603, 1%
R_{21}	10.0	Resistor, 1206, 1%
R_{22}	5.11	Resistor, 0603, 1%
R_{24}	3.92k	Resistor, 2512, 1%
R_3, R_{23}	100	Resistor, 0603, 1%
R_4	1.00	Resistor, 2512, 1%
R_5	221k	Resistor, 0603, 1%
R_6	75.0k	Resistor, 0603, 1%
R_8, R_{20}		OMIT
T_1		Transformer, MIDCOM 31555
U_2		Opto-coupler, NEC PS2801-1
U_3		Shunt Reference, National LM431BIM3
U_4		PWM, Renesas ISL6721A
V_{R1}		Zener, 15V, Zetex BZX84C15

5.10 References

(1) Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

(2) Dixon, Lloyd H., “Closing the Feedback Loop”, Unitrode Power Supply Design Seminar, SEM-700, 1990.

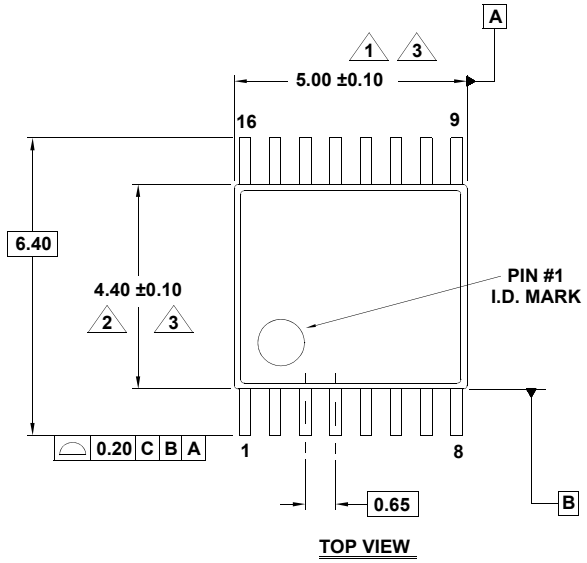
6. Revision History

Rev.	Date	Description
1.00	Jul 24, 2018	Applied new formatting and layout. Changed Feature bullet from “Adjustable overcurrent shutdown delay” to “Adjustable overcurrent shutdown threshold” on page 1. Added tape and reel column and updated Note 1 in Ordering Information table on page 7. Added Table 1 (Key Differences Between Family of Parts) on page 7. Updated the SYNC, UV, and ISENSE pin descriptions and moved to page 8. Removed the word “period” from the Input Frequency Range Max value on page 12. Changed the titles and y axis labels of Figures 11 and 12 from GAIN and PHASE MARGIN to Magnitude and Phase, respectively, on page 26. Added Revision History.

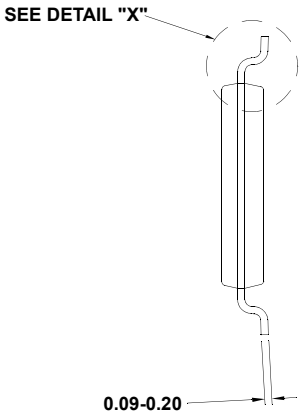
7. Package Outline Drawings

For the most recent package outline drawing, see M16.173.

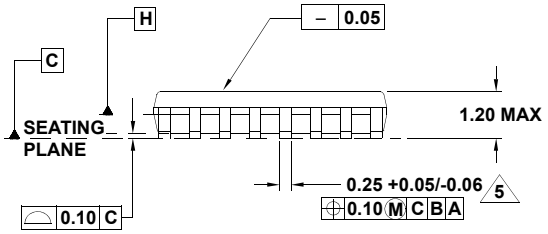
M16.173
16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 2, 5/10



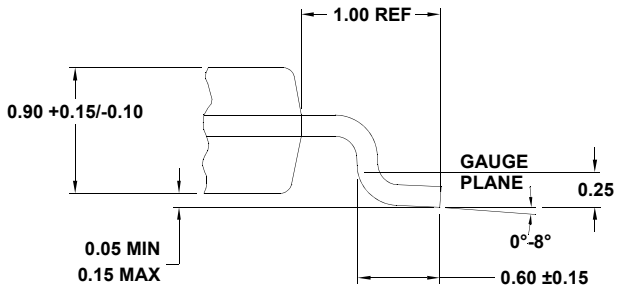
TOP VIEW



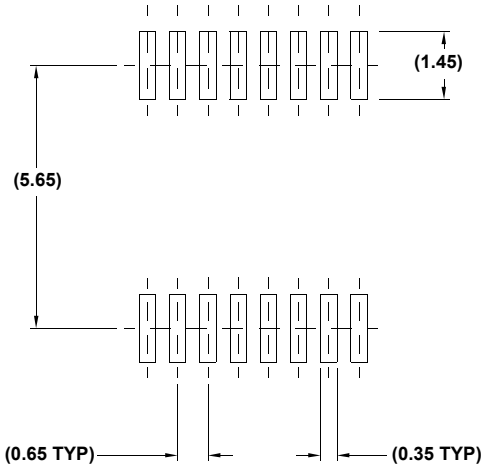
END VIEW



SIDE VIEW



DETAIL "X"



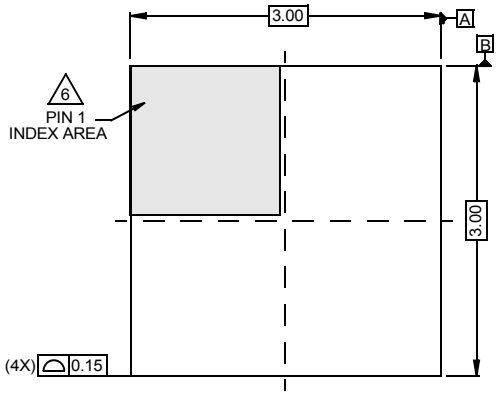
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

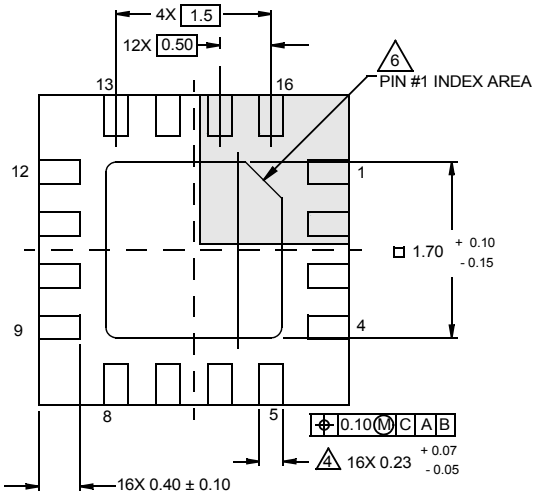
1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

L16.3x3B
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/07

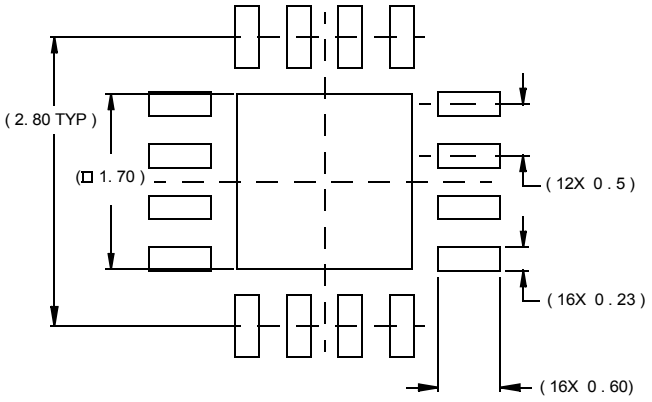
For the most recent package outline drawing, see L16.3x3B.



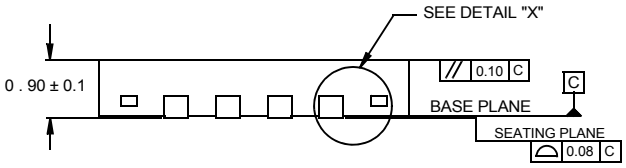
TOP VIEW



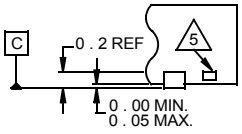
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.