ISL6745EVAL1Z 48V to 12V 120W Half-Bridge Power Supply for Telecom Applications

Application Note | November 5, 2008 | AN1439.0

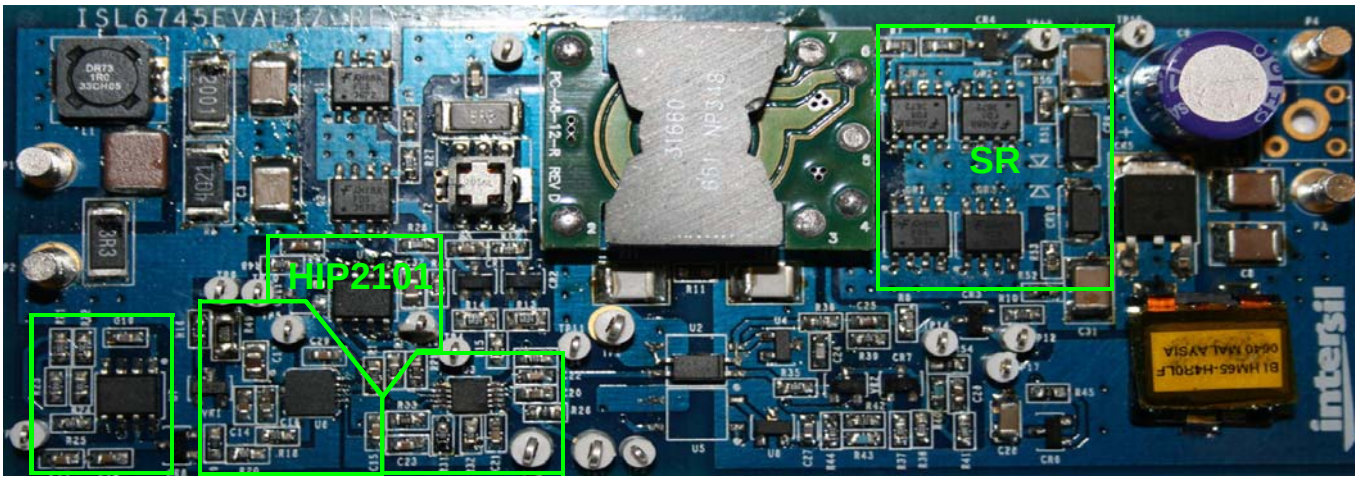

FIGURE 1. TOP VIEW OF THE ISL6745EVAL1Z EVALUATION BOARD

The ISL6745EVAL1Z evaluation board utilizes Intersil's double-ended voltage-mode PWM controller ISL6745A for half bridge converters with secondary side synchronous rectification. The voltage mode PWM controller ISL6745 is a 10 Ld MSOP device. The input of the evaluation board ranges from 36V to 75V, and the output voltage is regulated to 12V with a maximum load current of 10A. Planar transformers and inductors are used. The triple-output linear regulator ISL6720 is used to provide bias for the primary side controller and drivers. The main specifications are given in the following:

- Input voltage: 36V ~ 75V
- Output voltage: 12V
- Output power: 120W
- Output voltage ripple: 50mV
- Efficiency: about 90% at full load rated input voltage

This application note will give a brief introduction on the operation of the converter, the design constraints, the description of the evaluation board and the performance validation. Figure 1 shows the top view of the evaluation board.

Introduction

Half-bridge voltage mode converters are widely used in telecommunication systems as an isolated power supply of medium power level because of their simplicity and good performance. Compared with single-ended topologies, such as forward and flyback converters, the voltage stress over the primary switches of the half-bridge is the smallest. The gate driver is also simple. The two switches in the primary side of the transformer can be driven by a symmetrical PWM or asymmetrical PWM, as shown in Figure 2. In a symmetrical PWM scheme, both switches are driven with the same duty ratio and have a deadtime period when both switches are off. The two switches in the primary side are hard-switched and their switching loss will be significant. During this deadtime interval, the synchronous rectification switches in the secondary side are both turned on, which helps to reduce the conduction loss of the SR switches. These features make half-bridge voltage mode converters attractive and cost-effective for low frequency, high current applications.

The center-tapped rectification in the secondary side offers some additional advantages. First, the center-tapped structure has twice the frequency than that of the switching frequency. Therefore, the output filter size is smaller compared with converters with the forward structure (such as in an active clamp forward, or flyback). Second, the synchronous rectifier FETs are driven by the voltages from the auxiliary windings, which ensures that both switches are on during such deadtime intervals. The conduction loss in the switches of the center-tapped rectifier is the product of only half of the load current during the deadtime period. Thus, the overall conduction loss is smaller.

The ISL6745 is a simplified vision of the ISL6742, which supports the symmetrical PWM of the half-bridge converters with peak current limit and soft-start functions. The simplified circuit schematic of a half bridge converter with diode rectification in the secondary side is shown in Figure 2A The the typical current and voltage waveforms is shown in Figure 2B.

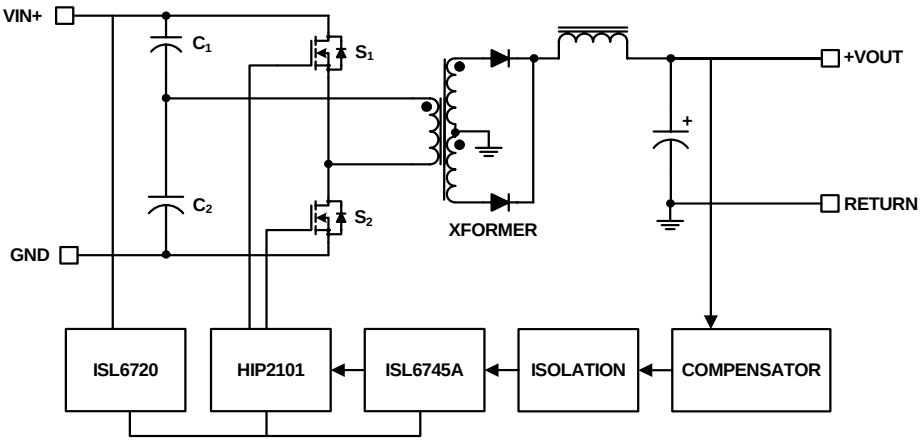

FIGURE 2A. SCHEMATICS BLOCK DIAGRAM

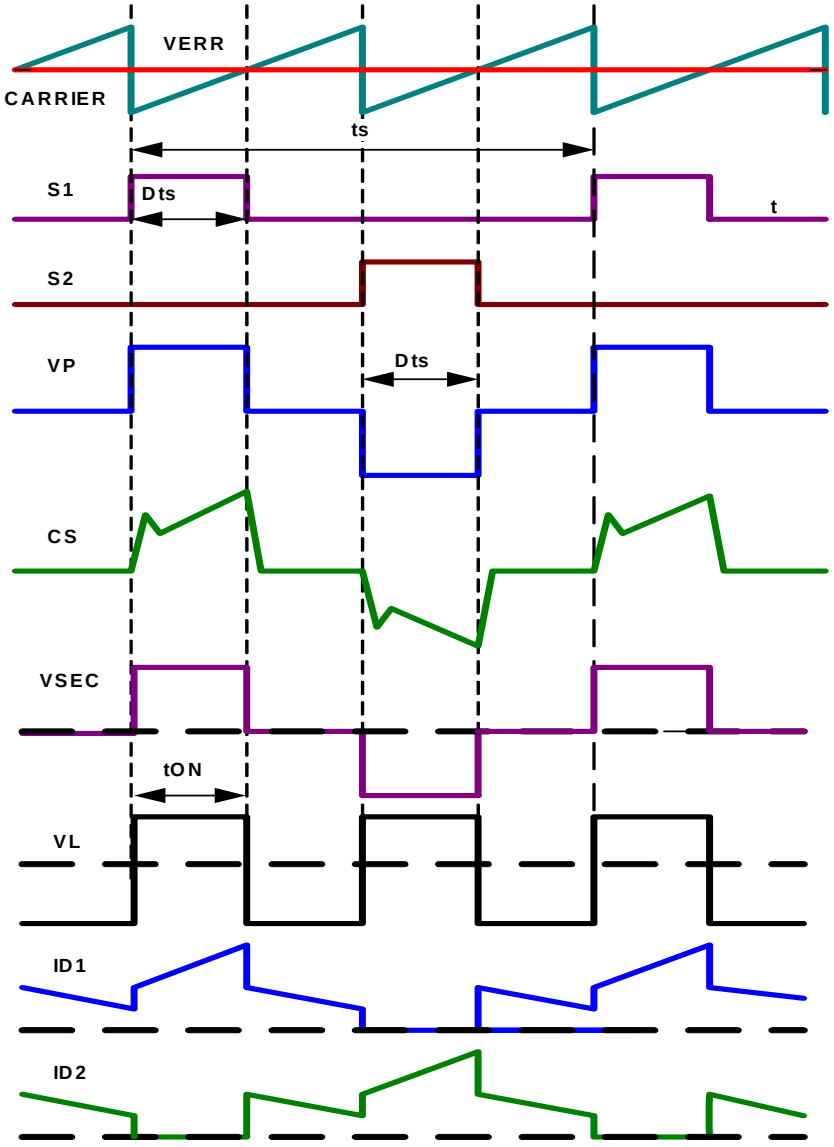

FIGURE 2B. SHB CONVERTER WAVEFORM

FIGURE 2. THE SYMMETRICAL PWM HALF BRIDGE CONVERTER PWM PATTERNS, AND SECONDARY SIDE RECTIFICATIONS

Design Criteria

The following specifies the design requirements:

- Switching Frequency, f_{SW}: 235kHz
- V_{IN}: 48V, Min 36V, Max 75V
- V_{OUT}: 12V (nominal) @ I_{OUT} = 8A
- P_{OUT}: 100W
- Efficiency: 85% ~ 90%
- Ripple: 1%

Power Stage Design Procedure

A symmetrical half-bridge (SHB) converter topology with secondary side central-tape SR is selected for this application. The ISL6745 is used as the PWM controller and HIP2101 is used as FET driver.

The relation of the input voltage V_{IN} and output voltage V_{OUT} is given in Equation 1, where D is the duty ratio and N is the transformer turns ratio (N = Ns/Np).

$$V_{OUT} = 2NDV_{IN} \quad \text{(EQ. 1)}$$

According to Equation 1, N should be large enough to ensure the rated output at low line operation. Consider the input range for typical telecommunication applications; the minimum input voltage is 36V. Allowing for some deadtime, a transformer of N = 3/4 can be used. Detailed design of the planar transformer is given in the Intersil Data Sheet “ISL6740, ISL6741: Flexible Double Ended Voltage and Current Mode PWM Controllers,” which can be found at: http://www.intersil.com/data/fn/fn9111.pdf

The criteria for selection of the primary side half-bridge FETs and the secondary side synchronous rectifier FETs is largely based on the current and voltage rating of the device. However, the FET drain-source capacitance and gate charge cannot be ignored. The gate charge affects the switching speed of the FETs. Higher gate charge translates into higher drive requirements and/or slower switching speeds. The energy required to drive the gates is dissipated as heat. The FET drain-source capacitance contributes to the switching losses in the SHB, since this portion of energy is not recycled, as in a soft-switched or zero-voltage switched converter.

The maximum input voltage, V_{IN}, plus transient voltage, determines the voltage rating required. For the symmetrical half-bridge converter, the voltage across the two primary side MOSFETs is half of the input voltage at steady state. That is, $V_P = 0.5V_{IN}$. The secondary side SR FET voltage stress is twice the transformer second side voltage and is expressed in Equation 2:

$$V_S = 2 \bullet 0.5NV_{IN} = NV_{IN} \quad \text{(EQ. 2)}$$

For this application, if we allow a 20% adder for transients with a maximum input voltage of 75V, a voltage rating of 100V or higher will suffice.

The average output current Iout is evenly distributed in the two MOSFETs in the (1 - 2D) interval. As both of the MOSFETs in the primary side are turned off, the load current is supposed to flow evenly in the two SRs, assuming the gate signals are applied. Therefore, the RMS current in each of the SRs is given in Equation 3, where 0 < D < 0.5.

$$\begin{aligned} I_{sR1rms} &= \sqrt{\frac{1}{Ts}\int_0^{ts}(ISR1)^2 dt} \\ &= \sqrt{\frac{1}{ts}\left\{\int_{Dts}^{[0.5-D]ts}(0.5I_{OUT})^2 dt + \int_0^{Dts}(I_{OUT})^2 d(t)\right\}} \\ &= I_{OUT}\sqrt{0.75D + 0.125} \end{aligned} \quad \text{(EQ. 3)}$$

From Equation 3, the conduction loss of the SR can be evaluated according to Equation 4:

$$PSr_{ON} = 2r_{DS(ON)}I_{RMS}^2 = 2r_{DS(ON)}(0.75D + 0.125)I_{OUT}^2 \quad \text{(EQ. 4)}$$

In order to avoid the hard turn-on of the SR, a delay resistor is needed to create the delay of the gate signal, so that the current first flows into the anti-parallel diode of the SRs. A diode is placed in parallel with the delay resistor in order to speed up the turn-off of the SRs and avoid shoot-through.

The gate drive loss of the SRs are a function of the switching frequency, driving voltage and Q, as expressed in Equation 5.

$$P_{GATE} = C_{GATE}V^2 fs \quad \text{(EQ. 5)}$$

When the primary switch is turned on, it conducts the output inductor current. The primary switch does not conduct current when it is turned off. Therefore, the RMS current in the primary switch is evaluated in Equation 6.

$$\begin{aligned} I_{PRMS} &= \sqrt{\frac{1}{ts}\int_0^{ts}(ISR1)^2 dt} \\ &= \sqrt{\frac{1}{ts}\left\{\int_0^{Dts}(NI_{OUT})^2 d(t)\right\}} = I_{OUT}N\sqrt{D} \end{aligned} \quad \text{(EQ. 6)}$$

The conduction loss of the primary switches can be estimated using Equation 7:

$$PPr_{ON} = 2r_{DS(ON)}I_{PRMS}2 = 2r_{DS(ON)}D(NI_{OUT})^2 \quad \text{(EQ. 7)}$$

The switching loss of the primary side MOSFET consists of two parts: 1) the overlap of the current and voltage and, 2) the discharge of the charges of the drain-source capacitance of the FET. The switching loss can be estimated using Equation 8:

$$PPr_{SW} = 2I_{PR}V_{FS} \quad \text{(EQ. 8)}$$

Therefore, the total loss that occurred in the switches can be estimated using Equation 9:

$$P_{LOSS} = PSr_{ON} + P_{GATE} + PPr_{SW} + PPr_{ON} \quad \text{(EQ. 9)}$$

Fairchild FDS3672 FETs, rated at 100V and 7.5A ($r_{DS}(ON)$ = 22m), were selected for the half-bridge switches. The synchronous rectifier FETs must withstand approximately 75% of the input voltage assuming no switching transients are present. A device capable of withstanding at least 55V is required. Empirical testing in the circuit revealed switching transients of 20V were present across the device indicating that a rating of at least 75V is required. The RMS current rating of 7.07A for each SR FET requires a low $r_{DS}(ON)$ to minimize conduction losses. It was decided to use two devices in parallel to simplify the thermal design.

The voltage of the output inductor L is related to the secondary side voltage V_{SEC} and output voltage V_{OUT}.

$$V_L = V_{SEC} - V_{OUT} \quad \text{(EQ. 10)}$$

Therefore, the ripple current through the output inductor is given in Equation 11. The frequency of the ripple current is twice that of the switching frequency.

$$\Delta IL = \frac{NV_{IN}(1-2D)}{2LFS} \quad \text{(EQ. 11)}$$

Clearly, from the ripple current point-of-view, a large inductor is preferable. However, the current slew rate will be impaired. The inductor and output capacitor contributes one double pole at the resonant frequency of the filter, indicating a narrow bandwidth with a large inductor.

With a maximum input voltage of 75V, the minimum duty ratio D is about 0.25. If we allow an inductor current ripple of 5% of the rated output current, the minimum inductance required can be calculated according to Equation 12. Here, an inductor of 2µH is selected.

$$L > \frac{V_L \bullet t_{ON}}{\Delta IL} \quad \text{(EQ. 12)}$$

Under steady state operating conditions, the ripple current in the capacitor is small, so it would seem appropriate to have a low ripple current rated capacitor. However, a high rated ripple current capacitor was selected based on the nature of the intended load and multiple buck regulators. In order to minimize the output impedance of the filter, a Sanyo OSCON 16SH150M capacitor was placed in parallel with a 22µF ceramic capacitor.

Control Stage Design Procedure

The ISL6745EVAL1Z demonstration platform implements a feedback control by means of the opto-coupler and Type 3 Error Amplifier. The system block diagram is shown in Figure 3. SHB is the symmetrical half-bridge converter consisting of the primary switches, transformer and the output filter. PWM is the voltage-mode pulse width modulator. The opto-coupler is used to transfer the error signal across the isolation barrier. The major components of the feedback control loop are a programmable shunt regulator and an opto-coupler.The opto-coupler offers a convenient means to cross the isolation barrier, but it adds complexity to the feedback control loop. It adds a pole at about 10kHz and a significant amount of gain variation due to the current transfer ratio (CTR). The CTR of the opto-coupler varies with initial tolerance, temperature, forward current, and age.

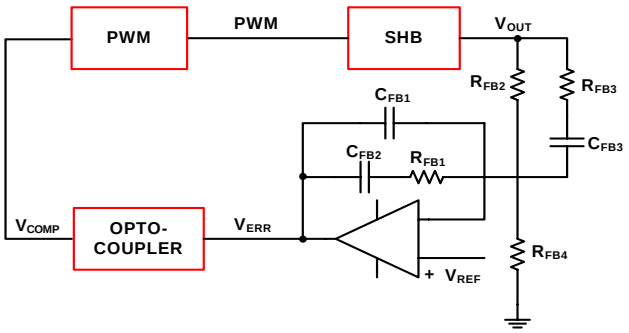

FIGURE 3. SYSTEM BLOCK DIAGRAM

From the small signal model of the half bridge converter, the control to output transfer function frequency dependence is a function of the output load resistance, the value of output capacitor and inductor, and the output capacitance ESR. These variations must be considered when compensating the control loop. The worst case small signal operating point for a voltage mode converter tends to be at maximum V_{IN}, maximum load, maximum C_{OUT}, and minimum ESR. The pole and zero of the transfer function are given in Equation 13.

$$G(s) = \frac{V_{OUT(S)}}{V_{C(S)}} = \frac{VN_S}{2N_P V_S} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2} \quad \text{(EQ. 13)}$$

where:

$$Q = (R_O)/(\omega_o L) \quad \text{(EQ. 14)}$$

$$\omega_o = 1/(\sqrt{(C_O L)}) \quad \text{(EQ. 15)}$$

$$\omega z = 1/(C_O R_C) \quad \text{(EQ. 16)}$$

R_O is the equivalent output load resistance

L is the output inductance

C_O is the output capacitor

R_C is the ESR of the output capacitor

V_S is the peak of the sawtooth ramp signal for PWM modulation.

The loop compensation is placed around the Error Amplifier (EA) on the secondary side of the converter. A Type 3 error

amplifier configuration was selected. The Type 3 compensation configuration has three poles and two zeros, and the configuration depends on the bandwidth requirement. The higher the desired bandwidth of the converter, the more difficult it is to create a solution that is stable over the entire operating range. A good rule of thumb is to limit the bandwidth to about $f_{SW}/4$, where f_{SW} is the switching frequency of the converter. However, due to the bandwidth constraints of the opto-coupler and the LM431 shunt regulator, the bandwidth was reduced to about 25kHz.

The first pole is placed at the origin by default (C_{20} is an integrating capacitor) which results in excellent DC regulation. If the two zeroes are placed at the same frequency, they should be placed at $f_{LC}/2$, where f_{LC} is the resonant frequency of the output L-C filter. To reduce the gain peaking at the L-C resonant frequency, the two zeroes are often separated. When they are separated, the first zero can be placed at $f_{LC}/5$, and the second at just above f_{LC}. The second pole is placed at the lowest expected zero cause by the output capacitor ESR. The third, and last pole is placed at about 1.5 times the crossover frequency. Some liberties where taken with the generally accepted compensation procedure previously described due to the transfer characteristics of the opto-coupler. The effects of the opto-coupler tend to dominate over those of the LM431 so the GBWP effects of the LM431 are not included here.

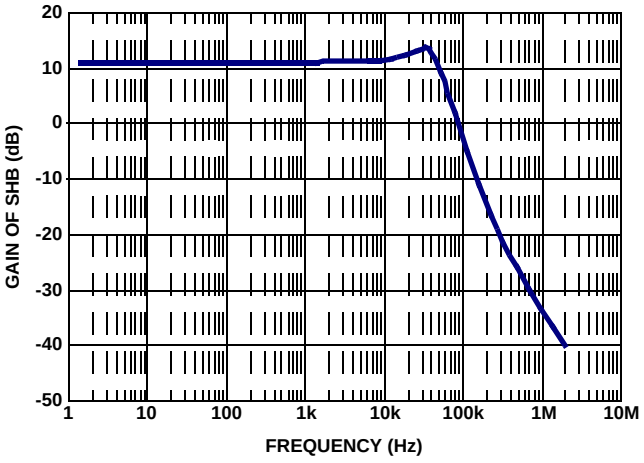

FIGURE 4. THE CONTROL TO OUTPUT GAIN OF THE SHB

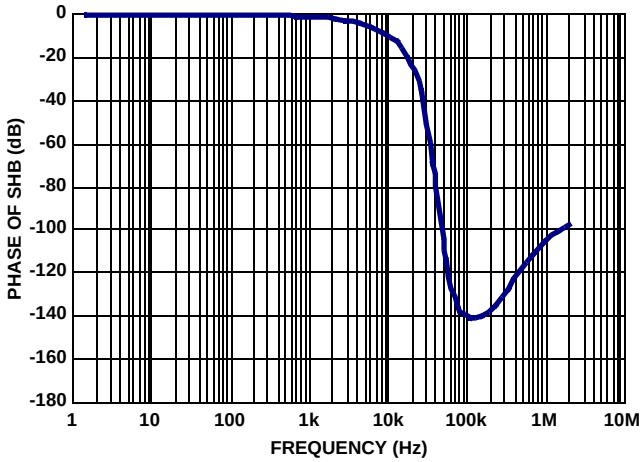

FIGURE 5. THE CONTROL TO OUTPUT PHASE OF THE SHB

Referring to the circuit block diagram, the transfer function of the Type 3 can be expressed in Equation 17:

$$G_{EA(S)} = \frac{V_{ERR(S)}}{V_{O(S)}} = \frac{(1 + sC_{FB2}R_{FB1})(1 + sC_{FB3}(R_{FB2} + R_{FB3}))}{s(C_{FB1} + C_{FB2})R_{FB2})(1 + sC_{FB3}R_{FB3})\left(1 + s\frac{C_{FB1}C_{FB2}R_{FB1}}{C_{FB1} + C_{FB2}}\right)} \quad \text{(EQ. 17)}$$

If $R_{FB2} >> R_{FB3}$, $C_{FB2} >> C_{FB1}$, the transfer function in Equation 17 can be reduced to the following:

$$G_{EA(S)} = \frac{V_{ERR(S)}}{V_{O(S)}} = \frac{(1 + sC_{FB2}R_{FB1})(1 + sC_{FB3}R_{FB2})}{sC_{FB1}R_{FB2}(1 + sC_{FB3}R_{FB3})(1 + R_{FB1}C_{FB1})} \quad \text{(EQ. 18)}$$

Then the poles and zeros can be determined with the Equations 19 through 22.

$$\omega p2 = \frac{1}{(C_{FB1}R_{FB1})} \quad \text{(EQ. 19)}$$

$$\omega P3 = \frac{1}{(C_{FB3}R_{FB3})} \quad \text{(EQ. 20)}$$

$$\omega z2 = \frac{1}{(C_{FB3}R_{FB2})} \quad \text{(EQ. 21)}$$

$$\omega z1 = \frac{1}{(C_{FB2}R_{FB1})} \quad \text{(EQ. 22)}$$

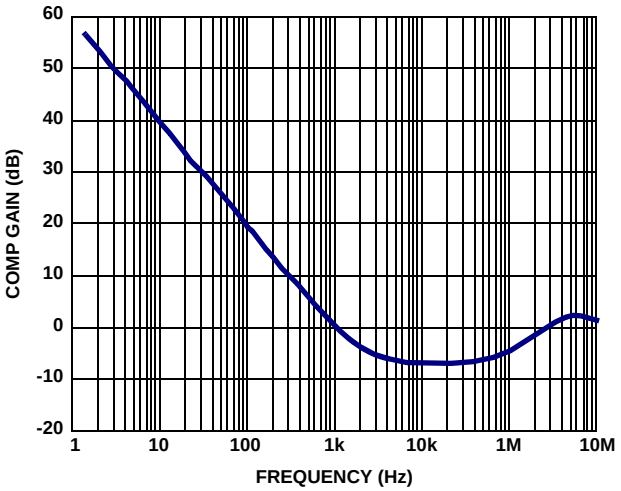

FIGURE 6. TYPE 3 ERROR AMPLIFIER (EA-3)

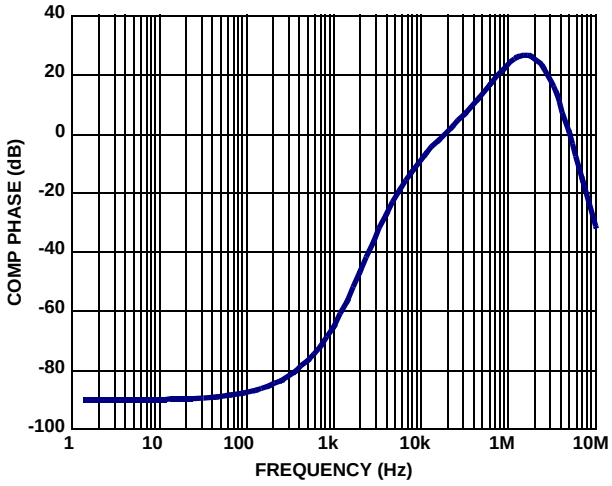

FIGURE 7. TYPE 3 ERROR AAMPLIFIER (EA-3)

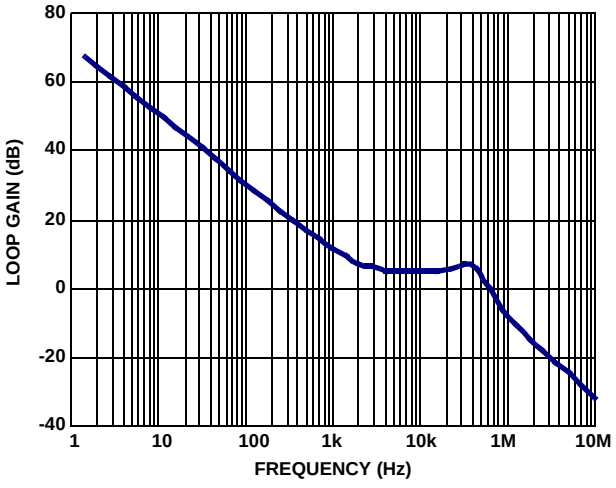

FIGURE 8. LOOP GAIN MARGIN

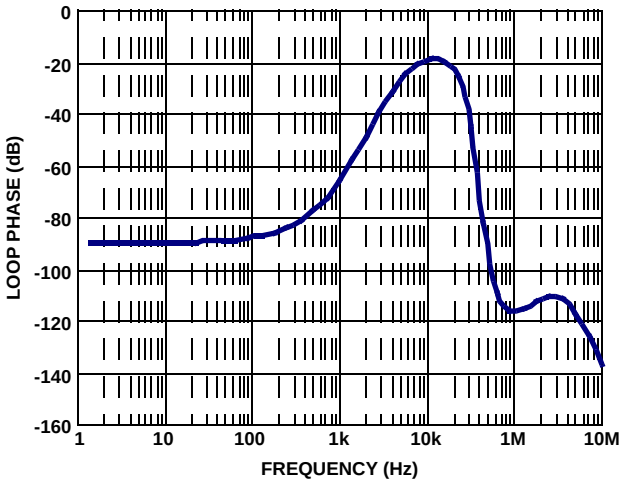

FIGURE 9. LOOP PHASE MARGIN

The loop transfer function Bode plots are given in Figures 8 and 9 for full load rated input voltage. Checking these plots, one will notice that the design gives 90° of phase margin and more than 40dB of gain margin.

Evaluation Board and Performance

The ISL6745EVAL1Z evaluation board is a 4-layer, 4.55”x1.87” RoHS compliant board. All the components are assembled in the top layer. The bill of materials, schematic, and waveforms are given in the following pages.

When applying power to the evaluation board, certain precautions need to be followed.

1. Powering Considerations: When operated at low input voltages, the evaluation board can draw up to 3.5A of current at a full load of 8A. It is important to choose the correct connector and wire size when attaching the source supply and the load. Monitor the input and output currents. An appropriate power supply is needed with adjustable output voltage (up to 100V) and current (up to 5A). The power supply must be of low impedance to avoid any interaction between the droop of the power supply and the undervoltage-lock-out protection of the evaluation board.
2. Loading Considerations: It is important to choose the correct connector and wire size when attaching the load. An appropriate electronic load with current up to 10A is desirable. The equivalent resistance of the load is 1.2Ω. Therefore, the connection wires should be thick enough. For accurate efficiency measurement, it is important to monitor the voltage directly at the output terminals of the evaluation board (preferably at the point of feedback) because the voltage drop across the load connecting wires will give inaccurate measurements.
3. Air Flow Conditions: Full rated power should never be attempted without providing the specified 200 CFM of air flow over the evaluation board. This can be provided by a stand-alone fan.

4. For the first time power-up, it is suggested to apply light load, and set the current limit of the source supply to less than 1.5 times of the wattage of the load. A quick efficiency check is the best way to confirm that everything is operating properly. It is common that the incorrect circuit parameters will affect the efficiency adversely.
5. When the current limit set on the source supply is insufficient for the load, the interaction of the source supply folding back and the evaluation board going into undervoltage shutdown will start an oscillation, or chatter, which may have highly undesirable consequences.
6. To measure the output voltage ripple more accurately, it is suggested to measure as closely as possible to the converter's output terminals. Since the signal being measured is in the millivolt range, the measurement set-up can be susceptible to picking up noise from external sources. The bandwidth of the oscilloscope can be set to 20MHz. Use very short and direct connections to the oscilloscope probe such that the total loop area in the signal and ground connections is as small as possible.

Some important waveforms are shown in the "Typical Performance Curves" on page 8.

Figures 11 and 12 show the ramp signal and the gate signal of the controller ISL6745. The frequency should match the waveform. The gate signals from the ISL6745A are sent to the half-bridge MOSFET driver HIP2101 for the two switches, and they should be symmetrical and 180° out-of-phase. Figure 13 shows the gate drive signals of the primary side switches. These signals are generated from HIP2101, the operation voltage of which is set by the ISL6720.

Figure 14 shows the typical current signal. The current signal should be less than 1V. Figures 15 and 16 show the drive signals and drain-source signals of the synchronous rectification in the secondary side.

The load/line regulation and efficiency curves are shown in Figures 17 and 18. The circuit has maximum efficiency at low line half load conditions. As the line voltage increases, the switching loss of the primary side MOSFET increases. The gate drive loss of the secondary side also increases as the gate drive loss is related to CV^2. As the duty ratio becomes small, the ripple in the inductor increases, and this leads to big transformer AC loss and rectifier reverse recovery loss, in addition to the AC loss of the output inductor. The efficiency drops significantly at high line voltages due to the incremental loss.

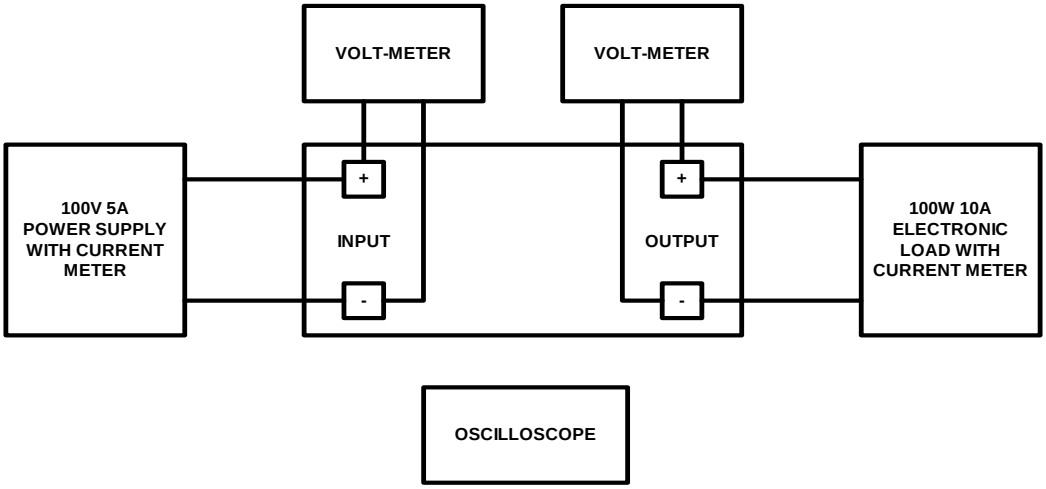

FIGURE 10. TYPICAL BENCH TEST SETUP

Typical Performance Curves

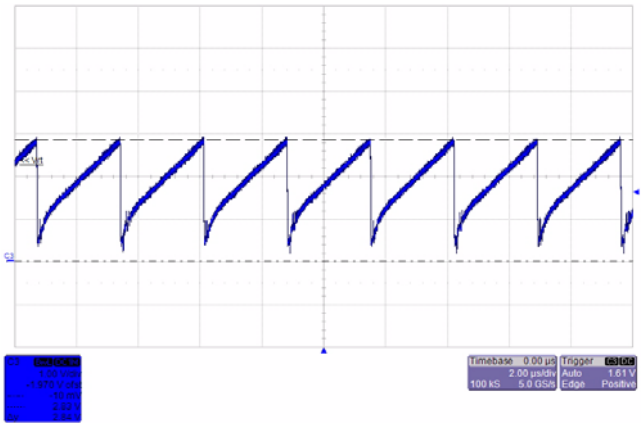

FIGURE 11. RAMP SIGNAL

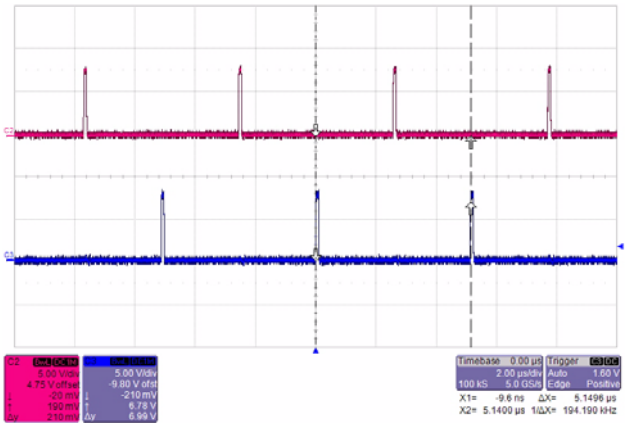

FIGURE 12. GATE SIGNALS FROM ISL6745

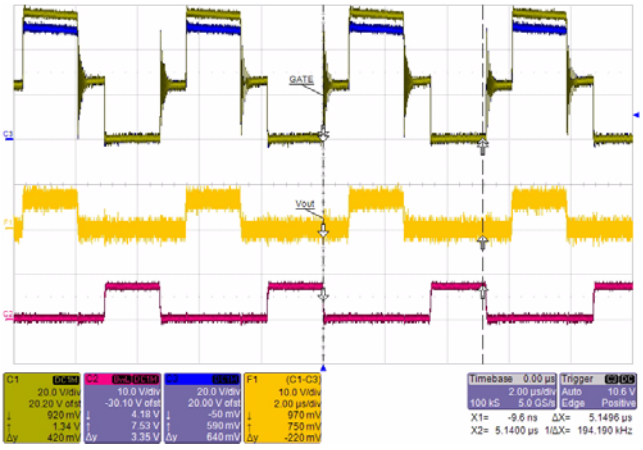

FIGURE 13. DRIVE SIGNALS FOR THE PRIMARY SWITCHES

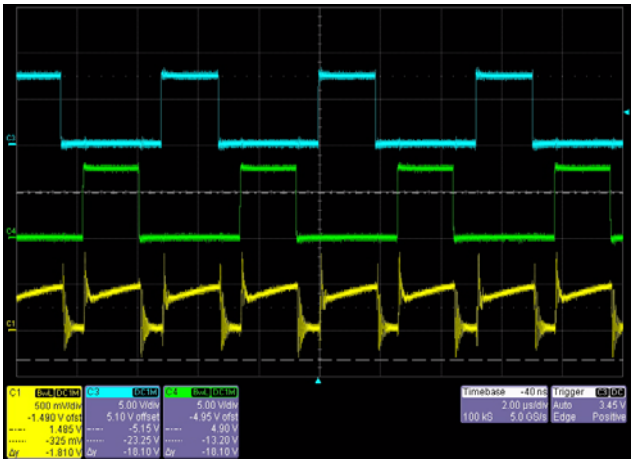

FIGURE 14. DRIVE SIGNAL AND CURRENT SIGNAL

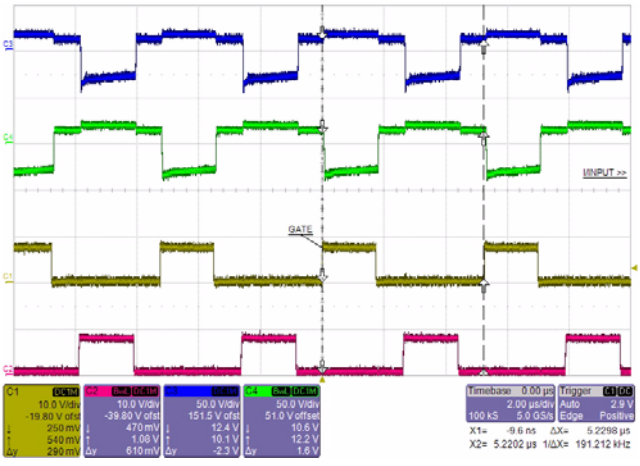

FIGURE 15. SECONDARY SIDE GATE DRIVE SIGNALS

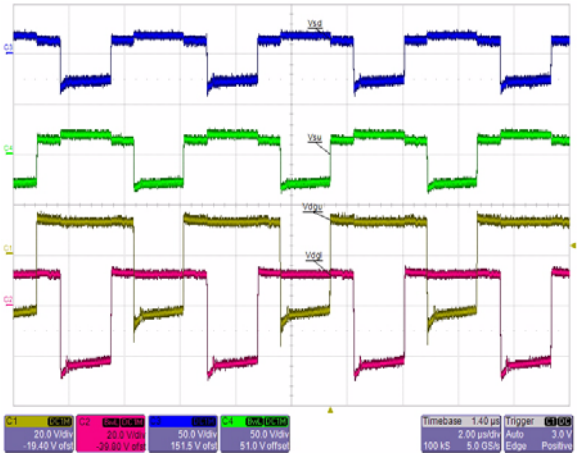

FIGURE 16. SECONDARY SIDE DRIVE SIGNAL AND DRAIN SOURCES

Typical Performance Curves

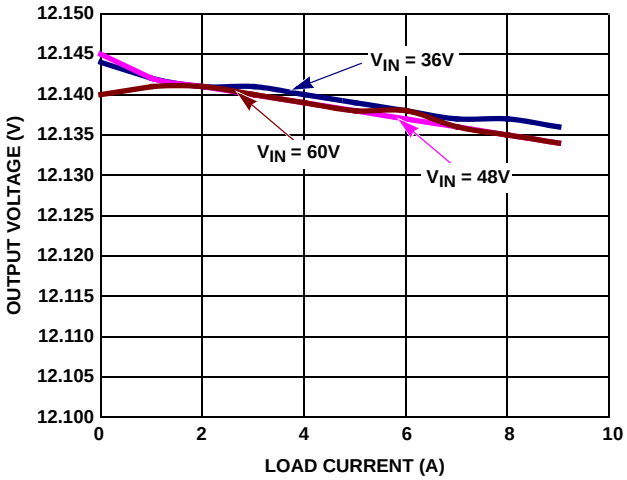

FIGURE 17. LINE AND LOAD REGULATION

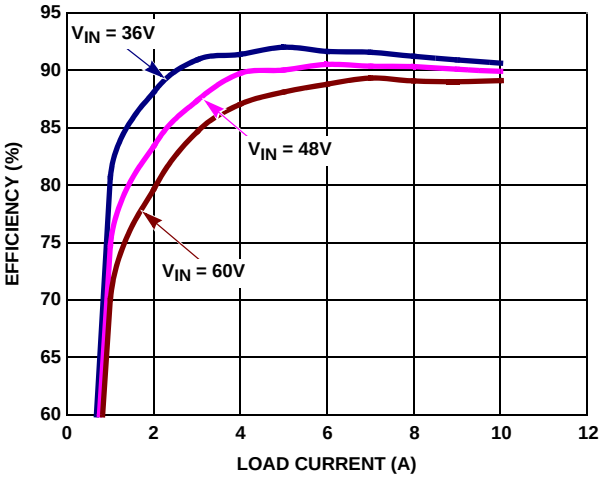

FIGURE 18. EFFICIENCY vs INPUT AND LOAD

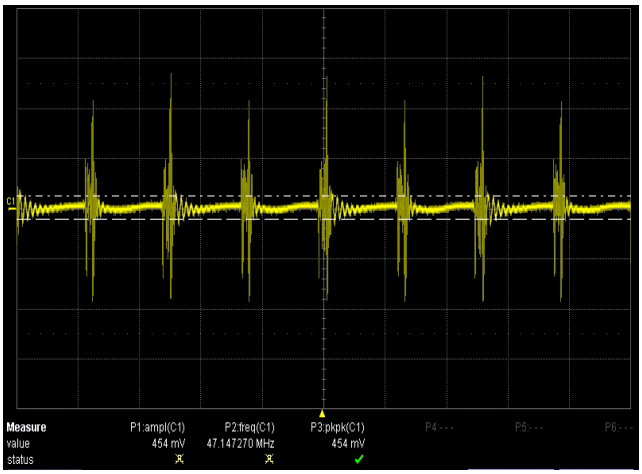

FIGURE 19. OUTPUT VOLTAGE RIPPLE AT 8A LOAD CURRENT, V_{IN} = 36V

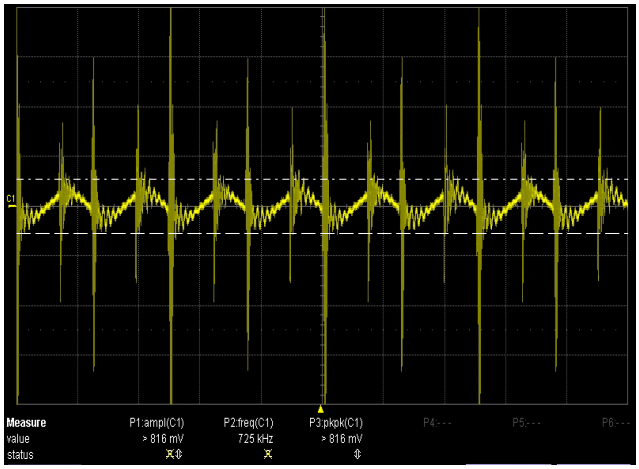

FIGURE 20. OUTPUT VOLTAGE RIPPLE AT 8A LOAD CURRENT, V_{IN} = 60V

ISL6745EVAL1Z Layout

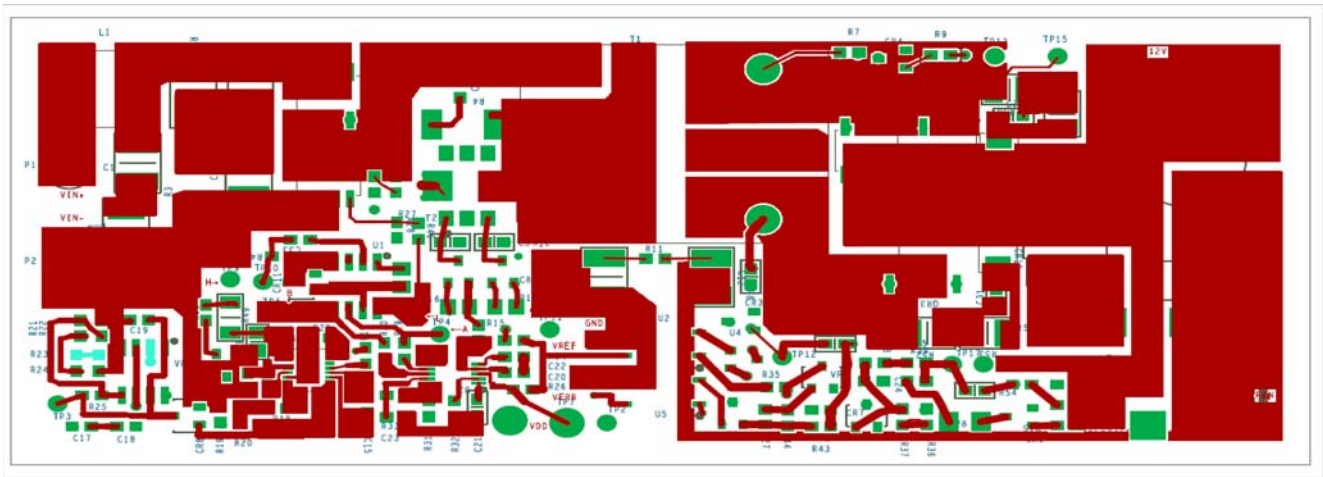

FIGURE 21. LAYER 1

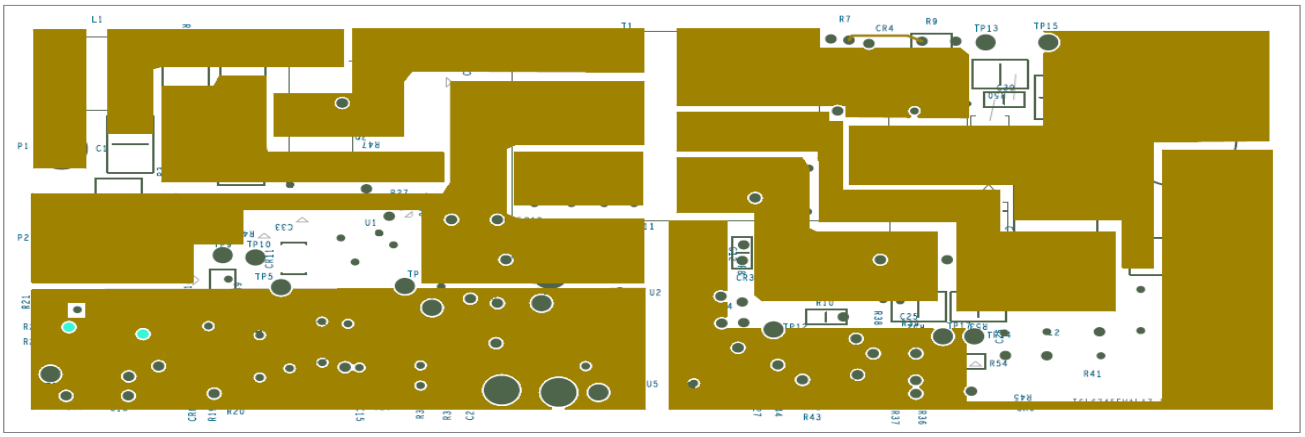

FIGURE 22. LAYER 2

FIGURE 23. LAYER 3

ISL6745EVAL1Z Layout (Continued)

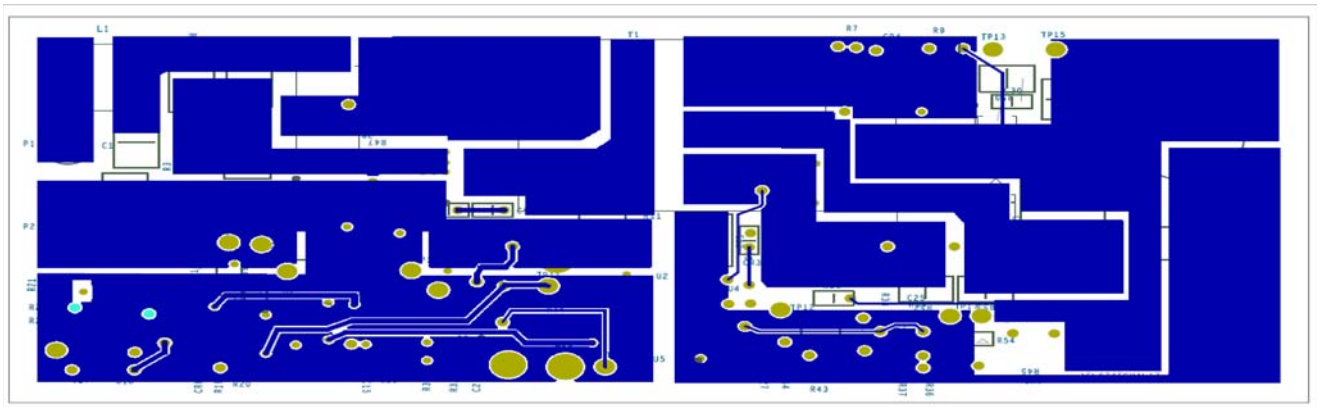

FIGURE 24. LAYER 4

ISL6745EVAL1Z Schematic

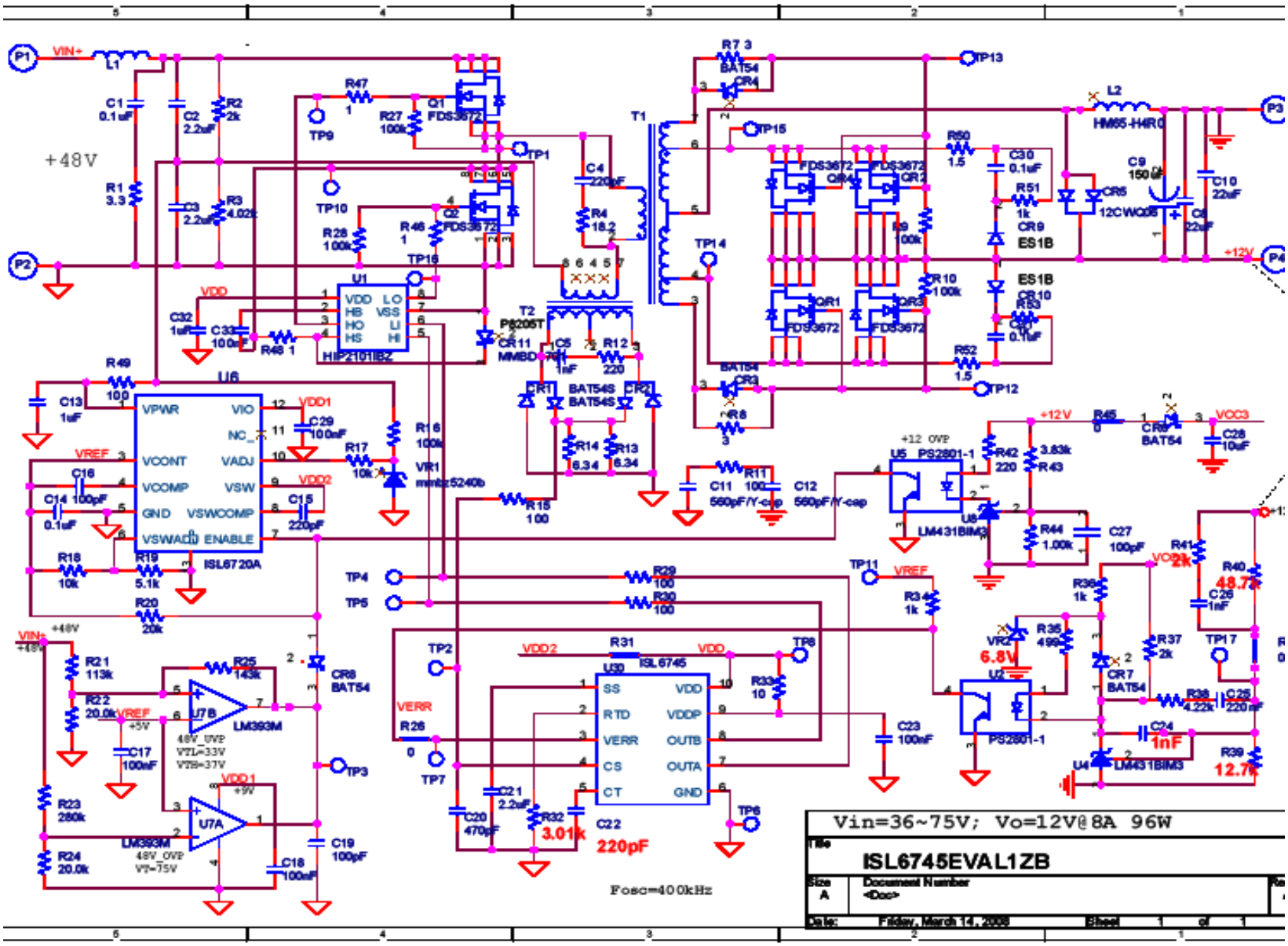

TABLE 1. BILL OF MATERIALS

PART NUMBER	QTY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
ISL6745EVAL1ZREVAPCB	1		PWB-PCB, ISL6745EVAL1Z, REVA, ROHS	TITAN
16SH150M	1	C9	CAP, TH, RADIAL, 150µF, 16V, 20%, OSCON	SANYO
GRM21BR71H105KA12L	2	C13, C32	CAP, SMD, 0805,1.0µF, 50V, 10%, X7R, ROHS	MURATA
GRM43ER72A225KA01B	2	C2, C3	CAP, SMD, 1812, 2.2µF, 100V, 10%, X7R, ROHS	MURATA
H1045-00101-50V5-T	3	C16, C19, C27	CAP, SMD, 0603, 100pF, 50V, 5%, COG, ROHS	PANASONIC
H1045-00102-100V10-T	2	C5, C26	CAP, SMD, 0603, 1000pF, 100V, 10%, X7R, ROHS	VENKEL
H1045-00104-50V10-T	6	C14, C17, C18, C23, C29, C33CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	TDK	
H1045-00221-100V10-T	4	C4, C15, C22, C24	CAP, SMD, 0603, 220pF, 100V, 10%, X7R, ROHS	PANASONIC
H1045-00224-25V10-T	1	C25	CAP, SMD, 0603, 0.22µF, 25V, 10%, X7R, ROHS	TDK
H1045-00225-16V10-T	1	C21	CAP, SMD, 0603, 2.2µF, 16V, 10%, X5R, ROHS	MURATA
H1045-00471-50V5-T	1	C20	CAP, SMD, 0603, 470pF, 50V, 5%, NPO, ROHS	PANASONIC
H1065-00106-25V10-T	1	C28	CAP, SMD, 1206, 10µF, 25V, 10%, X5R, ROHS	VENKEL
	1	C1	CAP, SMD, 2220, 4.7µF, 100V, 10%, X7R, ROHS	TDK
H1087-00104-100V10-T	2	C30, C31	CAP, SMD, 1812, 0.1µF, 100V, 10%, X7R, ROHS	VENKEL
H1087-00226-25V20-T	2	C8, C10	CAP, SMD, 1812, 22µF, 25V, 20%, X7R, ROHS	TDK
H1087-00561-100V10-T	2	C11, C12	CAP, SMD, 1812, 560pF, 100V, 10%, X7R, ROHS	VENKEL
DR73-1R0-R	1	L1	COIL-PWR inductor, 7.6mm, 1.0µH, 20%, 5.28A	COOPER
HM65-H4R0LF	1	L2	INDUCTOR, SMD, 13X12, 4.0µH, 20%, 10.3A, ROHS	BI TECHNOLOGIES
1514-2	4	P1, P2, P3, P4	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
5002	14	TP1-TP5, TP9-TP17CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	
5007	3	TP6, TP7, TP8	CONN-COMPACT TEST, VERTICAL, WHT, ROHS	KEYSTONE
12CWQ06FNPBF	1	CR5	DIODE-RECTIFIER, SMD,D-PAK, 60V, 12A, ROHS	IRF
	1	CR11	DIODE, SMD, SOT-23, 30V, 50mA, ROHS	FAIRCHILD
BAT54-T	5	CR3, CR4, CR6, CR7, CR8SCHOTTKY, SMD, SOT23, 3P, 30V, 200mA, SINGLE	FAIRCHILD	
BAT54S-T	2	CR1, CR2	SCHOTTKY, SMD, SOT23, 3P, 30V, 200mA, DUAL	FAIRCHILD
	1	VR2	ZENER, SMD, SOT23, 3P, 6.8V, 225mW, ROHS	ON SEMI
ES1B-13-F	2	CR9, CR10	DIODE-RECTIFIER, SMD, 2P, SMA, 100V, 1A, ROHS	DIODES INC.
	1	VR1	ZENER, SMD, SOT-23, 3P, 13V, 350mW, ROHS	ON SEMI
HIP2101IBZ	1	U1	IC-HALF BRIDGE DRIVER, 8P, SOIC, 100V, ROHS	INTERSIL
ISL6720AARZ	1	U6	IC-100V LINEAR REGULATOR, DFN, 4X4, ROHS	INTERSIL
ISL6745AUZ	1	U3	IC- CONTROLLER, 10P, MSOP, ROHS	INTERSIL
LM393M	1	U7	IC-DUAL COMPARATOR, 8P, SOP, ROHS	FAIRCHILD
	1	U5	DNP	
PS2801-1-A	1	U2	IC-HI ISO PHOTOCOUPLER, 4P, SSOP, ROHS	CA EASTERN LAB

TABLE 1. BILL OF MATERIALS (Continued)

PART NUMBER	QTY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER
	1	U8	DNP	
LM431BIM3	1	U4	Shunt regulator	National Semi
FDS3672-T	6	Q1, Q2, QR1, QR2, QR3, QR4, N-CHANNEL, 8P, SO-8, 100V, 7.5A, ROHS	FAIRCHILD	
H2511-00010-1/10W1-T	3	R46, R47, R48	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	PHILLIPS
H2511-00030-1/10W1-T	2	R7, R8	RES, SMD, 0603, 3Ω,1/10W, 1%, TF, ROHS	VENKEL
H2511-00100-1/10W1-T	1	R33	RES, SMD, 0603, 10Ω, 1/10W, 1%, TF, ROHS	KOA
H2511-001R5-1/10W1-T	2	R50, R52	RES, SMD, 0603, 1.5Ω,1/10W, 1%, TF, ROHS	VENKEL
H2511-00R00-1/10W-T	4	R26, R31, R45, R54	RESISTOR, SMD, 0603, 0Ω, 1/10W, TF, ROHS	
H2511-01000-1/10W1-T	4	R11, R15, R29, R30	RES, SMD, 0603, 100Ω, 1/10W, 1%,TF, ROHS	KOA
H2511-01001-1/10W1-T	5	R34, R36, R44, R51, R53RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	KOA	
H2511-01002-1/10W1-T	3	R17, R18, R16	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA
	2	R9, R10	DNP	
H2511-01003-1/10W1-T	2	R27, R28	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	
H2511-01133-1/10W1-T	1	R21	RES, SMD, 0603, 113k, 1/10W, 1%, TF, ROHS	PANASONIC
H2511-01433-1/10W1-T	1	R25	RES, SMD, 0603, 143k, 1/10W, 1%, TF, ROHS	VENKEL
H2511-02001-1/10W1-T	1	R37	RES, SMD, 0603, 2k, 1/10W, 1%, TF, ROHS	KOA
H2511-02002-1/10W1-T	3	R20, R22, R24	RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS	VENKEL
		R42, R43, R44	DNP	
H2511-02200-1/10W1-T	2	R12, R42	RES, SMD, 0603, 220Ω, 1/10W, 1%, TF, ROHS	YAGEO
H2511-02493-1/10W1-T	1	R39	RES, SMD, 0603, 2.49k, 1/10W, 1%, TF, ROHS	YAGEO
H2511-02803-1/10W1-T	1	R23	RES, SMD, 0603, 280k, 1/10W, 1%, TF, ROHS	PANASONIC
H2511-03011-1/10W1-T	1	R32	RES, SMD, 0603, 3.01k, 1/10W, 1%, TF, ROHS	KOA
H2511-03833-1/10W1-T	1	R43	RES, SMD, 0603, 3.83k, 1/10W, 1%, TF, ROHS	VENKEL
H2511-04221-1/10W1-T	1	R38	RES, SMD, 0603, 4.22k, 1/10W,1%,TF,ROHS	ROHM
H2511-04990-1/10W1-T	2	R35, R41	RES,SMD, 0603, 499Ω, 1/10W, 1%, TF, ROHS	KOA
H2511-05101-1/10W1-T	1	R19	RES, SMD, 0603, 5.11k, 1/10W, 1%, TF, ROHS	KOA
H2511-09533-1/10W1-T	1	R40	RES, SMD, 0603, 9.53k, 1/10W, 1%, TF, ROHS	VENKEL
H2512-06R34-1/8W1-T	2	R13, R14	RES, SMD, 0805, 6.34Ω, 1/8W, 1%, TF, ROHS	VENKEL
H2513-01000-1/4W1-T	1	R49	RES, SMD, 1206, 100Ω, 1/4W, 1%, TF, ROHS	STACKPOLE
H2515-003R3-1W1-T	1	R1	RES, SMD, 2512,3.3Ω, 1W, 1%, TF, ROHS	KOA
H2515-018R2-1W1-T	1	R4	RES, SMD, 2512, 18.2Ω, 1W, 1%, TF, ROHS	KOA
H2515-02001-1W1-T	1	R2	RES, SMD, 2512, 2k, 1W, 1%, TF, ROHS	PANASONIC
H2515-04021-1W1-T	1	R3	RES, SMD, 2512, 4.02k, 1W, 1%, TF, ROHS	PANASONIC
31660-LF1	1	T1	TRANSFORMER, SMD, 27.9X21.6, 83µH, 25%, 10kHz, CUSTOM, ROHS	MIDCOM
P8205NL	1	T2	TRANSFORMER-CURRENT SENSE, SMD, 8P, 500µH,10A, ROHS	PULSE