ISL76682

Automotive Low Power, High Sensitivity, Light-to-Digital Sensor with I2C Interface

The ISL76682 is a low power, high sensitivity, integrated light sensor with I^{2}C (SMBus Compatible) interface. Its state-of-the-art photo-diode array provides close-to human eye response and good IR rejection. This ADC is capable of rejecting 50Hz and 60Hz flicker caused by artificial light sources. The lux range select feature allows you to program the lux range for optimized counts/lux.

In normal operation, typical power consumption is 55µA. To further minimize power consumption, two power-down modes have been provided. If polling is chosen over continuous measurement of light, the automatic power-down function shuts down the whole chip after each ADC conversion for the measurement. The other power-down mode is controlled by software using an I^{2}C interface. The power consumption can be reduced to less than 1µA when powered down.

Operate on supplies from 2.25V to 3.3V with an I^{2}C supply from 1.7V to 3.6V, the ISL76682 is specified for operation across the -40°C to +105°C ambient temperature range.

Applications

- Automotive ambient light sensing
- Auto-dimming rear view mirror
- Central display and cluster dimming
- Industrial and medical light sensing

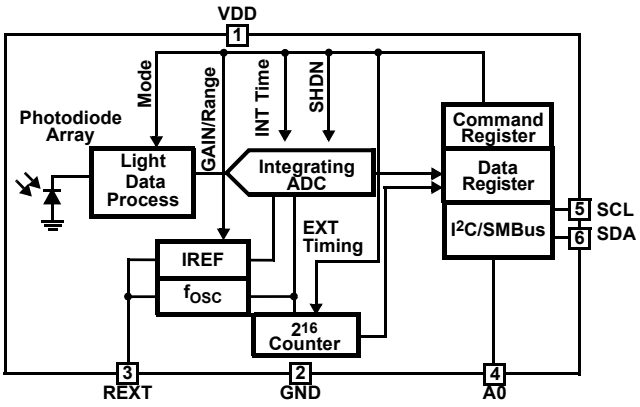

Figure 1. Block Diagram

Features

- Low power
  - 65µA maximum operating current
  - 0.5µA maximum shutdown current
  - Software shutdown and automatic shutdown
- Ideal spectral response
  - Close to Human eye response
  - Excellent IR and UV rejection
- Easy to use
  - Simple output code directly proportional to lux
  - I^{2}C (SMBus compatible) output
  - No complex algorithms needed
  - Variable conversion resolution up to 16-bits
  - Adjustable sensitivity up to 65 counts per lux
  - Works under various light sources, including sunlight
  - Selectable range (using I^{2}C)
  - Range 1 = 0.015 lux to 1,000 lux
  - Range 2 = 0.06 lux to 4,000 lux
  - Range 3 = 0.24 lux to 16,000 lux
  - Range 4 = 0.96 lux to 64,000 lux
  - Temperature compensated
  - Integrated 50/60Hz noise rejection
- Small form factor
  - 2.0mm×2.1mm×0.7mm 6 Ld ODFN Package
- Additional features
  - I^{2}C and SMBus compatible w/address selection Pin
  - 1.7V to 3.6V supply for I^{2}C interface
  - 2.25V to 3.3V supply
- AEC-Q100 Qualified
- Pb-Free (RoHS compliant)

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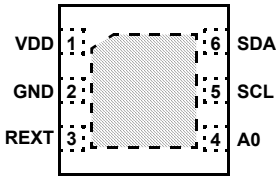
Contents

1. Pin Information

1.1 Pin Assignments



***Exposed Pad Can be Connected to GND or Electrically Isolated**

Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Description	
1	VDD	Positive supply; connect this pin to a 2.25V to 3.3V supply.	
2	GND	Ground pin.	
3	REXT	External resistor pin for ADC reference; connect this pin to ground through a (nominal) 500kΩ 1% resistor.	
4	A0	Bit 0 of I^2C address. This pin must be either tied to ground or to VDD. Do not left floating.	
5	SCL	I^2C serial clock	The I^2C bus lines can be pulled from 1.7V to above V_{DD}, 3.6V maximum.
6	SDA	I^2C serial data	

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VDD Supply Voltage between VDD and GND		3.6	V
I^2C Bus Pin Voltage (SCL, SDA)	-0.2	3.6	V
I^2C Bus Pin Current (SCL, SDA)		<10	mA
REXT, A0 Pin Voltage	-0.2	V_{DD}	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002)	2		kV
Charged Device Model (Tested per AEC-Q100-011)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

1. T_A = +25°C

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-40	+105	°C

2.3 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]
6 Ld ODFN Package	88

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.

Parameter	Minimum	Maximum	Unit
Maximum Die Temperature		+105	°C
Maximum Storage Temperature Range	-40	+105	°C
Pb-Free Reflow Profile	see TB493		

2.4 Electrical Specifications

V_{DD} = 3V, T_A = +25°C, R_{EXT} = 500kΩ 1% tolerance, 16-bit ADC operation, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Range	V_{DD}		2.25		3.3	V
Supply Current	I_{DD}			55	65	µA
Supply Current when Powered Down	I_{DD1}	Software disabled or auto power-down		0.01	0.5	µA
Supply Voltage Range for I^2C Interface	V_{I^2C}		1.7		3.6	V
Internal Oscillator Frequency	f_{OSC}		650	725	800	kHz
ADC Integration/Conversion Time	t_{int}	16-bit ADC data		90		ms
I^2C Clock Rate Range	F_{I^2C}			400		kHz
Count Output When Dark	DATA_0	E = 0 lux, Range 1 (1k lux)		1	5	Counts
Full Scale ADC Code	DATA_F				65535	Counts
Count Output Variation Over Three Light Sources: Fluorescent, Incandescent, and Sunlight	DDATA DATA	Ambient light sensing		±10		%
Light Count Output with LSB of 0.015 lux/count	DATA_1	E = 300 lux, Fluorescent light[1], Ambient light sensing, Range 1 (1k lux)	15000	20000	25000	Counts
Light Count Output with LSB of 0.06 lux/count	DATA_2	E = 300 lux, Fluorescent light[1], Ambient light sensing, Range 2 (4k lux)		5000		Counts
Light Count Output with LSB of 0.24 lux/count	DATA_3	E = 300 lux, Fluorescent light[1], Ambient light sensing, Range 3 (16k lux)		1250		Counts
Light Count Output with LSB of 0.96 lux/count	DATA_4	E = 300 lux, Fluorescent light[1], Ambient light sensing, Range 4 (64k lux)		312		Counts
Infrared Count Output	DATA_IR1	E = 210 lux, Sunlight[2], IR sensing, Range 1	15000	20000	25000	Counts
	DATA_IR2	E = 210 lux, Sunlight[2], IR sensing, Range 2		5000		Counts
	DATA_IR3	E = 210 lux, Sunlight[2], IR sensing, Range 3		1250		Counts
	DATA_IR4	E = 210 lux, Sunlight[2], IR sensing, Range 4		312		Counts
Voltage of R_{EXT} Pin	V_{REF}			0.52		V
SCL and SDA Input Low Voltage	V_{IL}				0.55	V
SCL and SDA Input High Voltage	V_{IH}		1.25			V
SDA Current Sinking Capability	I_{SDA}		4	5		mA

1. 550nm green LED is used in production test. The 550nm LED irradiance is calibrated to produce the same DATA count against an illuminance level of 300 lux fluorescent light.
2. 850nm green LED is used in production test. The 850nm LED irradiance is calibrated to produce the same DATA_IR count against an illuminance level of 210 lux sunlight at sea level.

3. Typical Performance Curves

V_{DD} = 3V, R_{EXT} = 500kΩ

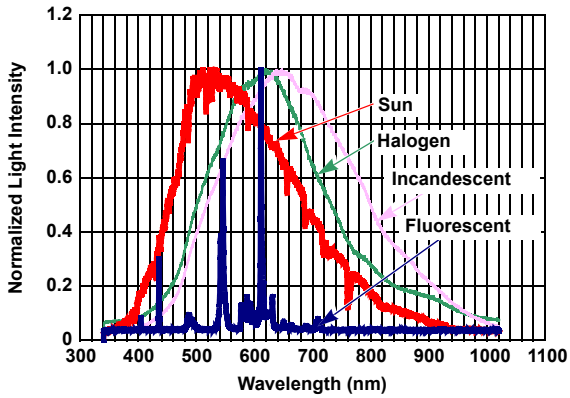


Figure 2. Spectral Response of Light Sources

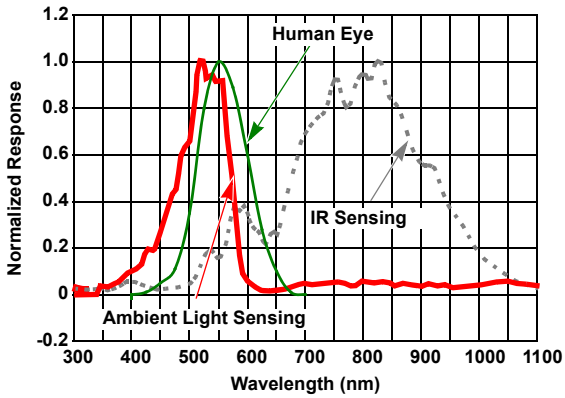


Figure 3. Spectral Response for Ambient Light Sensing and IR Sensing

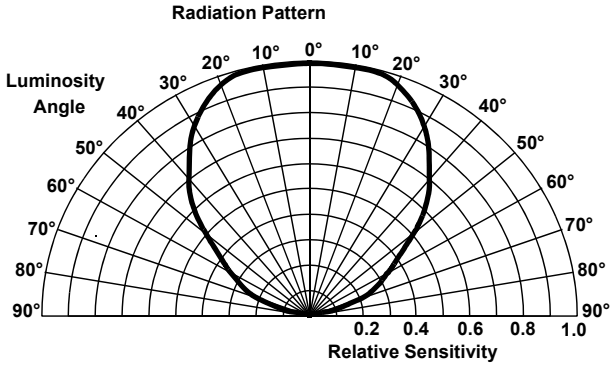


Figure 4. Radiation Pattern

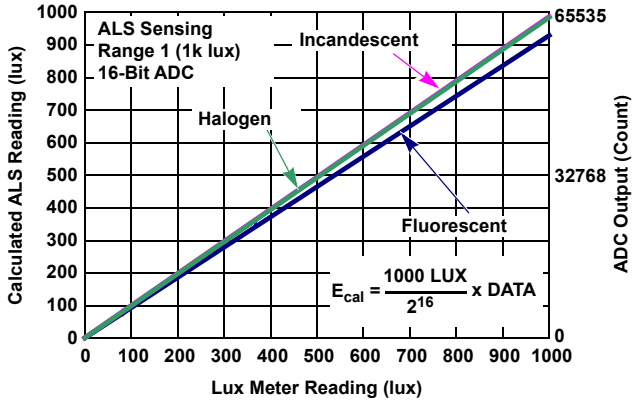


Figure 5. Sensitivity to Three Light Sources

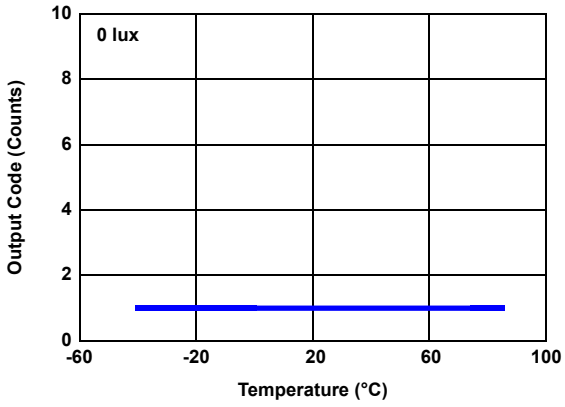


Figure 6. Output Code for 0 lux vs Temperature

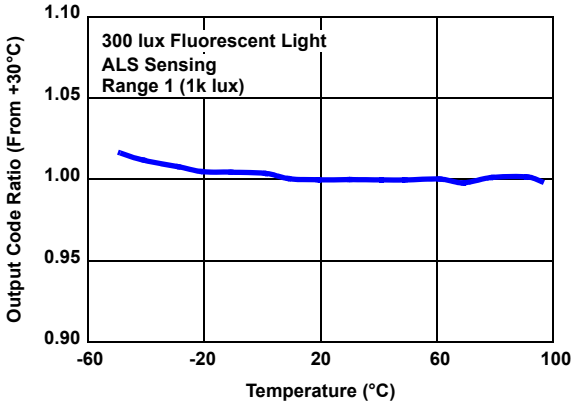


Figure 7. Output Code vs Temperature

V_{DD} = 3V, R_{EXT} = 500kΩ (Cont.)

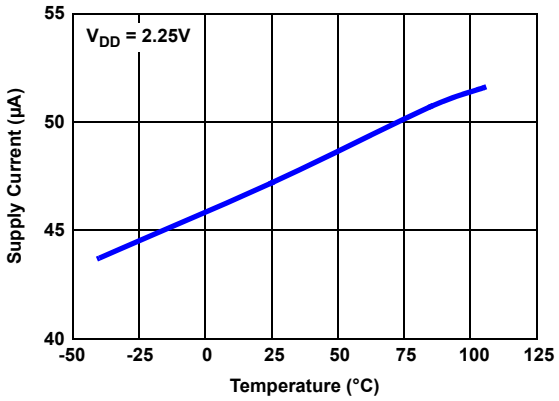


Figure 8. Supply Current vs Temperature

4. Principles of Operation

4.1 Photodiodes and ADC

The ISL76682 contains two photo-diode arrays that convert light into current. The spectral response for ambient light sensing and IR sensing are shown in Figure 3. After light is converted to current during the light signal process, the current output is converted to digital by a single built-in 16-bit Analog-to-Digital Converter (ADC). An I^2C command reads the ambient light or IR intensity in counts.

The converter is a charge-balancing integrating type 16-bit ADC. The chosen method for conversion is best for converting small current signals in the presence of an AC periodic noise. A 100ms integration time, for instance, highly rejects 50Hz and 60Hz power line noise simultaneously. For more information, see Integration Time or Conversion Time on and Noise Rejection.

The built-in ADC offers user flexibility in integration time or conversion time. There are two timing modes: Internal Timing Mode and External Timing Mode. In Internal Timing Mode, integration time is determined by an internal oscillator (f_{OSC}), and the n-bit (n = 4, 8, 12,16) counter inside the ADC. In External Timing Mode, integration time is determined by the time between two consecutive I^2C External Timing Mode commands. See External Timing Mode. A good balancing act of integration time and resolution depending on the application is required for optimal results.

The ADC has I^2C programmable ranges to dynamically accommodate various lighting conditions. For very dim conditions, the ADC can be configured at its lower range (Range 1). For bright conditions, the ADC can be configured at its higher range (Range 2).

4.2 I^2C Interface

There are three 8-bit registers available inside the ISL76682. The command register defines the operation of the device. The command register does not change until the register is overwritten. The two 8-bits data registers are Read-Only and combine to form the 16-bits ADC count or timer output. The data registers contain the latest digital output of the ADC or timer.

4.2.1 I^2C Slave Address

The I^2C interface slave address can be selected as 1000100b (44 hex) or 1000101b (45 hex) by connecting A0 pin to GND or VDD, respectively. When 1000100x or 1000101x with x as R or $\overline{W}$ is sent after the Start condition, this device compares the first seven bits of this byte to its address and matches.

4.2.2 I²C Transactions

Figure 9 shows a sample one-byte read. Figure 10 shows a sample one-byte write. Figure 11 shows a sync_I²C timing diagram sample for externally controlled integration time. The I²C bus master always drives the SCL (clock) line, while either the master or the slave can drive the SDA (data) line. Every I²C transaction begins with the master asserting a start condition (SDA falling while SCL remains high). The following byte is driven by the master and includes the slave address and read/write bit. The receiving device is responsible for pulling SDA low during the acknowledgment period. Every I²C transaction ends with the master asserting a stop condition (SDA rising while SCL remains high).

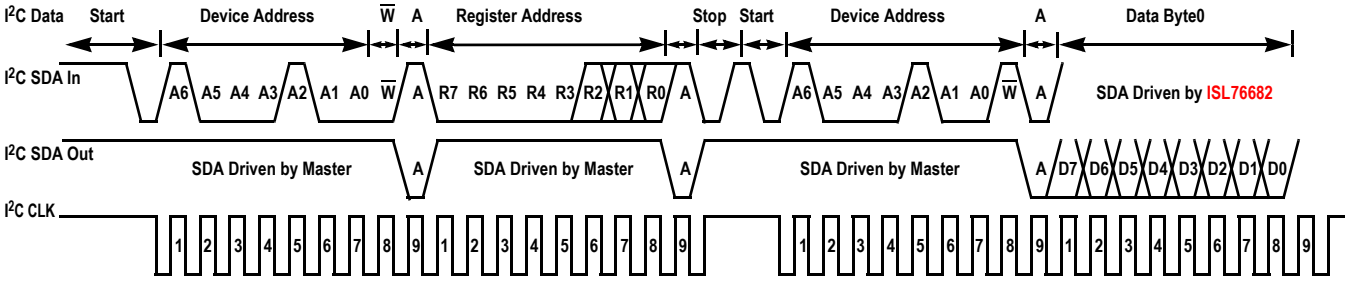


Figure 9. I²C Read Timing Diagram Sample

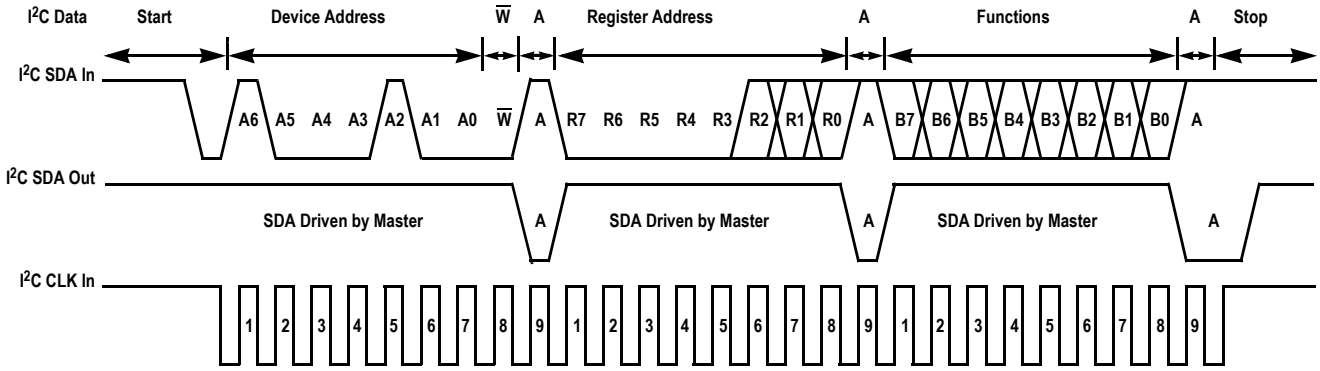


Figure 10. I²C Write Timing Diagram Sample

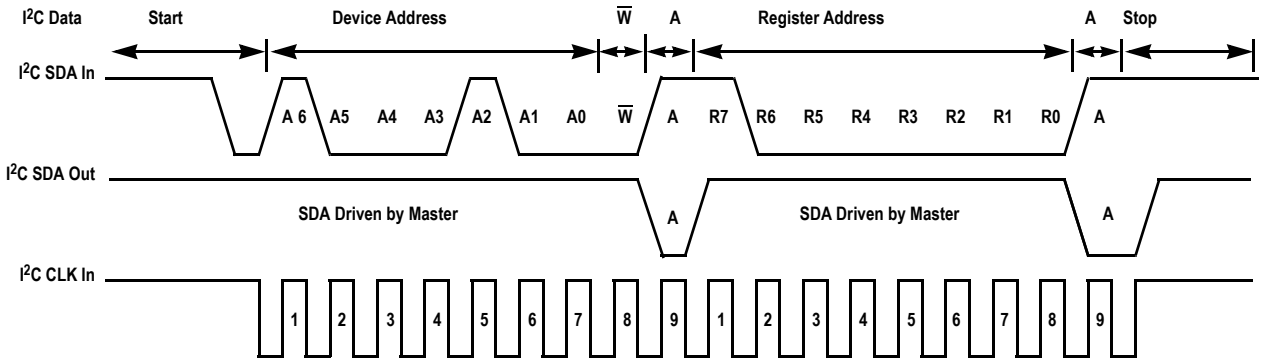


Figure 11. I²C SYNC_I²C Timing Diagram Sample

For more information about the I²C standard, please consult the NXP® I²C specification documents version 2.0.

4.3 Low-Power Operation

The ISL76682 initial operation is at the power-down mode after a supply voltage is provided. The data registers contain the default value of 0. When the ISL76682 receives an I^2C command to do a one-time measurement from an I^2C master, it starts light sensing and ADC conversions. It goes to the power-down mode automatically after one conversion is finished and keeps the conversion data available for the master to fetch anytime afterwards. The ISL76682 continuously does light sensing and ADC conversions if it receives an I^2C command of continuous measurement. It continuously updates the data registers with the latest conversion data. It goes to the power-down mode after it receives the I^2C command of power-down.

4.4 Register Set

There are three 8-bit registers in the ISL76682. Table 1 summarizes their functions.

Table 1. Register Set

Addr	Reg Name	Bit								Default
		7	6	5	4	3	2	1	0	
00h	COMMAND	EN	MODE	LIGHT	RES2	RES1	RES0	RANGE1	RANGE0	00h
01h	$DATA_{LSB}$	D7	D6	D5	D4	D3	D2	D1	D0	00h
02h	$DATA_{MSB}$	D15	D14	D13	D12	D11	D10	D9	D8	00h

Table 2. Write Only Registers

Address	Name	Functions/Description
b1xxx_xxxx	sync_I^2C	Writing a logic 1 to this address bit ends the current ADC-integration and starts another. Used only with External Timing Mode.

4.5 Command Register (00 hex)

The Read/Write command register has five functions:

- Enable: Bit 7. This bit enables the ISL76682 with logic 1 and powers down ISL76682 with logic 0.

Table 3. Enable

Bit 7	Operation
0	Power down the device
1	Enable the device

- Measurement Mode: Bit 6. This bit controls the two measurement modes of the device. A logic 0 puts the device in the one-time measurement mode in which the device is automatically shut down after each measurement. A logic 1 puts the device in the continuous measurement mode in which data is collected continuously.

Table 4. Measurement Mode

Bit 6	Operation
0	One-time measurement
1	Continuous measurement

- Light Sensing: Bit 5. This bit programs the device to do the ambient light or the infrared (IR) light sensing. A logic 0 requests for the ambient light sensing and a logic 1 requests for the IR sensing.

Table 5. Light Sensing

Bit 5	Operation
0	Ambient light sensing
1	Infrared light sensing

- Timing Mode and Resolution: Bits 4, 3, and 2. These three bits determine whether the integration time is done internally or externally, and the number of bits for ADC. In Internal Timing Mode, integration time is determined by an internal oscillator (f_{OSC}) and the n-bit (n = 4, 8, 12, 16) counter inside the ADC. In External Timing Mode, the integration time is determined by the time between two consecutive sync_I^2C pulse commands.

Table 6. Timing Mode and Resolution

Bits 4:3:2	Mode
0:0:0	Internal Timing, 16-bit ADC data output
0:0:1	Internal Timing, 12-bit ADC data output
0:1:0	Internal Timing, 8-bit ADC data output
0:1:1	Internal Timing, 4-bit ADC data output
1:0:0	External Timing, ADC data output
1:0:1	External Timing, Timer data output
1:1:0	Reserved
1:1:1	Reserved

With Bit 4 set to 0, the device is configured to run in the Internal-Timing mode. For example, the command register content should be 1xx000xx to request 16-bit ADC in the internal-timing mode.

With Bit 4 set to 1, the device is configured to run in the External-Timing mode. For the external timing, the command 1xx101xx needs to be sent to request the Timer data, the number of clock cycles counted within the duration between the two sync pulses (see Table 7). The Timer count is read from register 01h (LSB) and 02h (MSB). The command 1xx100xx needs to be sent to request the ADC conversion. The ADC data is also read from register 01h (LSB) and 02h (MSB).

Bits 3 and 2 determine the number of clock cycles per conversion in the Internal-Timing mode. Changing the number of clock cycles does more than just change the resolution of the device. It also changes the integration time, which the ADC uses to sample the photo-diode current signal for a measurement.

Table 7. Resolution/Width

Bits 3:2	Number of Clock Cycles
0:0	2^{16} = 65,536
0:1	2^{12} = 4,096
1:0	2^{8} = 256
1:1	2^{4} = 16

- Range: Bits 1 and 0. The Full-Scale Range (FSR) can be adjusted using an I^2C using Bits 1 and 0. Table 8 lists the possible values of FSR for the 500kΩ R_{EXT} resistor.

Table 8. Range/FSR Lux

Bits 1:0	k	Range (k)	FSR (lux) at ALS Sensing	FSR (lux) at IR Sensing
0:0	1	Range1	1,000	See page 5
0:1	2	Range2	4,000	See page 5
1:0	3	Range3	16,000	See page 5
1:1	4	Range4	64,000	See page 5

4.6 Data Registers (01 hex and 02 hex)

The device has two 8-bit read-only registers to hold a 16-bit data from ADC or Timer. The most significant byte is accessed at 02 hex, and the least significant byte is accessed at 01 hex. The registers are refreshed after every conversion cycle.

Table 9. Data Registers

Address (hex)	Contents
01	Least-significant byte of most recent ADC or Timer data.
02	Most-significant byte of most recent ADC or Timer data.

4.7 Calculating lx

The ADC output codes of the ISL76682 (DATA) are directly proportional to lux in the ambient light sensing, as shown in Equation 1.

(EQ. 1) $$E_{cal} = \alpha \times DATA$$

Here, E_{cal} is the calculated lux reading. The constant α is determined by the Full-Scale Range and the maximum output counts of the ADC. The constant can also be viewed as the sensitivity: the smallest lux measurement the device can measure, as shown in Equation 2.

(EQ. 2) $$\alpha = \frac{Range(k)}{Count_{max}}$$

Here, Range(k) is defined in Table 8. $Count_{max}$ is the maximum output counts from the ADC.

The transfer function used for each timing mode becomes the following:

- Internal Timing Mode
- External Timing Mode

4.7.1 Internal Timing Mode

In Equation 3, n = 4, 8, 12 or 16. This is the number of ADC bits programmed in the command register. 2^n represents the maximum number of counts possible from the ADC output in Internal-Timing mode. Data is the ADC output stored in the data registers (01 hex and 02 hex).

(EQ. 3) $$E = \frac{Range(k)}{2^n} \times DATA$$

4.7.2 External Timing Mode

In Equation 4, Timer sets up the maximum count reading of the ADC and it is the number of clock cycles accrued in the integration time (set by sync_I²C pulses) in External-Timing mode. It is stored in the data registers 01h and 02h when the command is coded as 1xx101xx. Data is the ADC output. In this mode, the command must be sent out again with code 1xx100xx to request the ADC output data from registers 01h and 02h.

(EQ. 4) $$E = \frac{Range(k)}{Timer} \times DATA$$

4.8 External Scaling Resistor R_{EXT} for f_{OSC} and Range

The ISL76682 uses an external resistor R_{EXT} to fix its internal oscillator frequency, f_{OSC} and the light sensing range, Range. f_{OSC} and Range are inversely proportional to R_{EXT}. For user simplicity, the proportionality constant is referenced to 500kΩ:

(EQ. 5) $$Range = \frac{500k\Omega}{R_{EXT}} \times Range(k)$$

(EQ. 6) $$f_{OSC} = \frac{500k\Omega}{R_{EXT}} \times 725kHz$$

4.9 Integration Time or Conversion Time

Integration time is the period during which the ADC converter of the device samples the photo-diode current signal for a measurement. Integration time, in other words, is the time to complete the conversion of analog photo-diode current into a digital signal (number of counts).

Integration time affects the measurement resolution. For better resolution, use a longer integration time. For short and fast conversions, use a shorter integration time.

The ISL76682 offers user flexibility in the integration time to balance resolution, speed and noise rejection. Integration time can be set internally or externally by programming the bit 4 of the command register 00(hex).

4.9.1 Integration time in Internal-Timing Mode

Most applications will use the Internal-Timing mode. In this mode, f_{OSC} and ADC n-bits resolution determine the integration time, t_{int}, as shown in Equation 7.

(EQ. 7) $$t_{int} = 2^n \times \frac{1}{f_{OSC}} = 2^n \times \frac{R_{EXT}}{725kHz \times 500k\Omega}$$

where n is the number of bits of resolution and n = 4, 8, 12 or 16. 2^n, therefore, is the number of clock cycles. n can be programmed at the command register 00(hex) Bits 3 and 2.

Table 10. Integration Time of n-Bit ADC

R_{EXT} (kΩ)	n = 16-Bit	n = 12-Bit	n = 8-Bit	n = 4-Bit
250	50ms	3.2ms	200µs	12.5µs
500[1]	100ms	6.25ms	390µs	24µs
1000	200ms	12.5ms	782µs	49µs
1500	300ms	18.8ms	1.17ms	73µs
2000	400ms	25ms	1.56ms	98µs

1. Recommended R_{EXT} resistor value.

4.9.2 Integration time in External Timing Mode

The External Timing Mode is recommended when the integration time is needed to synchronize to an external signal, such as a PWM to eliminate noise.

The synchronization can be implemented by using I^2C sync command. The 1st I^2C sync command starts the conversion. The 2nd completes the conversion then starts over again to commence the next conversion. The integration time, t_{int}, is the time interval between the two sync pulses:

(EQ. 8) $$t_{int} = \frac{Timer}{f_{OSC}}$$

where Timer is the number of internal clock cycles obtained from data registers and f_{OSC} is the internal oscillator frequency.

The internal oscillator, f_{OSC}, operates identically in both the internal and external timing modes. However, in External Timing Mode, the number of clock cycles per integration is no longer fixed at 2^n. The number of clock cycles varies with the chosen integration time and is limited to 2^{16} = 65,536. To avoid erroneous readings, the integration time must be short enough not to allow an overflow in the counter register.

(EQ. 9) $$t_{int} < \frac{65{,}535}{f_{OSC}}$$

4.10 Noise Rejection

In general, integrating type ADCs have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. For instance, a 60Hz AC unwanted signal sum from 0ms to k*16.66ms (k = 1,2...k_i) is zero. Similarly, setting the integration time of the device to be an integer multiple of the periodic noise signal, greatly improves the light sensor output signal in the presence of noise.

5. Optical Design

5.1 Flat Window Lens Design

A window lens surely limits the viewing angle of the ISL76682. The window lens should be placed directly on top of the device. Keep the thickness of the lens at minimum to minimize loss of power because of reflection and to minimize loss because of absorption of energy in the plastic material. A thickness of t = 1mm is recommended for a window lens design. The bigger the diameter of the window lens, the wider the viewing angle is of the ISL76682. Table 11 shows the recommended dimensions of the optical window to ensure both 35° and 45° viewing angle. These dimensions are based on a window lens thickness of 1.0mm and a refractive index of 1.59.

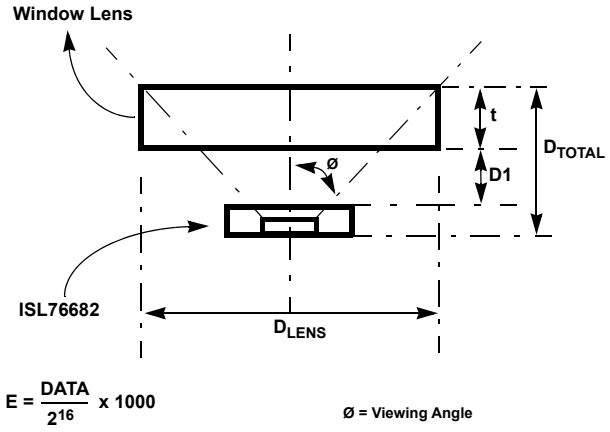


Figure 12. Flat Window Lens

Table 11. Recommended Dimensions for a Flat Window Design[1][2]

D_{TOTAL}[3]	D1[4]	D_{LENS}[5] at 35° Viewing Angle	D_{LENS} at 45° Viewing Angle
1.5	0.50	2.25	3.75
2.0	1.00	3.00	4.75
2.5	1.50	3.75	5.75
3.0	2.00	4.30	6.75
3.5	2.50	5.00	7.75

1. All dimensions are in mm.
2. t = 1 thickness of the lens.
3. D_{TOTAL} is the distance constraint between the ISL76682 and the lens outer edge.
4. D1 is the distance between ISL76682 and inner edge of lens.
5. D_{LENS} is the diameter of the lens.

5.2 Window with Light Guide Design

If a smaller window is required while maintaining a wide effective viewing angle of the ISL76682, a cylindrical piece of transparent plastic is needed to trap the light and then focus and guide the light onto the device. Therefore, the name light guide or also known as light pipe. Place the pipe directly on top of the device with D1 = 0.5mm to achieve peak performance. The light pipe should have minimum of 1.5mm in diameter to ensure that whole area of the sensor is exposed. See Figure 13.

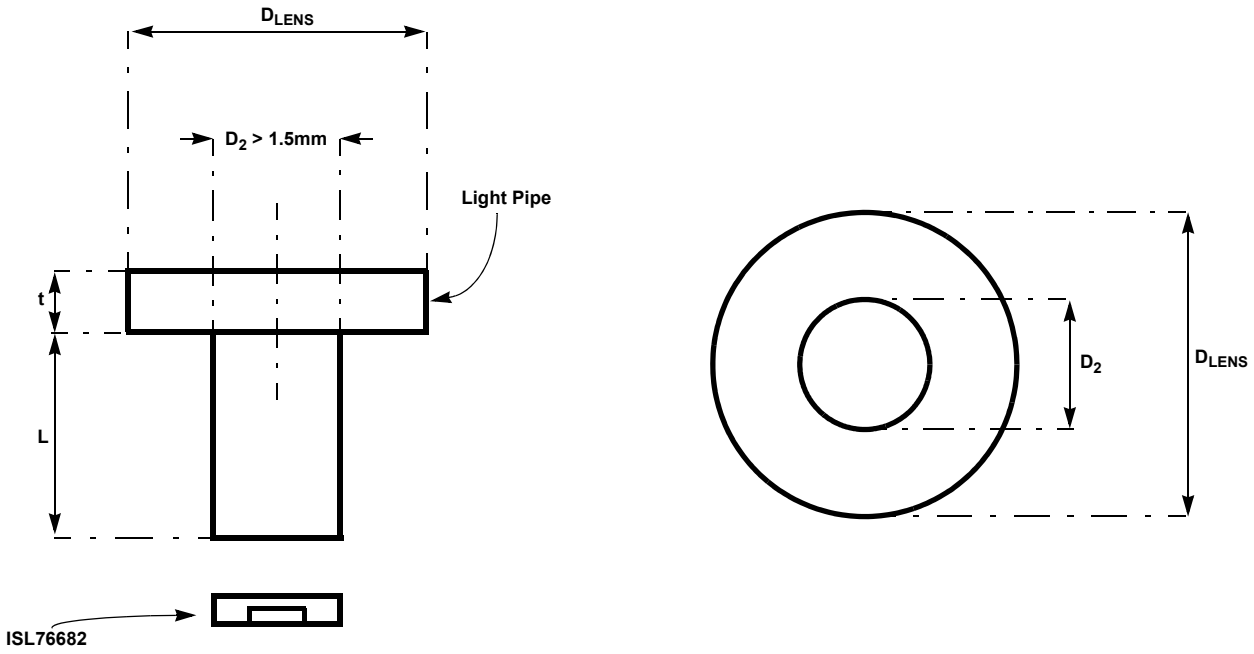


Figure 13. Window with Light Guide/Pipe

6. Suggested PCB Footprint

It is important that you review *TB477*, *Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package* before starting ODFN product board mounting.

6.1 Layout Considerations

The ISL76682 is relatively insensitive to layout. Like other I²C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that ensures best performance.

Route the supply and I²C traces as far as possible from all sources of noise. Use one 0.01µF power-supply decoupling capacitor, placed close to the device.

7. Typical Circuit

A typical application for the ISL76682 is shown in Figure 14. The ISL76682's I²C address is hardwired as 1000100b. The device can be tied onto a system's I²C bus together with other I²C compliant devices.

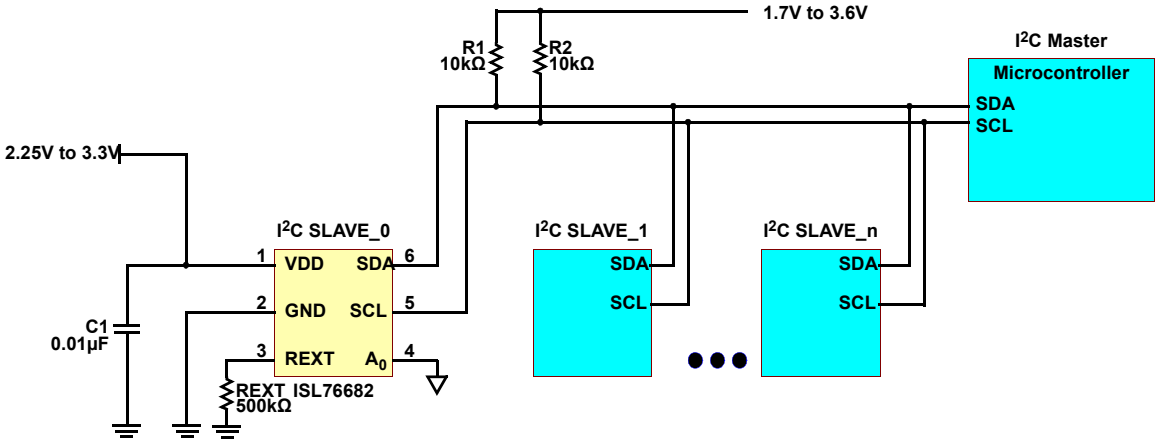


Figure 14. ISL76682 Typical Circuit

7.1 Soldering Considerations

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

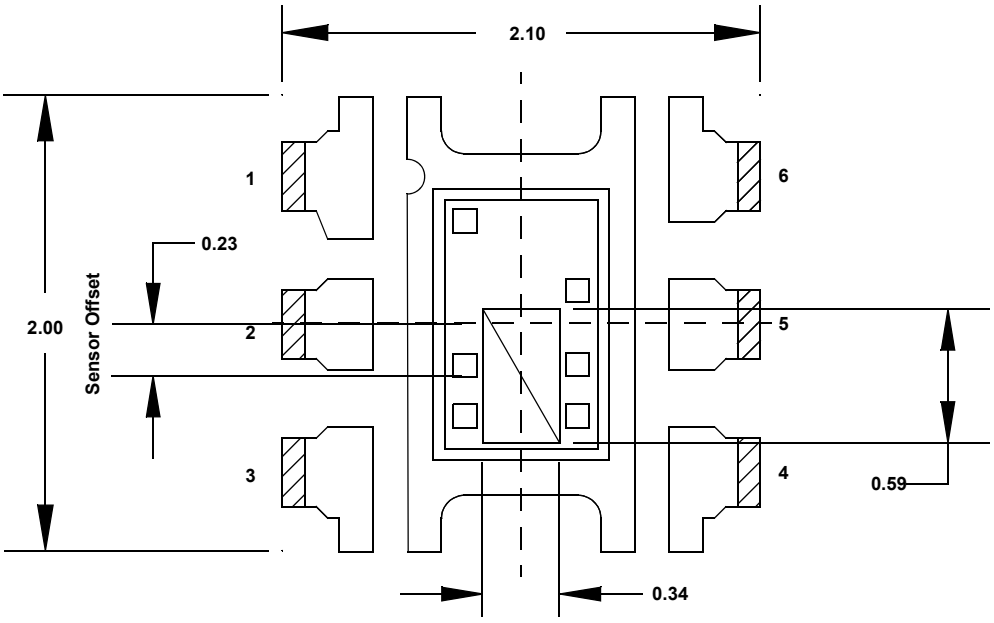
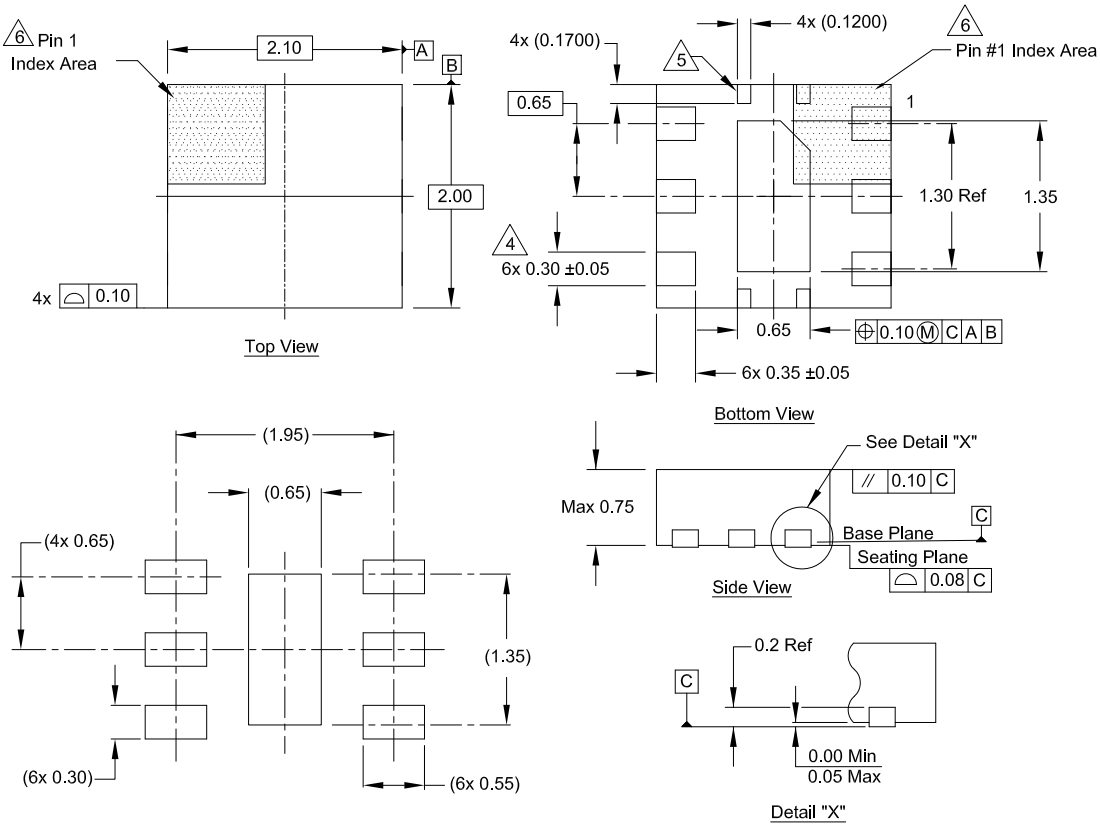


Figure 15. Sensor Location Outline

8. Package Outline Drawing

For the most recent package outline drawing, see L6.2x2.1Z.

L6.2x2.1Z
6 Lead Optical Dual Flat No-Lead Plastic Package (ODFN)
Rev 0, 5/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tie bar shown (if present) is a non-functional feature connected to paddle for mechanical locking purpose.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.

9. Ordering Information

Part Number[1][2]	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type [3]	Temp. Range
ISL76682AROZ-T7	6 Ld ODFN	L6.2x2.1Z	Reel, 3k	-40 to +105°C
ISL76682EVAL1Z	Evaluation Board			

1. These Renesas Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Renesas Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL), see the Product Options on the ISL76682 product page (click the packaging icon). For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.00	Oct 6, 2021	Initial release

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