ISL78010EVAL1Z

Evaluation Board

AN1523
Rev 0.00
January 14, 2010

The ISL78010EVAL1Z evaluation board is used to demonstrate the performance of the ISL78010 IC used for automotive grade TFT-LCD power supply solution.

The top side and the bottom side of ISL78010EVAL1Z are shown in Figures 1 and 2, respectively. This board consists of power and load connectors for source and load side, external passive components, and the place holders reserved for the following applications:

1. Place holder for second stage positive charge pump for high voltage application at V_{ON} rail.
2. Place holder for additional external compensation.
3. Place holder for snubber circuits to improve EMI performance.

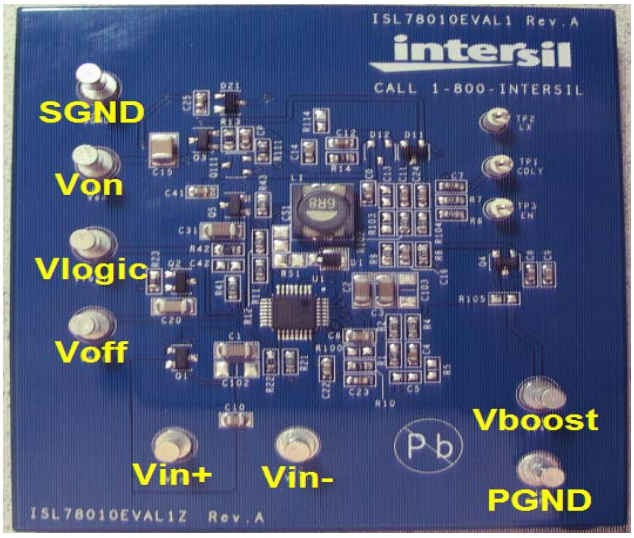


FIGURE 1. TOP VIEW OF ISL78010EVAL1Z

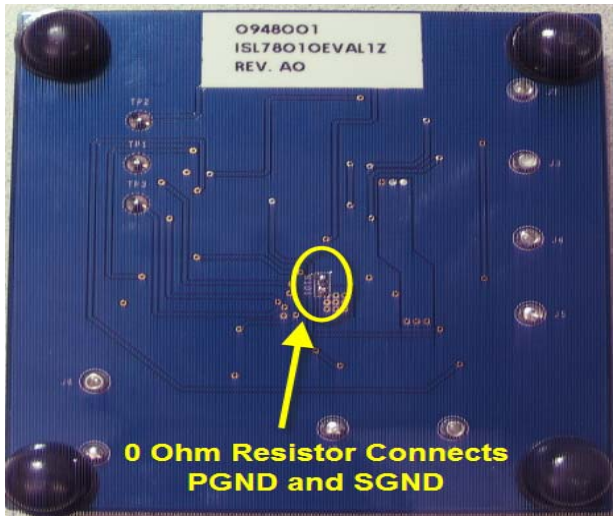


FIGURE 2. BOTTOM VIEW OF ISL78010EVAL1Z

The input voltage range is from 3V to 5V, and the maximum output voltage on main boost rail is 20V.

Reference Documents

- ISL78010 Data Sheet (FN6501)

Key Features

- 2A current FET
- 3V to 5V input
- Up to 20V boost output
- 1% regulation on boost output
- V_{LOGIC}-V_{BOOST}-V_{OFF}-V_{ON} or V_{LOGIC}-V_{OFF}-V_{BOOST}-V_{ON} sequence control
- Programmable sequence delay
- Fully fault protected
- Thermal shutdown
- Internal soft-start
- 32 Ld 5x5 TQFP packages
- Pb-free plus anneal available (RoHS compliant)

Recommended Equipment

The following materials are recommended to perform testing:

- 0V to 10V Power Supply with at least 5A source current capability
- Electronic Loads capable of sinking current up to 5A
- Digital Multimeters (DMMs)
- 100MHz quad-trace oscilloscope

Quick Setup Guide

1. Set power source to be 5V and with 0.5A current limiting.
2. Apply 5V to the input: J1 (V_{IN+}) is input+, J2 (V_{IN-}) is input-. Check the power source to make sure that no current limiting occurs.
3. Release the input power source's current limiting to 5A.
4. Turn off the input power source. Set the electronic load to constant current load of 100mA, connect the electronic load to the V_{BST} output: J6 (V_{BST}) is output+, J8 (PGND) is output-.
5. Turn on the input power source, verify the output voltage is around 12V for V_{BST} (J6, J8).
6. Verify that the ripple voltage (about 1MHz frequency) for the V_{BST} voltage is around 50mV.
7. Verify the voltage at V_{ON} rail (between J3 and J7) is 20V.
8. Verify the voltage at V_{LOGIC} rail (between J4 and J7) is 2.5V.
9. Verify the voltage at V_{OFF} rail (between J5 and J7), is -8V.

Quick Start to Measure the Boost Output Voltage

The evaluation board can be evaluated simply. Figure 3 shows the quick configuration to measure the boost rail output voltage. After powering on the input power supply, the oscilloscope probes can be placed at V_{BST} pin to check the output voltage, and at LX pin to check the phase node voltage.

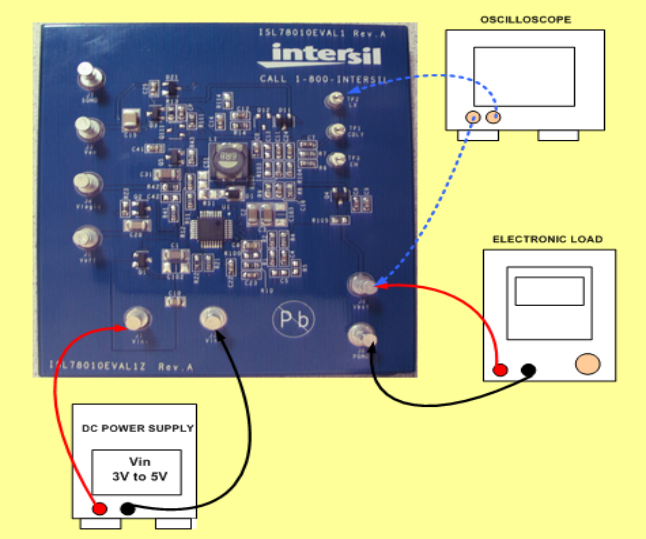


FIGURE 3. QUICK SET UP TO MEASURE THE V_{BST} VOLTAGE

Efficiency Measurement

Figure 4 shows the efficiency measurement set up for the ISL78010EVAL1Z Eval Board. The voltage and current meter can be used to measure input/output voltage and current. In order to obtain an accurate measurement and prevent the voltage drop of PCB or wire trace, the voltage meter must be close to the input/output terminals.

The efficiency equation is shown in Equation 1:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} \bullet I_{OUT})}{(V_{IN} \bullet I_{IN})} \qquad \text{(EQ. 1)}$$

As shown in Figure 4, the measuring point for the input voltage meter is at the C_{10} terminal, and the measuring point for the output voltage meter is at the C_9 terminal.

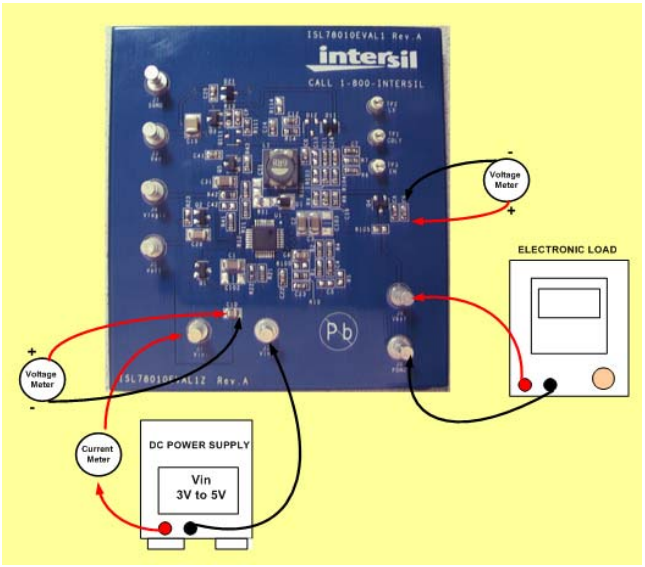


FIGURE 4. EFFICIENCY MEASUREMENT SET UP

Output Ripple / Noise Measurement

The total noise is equal to the sum of the ripple and noise components. Simple steps should be taken to assure that there is minimum pickup noise due to the high frequency events, which can be magnified by the large ground loop formed by the oscilloscope probe ground. This means that even a few inches of ground wire on the oscilloscope probe may result in hundreds of millivolts of noise spikes when improperly routed or terminated. This effect can be overcome by using the short loop measurement method to minimize the measurement loop area for reducing the pickup noise. The short loop measurement method is shown in Figure 5. For ISL78010EVAL1Z evaluation board, the output ripple/noise measurement point is located at the C_9 terminal.

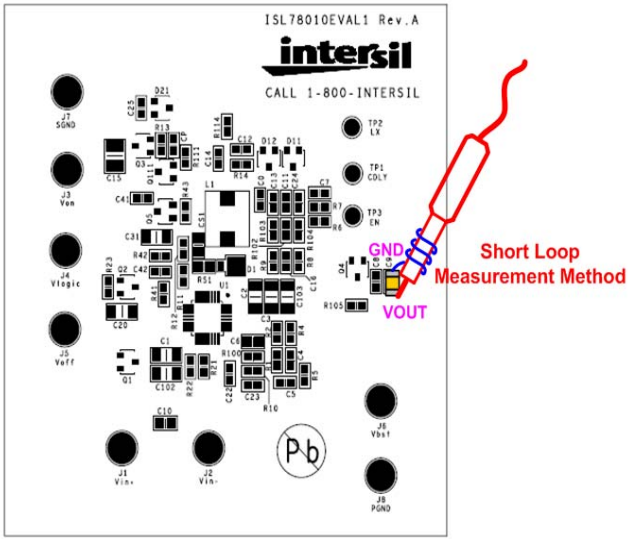
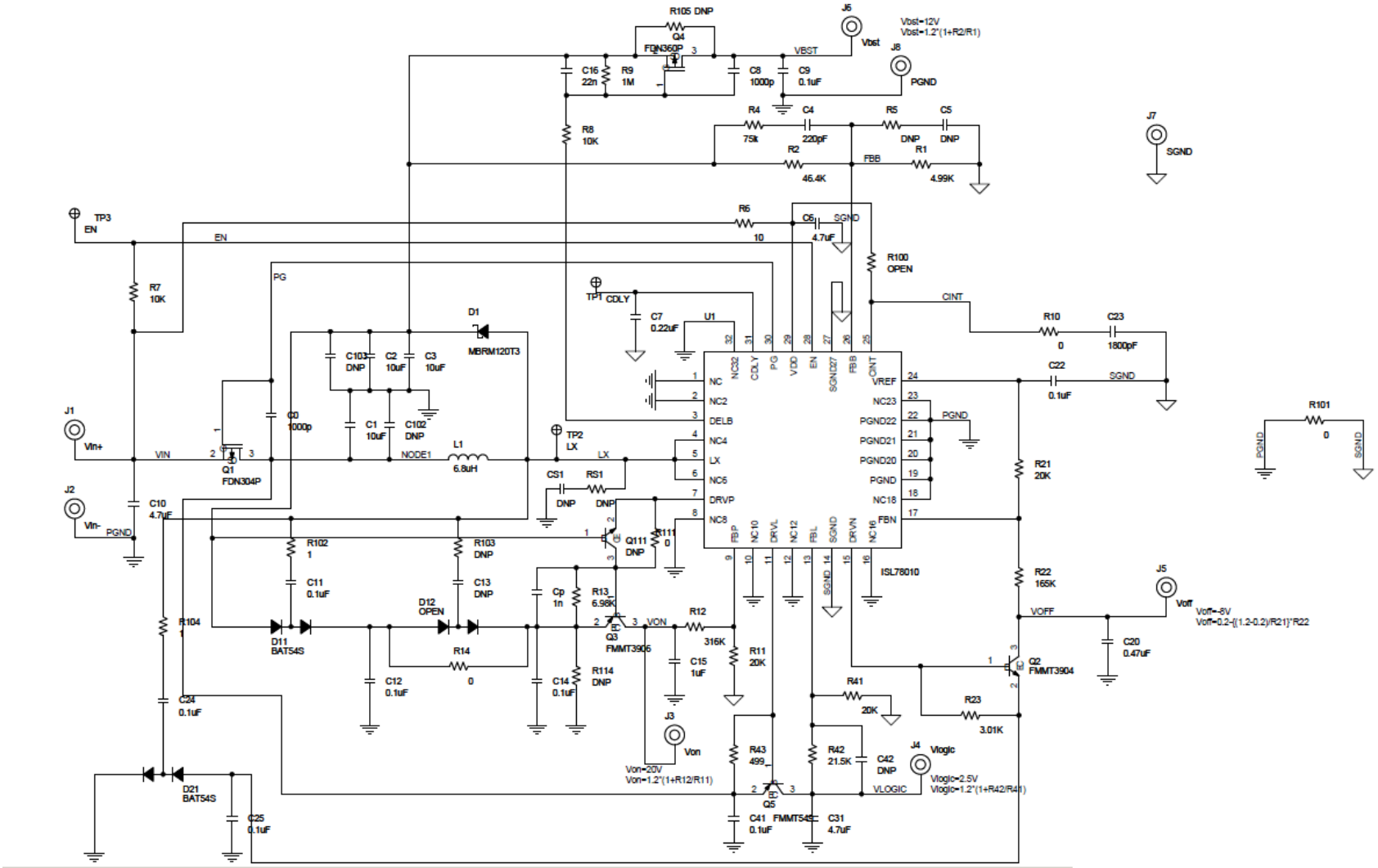


FIGURE 5. OUTPUT RIPPLE/NOISE MEASUREMENT

ISL78010EVAL1Z Eval Board Application Diagram



ISL78010EVAL1Z Eval Board Bill of Materials (BOM)

DEVICE #	DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
Cp, C0, C8	CAP, SMD, 0603, 1000pF, 16V, 10%, X7R, RoHS	VENKEL	C0603X7R160102KNE
C9, C11, C12, C14, C22, C24, C25, C41	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, RoHS	TDK	C1608X7R1H104K
C23	CAP, SMD, 0603, 1800pF, 50V, 10%, X7R, RoHS	MURATA	GRM39X7R182K050AQ
C4	CAP, SMD, 0603, 220pF, 50V, 10%, X7R, RoHS	MURATA	GRM188R71H221KA01D
C16	CAP, SMD, 0603, 0.022µF, 25V, 10%, X7R, RoHS	MURATA	GRM39X7R223K025AQ
C7	CAP, SMD, 0603, 0.22µF, 16V, 10%, X7R, RoHS	TDK	C1608X7R1C224K
C6, C10	CAP, SMD, 0805, 4.7µF, 16V, 10%, X5R, RoHS	MURATA	GRM21BR61C475KA88L
C1, C2, C3	CAP, SMD, 1206, 10µF, 25V, 10%, X5R, RoHS	VENKEL	C1206X5R250-106KNE
C20	CAP, SMD, 1206, 0.47µF, 25V, 10%, X7R, RoHS	PANASONIC	ECJ-3YB1E474K
C31	CAP, SMD, 1206, 4.7µF, 16V, 10%, X7R, RoHS	MURATA	GRM31CR71C475KA01L
C15	CAP, SMD, 1210, 1µF, 50V, 10%, X7R, RoHS	VENKEL	C1210X7R500-105KNE
L1	COIL-PWR INDUCTOR, SMD, 7.3X6.8mm, 6.8µH, 20%, 2.8A, RoHS	TDK	RLF7030T-6R8M2R8
J1-J8	CONN-TURRET, TERMINAL POST, TH, RoHS	KEYSTONE	1514-2
TP1-TP3	CONN-MINI TEST POINT, VERTICAL, WHITE, RoHS	KEYSTONE	5002
D11, D21	DIODE-SCHOTTKY, SMD, SOT23, 3P, 30V, 200mA, DUAL DIODE	FAIRCHILD	BAT54S
D1	DIODE-SCHOTTKY, SMD, POWERMITE, 20V, 1A, RoHS	ON SEMI	MBRM120ET1G
U1	IC-TFT-LCD POWER SUPPLY, 32P, TQFP, 5x5, RoHS	INTERSIL	ISL78010ANZ
Q1	TRANSIST-MOS, P-CHANNEL, SMD, SUPERSOT3, -20V, -2.4A, RoHS	FAIRCHILD	FDN304P
Q2	TRANSISTOR-NPN, SMD, SOT-23, 40V, 200mA, 350mW, RoHS	FAIRCHILD	MMBT3904
Q3	TRANSISTOR-PNP, SMD, SOT-23, 40V, 200mA, 350mW, RoHS	FAIRCHILD	MMBT3906
Q4	TRANSIST-MOS, P-CHANNEL, SMD, SUPERSOT3, -30V, -2A, RoHS	FAIRCHILD	FDN360P
Q5	TRANSISTOR, PNP, SMD, SOT23, -30V, -1A, 500mW, RoHS	FAIRCHILD	FMMT549
R102, R104	RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-1R00FT
R6	RES, SMD, 0603, 10Ω, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-10R0FT
R10, R14, R101, R111	RES, SMD, 0603, 0Ω, 1/10W, TF, RoHS	VENKEL	CR0603-10W-000T
R7, R8	RES, SMD, 0603, 10k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-1002FT
R9	RES, SMD, 0603, 1M, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-1004FT

ISL78010EVAL1Z Eval Board Bill of Materials (BOM) (Continued)

DEVICE #	DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
R22	RES, SMD, 0603, 165k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-1653FT
R11, R21, R41	RES, SMD, 0603, 20k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-2002FT
R42	RES, SMD, 0603, 21.5k, 1/10W, 1%, TF, RoHS	VENKEL	9C06031A2152FKHFT
R23	RES, SMD, 0603, 3.01k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-3011FT
R12	RES, SMD, 0603, 316k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-3163FT
R2	RES, SMD, 0603, 46.4k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-4642FT
R43	RES, SMD, 0603, 499Ω, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-4990FT
R1	RES, SMD, 0603, 4.99k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-4991FT
R13	RES, SMD, 0603, 6.98k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-6981FT
R4	RES, SMD, 0603, 75.0k, 1/10W, 1%, TF, RoHS	VENKEL	CR0603-10W-7502FT
Bottom four corners.	BUMPONS, 0.44inW x 0.20inH, DOMETOP, BLACK	3M	SJ-5003SPBL
Place assy in bag.	BAG, STATIC, 5x8, ZIP LOC	INTERSIL	212403-013
CS1, C5, C13, C42, C102, C103	Do Not Populate Or Purchase (DNP)		
D12	Do Not Populate Or Purchase (DNP)		
Q111	Do Not Populate Or Purchase (DNP)		
RS1, R5, R100, R103, R105, R114	Do Not Populate Or Purchase (DNP)		

ISL78010EVAL1Z Board Layout

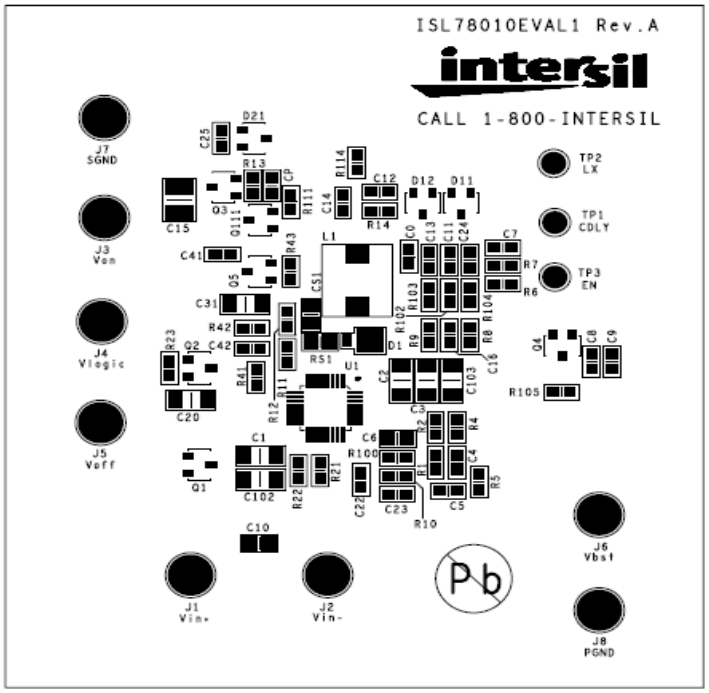


FIGURE 6. TOP COMPONENTS

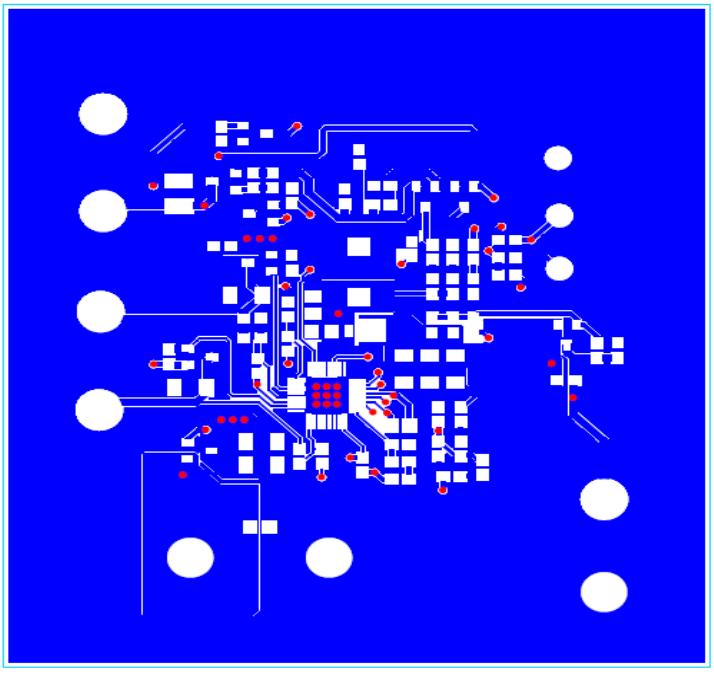


FIGURE 7. TOP LAYER ETCH

ISL78010EVAL1Z Board Layout (Continued)

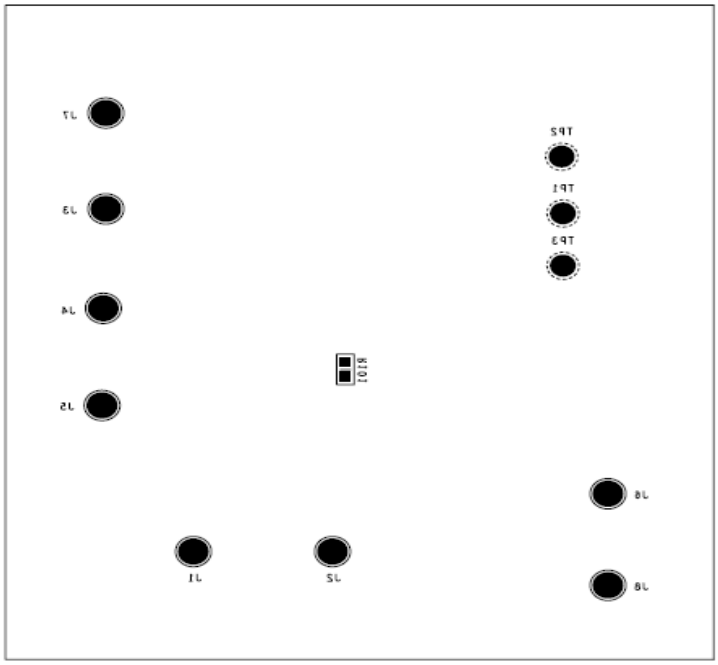


FIGURE 8. BOTTOM LAYER COMPONENTS (MIRROR)

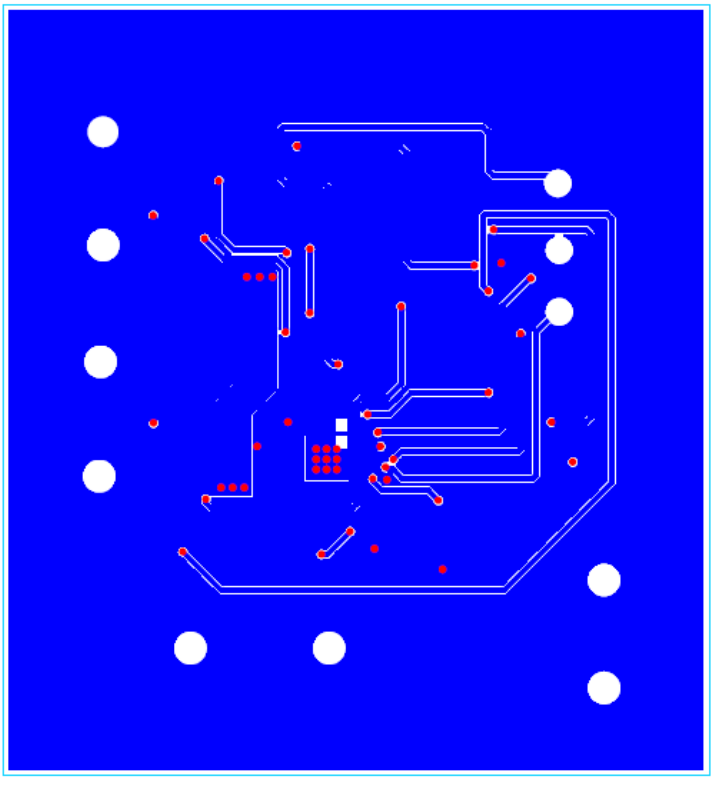


FIGURE 9. BOTTOM LAYER ETCH (MIRROR)