ISL78264

Automotive Dual Synchronous Buck Controller with Integrated Drivers

The ISL78264 is a dual buck controller that can operate across a wide V_{IN} range of 3.75V to 42V. It is designed to support wide duty-cycle operation for switching frequencies from 200kHz up to 2.2MHz. To mitigate EMI, it supports synchronization to an external clock or programmable spread spectrum clocking. Its current-mode modulator is ideally suited to tolerate severe line transients. Also, the ISL78264 supports dropout operation and low 25ns on-time to operate through automotive cranking and load dump pulses.

The ISL78264 integrates robust MOSFET drivers and readily supports step-down applications requiring high output currents in normal operation. For applications that must also sustain extremely low power, always-on operation, its energy conservation mode can reduce operating current to 6µA. Integrated feedback for VOUT1 is provided for 3.3V or 5V applications to eliminate the current otherwise flowing in external feedback resistors. An automatic switchover to an external supply is also supported to maximize efficiency. A blocking diode is activated after startup to prevent the external supply from back-biasing a low input voltage at VIN.

The ISL78264 is qualified to AEC-Q100 Grade 1, specified to operate across an ambient temperature range of -40°C to 125°C, and is available in a 5mmx5mm, 32 Ld WFQFN (Wettable Flank) package.

Features

- V_{IN} operating range: 3.75V to 42V
- Low quiescent current: 6µA typical, one channel
- Switching frequency: 200kHz to 2.2MHz
- Dropout mode for high duty-cycle operation
- 25ns on-times for low duty-cycle operation
- External synchronization
- Programmable spread spectrum clocking
- 180° phase shift between channels
- 2A Sourcing/3A sinking MOSFET drivers
- Boot UVLO and programmable boot refresh time
- Extensive protection mechanisms for OV/UV/OC/OT

Table 1. Output Configurations

VOUT1 Selection	VOUT2 Selection
3.3V	Adjustable 0.8V to 32V
5.0V	
Adjustable 0.8V to 5V	

Applications

- Automotive 12V Systems
- Infotainment/Multimedia Systems
- Cockpit safety systems
- Advanced Driver Assist Systems (ADAS)

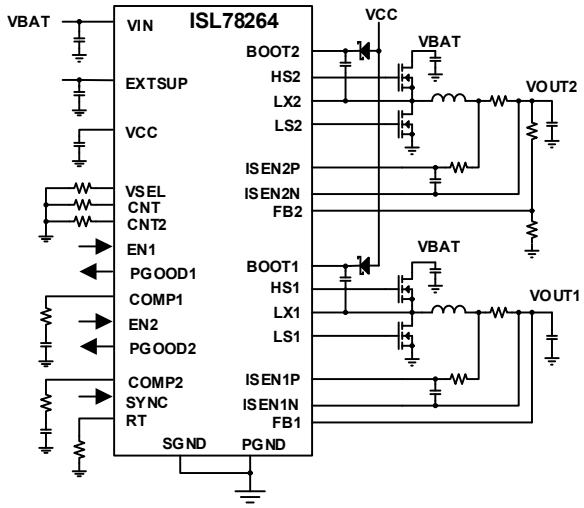


Figure 1. Typical Application Schematic

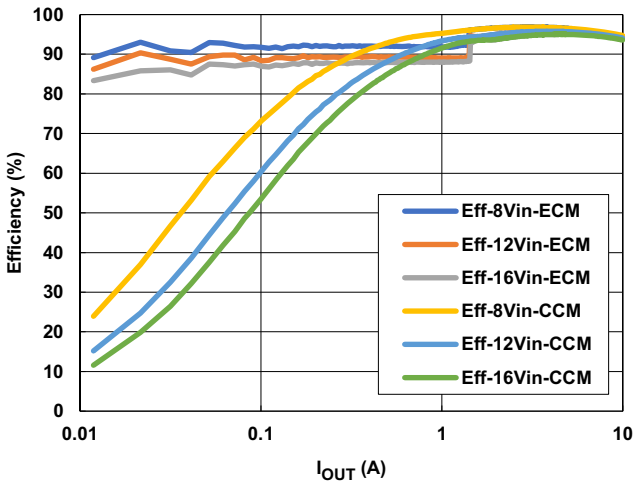


Figure 2. Buck 1 Efficiency VOUT1 = 5V at 400 kHz

Contents

1. Overview

1.1 Typical Application Schematics

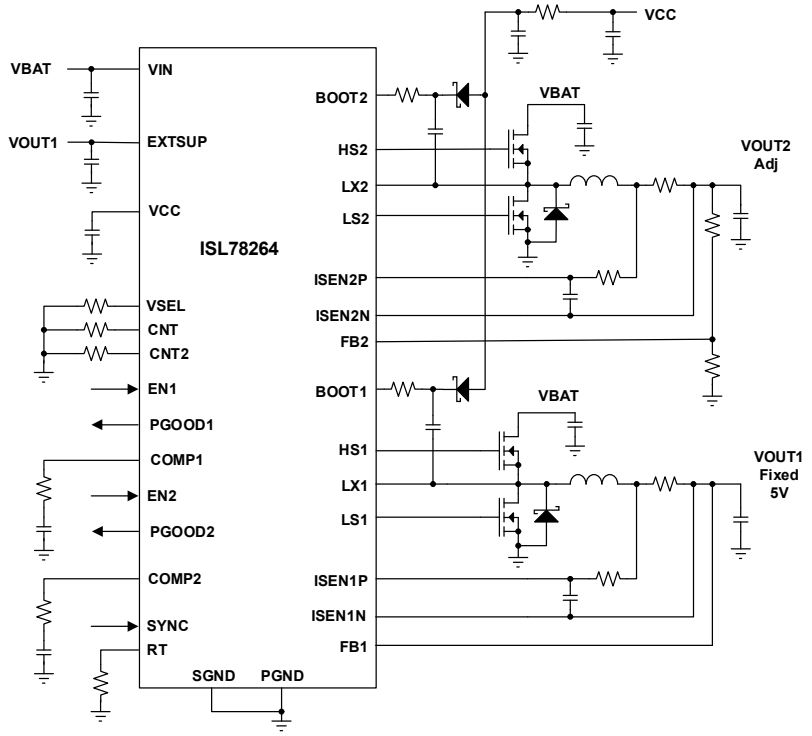


Figure 3. Channel 1 Fixed at 5V

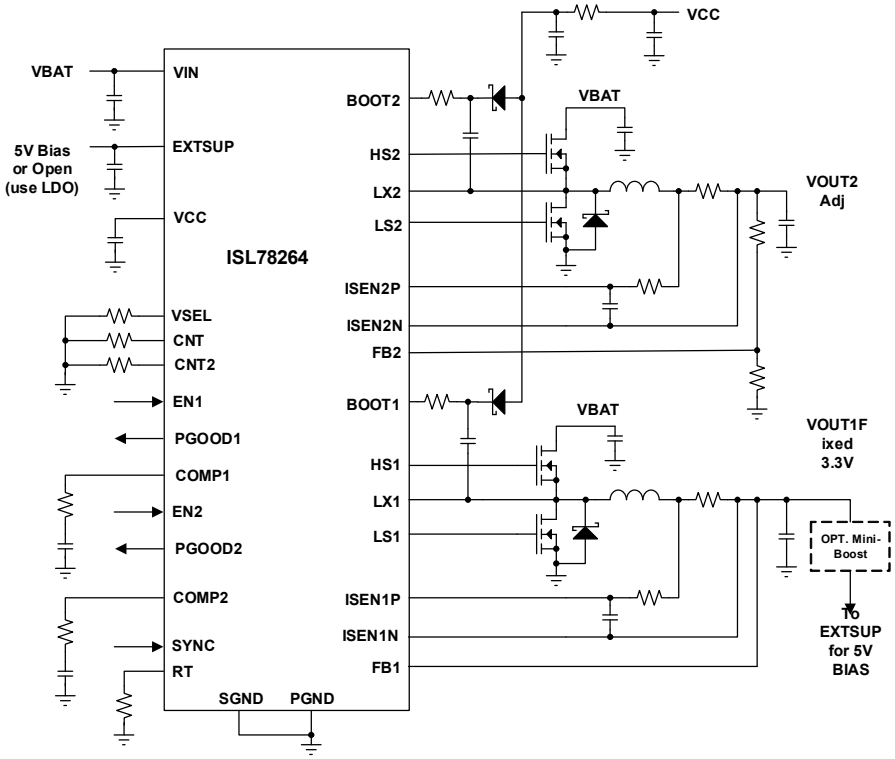


Figure 4. Channel 1 Fixed at 3.3V

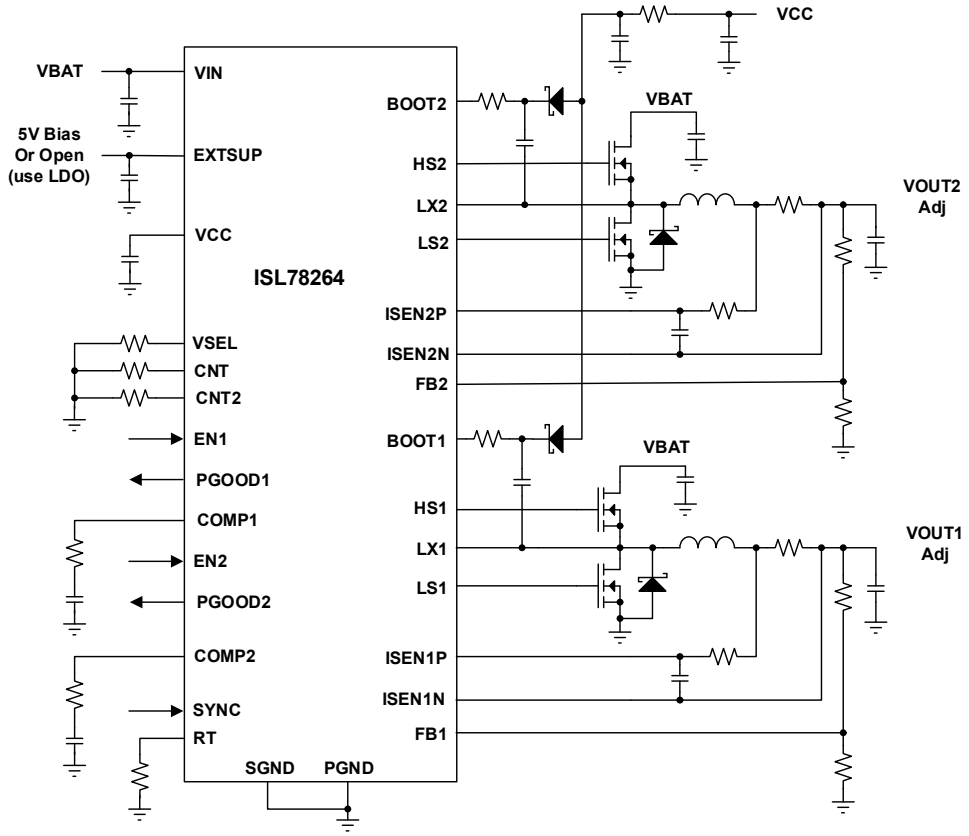


Figure 5. Both Channels Adjustable Output

1.2 Block Diagram

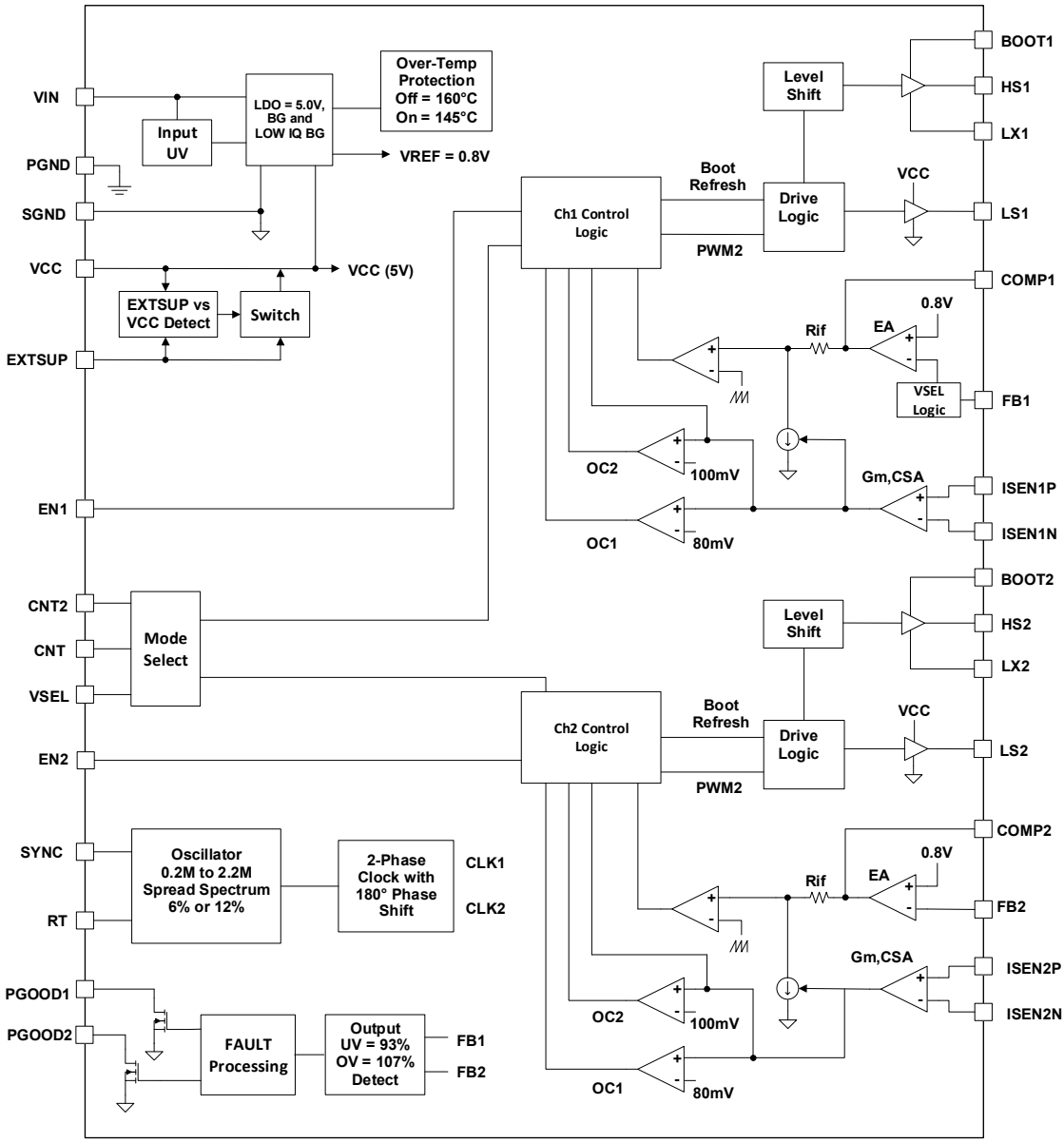


Figure 6. Block Diagram

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp Range (°C)
ISL78264ARZ	ISL7826 4ARZ	32 Ld 5x5 WFQFN	L32.5x5H	Tube	-40 to +125°C
ISL78264ARZ-T				6k	
ISL78264ARZ-T7A				250	
ISL78264EVAL1Z	Evaluation Board				

Notes:

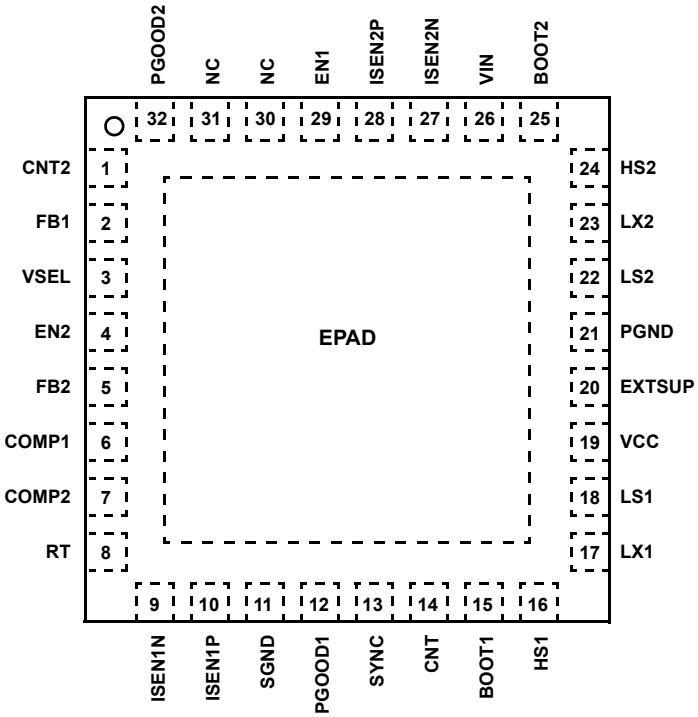
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78264 device page. For more information about MSL see TB363.

Table 2. Key Differences Between Family of Parts

Part #	Channel 1	Channel 2	Channel 1 Output Range	Channel 2 Output Range
ISL78263	Buck	Boost	3.3V, 5V, 0.8V to 5V Adjustable	5V to 40V Adjustable
ISL78264	Buck	Buck	3.3V, 5V, 0.8V to 5V Adjustable	0.8V to 32V Adjustable

1.4 Pin Configuration

32 Ld, 5x5 WFQFN



1.5 Pin Descriptions

Pin #	Pin Names	Description
1	CNT2	This pin sources a current at startup and reads the voltage across a resistor to ground to program internal boot refresh on-time of the low-side switch for 180ns or 360ns (see Table 5 on page 18).
2	FB1	Feedback pin for Channel 1 buck. For fixed output voltages of 5.0V or 3.3V, this pin is connected directly to the output of Channel 1 buck. For an adjustable output, this pin connects to a resistive divider from Channel 1 output to ground, and the FB1 voltage is regulated to 0.8V.
3	VSEL	This pin sources a current at startup and reads the voltage across a resistor to ground to program the Channel 1 buck output to a fixed voltage of 5.0V or 3.3 V, or as an adjustable voltage in the range of 0.8V to 5.0V (see Table 3 on page 17).
4	EN2	Enable control pin of Channel 2 with a logic high voltage enabling operation of Channel 2.
5	FB2	Feedback pin for Channel 2 buck regulator with adjustable output. This pin connects to a resistive divider from Channel 2 output to ground, and the FB2 voltage is regulated to 0.8V.
6	COMP1	Loop compensation pin for Channel 1 with a resistor/capacitor network connected to ground to provide control loop compensation for Channel 1 buck regulator.
7	COMP2	Loop compensation pin for Channel 2 with a resistor/capacitor network connected to ground to provide control loop compensation for Channel 2 buck regulator.

Pin #	Pin Names	Description
8	RT	A resistor from RT to GND programs the buck switching frequency for Channel 1 and Channel 2, with Channel 2 shifted 180° in phase from Channel 1 to minimize input ripple current. This pin is pulled to ground while in ECM and is otherwise 0.5V.
9	ISEN1N	Output current sense pin connected to the negative terminal of the current sense resistor, also connected to the output voltage of Channel 1.
10	ISEN1P	Output current sense pin connected to the junction of the positive terminal of the current sense resistor and the power inductor of Channel 1.
11	SGND	Analog GND for the IC, connect to the PGND pin in the top copper trace under the IC.
12	PGOOD1	Power-good pin for Channel 1 with an open-drain output, producing a low output if the Channel 1 output is not within ±7% (typical) of the programmed output voltage, and a logic high output if the output is within regulation.
13	SYNC	Connect SYNC to an external clock in the range of 200kHz to 2.4MHz to synchronize the internal clock with operation in FCCM. Connect to VCC to force the part into Fixed frequency Continuous Conduction Mode (FCCM) operation using the internal oscillator. Connect to GND to allow the controller to automatically switch between Continuous Conduction Mode, and Diode Emulation Mode (DEM), or ECM mode depending on load current level. In DEM and CCM, the device uses the internal oscillator programmed by RT pin. The pin can be switched during operation (VCC to GND, or GND to VCC) to change the mode of operation.
14	CNT	This pin sources a current at startup and reads the voltage across a resistor to ground to program the spread spectrum (ON/OFF, and frequency variation) and dead time (see Table 4 on page 17).
15	BOOT1	Provides connection point for a ceramic boot capacitor providing high-side gate voltage supply for Channel 1. The capacitor is charged through an external diode connected to VCC through an R-C filter.
16	HS1	The output of Channel 1 high-side MOSFET gate driver.
17	LX1	Connected to the Channel 1 switch node, providing the return path for the high-side MOSFET gate driver back to BOOT1.
18	LS1	The output of Channel 1 low-side MOSFET gate driver swinging between VCC and GND.
19	VCC	Bias supply (5V typical) for the IC and MOSFET gate drivers, and should be decoupled with a ceramic capacitor of 10µF. This pin is supplied by internal LDO during start-up and can be powered from EXTSUP after initial start-up, using the automatic switchover function.
20	EXTSUP	Accepts external bias input of 5V typical that can be supplied from Channel 1 or Channel 2 output of 5V, or an independent supply derived from other sources. If the external bias is applied before VIN is applied then the startup enable circuit should be powered from the external bias source (and not VIN).
21	PGND	Connection point for power ground of the switching circuits for Channel 1 and Channel 2, and serves as the return path for the low-side MOSFET gate drive.
22	LS2	The output of Channel 2 low-side MOSFET gate driver swinging between VCC and GND.
23	LX2	Connected to the Channel 2 switch node, providing the return path for the high-side MOSFET gate driver back to BOOT2.
24	HS2	The output of Channel 2 high-side MOSFET gate driver.
25	BOOT2	Provides connection point for a ceramic boot capacitor providing high-side gate voltage supply for Channel 2. The capacitor is charged through an external diode connected to VCC.
26	VIN	Connected to the high voltage input supply for the buck regulators, and is normally supplied from a battery. This pin is decoupled using a 0.1µF or larger ceramic capacitor.
27	ISEN2N	Output current sense pin connected to the negative terminal of the current sense resistor, also connected to the output voltage of Channel 2.
28	ISEN2P	Output current sense pin connected to the junction of the positive terminal of the current sense resistor and the power inductor of Channel 2.
29	EN1	Enable control pin of Channel 1 with a logic high voltage enabling operation of Channel 1. For the initial start-up, this pin can be connected to the VIN supply through a 100kΩ resistor.
30, 31	NC	Not internally connected; leave unconnected or tie to GND.
32	PGOOD2	Power-good pin for Channel 2 with an open-drain output, producing a low output if the Channel 2 output is not within ±7% (typical) of the programmed output voltage, and a logic high output if the output is within regulation.
	EPAD	The bottom pad of the IC, to be connected to PGND and SGND under the IC. Connect to internal PCB GND layers using multiple vias.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VIN, EN1, FB2, ISEN2N and ISEN2P	-0.3	45	V
HS1, HS2, LX1, LX2, BOOT1, BOOT2	-0.3	65	V
EN2, FB1,COMP1, COMP2, PGOOD1, PGOOD2, CNT, RT, SYNC	-0.3	6.5	V
ISEN1N and ISEN1P, LS1, LS2, VCC, EXTSUP, VSEL,CNT2	-0.3	6.5	V
All Other Pins	-0.3	6.5	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per AEC-Q100-002)	2		kV
Charged Device Model (Tested per AEC-Q100-001)	750		V
Latch-Up (Tested per AEC-Q100-004)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld 5x5 WFQFN Package (Notes 4, 5)	30	1.2

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+125	°C
Start-Up Voltage Range V_{IN}	6.0	42	V
Supply Voltage Range V_{IN} (EXTSUP ≥4.2V after start-up)	3.75	42	V
Buck CH1 V_{OUT} Fixed options	3.3	5.0	V
Buck CH1 V_{OUT} Adjustable Range	0.8	5	V
Buck CH2 V_{OUT} Adjustable Range	0.8	32	V

2.4 Electrical Specifications

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
Power Supply						
V_{IN} Undervoltage Lockout Threshold	$V_{IN,UVLO}$	Rising	**5.455**	5.650	**5.845**	V
V_{IN} Supply Current in Low Power Mode	I_{QLPM}	ECM mode, no external load on V_{OUT} (Note 8)		6		µA
V_{IN} Supply Current During Normal Switching (includes EXTSUP)	I_Q	PWM mode, no external load on V_{OUT}, EN1 = EN2 = HIGH, f_{SW} = 2.2MHz, gate drive no load		11	**25**	mA
V_{IN} Supply Current, Shutdown	I_{SD}	EN1 = EN2 = SGND		0.3	**6**	µA
LDO and EXTSUP						
Output Voltage of Internal LDO	V_{VCC}	V_{IN} = 6.0V to 42V, I_{OUT} = 130mA	**4.75**	5	**5.25**	V
Output Current of Internal Regulator	I_{VCC}	V_{IN} = 6.0V to 42V			**0.13**	A
Dropout Voltage of Internal Regulator	D_{VCC}	V_{IN} = 4.5V, I_{LDO} = 130mA			**1**	V
LDO Current Limit	I_{LMTLDO}	V_{CC} = 4.5V	**130**		**250**	mA
LDO Current Limit	I_{LMTLDO}	V_{CC} = 0V	**130**		**250**	mA
VCC Undervoltage Lockout Threshold	$V_{CC,UVLO}$	Falling	**3.8**	4.0	**4.1**	V
External Bias Voltage	V_{EXTSUP}	For V_{OUT} buck = 5V ±5%	**4.75**	5	**5.25**	V
External Bias Voltage Switchover Threshold	VTH_{EXTSUP}	Rising	**4.462**	4.6	**4.738**	V
		Falling	**4.268**	4.4	**4.532**	V
		Hysteresis	**0.15**	0.2	**0.25**	V
Oscillator, Spread Spectrum						
Internal Switching Frequency	f_{SW}	RT to GND resistor = 86.6kΩ	**0.18**	0.2	**0.22**	MHz
Internal Switching Frequency	f_{SW}	RT to GND resistor = 6.81kΩ	**2.0**	2.2	**2.4**	MHz
External Switching Frequency	f_{SW}	Applied to SYNC pin	**0.2**		**2.4**	MHz
RT Pin Voltage	V_{RT}			0.5		V
Spread Spectrum Narrow Mode	F_{SSNAR}	Spread Spectrum ON narrow mode, see CNT configuration Table 4 on page 17		+6		%
Spread Spectrum Wide Mode	F_{SSWID}	Spread Spectrum ON wide mode, see CNT configuration Table 4 on page 17		+12		%
Controller 1 Specification (Buck)						
Output Voltage	V_{OUTCH1}	VSEL to GND resistor = 6.04kΩ, see VSEL configuration Table 3 on page 17	**3.2505**	3.3	**3.3495**	V
Output Voltage	V_{OUTCH1}	VSEL to GND resistor = 75kΩ, see VSEL configuration Table 3 on page 17	**4.925**	5.0	**5.075**	V
FB1 Pin Voltage Regulation (Adjustable)	$V_{FBCH1ADJ}$	VSEL to GND resistor = 37.4kΩ, see VSEL configuration Table 3 on page 17	**0.788**	0.8	**0.812**	V
V_{OUT} Comparator Threshold at ECM	V_{FBCH1}	V_{OUT} = 3.3V	**3.234**	3.3	**3.366**	V
	V_{FBCH1}	V_{OUT} = 5.0V	**4.9**	5.0	**5.1**	V
	$V_{FBCH1ECM}$	V_{FB} = 0.8V in adjustable VOUT mode	**0.784**	0.80	**0.816**	V
FB Pin Leakage Current	I_{FBCH1}				**0.25**	µA
Forward CH1 Cycle-by-Cycle Current Limit	$I_{LMT1CH1+}$		**64**	80	**100**	mV
Forward CH1 Hiccup Current Limit	$I_{LMT2CH1+}$		**80**	100	**124**	mV

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
Reverse CH1 Current Limit	$I_{LMTCH1-}$		**-50**	-40	**-33**	mV
CH1 Zero Cross	I_{ZCDCH1}		**-4**	2	**9**	mV
CH1 Dead Time	T_{DTLH1S}	Low-side low to high-side high, see CNT configuration Table 4 on page 17	**15**	27	**40**	ns
	T_{DTHL1S}	High-side low to low-side high, see CNT configuration Table 4 on page 17	**30**	43	**70**	ns
	T_{DTLH1L}	Low-side low to high-side high, see CNT configuration Table 4 on page 17	**70**	100	**120**	ns
	T_{DTHL1L}	High-side low to low-side high, see CNT configuration Table 4 on page 17	**70**	100	**120**	ns
CH1 Max Duty	$T_{DTMAXCH1}$	V_{IN} = 4.5V	**97**	98.75		%
CH1 Min ON Time	$T_{ONMINCH1}$		**15**	25	**35**	ns
CH1 Min OFF Time	$T_{OFFMINCH1}$		**30**	40	**55**	ns
CH1 Soft-Start Time	T_{SSCH1}			4.5		ms
CH1 Buck Error Amp (OTA) GM	$CH1_{EAOTA}$			1.7		mS
Boot Refresh	$V_{BRFRESH}$	Rising	**3.3**	3.5	**3.7**	V
		Falling	**3.2**	3.4	**3.6**	V
		Hysteresis	**0.04**	0.08	**0.160**	V
CH1 Overvoltage Protection	$CH1_{OVP}$	Rising	**105**	107	**109**	%
		Falling	**103**	105	**107**	%
		Hysteresis	**1.5**	2.2	**3**	%
CH1 Undervoltage Protection	$CH1_{UVP}$	Rising	**93**	95	**97**	%
		Falling	**91**	93	**95**	%
		Hysteresis	**1.5**	2.2	**3**	%
V_{IN} Pulse Skip Threshold	VTH_{PSKIP}	Rising	**18**	18.6	**19.5**	V
		Falling	**17.7**	18.2	**18.7**	V
		Hysteresis	**0.4**	0.55	**0.7**	V
ECM Entry Threshold	VTH_{ECMENT}	Rising VIN	**5.6**	5.7	**5.85**	V
		Falling VIN	**5.3**	5.4	**5.55**	V
		Hysteresis	**0.2**	0.27	**0.35**	V
Controller 2 Specification (Buck)						
FB2 Pin Voltage Regulation	V_{FBCH2}		**0.788**	0.8	**0.812**	V
FB2 Pin Leakage Current	I_{FBCH2}				**0.25**	µA
Forward CH2 Cycle-by-Cycle Current Limit	$I_{LMT1CH2+}$		**64**	80	**100**	mV
Forward CH2 Hiccup Current Limit	$I_{LMT2CH2+}$		**80**	100	**124**	mV
Reverse CH2 Current Limit	$I_{LMTCH2-}$		**-50**	-40	**-33**	mV
CH2 Zero Cross	I_{ZCDCH2}		**-4**	2	**9**	mV

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
CH2 Dead Time	T_{DTLH2S}	Low-side low to high-side high, see CNT configuration Table 4 on page 17	**15**	27	**40**	ns
	T_{DTHL2S}	High-side low to low-side high, see CNT configuration Table 4 on page 17	**30**	43	**70**	ns
	T_{DTLH2L}	Low-side low to high-side high, see CNT configuration Table 4 on page 17	**70**	100	**120**	ns
	T_{DTHL2L}	High-side low to low-side high, see CNT configuration Table 4 on page 17	**70**	100	**120**	ns
CH2 Maximum Duty	$T_{DTMAXCH2}$		**97**	98.75		%
CH2 Minimum ON Time	$T_{ONMINCH2}$		**15**	25	**35**	ns
CH2 Minimum OFF Time	$T_{OFFMINCH2}$		**30**	40	**55**	ns
CH2 Soft-Start Time	T_{SSCH2}			4.5		ms
Buck Error Amp (OTA) GM	$CH2EA_{OTA}$			1.7		mS
Boot Refresh	$V_{BRFRESH}$	Rising	**3.3**	3.5	**3.7**	V
		Falling	**3.2**	3.4	**3.6**	V
		Hysteresis	**0.04**	0.1	**0.16**	V
CH2 Overvoltage Protection	$CH2_{OVP}$	Rising	**105**	107	**109**	%
		Falling	**103**	105	**107**	%
		Hysteresis	**1.5**	2.2	**3**	%
CH2 Undervoltage Protection	$CH2_{UVP}$	Rising	**93**	95	**97**	%
		Falling	**91**	93	**95**	%
		Hysteresis	**1.5**	2.2	**3**	%
V_{IN} Pulse Skip Threshold	VTH_{PSKIP}	Rising	**18**	18.6	**19.5**	V
		Falling	**17.7**	18.2	**18.7**	V
		Hysteresis	**0.4**	0.55	**0.7**	V
ECM Entry Threshold	VTH_{ECMENT}	Rising V_{IN}	**5.6**	5.7	**5.85**	V
		Falling V_{IN}	**5.3**	5.4	**5.55**	V
		Hysteresis	**0.2**	0.27	**0.35**	V
Output Drivers						
High-Side Drive Source Current	$I_{HS,SRC}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V		2		A
High-Side Drive Source Resistance	$R_{HS,SRC}$	100mA source current, V_{BOOT} - V_{LX} = 4.4V		1.2		Ω
High-Side Drive Sink Current	$I_{HS,SNK}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V		2		A
Hide-Side Drive Source Resistance	$R_{HS,SNK}$	100mA sink current, V_{BOOT} - V_{LX} = 4.4V		0.6		Ω
Low-Side Drive Source Current	$I_{LS,SRC}$	V_{LS} - V_{PGND} = 2.5V, VCC = 5V		2		A
Low-Side Drive Source Resistance	$R_{LS,SRC}$	100mA source current, VCC = 5V		1.2		Ω
Low-Side Drive Sink Current	$I_{LS,SNK}$	V_{LS} - V_{PGND} = 2.5V, VCC = 5V		3		A
Low-Side Drive Sink Resistance	$R_{LS,SNK}$	100mA sink current, VCC = 5V		0.55		Ω
Input Pins						
ENABLE Input Low Voltage Threshold	VIL_{EN1}	EN1 = CH1) = buck turned OFF; CH2 can be ON/OFF	0.4	1.0		V
ENABLE Input High Voltage Threshold	VIH_{EN1}	EN1 = CH1 = buck turned ON; CH2 can be ON/OFF		1.2	1.4	V

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ (Note 7)	Max (Note 6)	Unit
ENABLE Leakage Current	ILK_{EN1}		-0.5		0.5	µA
ENABLE Input Low Voltage Threshold	VIL_{EN2}	EN2 = CH2 = buck turned OFF; CH1 can be ON/OFF	0.4	1.0		V
ENABLE Input High Voltage Threshold	VIH_{EN2}	EN2 = CH2 = buck turned ON; CH1 can be ON/OFF		1.2	1.4	V
ENABLE Leakage Current	ILK_{EN2}		-0.5		0.5	µA
SYNC Input Low Voltage	VIL_{SYNC}				0.3xVCC	V
SYNC Input High Voltage	VIH_{SYNC}		0.7xVCC			V
SYNC Pulse Width High	$T_{SYNCMINH}$		**50**			ns
SYNC Pulse Width Low	$T_{SYNCMINL}$		**50**			ns
Switching Frequency SYNC Range	F_{SYNC}		0.2		2.2	MHz
CNT/CNT2/VSEL Level 0 Voltage	V_0				**35**	mV
CNT/CNT2/VSEL Level 1 Voltage	V_1		**75**		**180**	mV
CNT/CNT2/VSEL Level 2 Voltage	V_2		**225**		**360**	mV
CNT/CNT2/VSEL Level 3 Voltage	V_3		**415**		**560**	mV
CNT/CNT2/VSEL Level 4 Voltage	V_4		**615**		**870**	mV
CNT/CNT2/VSEL Level 5 Voltage	V_5		**940**		**1240**	mV
CNT/CNT2/VSEL Level 6 Voltage	V_6		**1.33**		**1680**	V
CNT/CNT2/VSEL Level 7 Voltage	V_7		**1.78**		**VCC**	V
Output Pins						
PGOOD1 Pin Voltage	VOL_{PGOOD1}	V_{OUT1} = OFF; sink current = 3mA	-	0.3	0.6	V
PGOOD2 Pin Voltage	VOL_{PGOOD2}	V_{OUT2} = OFF; sink current = 3mA	-	0.3	0.6	V
PGOOD1 Pin Leakage Current	ILK_{PGOOD1}	V_{PULLUP} = 5V		0.01	1	µA
PGOOD2 Pin Leakage Current	ILK_{PGOOD2}	V_{PULLUP} = 5V		0.01	1	µA
PGOOD1 Pin Filter Delay	T_{PGOOD1}		**10**	15	**20**	µs
PGOOD2 Pin Filter Delay	T_{PGOOD2}		**10**	15	**20**	µs
Thermal Shutdown	T_{OTP}	Rising		160		°C
		Falling		145		°C
		Hysteresis		15		°C

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for T_A = +25°C and V_{IN} = 12V.
8. Quiescent current measurements are taken when the output is not switching.

3. Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V

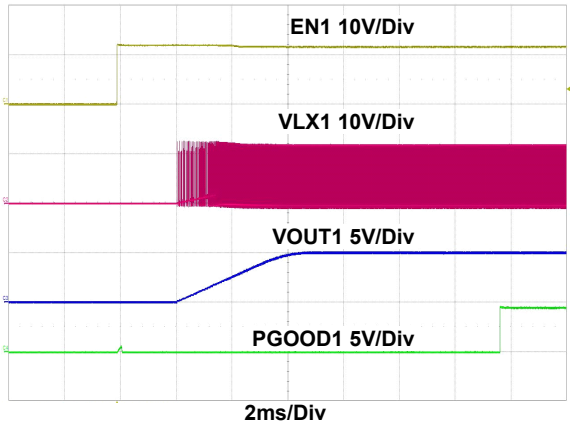


Figure 7. Buck 1 Start-Up with 10 A Load

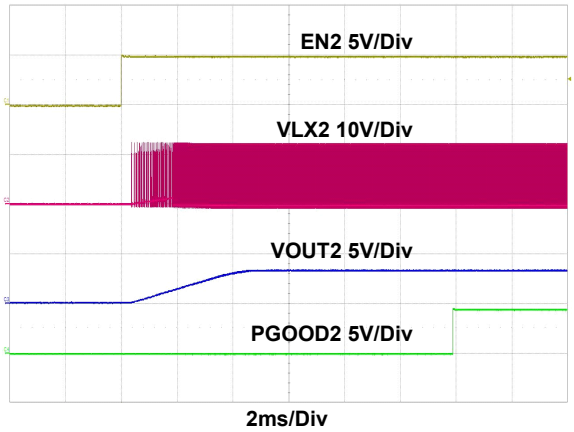


Figure 8. Buck 2 Start-Up with 10 A Load

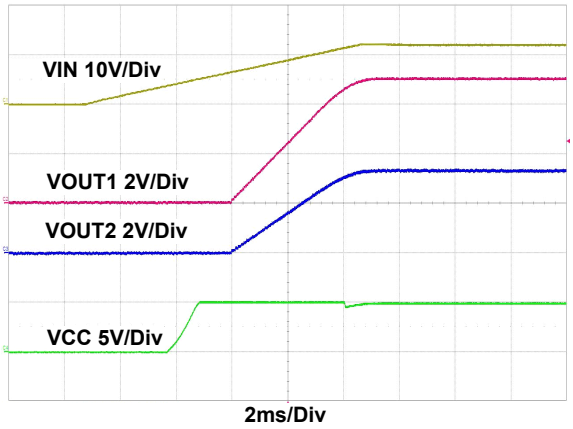


Figure 9. Buck 1/2 Start-Up with V_{IN} Rising

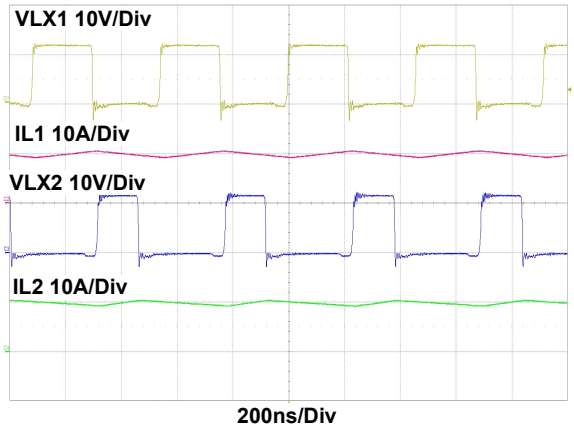


Figure 10. Buck 1/2 with 180 degree Phase Shift)

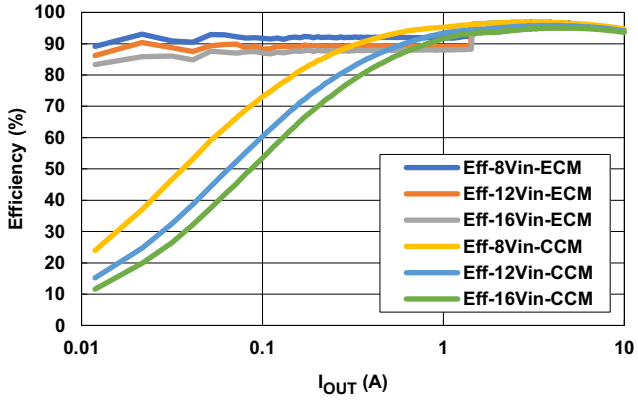


Figure 11. Buck 1 Efficiency VOUT1 = 5V at 400 kHz

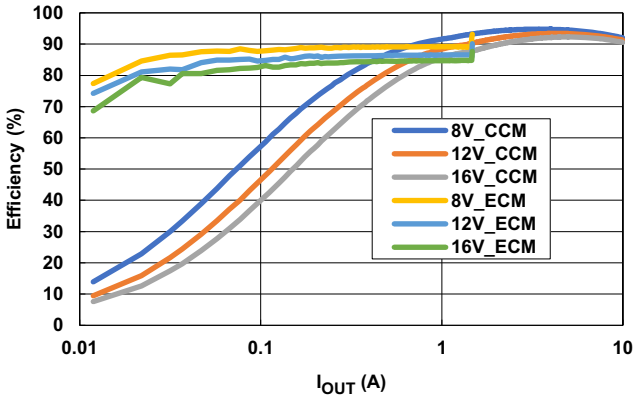


Figure 12. Buck 1 Efficiency VOUT1 = 3.3V at 400 kHz

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V **(Continued)**

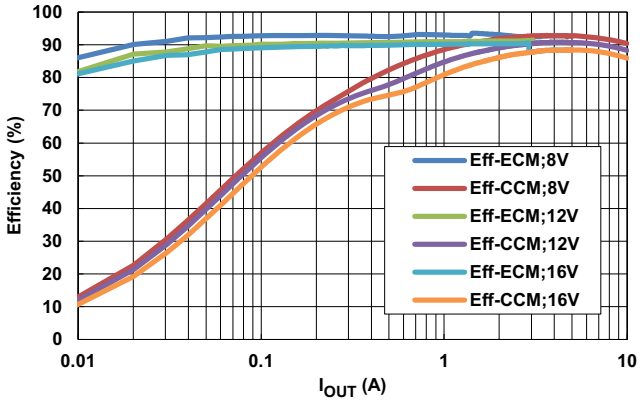


Figure 13. Buck 1 Efficiency VOUT1 = 5V at 2.2MHz

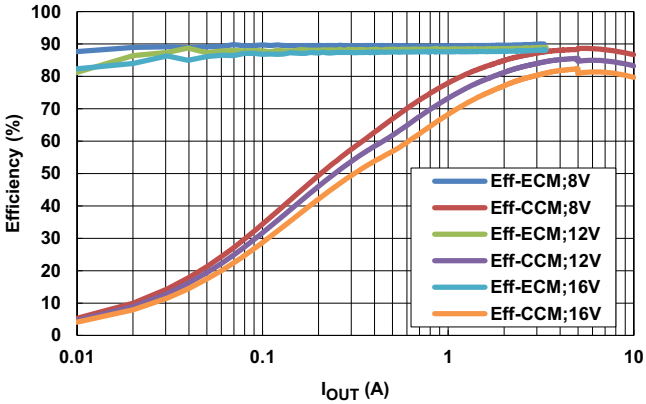


Figure 14. Buck 2 Efficiency VOUT2 = 3.3V at 2.2MHz

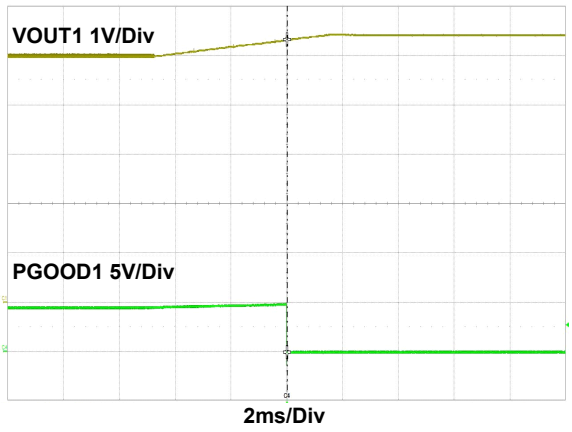


Figure 15. Buck 1 Overvoltage Detection

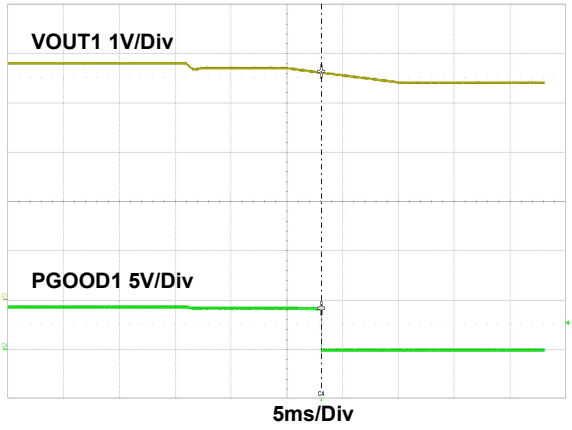


Figure 16. Buck 1 Undervoltage Detection

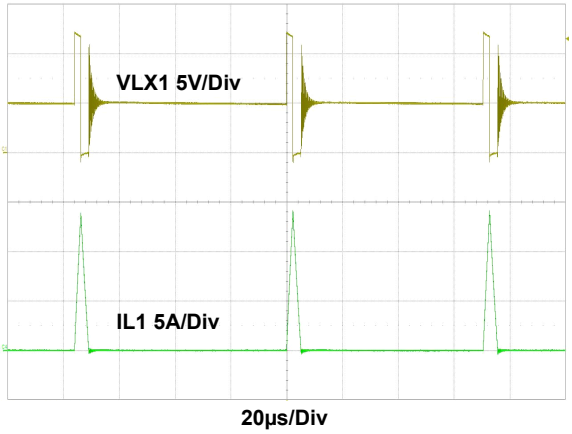


Figure 17. Steady State ECM Operation with Io1 = 0.5 A

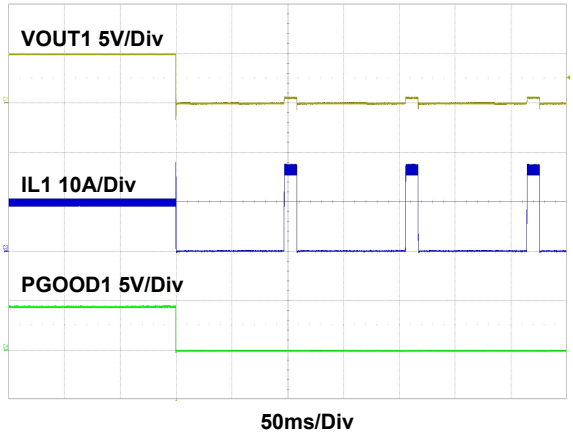


Figure 18. Buck 1 with 10 A Load, then Short Output

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V **(Continued)**

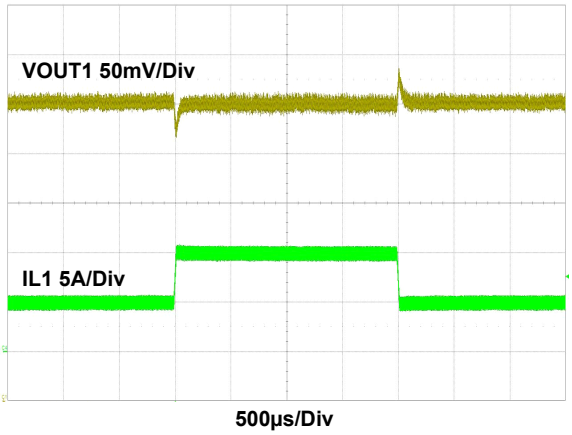


Figure 19. Buck 1 Load Transient from 5A to 10A in FCCM

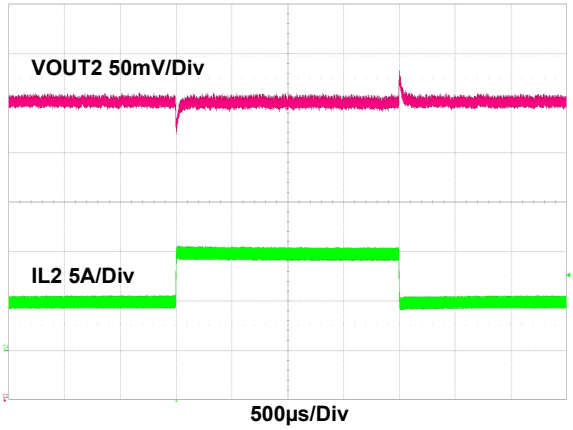


Figure 20. Buck 2 Load Transient from 5A to 10A

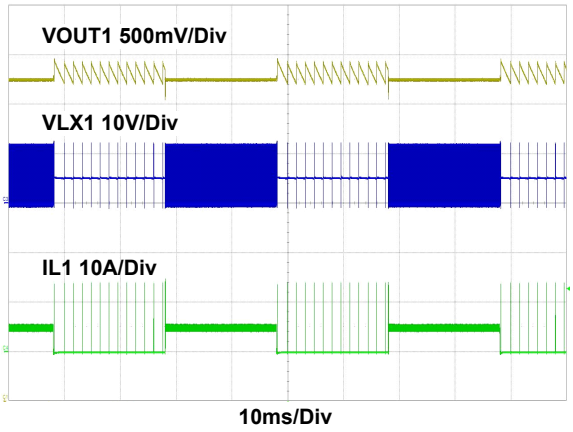


Figure 21. Buck 1 Load Transient from 0A to 5A with ECM

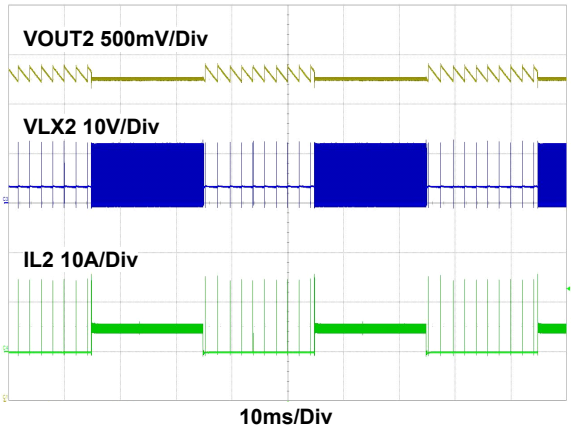


Figure 22. Buck 2 Load Transient from 0A to 5A with ECM

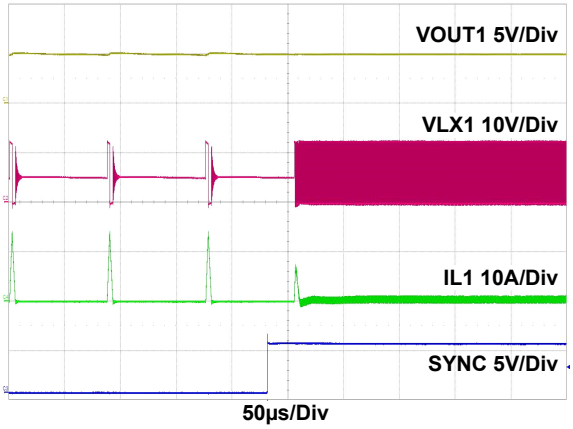


Figure 23. Buck 1 SYNC High ECM Exit

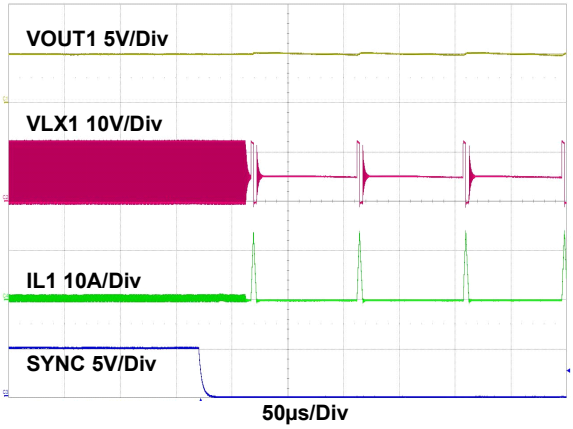


Figure 24. Buck 1 SYNC Low ECM Entry

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 12V, V_{OUT1} = 5V, V_{OUT2} = 3.3V **(Continued)**

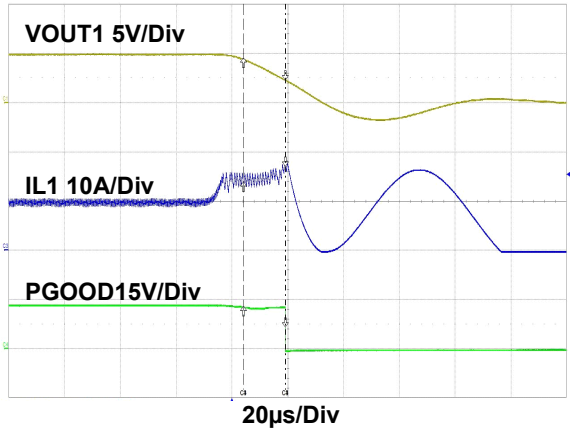


Figure 25. Buck 1 Short-Circuit PGOOD1 Fault Signal; Buck 2 would exhibit similar operation

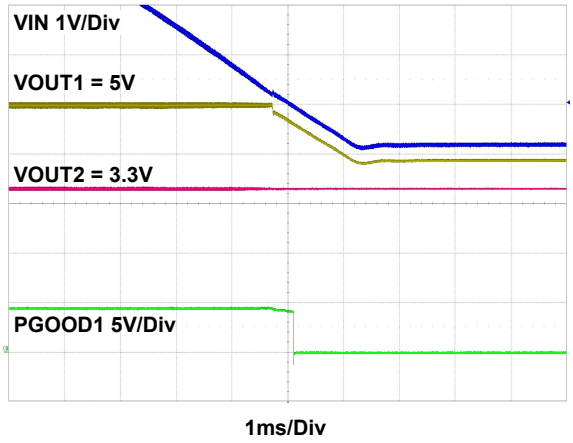


Figure 26. V_{IN} Falling below 4.5V with CH1 Dropout, Ch2 no Dropout

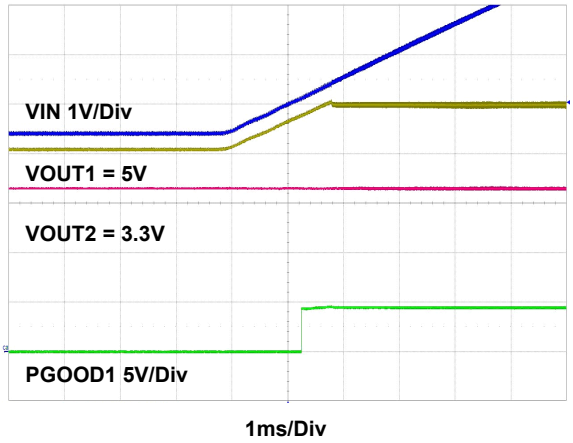


Figure 27. V_{IN} rising from 4.4V after Ch1 in Dropout

4. Functional Description

4.1 Functional Overview

The ISL78264 has controllers that support two DC/DC converters Buck 1 and Buck 2 that can be configured in various modes and operate across a V_{IN} range of 3.75V to 42V. Buck Converter 1 can be configured as a fixed 3.3V, fixed 5.0V, or as an adjustable output buck regulator from 0.8V to 5.0V. Buck Converter 2 has an adjustable output that can be set in the range of 0.8V to 32V. If the proper external components are selected, the ISL78264 can support significantly more than 10 A of load current with each buck converter.

4.1.1 Configurations for VSEL, CNT, and CNT2

Before operation, the ISL78264 has three configuration pins (VSEL, CNT, and CNT2) that must be individually programmed with a resistor to ground. During start-up procedure (before power pulses begin) the IC sources a small current from these three pins, and the internal circuitry reads the resultant voltage and implements configuration settings according to Tables 3, 4, and 5.

4.1.1.1 VSEL

The VSEL pin allows the Channel 1 voltage selection as fixed at 5V or 3.3V using an internal voltage divider or adjustable with an external voltage divider. Select values for the VSEL configuration resistor to ground are listed in Table 3.

Table 3. VSEL Configuration Values

Resistor (kΩ)	Ch1 V_{OUT}	Note
75	5V	-
37.4	Adjustable	-
6.04	3.3V	-

4.1.1.2 CNT

The CNT pin allows the spread spectrum ON or OFF selection and dead time between gate pulses that control external MOSFETs. If the spread spectrum is selected as ON, the modulation depth can be +6% or +12%. The dead time choices of SHORT (30ns) or LONG (100ns) are available to facilitate the usage of various external MOSFETs or switching frequency selections. For example, for the smallest solution size, a high switching frequency of 2.2MHz can be selected and external MOSFETs with a small gate charge can be used with SHORT dead time. For highest efficiency designs, a lower switching frequency can be selected, and MOSFETs with lower $r_{DS(ON)}$ values can require LONG dead time selection. Select values for CNT configuration are listed in Table 4.

Table 4. CNT Configuration Values

Resistor (kΩ)	Spread Spectrum	Dead Time (ns)
75	+12%	Short 30
54.9	+12%	Long 100
37.4	+6%	Short 30
24.9	+6%	Long 100
14.7	Off	Short 30
6.04	Off	Long 100

4.1.1.3 CNT2

The CNT2 pin allows the minimum boot refresh time selection of 180ns or 360ns, with a longer time preferable for typical applications. Resistor values for CNT2 configuration are listed in Table 5.

Table 5. CNT2 Configuration Values

Resistor (kΩ)	Boot Refresh Time (ns)
54.9	360
14.7	180
6.04	Does not start

4.1.2 Start-Up Operation

The ISL78264 start-up procedure requires that V_{IN} is greater than the undervoltage lockout rising threshold that has a maximum value of 5.845V. After this condition is met, start-up can be initiated by driving either EN1 or EN2 to its respective logic high level, which activates the internal regulator to supply VCC to provide bias for the control circuitry and gate drive for the external MOSFETs. The enabled converter goes through a soft-start sequence and after the output reaches a steady-state level the power-good pin signal (open-drain) can be used in implementing additional sequencing requirements. The circuit continues operation until the V_{CC} voltage level reduces below the V_{CC} UVLO falling threshold.

The EN1 pin can withstand high voltage and can connect to VIN through a resistor for initial start-up. The EN2 pin can only accept voltage from 0V to 5.5V and can be enabled from a resistor pull-up to VCC after EN1 is high. However, EN2 can be enabled first to begin the start-up sequence under the constraint that the voltage on the EN2 pin must be limited to 6V maximum. For simultaneous start-up of Converter 1 and Converter 2 the enable pins (EN1 and EN2) can be resistively pulled to respective logic levels when VIN is applied. In this scenario V_{CC} rises, followed by V_{OUT1} and V_{OUT2} rising simultaneously to their final voltage during the soft-start interval.

4.1.3 Internal LDO and EXTSUP

The internal LDO derives power from VIN and provides an output on VCC of 5.0V (typical) during the start-up of the device and can also be used in continuous operation. Because VCC provides bias power for both IC supply and gate drive current, this can produce high power dissipation in the internal regulator. To minimize IC dissipation and increase system efficiency the EXTSUP pin provides an input that can supply 5V from a voltage source other than the internal LDO regulator. An internal circuit senses the EXTSUP and switches it to supply VCC if within an acceptable range. If EXTSUP is not used, Pin 20 is grounded, and the internal LDO supplies VCC.

In a typical application, the Channel 1 output voltage of 5V is connected to the EXTSUP pin so that after start-up VOUT1 can supply bias power to eliminate LDO dissipation in normal operation. During restarts, the internal EXTSUP switch is turned OFF, and this power handover between LDO to EXTSUP pin takes place during each power up. If Channel 1 and Channel 2 are 3.3V outputs, the EXTSUP can accept 5V from an independent source, such as a small 3.3V to 5V boost converter. If the external bias is applied before VIN is applied then the startup enable circuit should be powered from the external bias source (and not VIN).

4.2 Buck Stage (Converter 1)

4.2.1 Operation

The synchronous buck stage operates across an input voltage range of 3.75V to 42V and is offered in fixed output voltage options of 5.0V and 3.3V, or adjustable. In adjustable mode, Channel 1 output can be set in a range of V_{OUT1} = 0.8V to 5V using an external resistive voltage divider from V_{OUT1} to FB1, and Ground. The adjustable range for V_{OUT1} is limited by the voltage rating of the current sense circuitry.

Equation 1 can derive the R_{UPPER1} and R_{LOWER1} resistor values:

$$V_{OUT1} = 0.8V \bullet \left(1 + \frac{R_{UPPER1}}{R_{LOWER1}}\right) \quad \text{(EQ. 1)}$$

where R_{UPPER1} = resistor between V_{OUT1} and FB1 and R_{LOWER1} is the resistor between FB1 and GND.

The minimum input voltage selection for a given V_{OUT} should consider the headroom required for regulation. For example, a V_{OUT} of 5V would need a minimum V_{IN} of 5.7V for normal operation. The Buck converter has a separate enable line EN1 that has to be asserted HIGH for the buck to power up. The V_{OUT} accuracy is ±1% in normal mode and is ±3% in the low power mode. The error amplifier compensation is achieved using a series resistor and capacitor combination from the COMP1 pin to GND.

4.2.2 Oscillator

The buck switching frequency is programmable in the range from 0.2MHz to 2.2MHz by connecting a resistor from the RT pin to GND. External synchronization is possible in the range of 0.2MHz to 2.4MHz by connecting an external clock to the SYNC pin. The device syncs on the rising edge. The RT and SYNC pins set the mode of operation as shown in Table 6.

Table 6. Oscillator and SYNC Configuration

Pin	Connect to	Buck Frequency
RT	Resistor + GND	Programmable range 0.2MHz to 2.2MHz
SYNC	VCC	Forced CCM mode
	GND	CCM, DEM, ECM, Automatic
	0.2MHz < External Clock < 2.2MHz	Overrides internal frequency

The chart in Figure 28 can determine the relationship of RT and the switching frequency.

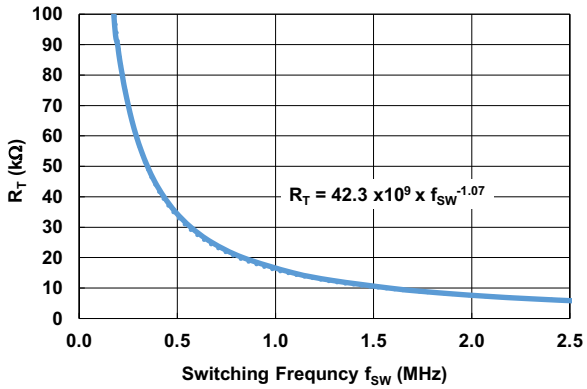


Figure 28. R_T vs f_{SW}

4.2.3 Phase Shift

Converter 1 and Converter 2 are 180° out of phase, which helps lower the noise by reducing the peak current during switching.

4.2.4 Boot Refresh

The BOOT to LX voltage is constantly monitored and if it is lower than 3.4V ±0.2V, the device inserts a 180ns/360ns pulse onto the low gate on-time. If in the Pulse Skip mode, the ISL78264 inserts a 180ns/360ns low gate on-time before the high gate starts switching. When in the Low Power mode, the device inserts a 360ns low gate on-time before the high gate starts switching. It is assumed that logic level FETs are being used.

4.2.5 Current Limit

The ISL78264 requires that the Converter 1 inductor current is sensed by a current sense amplifier to provide both control and overcurrent protection. This is accomplished by inserting a current sense resistor in series with the power inductor with a resistance value that produces a 50mV signal between ISENxP and ISENxN when the full load current is applied to the output in FCCM. Inductor DCR current sensing also can be used. If the load is increased so the voltage across the current sense resistor is 80mV, the circuit begins limiting current on a

cycle-by-cycle basis (OC1). If the load continues to increase so the current sense resistor signal reaches 100mV, the hiccup current limit (OC2) forces the IC to shut down and a restart is attempted.

4.2.6 Undervoltage and Overvoltage

The ISL78264 Buck Converter 1 and converter 2 have an overvoltage limit of +7% typical with a hysteresis of 2% and an undervoltage limit of -7% typical with a hysteresis of 2%. At startup, PGOOD1 and PGOOD2 are initially pulled low using an internal MOSFET in an open-drain configuration, and when the corresponding output voltage exceeds the undervoltage threshold PGOOD1 and PGOOD2 rise using an external pull-up resistor connected to VCC. If an overvoltage condition is detected on either output, the corresponding PGOOD signal is pulled low and the circuit enters a hiccup mode of operation with successive shutdowns with restarts to detect if the overvoltage fault is cleared. If an undervoltage condition is detected during operation, the controller continues to operate and corresponding PGOOD1 and PGOOD2 are pulled low.

4.3 Buck Stage (Converter 2)

4.3.1 Operation

The synchronous buck stage operates across an input voltage range of 3.5V to 42V and has an adjustable output voltage. The V_{OUT} can be set in the range of 0.8V to 32V using two resistors (see Buck Output Voltage Programming). The high-side and low-side FET drivers of the ISL78264 can source a current = 2A and sink = 3A.

4.3.2 Buck Output Voltage Programming

Connecting a resistor from V_{OUT2} to the FB2 pin and another from FB2 to GND programs the output voltage of the device. The required resistor values for a given V_{OUT2} can be calculated using Equation 2 to derive the R_{UPPER2} and R_{LOWER2} resistor values:

$$V_{OUT2} = 0.8V \bullet \left(1 + \frac{R_{UPPER2}}{R_{LOWER2}}\right) \quad \text{(EQ. 2)}$$

where R_{UPPER2} = Resistor between V_{OUT2} and FB2 and R_{LOWER2} is the resistor between FB2 and GND.

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Resistors R_{UPPER2} and R_{LOWER2} are positioned close to the FB pin.

4.3.3 Boot Refresh

The BOOT to LX voltage is constantly monitored and if it is lower than 3.4V ±0.2V, the device inserts a 180ns/360ns pulse onto the low gate on-time. If in the Pulse Skip mode, the ISL78264 inserts a 180ns/360ns low gate on-time before the high gate starts switching. When in the Low Power mode, the device inserts a 360ns low gate on-time before the high gate starts switching. It is recommended to use logic level FETs that are specified for 4.5 V operation.

4.3.4 Current Limit

The ISL78264 requires that the Converter 2 inductor current is sensed by a current sense amplifier to provide both control and overcurrent protection. This is accomplished by inserting a current sense resistor in series with the power inductor with a resistance value that produces a 50mV signal between ISENxP and ISENxN when full load current is applied to the output in FCCM. If the load is increased so the voltage across the current sense resistor is 80mV, the circuit begins limiting current on a cycle-by-cycle basis (OC1). If load continues to increase so that the current sense resistor signal reaches 100mV, the hiccup current limit (OC2) forces the IC to shutdown and a restart is attempted.

4.3.5 Undervoltage and Overvoltage

The ISL78264 Buck Converter 2 has an overvoltage limit of +7% typical with a hysteresis of 3%. The device has an undervoltage limit of -7% typical with a hysteresis of 3%. At startup, PGOOD2 is pulled low using an internal MOSFET in an open-drain configuration, and when VOUT2 exceeds the undervoltage threshold the PGOOD2

rises using an external pull-up resistor connected to VCC. If an overvoltage condition is detected during operation, PGOOD2 is pulled low and the circuit enters a hiccup mode of operation with successive shutdowns with restarts to detect if the overvoltage fault is cleared. If an undervoltage condition is detected during operation, the controller continues to operate and PGOOD2 is pulled low.

4.4 Over-Temperature Shutdown

The ISL78264 has an over-temperature shutdown threshold of 160°C with a hysteresis of 15°C. When crossing the threshold, the device shuts down for 100ms and then attempts to restart the device. The device resumes operation when the over-temperature fault is cleared.

4.5 Energy Conservation Mode (ECM)

The ISL78264 can be configured to enter Energy Conservation Mode (ECM) to reduce quiescent power consumption as the load current is reduced. ECM allows a buck converter to be supplied from a car battery to provide a 5V output (with no load) while drawing less than 6µA average current from the battery. During ECM operation, the ISL78264 delivers power pulses to the output filter and load at a frequency that is much lower than the normal switching frequency range of 200kHz to 2.2MHz. Each power pulse supplies sufficient energy to supply small load currents with no requirement for high-frequency multi-pulse burst operation as described in the following sections. In the time interval between consecutive ECM power pulses, the ISL78264 can drastically reduce its operating current requirement to minimize average standby current drawn from the input supply that is normally a car battery. With the proper component selection, the circuit can automatically enter or exit ECM with minimal disturbance on the output within a wide range of operating conditions.

4.5.1 Overview of ECM Setup and Operation

There are multiple factors that determine whether ECM can be entered, maintained, or exited. If a converter is configured to allow ECM at light loads, it automatically exits ECM under certain conditions. Therefore, ECM is allowed at light loads, but the circuit functions in Fixed Frequency Continuous Conduction Mode (FCCM) if the load currents exceed one-third of the full load level as defined below. The factors that impact ECM operation are the following:

- SYNC voltage level
- V_{IN} level
- EN1 and EN2 status
- R_{SEN} value
- Full load current determined by 50mV across R_{SEN}
- Output voltage ripple
- Load current changes

To permit ECM operation, the voltage on VIN (Pin 26) must be in a range from 6V to 18.5V and the SYNC pin must be logic low. If SYNC is directly connected to VCC, the circuit always operates in FCCM. To command ECM enter/exit on-the-fly, a simple switch circuit can be used to drive SYNC pin from logic high (VCC) to GND to inhibit or permit ECM. SYNC can also be held low to keep the converter in ECM when the load is small, then SYNC can be driven to provide an external clock for synchronized operation which forces ECM exit and FCCM operation.

The RT pin is a good indicator to determine the mode of operation of the converter. In normal FCCM mode RT has 0.5V level, and while in ECM RT is pulled to 0V by an internal circuit. Either Controller 1 or Controller 2 can operate in ECM if the corresponding EN pin is logic high. Optimum performance can be achieved with only one channel enabled in ECM, however both channels can be operated simultaneously in ECM. At initial startup, with SYNC low and one controller enabled, the output ramps up operating in FCCM/DEM throughout the soft-start interval and power-good output transitions high. If ECM entry criteria are met, ECM operation begins 20ms to 30ms after startup.

Steady-state ECM power pulse operation uses a voltage comparator in conjunction with an accurate current sense resistor and amplifier to detect loading and current thresholds. Between ECM power pulses, the ISL78264

operates with extremely low current using a voltage comparator to sense the output voltage level as it slowly decays with a rate proportional to output load current. During this interval, the output capacitors supply the load on the output. When the comparator detects the lower voltage threshold, the device turns fully ON to generate a power pulse that stores energy in the output inductor to replenish output capacitors and supply loading, if present.

The ECM power pulse can be terminated by two methods:

- Reaching peak inductor current threshold
- Reaching output voltage OVP level

Individual ECM power pulses are generated by the following procedure as shown in Figure 29. First, the high-side MOSFET is turned ON to apply V_{IN}-V_{OUT} across the output inductor to ramp the inductor current up at a controlled rate. The current sense amplifier monitors the voltage level across the current sense resistor until the voltage reaches 60mV, which equates to a peak inductor current I_{PK}, ECM, which is 120% of the full load current. When the 60mV threshold is attained, the high-side MOSFET is turned OFF and the low-side MOSFET is turned ON, applying V_{OUT} across the output inductor. This forces the inductor current to ramp down to approximately 0A at which time an internal zero current comparator turns the low-side MOSFET OFF. After the power pulse, the device returns to an ultra-low quiescent current consumption. Alternatively, if the output rises to approximately 3% of VOUT target level before the peak current is detected, the high-side pulse is truncated.

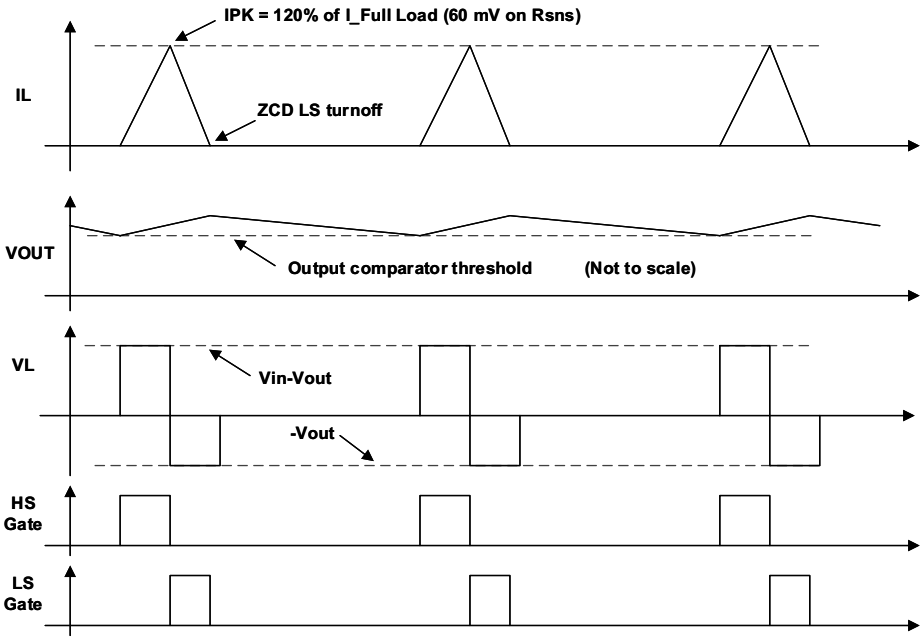


Figure 29. ECM Operational Waveforms

4.5.2 ECM Load Based Entry and Exit

The current sense resistor and amplifier set thresholds to monitor and control ECM entry, exit, and power pulse generation. To understand ECM power pulse operation, first, note that the current sense resistor (in series with the power inductor) is initially selected to produce a 50mV signal between ISENxP and ISENxN when the full load current is applied to the output in FCCM. The ISL78264 can transition in and out of ECM in multiple ways, this section focuses on ECM entry and exit as the load is changed relatively slowly. If ECM is allowed (SYNC = GND) and the load reduces to approximately 1/6th of the full load setting, the signal across the current sense resistor is 8mV and the circuit enters ECM. The circuit remains in ECM as the load is further reduced to minimal or no load. If the load increases, the circuit exits ECM when the current sense amplifier surpasses 18mV, which indicates the load has surpassed approximately 1/3rd of the full load current.

Discussion so far has presented operation as the load current has changed slowly for ECM entry/exit. However, ECM entry/exit is designed to support transient load step requirements as needed. For example, if the current is

large and steps to a small value (less than 1/6th of I_{OUT}, nominal), the current sense circuitry detects low current and enters ECM within a few milliseconds. Conversely, if the converter is operating in ECM with a small load and a large load step is applied, the circuit responds with more power pulses to support the full load rating as shown in Figure 30 below. During the large load step, the VOUT comparator continues to monitor the output voltage following the initial power pulse from 0A to I_{PK} and back to 0A. If the output voltage is below the required level, the converter immediately produces a second power pulse. If V_{OUT} is still below the required level after the second power pulse peak, the subsequent pulses have a higher valley, greater than 0, and no tri-state period. The peak-valley sequence continues until V_{OUT} reaches the required level, or four pulses are counted, and the circuit transitions to FCCM.

Note: The average of the peak valley operation from 60mV to 45mV is capable of supplying a full load that equates to a 50mV level.

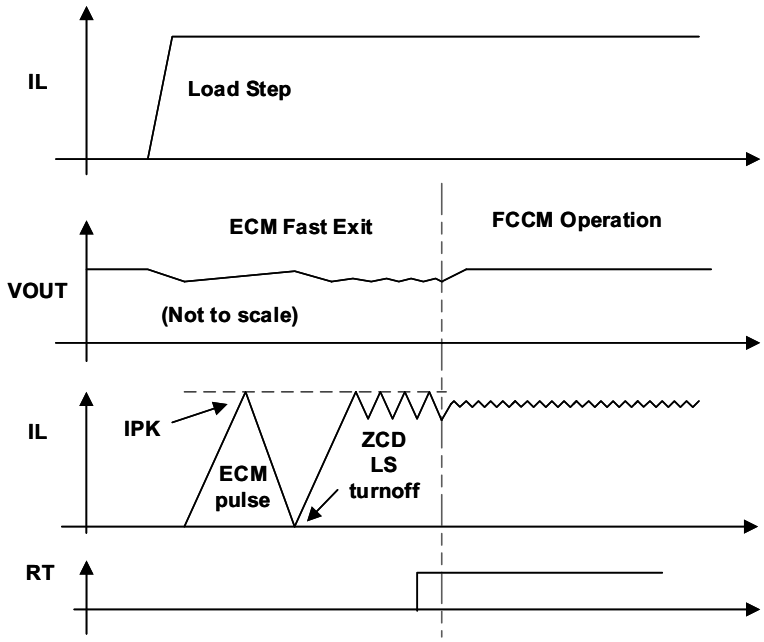


Figure 30. ECM Fast Exit with Large Load Step

5. Application Information

There are many considerations in the selection of the external components for buck regulators. This section discusses some examples of how to decide the parameters of the external components based on the typical application schematic shown in Figure 1 on page 1. In the actual application, the parameters may need to be adjusted and also a few more additional components may need to be added for the application specific noise, physical sizes, thermal, testing, and other requirements.

5.1 Buck Converter

5.1.1 Buck Inductor Selection

While the buck converter is operating in stable Continuous Conduction Mode (CCM), the output voltage and on-time of the high-side transistor is determined by Equation 3:

$$V_{OUT} = V_{IN} \bullet \frac{t_{ON}}{T} = V_{IN} D \quad \text{(EQ. 3)}$$

where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the on-duty of the high-side transistor.

Under this CCM condition, the inductor ripple current can be defined as Equation 4:

$$I_{L,p\text{-}p} = t_{ON} \bullet \frac{V_{IN} - V_{OUT}}{L} = t_{OFF} \bullet \frac{V_{OUT}}{L} \quad \text{(EQ. 4)}$$

From the previous equations, the inductor value is determined as Equation 5:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW}} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 5)}$$

In general, when the inductor value is determined, the ripple current varies by the input voltage. At the maximum input voltage, the on-duty becomes minimum and the ripple current becomes maximum. So, the minimum inductor value can be estimated from Equation 6.

$$L_{min} = \frac{V_{IN} - V_{OUT}}{f_{SW} \bullet \Delta I_{L,\,max}} \bullet \frac{V_{OUT}}{V_{IN,\,max}} \quad \text{(EQ. 6)}$$

In a DC/DC converter design, this ripple current is normally selected to be 20% to 50% of maximum DC output current. A reasonable starting point to adjust the inductor value is around 30% of the maximum DC output current. Increasing the inductor value reduces the ripple current and ripple voltage. However, the large inductance value can increase the converter's response time to a load transient. Also, this reduces the ramp signal and can cause a noise sensitivity issue.

Under stable operation, the peak current flow in the inductor is the sum of output current and 1/2 of ripple current.

$$I_{L,pk} = \frac{I_{L,p\text{-}p}}{2} + I_{OUT} \quad \text{(EQ. 7)}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the start-up or heavy load transient. Therefore, the size of the inductor needs to be determined with the consideration of these conditions. In addition, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the inductor's saturation current rating.

Note: The OC1 signal is fixed at 80mV (160% of full load) and the OC2 hiccup threshold is fixed at 100mV; therefore, the inductor should have a saturation value exceeding 2x full load current. The ECM operation is based on a fixed 60mV signal (120% of full load), which is less than the OC1 level, so there are no special considerations for inductor selection for ECM.

5.1.2 Buck Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. The current mode control loop allows the usage of low ESR ceramic capacitors for smallest size, and/or electrolytic and polymer capacitors that offer larger capacitance values but with higher ESR and increased physical size. While the ceramic capacitor offers excellent overall performance and reliability, the actual capacitance may be considerably lower than the advertised value when operated with significant DC bias voltage in relation to rated voltage, so the manufacturer information should be carefully reviewed.

The following are equations for the required capacitance value to meet the desired ripple voltage level. Additional capacitance can be used to lower the ripple voltage and to improve transient response.

For the ceramic capacitor (low ESR):

$$V_{OUT,rip} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet C_{OUT}} \quad \text{(EQ. 8)}$$

where ΔI_L is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

Required minimum output capacitance based on ripple current is:

$$C_{OUT,min} = \frac{\Delta I_L}{8 \bullet f_{SW} \bullet V_{OUT,rip}} \quad \text{(EQ. 9)}$$

If using electrolytic capacitors, the ESR is the dominant portion of the ripple voltage.

$$V_{OUT,rip,ESR} = \Delta I_L \bullet ESR \quad \text{(EQ. 10)}$$

So, to reduce the ripple voltage, select the electrolytic capacitor based on maximum ESR, use multiple capacitors in parallel to reduce the ESR, or increase inductor value to reduce the ripple current.

The output capacitor value selected for FCCM may require adjustment for ECM operation depending on the magnitude of ripple voltage allowed on VOUT. In standard ECM operation when there is no external loading, the output capacitor must absorb the complete pulse of energy from the output inductor peak current of 120% of full load current. Both the capacitance value and ESR should be considered for ECM operation. The capacitance should be large enough to absorb the energy with acceptable voltage rise, and the ESR must be small enough to control the potentially large step in voltage equal to Ipk,ECM x ESR

In addition to output voltage ripple requirements, select the buck output capacitor value in conjunction with the inductor to meet output deviation requirements during normal FCCM operation, ECM (Energy Conservation Mode), and load transients.

Equation 11 calculates the value of C_{OUT} required during load reduction and the output voltage overshoots the nominal level.

$$C_{OUT\_MIN\_STEP\_DOWN} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2V_{OUT}\Delta V} \quad \text{(EQ. 11)}$$

When the load is increased, the output undershoots the nominal value, and the value of C_{OUT} required is calculated using Equation 12.

$$C_{OUT\_MIN\_STEP\_UP} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2(V_{IN} - V_{OUT})\Delta V} \quad \text{(EQ. 12)}$$

5.1.3 Buck Input Capacitor

The system input power rail can incorporate a combination of electrolytic and ceramic capacitors to provide a stable input voltage while supplying pulse currents at the buck switching frequency. The voltage rating of the capacitors should exceed the maximum voltage which can be connected to the input of the regulator and it is common to provide a rating margin over 20% of the maximum input voltage.

The minimum value of the input capacitors can be estimated by limiting the drop in VIN (ΔVIN below) to approximately 1% when delivering the full load current during the on-time of the high-side MOSFET:

(EQ. 13) $$C_{IN,MIN} = \frac{I_{LOAD,MAX} \bullet D \bullet (1 - D)}{f_{SW} \bullet \Delta VIN}$$

The specific capacitor(s) used should be selected with an RMS current capability exceeding the value estimated by the relation below.

(EQ. 14) $$I_{CIN,RMS} \cong I_{LOAD,MAX} \bullet \sqrt{D \bullet (1 - D)}$$

5.1.4 Buck MOSFET Selection

The external MOSFETs that are driven by the ISL78264 controller need to be carefully selected to optimize the design of the synchronous buck regulator. The input voltage is typically the automotive range for battery supply, so the MOSFETs are normally rated at 40V BVdss. As the high-side and low-side gate drivers are 5V output, the MOSFET VGS needs to be specified in this range. The MOSFET should have a low total gate charge (Qgd), low ON-resistance ($r_{DS(ON)}$) at VGS = 4.5V (10mΩ to 20mΩ), and small gate resistance (Rg <1.5Ω is recommended). It is recommended that the minimum VGS threshold should be higher than 1.2V, but not exceeding 2.5V to make sure the MOSFETs can be switched off reliably throughout the complete V_{CC} range.

Table 7. Capacitor Vendor Information

Manufacturer	Series	Website
AVX	X7R	www.avx.com
Murata	X7R	www.murata.com
Taiyo Yuden	X7R	www.t-yuden.com
TDK	X7R	www.tdk.com

6. Control Loop Compensation for the Buck Regulators

Several components selected for the power, filtering, and current sense circuits play a role in the determination of the compensating components.

- R_{SENSE} = 50mV/IOUT = 5mΩ (with IOUT = 10A)
- Ramp slope = 38.1mV per volt of VIN
- Ramp valley = 1V
- Current sense amplifier transconductance = $G_{m,CSA}$ = 91.25µS
- Current feedback resistor value = R_{IFB} = 60kΩ
- Reference voltage V_{REF} = 0.8V
- $G_{m,EA}$ = 1.7mS

Calculate current loop pole frequency

$$f_{cp} = \frac{R_{sns}}{2\pi \bullet L_{OUT}} \quad \text{(EQ. 15)}$$

Determine PWM_{gain}

$$PWM_{gain} = \frac{1}{\text{ramp slope}} = \frac{1}{38.1\text{mV}} = 26.2 \quad \text{(EQ. 16)}$$

Calculate current loop unity gain frequency

$$f_{tc} = PWM_{gain} \bullet G_{m,\,CSA} \bullet R_{ifb} \bullet f_{cp} \quad \text{(EQ. 17)}$$

This allows you to calculate the command voltage (+1V for ramp valley voltage) for the specific conditions:

$$V_{cmd} = R_{sns} \bullet I_{max} \bullet G_{m,\,CSA} \bullet R_{ifb} \quad \text{(EQ. 18)}$$

Determine the equivalent transconductance of the modulator (I_{OUT}/V_{cmd})

$$GM = \frac{1}{R_{sns} \bullet G_{m,\,CSA} \bullet R_{ifb}} \quad \text{(EQ. 19)}$$

Calculate the unity gain frequency of the modulator.

$$f_{tm} = \frac{GM}{2\pi \bullet C_{OUT}} \quad \text{(EQ. 20)}$$

Constrain the voltage loop f_t to be less than current loop f_{tc}.

$$\frac{f_t}{f_{tc}} = 0.5 \quad \text{(EQ. 21)}$$

This allows you to calculate compensation resistor R_{COMP}.

$$R_{COMP} > \frac{f_{tc} \bullet V_{OUT} \bullet 0.5}{f_{tm} \bullet G_{m,\,EA} \bullet V_{REF}} \quad \text{(EQ. 22)}$$

Now calculate compensation capacitor C_{COMP}.

$$C_{COMP} = \frac{15}{2\pi \bullet R_{COMP} \bullet f_{tc}} \quad \text{(EQ. 23)}$$

7. Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL78264. Each channel of the switching buck converters requires specific attention to minimize power loop area for highly efficient, stable operation. It is also important to consider routing the shared common areas between the two converters. Route the primary paths in single layer copper if possible to reduce parasitic inductance in the power current paths.

The following layout instructions see Figures 31 and 32 as noted.

1. In Figure 31 the common connection between input capacitors, output capacitors, and low-side FET for each buck converter should be connected through the central ground (gray) area.
2. When the high-side MOSFET is switched ON and OFF the power current alternates flowing through the input capacitor and high-side MOSFET, or the low-side MOSFET. Minimize the loop area between CIN, high-side MOSFET, and low-side MOSFET to reduce interference from the high dI/dT intervals as the current alternates between the MOSFETs.
3. The first inner layer below the top copper layer with power components should be ground layer that is as complete as possible, as indicated in Figure 32 using light green fill. This provides a tightly coupled ground return path for the power circuitry. This layer is also used in conjunction with many vias to create a low impedance connection from the common power GND region to the ISL78264 controller. Connect the thermal pad underneath the IC to inner planes with at least six vias, each with 0.3mm diameter, spaced 1mm apart
4. Connect the signal ground (Pin 11) to the thermal pad ground directly under the IC. For best noise immunity, signal pins such as COMP, RT, and configuration resistors can be connected in a small SGND pour that connects to Pin 11, which connects to PGND in a single point connection under the IC.
5. Each converter has ISNS connections that should be routed as shown in Figure 32. The ISNS traces are routed on the second inner layer, which is shielded from power switching currents by the ground area on inner layer 1. The ISNS traces should begin as a Kelvin connection through a via in the center of the sense resistor in each converter.
6. Minimize the trace lengths on the feedback loop and rout around switching power circuits to minimize noise pick-up.
7. Place the capacitors on Vin (Pin 26) and VCC (Pin 19) close to respective pins and ground connection.

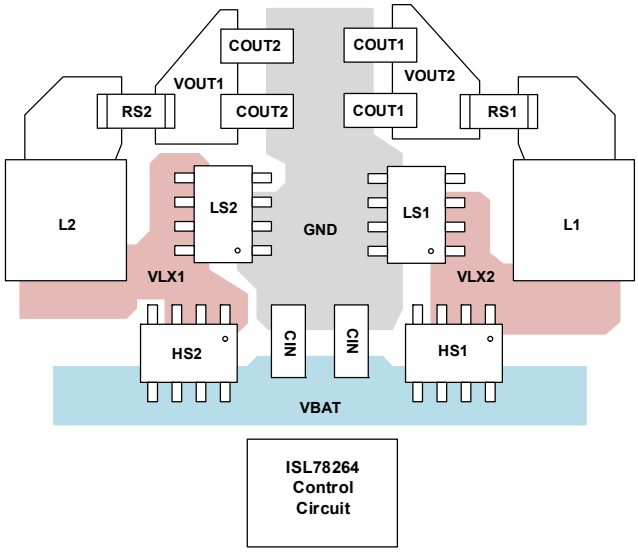


Figure 31. PCB Layout Illustrating Power Component Placement

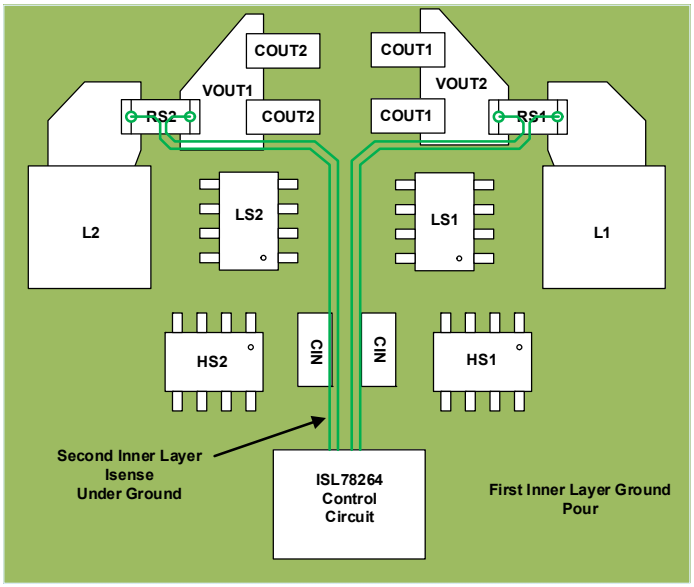


Figure 32. PCB Layout Illustrating Current Sense Routing

8. Revision History

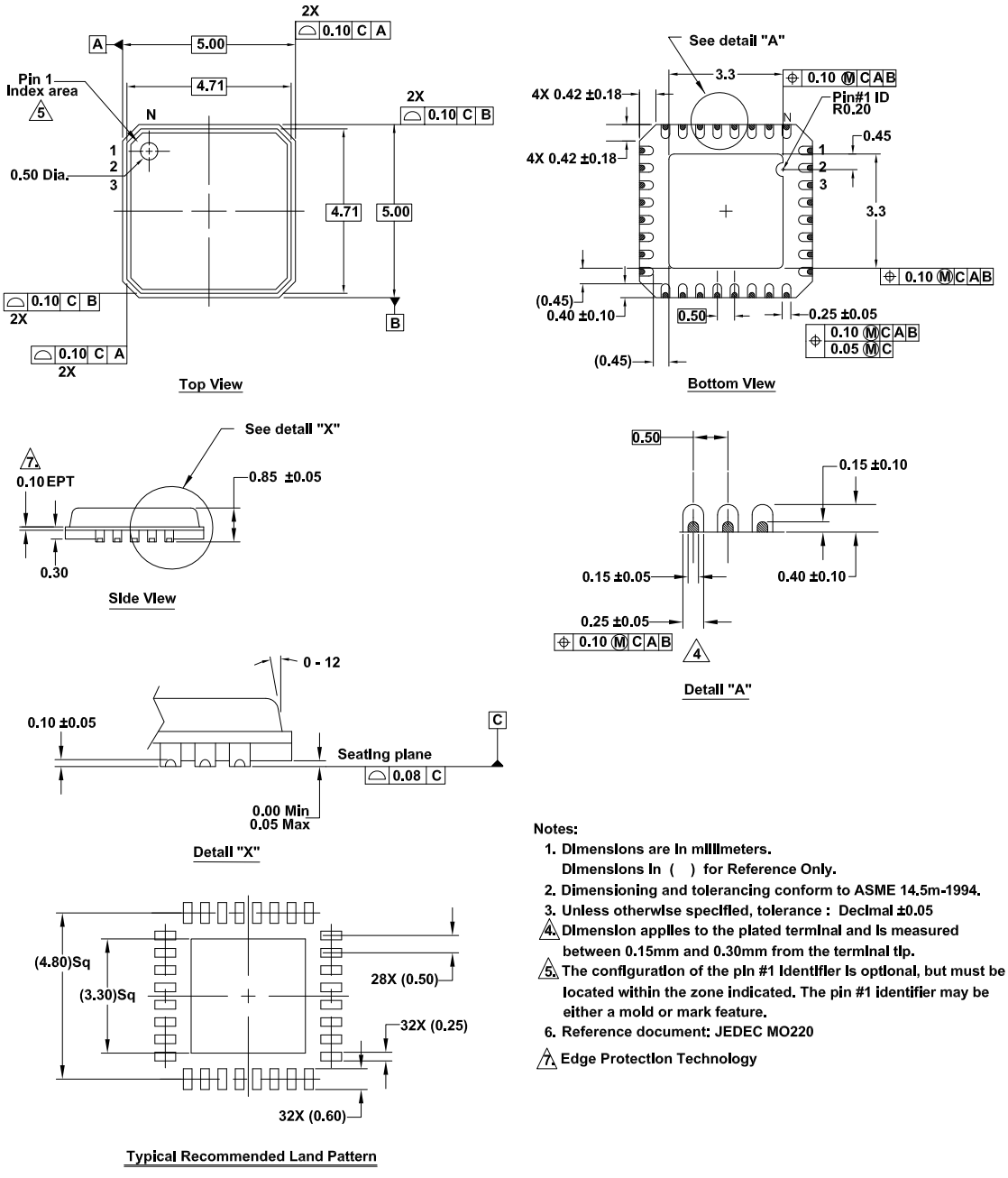
Rev.	Date	Description
2.00	Oct 14, 2021	Removed Related Literature section. Updated Ordering Information table format. Updated POD L32.5X5H to the latest revision, changes are as follows: -Added Note 7 for Edge Protection Technology -Updated D1 and E1 dimensions in Top View changing them from 4.75 to 4.71. -Updated side view by adding Edge protection information.
1.00	Jul 24, 2020	Initial release

9. Package Outline Drawing

For the most recent package outline drawing, see L32.5x5H.

L32.5x5H

32 Lead Quad Flat No-Lead Plastic Package (Punch QFN with Wetable Flank)
Rev 3, 8/2021



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