# ISL78420

## 100V, 2A Peak, Half-Bridge Driver with Tri-Level PWM Input and Adjustable Dead-Time

FN8296
Rev 4.00
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The ISL78420 is a 100V, 2A high frequency half-bridge NMOS FET driver with a tri-level PWM input. With an operating supply range of 8V to 14V and integrated high-side bootstrap bias, it supports driving the high-side and low-side NMOS in 100V half-bridge applications.

This driver is designed to work in conjunction with the ISL78220 and ISL78225 "Multi-Phase Interleaved Boost PWM Controller" and the ISL78226 "6-Phase 12V/48V Bidirectional Synchronous PWM Controller". It can also be used in applications where a standard half-bridge driver is needed.

This driver has a programmable dead-time to ensure break-before-make operation between the high-side and low-side MOSFET. A resistor is used to set the dead-time from 35ns to 220ns.

The PWM pin's tri-level input allows control of the high-side and low-side drivers with a single pin. When the PWM input is at logic high, the high-side bridge FET is turned on and the low-side FET is off. When the input is at logic low, the low-side bridge FET is turned on and the high-side FET is turned off. When the input voltage is in mid-level state, both the high and low-side bridge FETs are turned off. The enable pin (EN), when low, also turns both bridge FETs off. This EN input can be used when the controller driving the ISL78420 does not utilize a tri-level output. Both PWM and EN logic inputs are $V_{DD}$ tolerant.

The ISL78420 is offered in a 14 Ld HTSSOP package and complies with 100V conductor spacing per IPC-2221. The device is Automotive AEC-Q100 qualified for the temperature range of -40°C to +125°C.

# Features

- 114VDC bootstrap supply maximum voltage
- 2A source and sink driver for 100V half-bridge NMOS FETs
- Programmable dead-time prevents shoot-through; adjustable from 35ns to 220ns with a single resistor
- Unique tri-level PWM input logic enables phase shedding when using multiphase PWM controllers (e.g. ISL78220/225/226)
- On-chip 1Ω (dynamic) bootstrap diode
- 10ns rise and fall times with 1000pF load
- 8V to 14V operating voltage range
- $V_{DD}$ and Boostrap supply Undervoltage Lockout (UVLO)
- 14 Ld HTSSOP package compliant with 100V conductor spacing guidelines per IPC-2221
- AEC-Q100 qualified

# Applications

- Automotive applications
- 12V/48V bi-directional converter (ISL78226)
- Multiphase boost (ISL78220/225)
- Class-D amplifiers

# Related Literature

- For a full list of related documents, visit our web page
  - ISL78420 product page

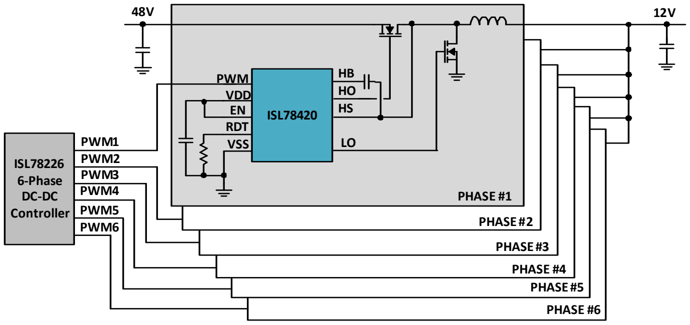


FIGURE 1. NMOS DRIVER FOR 6-PHASE BIDIRECTIONAL BUCK AND BOOST CONVERTER

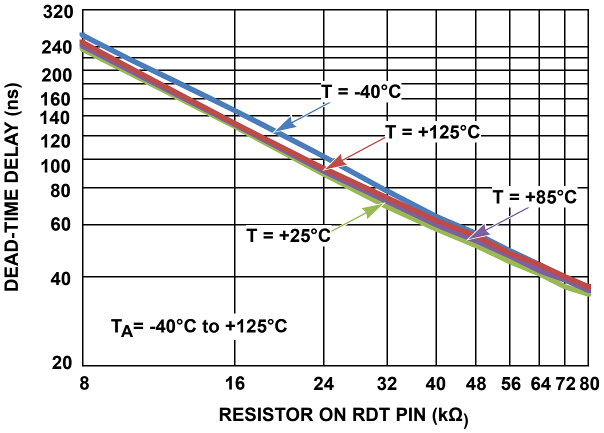


FIGURE 2. DEAD-TIME vs TIMING RESISTOR

## Block Diagram

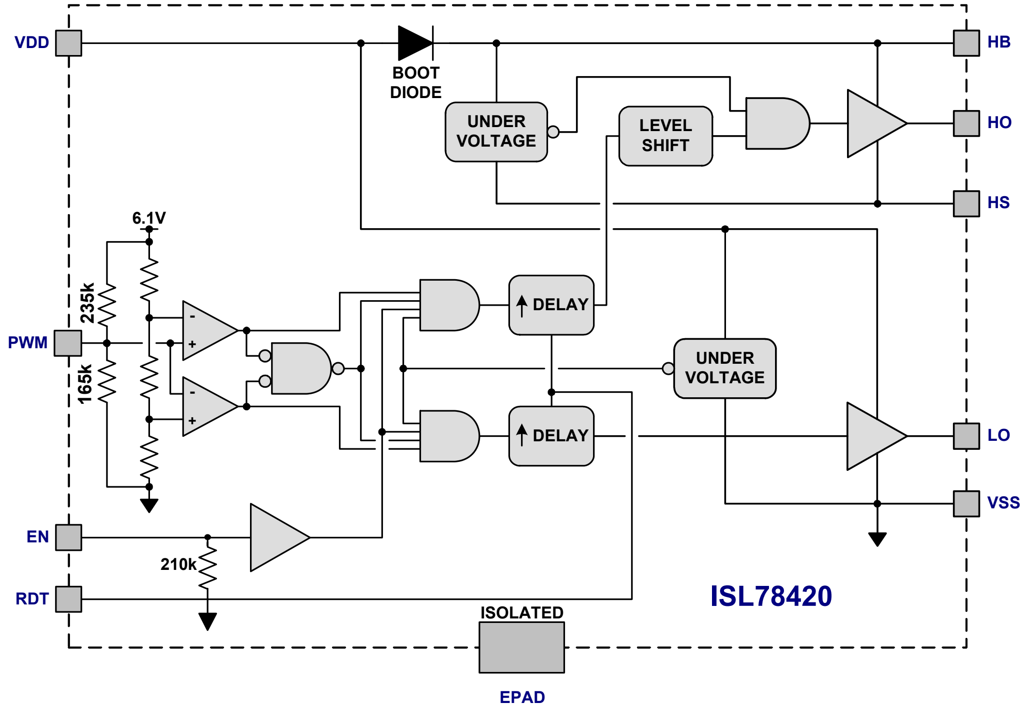
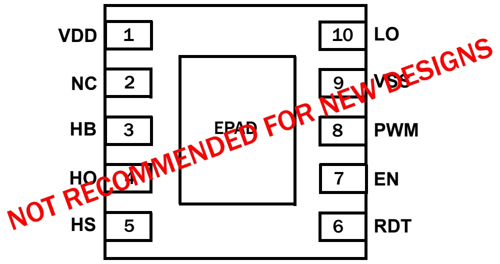


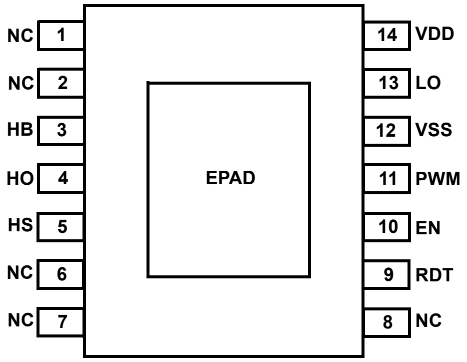
FIGURE 3. ISL78420 BLOCK DIAGRAM

## Pin Configurations

ISL78420ARTAZ
(10 LD 4X4 TDFN)
TOP VIEW



ISL78420AVEZ
(14 LD TSSOP)
TOP VIEW



## Pin Descriptions

| 10 LD | 14 LD | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | 14 | VDD | Analog input supply voltage and positive supply for lower gate driver. Decouple this pin to ground with a 4.7µF or larger high frequency ceramic capacitor to $V_{SS}$. A 0.1µF ceramic decoupling capacitor placed close to VDD and VSS pin is recommended. |
| 3 | 3 | HB | High-side bootstrap supply voltage for upper gate driver referenced to HS. Connect the bootstrap capacitor to this pin and HS. |
| 4 | 4 | HO | High-side output driver connected to gate of high-side NMOS FET. |
| 5 | 5 | HS | High-side gate driver reference node. Connect to source of high-side NMOS FET. Connect bootstrap capacitor to this pin and HB. |
| 8 | 11 | PWM | Tri-level PWM input. Logic high drives HO high and LO low. Logic low drives HO low and LO high. In mid-level state, both outputs are driven low. |
| 7 | 10 | EN | Output enable pin. When EN is low, HO = LO = 0. An internal 210kΩ pull-down resistor places EN in the low state when the pin is left floating. |
| 9 | 12 | VSS | Analog supply ground. Decouple this pin to VDD with a 4.7µF or larger capacitor. |
| 10 | 13 | LO | Low-side output driver connected to gate of low-side NMOS FET. |
| 2 | 1, 2, 6, 7, 8 | NC | No Connect. This pin is isolated from all other pins. May optionally be connected to VSS. |
| 6 | 9 | RDT | A resistor connected between this pin and VSS adds dead time by adding delay time between the falling edge of LO to rising edge of HO and falling edge of HO to rising edge of LO. |
| - | - | EPAD | The EPAD is electrically isolated. It is recommended that the EPAD be connected to the VSS plane for heat removal. |

## Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS COMPLIANT) | PKG. DWG. # |
|---|---|---|---|---|
| ISL78420AVEZ (Note 4) | 78420 AVEZ | -40 to +125 | 14 Ld HTSSOP | M14.173B |
| *Not Recommended for New Designs*<br>ISL78420ARTAZ | 78420 AZ | -40 to +125 | 10 Ld 4x4 TDFN | L10.4x4 |

NOTES:

1. Add "-T" suffix for 2.5k unit or "-T7A" suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications. .
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78420. For more information on MSL please see tech brief TB363.
4. These packages meet compliance with 100V Conductor Spacing Guidelines per IPC-2221.

## Absolute Maximum Ratings (Note 5)

| | |
|---|---|
| Supply Voltage, VDD, $V_{HB}$ - $V_{HS}$ (Note 6) | -0.3V to 18V |
| PWM and EN Input Voltage | -0.3V to $V_{DD}$ + 0.3V |
| Voltage on LO | -0.3V to $V_{DD}$ + 0.3V |
| Voltage on HO | $V_{HS}$ - 0.3V to $V_{HB}$ + 0.3V |
| Voltage on HS (Continuous) | -1V to 110V |
| Voltage on HB | 118V |
| Average Current in $V_{DD}$ to HB Diode | 100mA |
| ESD Ratings | |
| Human Body Model (Tested per AEC-Q100-002) | 2kV |
| Charged Device Model (Tested per AEC-Q100-011) | 1.5kV |
| Latch-up (Tested per AEC-Q100-004) | 100mA |

## Maximum Recommended Operating Conditions (Note 5)

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 8V to 14V |
| Voltage on HS | -1V to 100V |
| Voltage on HS | (Repetitive Transient) -5V to 105V |
| Voltage on HB (Note 6) | $V_{HS}$ + 8V to $V_{HS}$ + 14V |
| HS Slew Rate | <50V/ns |
| Temperature | -40°C to +125°C |

## Thermal Information

| Thermal Resistance (Typical) (Notes 7, 8) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 14 Ld HTSSOP | 35 | 2.5 |
| 10 Ld TDFN | 42 | 4 |

Max Power Dissipation at +25°C in Free Air (Note 9)

| | |
|---|---|
| 14 Ld HTSSOP | 3.5W |
| 10 Ld TDFN | 3.0W |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature Range | -55°C to +150°C |
| Pb-Free Reflow Profile | see TB493 |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. All voltages referenced to $V_{SS}$ unless otherwise specified.
6. The operating voltage from HB to GND is the sum of VDD and the HS voltage. The maximum operating voltage from HB to GND is recommended to be under 114V.
7. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
8. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
9. Specified at published junction to ambient thermal resistance for a junction temperature of 150°C. Refer to Note 7 for test condition to establish junction to ambient thermal resistance.

## Electrical Specifications

$V_{DD}$ = $V_{HB}$ = EN = 12V, $V_{SS}$ = $V_{HS}$ = 0V. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_A$ = +25°C | | | $T_A$ = -40°C to +125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 10) | MAX (Note 10) | |
| **SUPPLY CURRENTS** | | | | | | | | |
| $V_{DD}$ Quiescent Current | $I_{DD8k}$ | $R_{DT}$ = 8kΩ; PWM = 12V | - | 0.65 | 0.95 | - | **1** | mA |
| | $I_{DD80k}$ | $R_{DT}$ = 80kΩ; PWM = 12V | - | 1.0 | 2.1 | - | **2.2** | mA |
| $V_{DD}$ Operating Current | $I_{DDO8k}$ | $f_{PWM}$ = 500kHz, $R_{DT}$ = 8kΩ | - | 2.5 | 3 | - | **3** | mA |
| | $I_{DDO80k}$ | $f_{PWM}$ = 500kHz, $R_{DT}$ = 80kΩ | - | 3.4 | 4 | - | **4** | mA |
| HB to HS Quiescent Current | $I_{HB}$ | PWM = EN = 0V | - | 65 | 115 | - | **150** | µA |
| HB to HS Operating Current | $I_{HBO}$ | $f_{PWM}$ = 500kHz | - | 2.0 | 2.5 | - | **3** | mA |
| HB to $V_{SS}$ Leakage Current | $I_{HBS}$ | PWM = EN = 0V; $V_{HB}$ = $V_{HS}$ = 100V | - | 0.05 | 1.5 | - | **10** | µA |
| HB to $V_{SS}$ Current, Operating | $I_{HBSO}$ | $f_{PWM}$ = 500kHz; $V_{HB}$ = $V_{HS}$ = 100V | - | 1.2 | 1.5 | - | **1.6** | mA |
| **TRI-LEVEL PWM INPUT** | | | | | | | | |
| High Level Threshold | $V_{PWMH}$ | | - | 3.6 | 4.0 | **-** | **4.1** | V |

## Electrical Specifications

$V_{DD} = V_{HB}$ = EN = 12V, $V_{SS} = V_{HS}$ = 0V. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_A$ = +25°C MIN | $T_A$ = +25°C TYP | $T_A$ = +25°C MAX | $T_A$ = -40°C to +125°C MIN (Note 10) | $T_A$ = -40°C to +125°C MAX (Note 10) | UNIT |
|---|---|---|---|---|---|---|---|---|
| Mid-Level Range | $V_{MIDH}$ | Mid-level range upper limit | 3.0 | 3.4 | - | **2.9** | **-** | V |
| | $V_{MIDL}$ | Mid-level range lower limit | - | 1.6 | 2.1 | **-** | **2.2** | V |
| Low Level Threshold | $V_{PWML}$ | | 0.8 | 1.1 | - | **0.7** | **-** | V |
| PWM Pull-Up Resistor | $R_{UP}$ | To internal 6.1V reference | - | 235 | - | - | - | kΩ |
| PWM Pull-Down Resistor | $R_{DOWN}$ | To $V_{SS}$ | - | 165 | - | - | - | kΩ |
| EN INPUT | | | | | | | | |
| Low Level Threshold | $V_{ENL}$ | | 1.8 | 2.5 | - | **1.8** | **-** | V |
| High Level Threshold | $V_{ENH}$ | | - | 2.8 | 4.0 | **-** | **4.1** | V |
| EN Pull-Down Resistor | $R_{EN}$ | To $V_{SS}$ | - | 210 | - | **100** | **320** | kΩ |
| **UNDERVOLTAGE PROTECTION** | | | | | | | | |
| $V_{DD}$ Rising Threshold | VDDR | | 6.8 | 7.3 | 7.8 | **6.5** | **8.0** | V |
| $V_{DD}$ Threshold Hysteresis | VDDH | | - | 0.6 | - | - | - | V |
| $V_{HB}$ Rising Threshold | VHBR | | 6.2 | 6.9 | 7.5 | **5.9** | **7.8** | V |
| $V_{HB}$ Threshold Hysteresis | VHBH | | - | 0.6 | - | - | - | V |
| **BOOTSTRAP DIODE** | | | | | | | | |
| Low Current Forward Voltage | $V_{DL}$ | $I_{VDD-HB}$ = 100µA | - | 0.6 | 0.7 | - | **0.8** | V |
| High Current Forward Voltage | $V_{DH}$ | $I_{VDD-HB}$ = 100mA | - | 0.7 | 0.9 | - | **1** | V |
| Dynamic Resistance | $R_D$ | $R_D = \Delta V_D / \Delta I_{VDD-HB}$<br>$I_{VDD-HB}$ = 50mA and 100mA | - | 0.8 | 1 | - | **1.5** | Ω |
| **LO GATE DRIVER** | | | | | | | | |
| Low Level Output Voltage | $V_{OL\_LO}$ | $I_{LO}$ = 100mA sink | - | 0.25 | 0.4 | - | **0.5** | V |
| High Level Output Voltage | $V_{OH\_LO}$ | $I_{LO}$ = 100mA source<br>Voltage below VDD<br>$V_{OH\_LO} = V_{DD} - V_{LO}$ | - | 0.25 | 0.4 | - | **0.5** | V |
| Peak Pull-Up Current | $I_{OH\_LO}$ | $V_{LO}$ = 0V | - | 2 | - | - | - | A |
| Peak Pull-Down Current | $I_{OL\_LO}$ | $V_{LO}$ = 12V | - | 2 | - | - | - | A |
| **HO GATE DRIVER** | | | | | | | | |
| Low Level Output Voltage | $V_{OL\_HO}$ | $I_{HO}$ = 100mA sink | - | 0.25 | 0.4 | - | **0.5** | V |
| High Level Output Voltage | $V_{OH\_HO}$ | $I_{HO}$ = 100mA source<br>Voltage below $V_{HB}$<br>$V_{OH\_HO} = V_{HB} - V_{HO}$ | - | 0.25 | 0.4 | - | **0.5** | V |
| Peak Pull-Up Current | $I_{OH\_HO}$ | $V_{HO}$ = 0V | - | 2 | - | - | - | A |
| Peak Pull-Down Current | $I_{OL\_HO}$ | $V_{HO} = V_{HB}$ | - | 2 | - | - | - | A |

## Switching Specifications

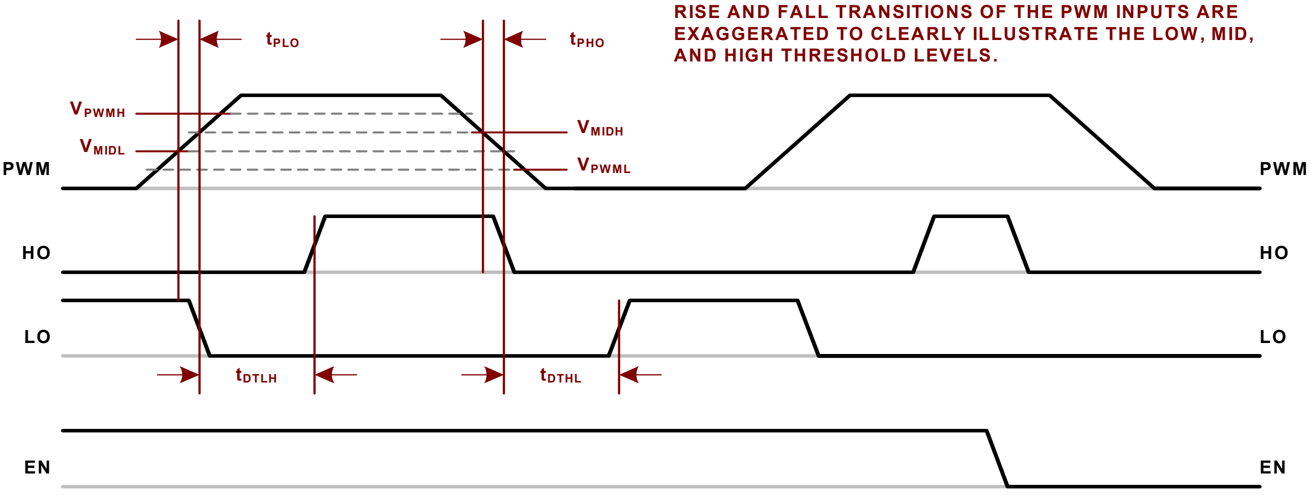
VDD = VHB = 12V, VSS = VHS = 0V, PWM = 0V to 12V, RDT = 8kΩ or 80kΩ. No Load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = +25°C | | | $T_J$ = -40°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 10) | MAX (Note 10) | |
| HO Turn-Off Propagation Delay<br>PWM Falling to HO Falling | $t_{PHO}$ | | - | 32 | 50 | - | 60 | ns |
| LO Turn-Off Propagation Delay<br>PWM Rising to LO Falling | $t_{PLO}$ | | - | 32 | 50 | - | **60** | ns |
| Minimum Dead-Time Delay (Note 11)<br>HO Falling to LO Rising | tDTHL_min | $R_{DT}$ = 80kΩ,<br>PWM high to low | 15 | 34 | 50 | **10** | **60** | ns |
| Minimum Dead-Time Delay (Note 11)<br>LO Falling to HO Rising | tDTLH_min | $R_{DT}$ = 80kΩ<br>PWM low to high | 15 | 27 | 50 | **10** | **60** | ns |
| Maximum Dead-Time Delay (Note 11)<br>HO Falling to LO Rising | tDTHL_max | $R_{DT}$ = 8kΩ,<br>PWM high to low | 150 | 220 | 300 | - | - | ns |
| Maximum Dead-Time Delay (Note 11)<br>LO Falling to HO Rising | tDTLH_max | $R_{DT}$ = 8kΩ,<br>PWM low to high | 150 | 220 | 300 | - | - | ns |
| Dead-Time Delay Matching (Note 11)<br>$\lvert t_{DTHL}-t_{DTLH} \rvert$ | $t_{MATCH\_min}$ | $R_{DT}$ = 80kΩ | - | 7 | 17 | - | - | ns |
| | tMATCH_max | $R_{DT}$ = 8kΩ | - | 10 | 50 | - | - | ns |
| Either Output Rise/Fall Time<br>(10% to 90%/90% to 10%) | $t_R$,$t_F$ | $C_L$ = 1nF | - | 10 | - | - | - | ns |
| Bootstrap Diode Turn-On or Turn-Off Time | $t_{BS}$ | | - | 10 | - | - | - | ns |

NOTES:

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
11. Dead Time is defined as the time between LO falling and HO rising or between HO falling and LO rising. See "Timing Diagram" for measurement specification.

## Timing Diagram



RISE AND FALL TRANSITIONS OF THE PWM INPUTS ARE EXAGGERATED TO CLEARLY ILLUSTRATE THE LOW, MID, AND HIGH THRESHOLD LEVELS.

**$t_{DTLH}$: Dead-Time Delay from LO falling to HO rising. Measured from 50% of LO to 50% of HO.**

**$t_{DTHL}$: Dead-Time Delay from HO falling to LO rising. Measured from 50% of HO to 50% of LO.**

**$t_{PLO}$: Propagation Delay from PWM rising to LO falling. Measured from $V_{MIDL}$ to 50% of LO.**

**$t_{PHO}$: Propagation Delay from PWM falling to HO falling. Measured from $V_{MIDH}$ to 50% of HO.**

FIGURE 4. TIMING DIAGRAM

## Typical Performance Curves

Unless otherwise specified, operating conditions at: T = +25°C; $V_{DD}$ = EN = 12V; $V_{SS}$ = HS = 0V; Capacitor from HB to HS pin $C_{BOOT}$ = 0.47µF; 100kΩ load on LO and HO to VSS.

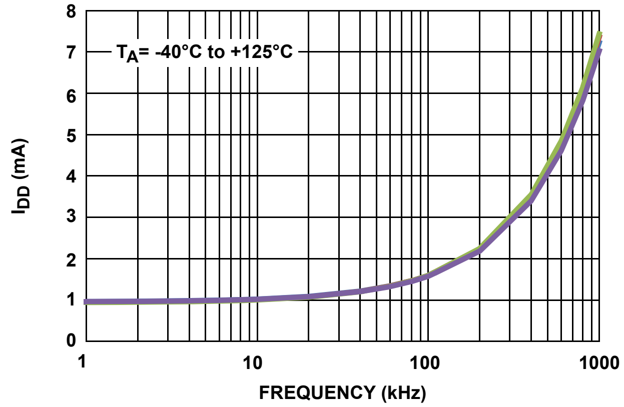


FIGURE 5. $I_{DD}$ OPERATING CURRENT vs FREQUENCY, $R_{DT}$ = 8kΩ

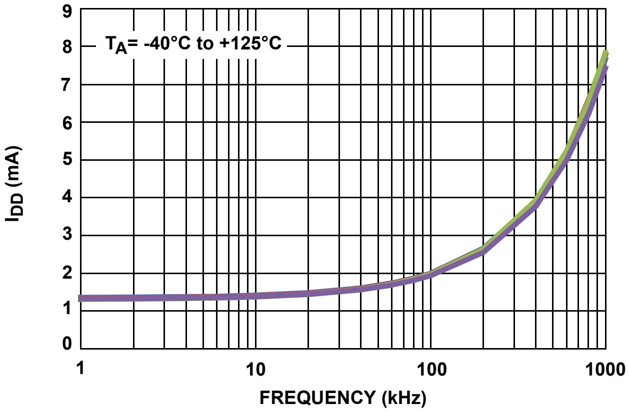


FIGURE 6. $I_{DD}$ OPERATING CURRENT vs FREQUENCY, $R_{DT}$ = 47kΩ

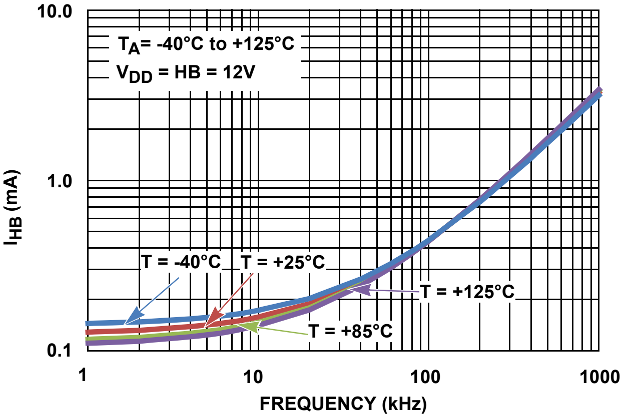


FIGURE 7. $I_{HB}$ OPERATING CURRENT vs FREQUENCY, $R_{DT}$ = 8kΩ

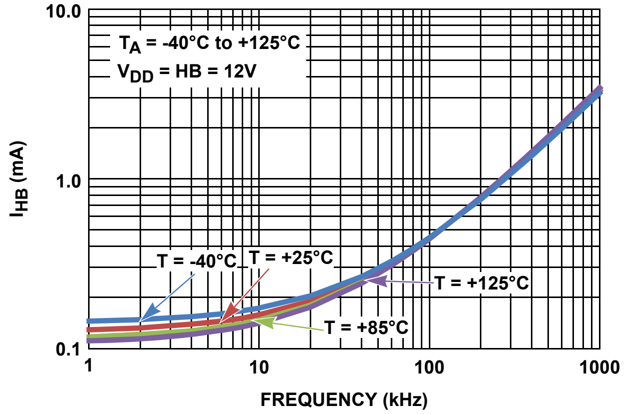


FIGURE 8. $I_{HB}$ OPERATING CURRENT vs FREQUENCY, $R_{DT}$ = 47kΩ

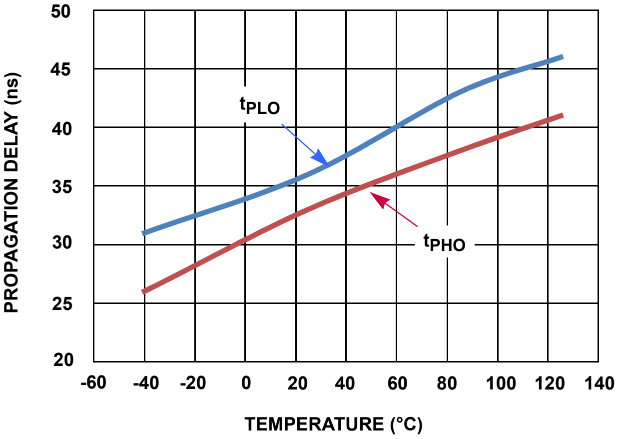


FIGURE 9. PROPAGATION DELAYS vs TEMPERATURE

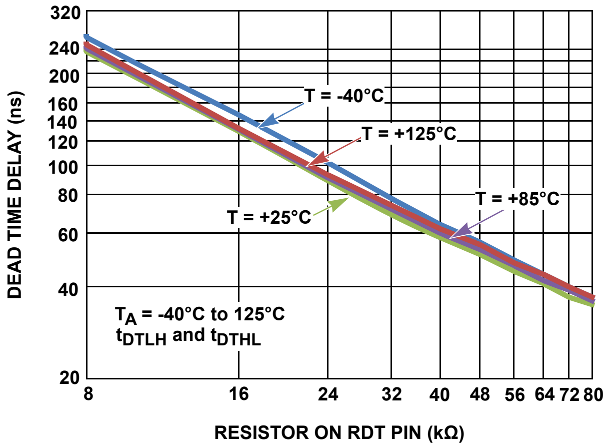


FIGURE 10. DEAD-TIME DELAY VS RDT RESISTOR

## Typical Performance Curves

Unless otherwise specified, operating conditions at: T = +25°C; $V_{DD}$ = EN = 12V; $V_{SS}$ = HS = 0V; Capacitor from HB to HS pin $C_{BOOT}$ = 0.47µF; 100kΩ load on LO and HO to VSS. **(Continued)**

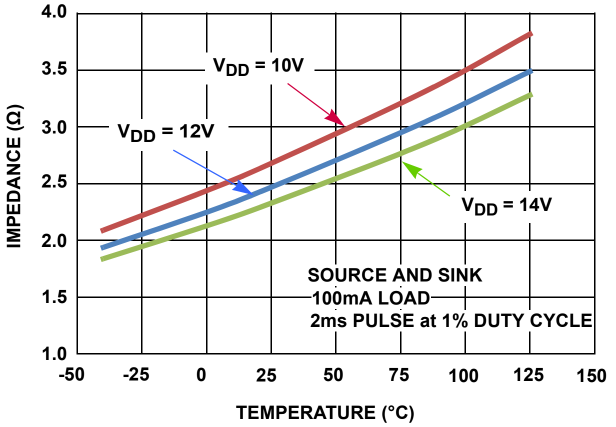


FIGURE 11. HO and LO PIN OUTPUT IMPEDANCE vs TEMPERATURE

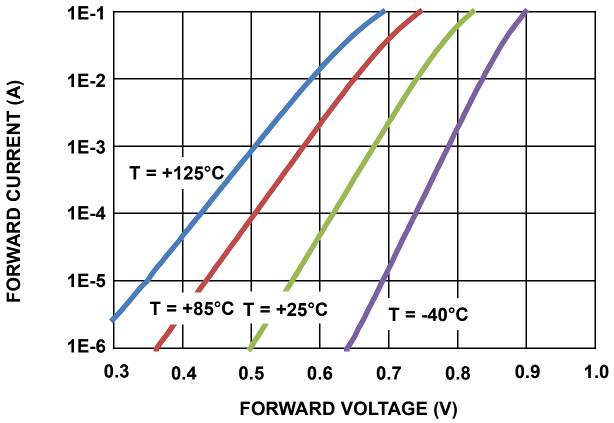


FIGURE 12. BOOTSTRAP DIODE I-V CHARACTERISTICS

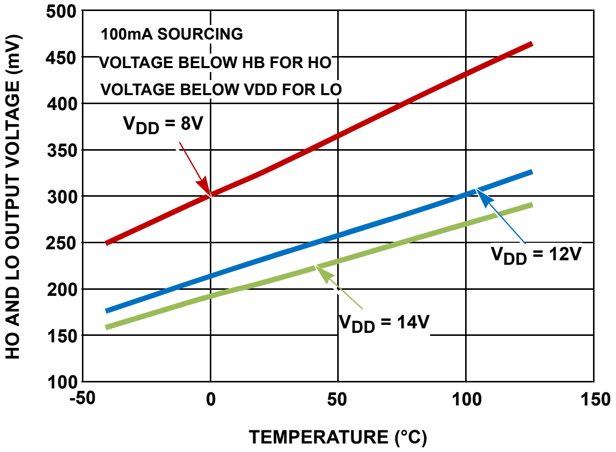


FIGURE 13. OUTPUT HIGH (VOH) VOLTAGE vs TEMPERATURE

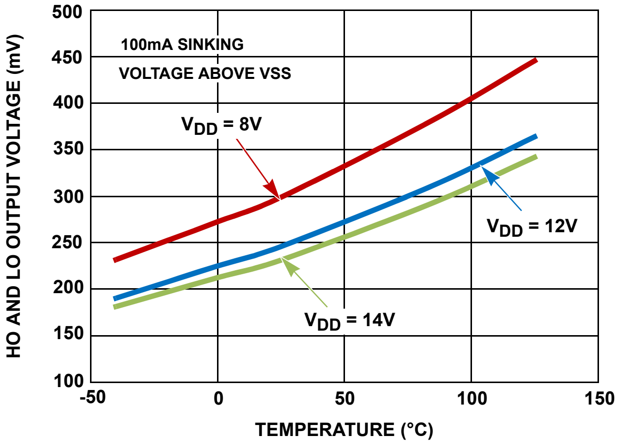


FIGURE 14. OUTPUT LOW (VOL) VOLTAGE vs TEMPERATURE

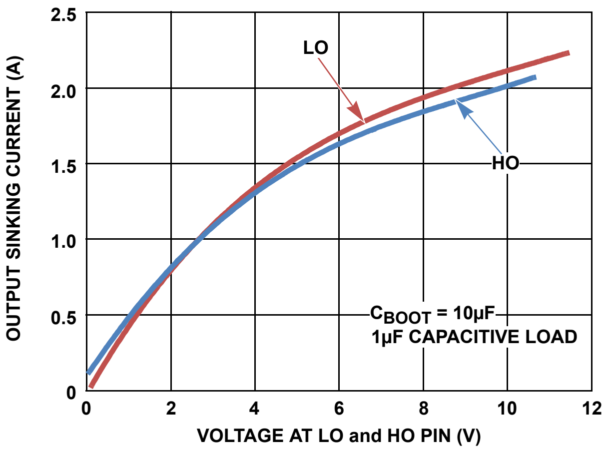


FIGURE 15. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

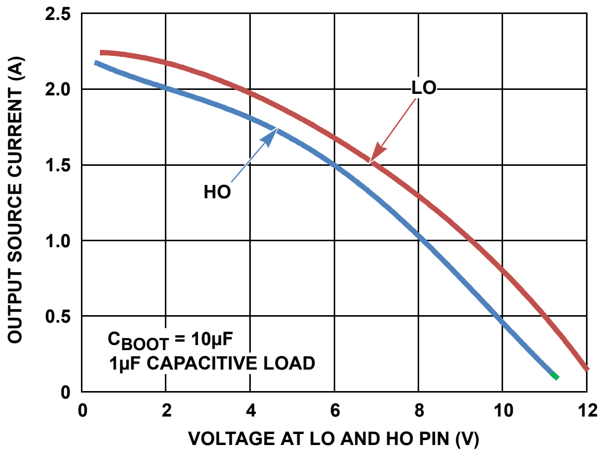


FIGURE 16. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

## Typical Performance Curves

Unless otherwise specified, operating conditions at: T = +25°C; $V_{DD}$ = EN = 12V; $V_{SS}$ = HS = 0V; Capacitor from HB to HS pin $C_{BOOT}$ = 0.47µF; 100kΩ load on LO and HO to VSS. **(Continued)**

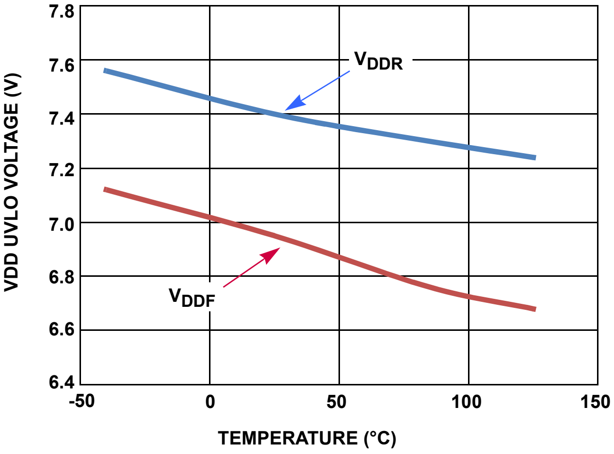


**FIGURE 17. VDD UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE**

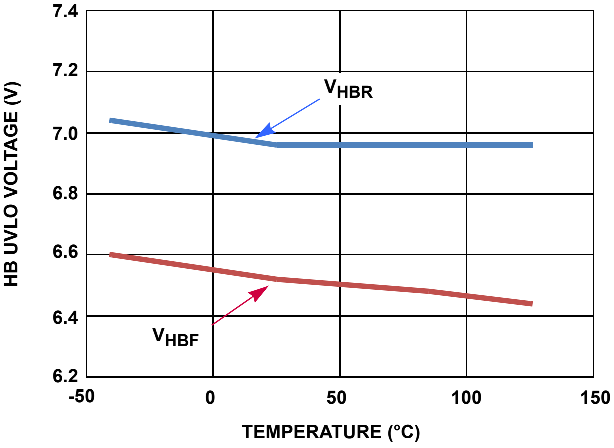


**FIGURE 18. $V_{HB}$ UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE**

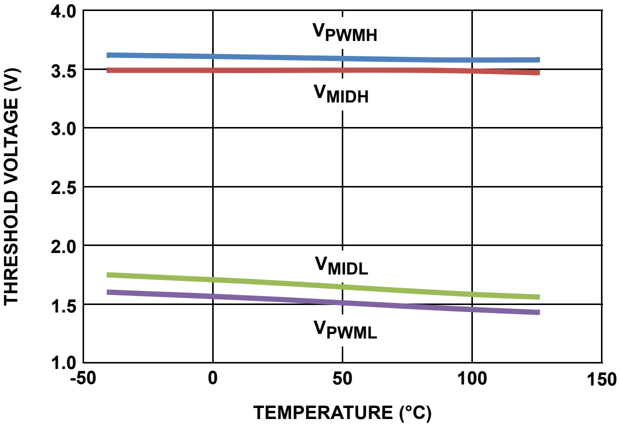


**FIGURE 19. PWM LOGIC THRESHOLD vs TEMPERATURE**

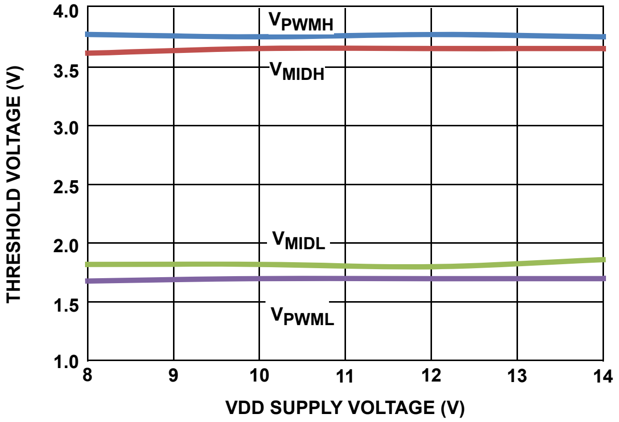


**FIGURE 20. PWM LOGIC THRESHOLD VS SUPPLY VOLTAGE**

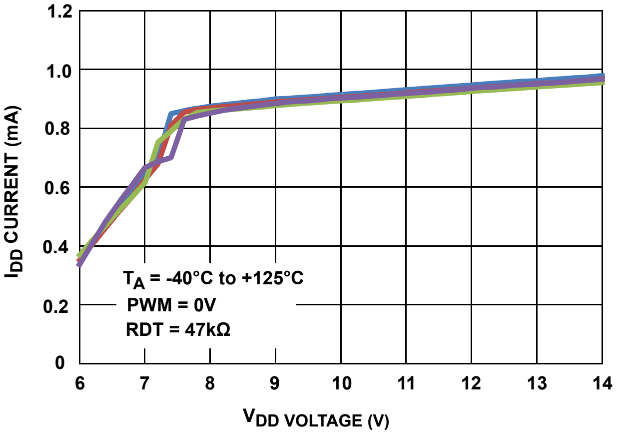


**FIGURE 21. $I_{DD}$ QUIESCENT CURRENT vs SUPPLY VOLTAGE**

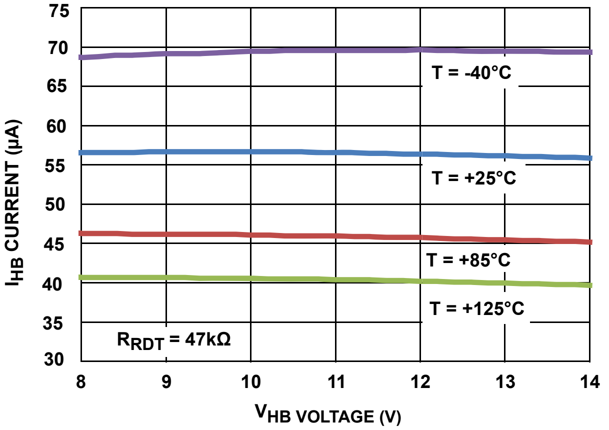


**FIGURE 22. $I_{HB}$ QUIESCENT CURRENT vs VOLTAGE**

# Functional Description

## Gate Drive for NMOS Half-Bridge

The ISL78420 is a NMOS FET driver for up to 100V half-bridge configurations. In a half-bridge configuration the low-side FET source is connected to ground while the low-side FET drain and the high-side FET source are connected together to form the phase or switching node. The drain of the high-side FET is connected to the high voltage power supply.

The gate of the low-side FET requires a ground referenced drive signal to switch on and off. The signal needs to be above the gate threshold VGS of the FET. The gate drive of the high-side FET is more challenging and is what the ISL78420 is designed for. The high-side FET source is the phase node, which switches between ground and the high voltage supply connected to the high-side FET drain. The gate voltage needs to be above the source voltage by $V_{GS}$ to turn on (the source can be as high as 100V). A bootstrap circuit is implemented to generate a bias voltage above the voltage seen at the phase node to drive the gate of the high-side FET.

Key properties of a half-bridge gate driver are:

1. Gate drive signals needs to be sufficiently higher than the $V_{GS}$ specified in MOSFET datasheets for proper operation. For 60V to 100V NMOS FETs the gate threshold is in the range of 2V to 4V. For switching operation, the $V_{GS}$ is typically specified in a range of 8V to 12V.
2. Gate drive signal needs to provide sufficient current to charge and discharge the dynamic gate capacitance of power MOSFETs in the target switching frequencies up to 1MHz. For 60V to 100V NMOS FETs, the typical gate charge can be as high as 80nC.

## Functional Overview

The ISL78420 is a 100V, 2A high frequency half-bridge driver designed to deliver the fast gate charge needed to switch half-bridge configured NMOS FETs. The ISL78420 features a tri-level logic input to control the high- and low-side gate driver using only a single input pin. Typically, bridge drivers have independent inputs to add dead-time control. The ISL78420 also features a dead-time control allowing the user to program dead time from a range of 35ns to 220ns with a single resistor to ground.

A unique feature of the ISL78420 is the PWM pin's tri-level logic input. It allows control of the high-side and low-side drivers with a single pin. When the PWM input is at logic high, the high-side bridge FET is turned on and the low-side FET is off. When the input is at logic low, the low-side bridge FET is turned on and the high-side FET is turned off. When the input voltage is in tri-level state, both the high and low-side bridge FETs are turned off. This driver is designed to work in conjunction with the ISL78220 and ISL78225 "Multi-Phase Interleaved Boost PWM Controller" and the ISL78226 "6-Phase 12V/48V Bidirectional Synchronous PWM Controller". The enable pin (EN) when low turns both bridge FETs off. The EN input is used when the interfacing controller does not utilize a tri-level output. Both PWM and EN logic inputs are $V_{DD}$ tolerant.

The ISL78420 high-side driver bias is established by the internal boot diode and the external boot capacitor connected between the HB and HS pins. The charge on the boot capacitor is provided by the internal boot diode that is connected from VDD to HB (referred to as boot refresh). The current path to charge the boot capacitor occurs when the low-side bridge FET is on, which takes the phase node (HS pin) to ground. The charge current is limited in amplitude by the internal resistance of the boot diode and the low-side FET $r_{DS(ON)}$. Assuming that the on time of the low-side FET is sufficiently long to fully charge the boot capacitor, the boot voltage on the HB pin ($V_{HB}$) will charge to VDD minus the boot diode drop and the on-voltage of the low-side bridge FET.

When the PWM input transitions high, the high-side bridge FET is driven on after the low-side FET is turned off. The HS node is connected to the source of the high-side FET and the HS node will rise almost to the level of the bridge voltage $V_{BRIDGE}$ (minus the on-voltage drop across the high-side FET). The boot capacitor voltage is referenced to the source voltage of the high-side FET so the $V_{HB}$ voltage is approximately $V_{DD}$ volts above the HS node and the boot diode is reversed biased by $V_{BRIDGE}$. Because the high-side driver circuit is referenced to the HS node, the HO output is now approximately $V_{HB}$ + $V_{BRIDGE}$ above ground. More importantly, the HO gate drive is approximately $V_{DD}$ above the HS node to provide the proper $V_{GS}$ to turn on the high-side FET.

During the low-to-high transition of the HS node, the boot capacitor supplies the necessary charge current to fully turn on the high-side FET gate. After the gate is fully charged, the boot capacitor voltage continues to provide bias to the high-side gate to keep the FET on. The stored charge of the boot capacitor must be substantially larger than the required gate charge of the high-side FET and the bias current of the high-side driver otherwise the boot voltage will sag excessively. If the boot capacitor value is too small for the required on-time of the high-side FET, causing the boot voltage to drop below the high-side bias HB pin UVLO falling threshold (6.3V typical), the high-side driver is disabled resulting in undesireable operation. See "Selecting the Boot Capacitor Value" for choosing the proper capacitor value.

# Application Information

## Selecting the Boot Capacitor Value

The boot capacitor value is chosen not only to supply the internal bias current of the high-side driver but also, and more significantly, to provide the gate charge of the high-side driven FET without causing the boot voltage to sag excessively. As good practice, the boot capacitor should have a total charge that is 10x to 20x the gate charge of the power FET to achieve a 5% to 10% drop in voltage after the charge has been transferred from the boot capacitor to the gate capacitance. The high-side driver bias voltage is $V_{DD}$ - VF where VF is the voltage drop of the boot diode. If the boot voltage (HB - HS) is allowed to drop below the HB UVLO falling threshold (6.3V typical) this will disable the high-side driver.

The boot capacitor is discharged by three means:

1. The bias current of the high-side gate driver.
2. Current flowing through the resistor across the gate-to-source of the high-side FET.
3. Gate current when the high-side FET is turned ON.

The boot capacitor is recharged through the boot diode internal to the ISL78420 during the time the low-side FET turns on, taking the HS pin to ground. The ISL78420's internal boot diode has a typical dynamic impedance of 0.8Ω, which recharges the boot capacitor quickly. The low dynamic impedance allows the ISL78420 to drive the high frequency half-bridge, depending on the boot capacitor value used.

The following parameters are required to calculate the value of the boot capacitor for a specific amount of voltage droop. In this example, the values used are arbitrary. They should be changed to comply with the actual application.

| | |
|---|---|
| $V_{DD}$ = 12V | $V_{DD}$ can be any value between 8V and 14V |
| $V_{HB}$ = $V_{DD}$ - 0.7V = $V_{HO}$ | High-side driver bias voltage ($V_{DD}$ - boot diode voltage) referenced to $V_{HS}$ |
| Period = 1ms | This is the longest expected switching period |
| $I_{HB}$ = 150µA | Worst case high-side driver current when xHO = high (this value is specified for $V_{DD}$ = 12V) |
| $R_{GS}$ = 100kΩ | Gate-source resistor (usually not needed) |
| Ripple = 5% | Discharge droop voltage on the boot capacitor (larger droop is not recommended) |
| $I_{gate\_leak}$ = 100nA | From the FET vendor’s datasheet |
| Qgate at 80V = 80nC | From Figure 23 |

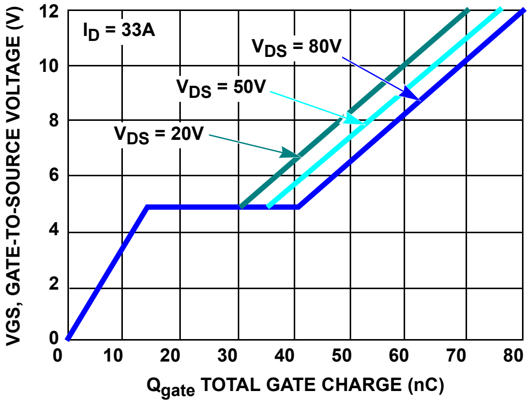


FIGURE 23. TYPICAL GATE CHARGE OF A POWER NMOS FET

The following equations calculate the total charge required for one switching cycle of the high-side FET. These equations assume that all of the parameters are constant during the period duration. The error is insignificant if the ripple voltage allowed is small (5% or less as specified above).

$$Q_C = Q_{gate} + \text{Period} \times (I_{HB} + V_{HO}/R_{GS} + I_{gate\_leak}) \quad \text{(EQ. 1)}$$

$$C_{boot} = Q_C/(\text{Ripple}*\text{VDD}) \quad \text{(EQ. 2)}$$

$$C_{boot} = 0.57\mu F$$

If the gate-to-source resistor is removed ($R_{GS}$ is usually not needed) then:

$C_{boot}$ = 0.38µF

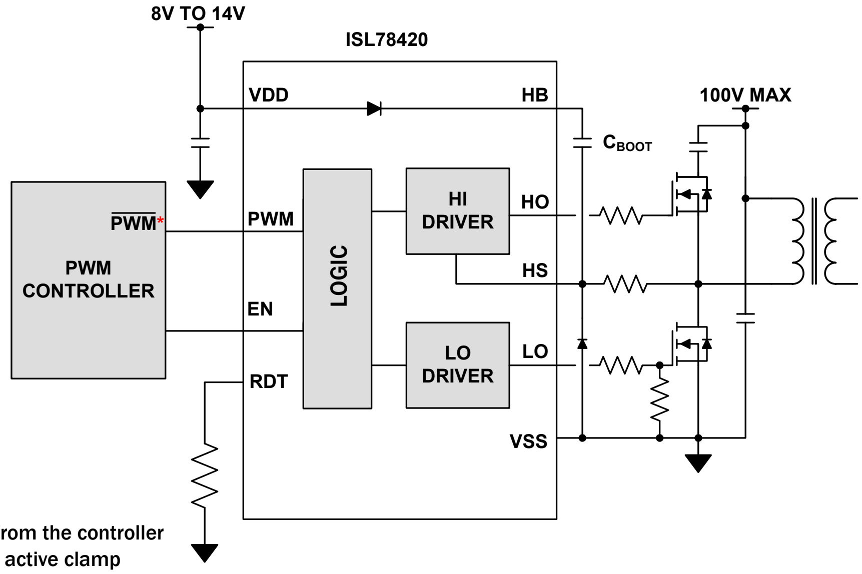
## Input Capacitor

The input capacitor to the VDD pin serves two main purposes. It provides AC decoupling and transient current for the dynamic switching of the high and low-side gate drivers of the ISL78420. The second and more critical function is to provide the gate charge to the low-side driven FET while keeping the VDD voltage ripple to a minimum, similar to the function of the boot capacitor. Improper input capacitance may cause excessive ripple on VDD that triggers the UVLO falling threshold (6.7V typical), disabling the driver. The minimum input capacitance required for the low-side gate charge while maintaining an allowed ripple on VDD is calculated similarly as the boot capacitor described in the previous section. To account for the increased current of $I_{DD}$ vs $I_{HB}$, it is recommended to have the input capacitance be at minimum 10x of the boot capacitor value. In addition, a 0.1µF capacitor in parallel is recommended for high frequency decoupling. For optimal performance, place these capacitors close to the VDD and VSS pins.

## Dead-Time Delay

When the PWM input transitions high or low, it is necessary to ensure that both bridge FETs are not on at the same time to prevent shoot-through currents. The ISL78420 programmable timers delay the rising edge of the high-side (HO) and low-side (LO) gate drives so that both FETs are off before one of them is turned on. The dead-time delay on the rising edge of LO and HO is programmable with a single resistor from the RDT pin to $V_{SS}$. The dead time is adjustable from 35ns ($R_{RDT}$ = 80kΩ) to 220ns ($R_{RDT}$ = 8kΩ). It is not recommended to use resistors beyond these values. The dead time is set equal on both falling edges of LO and HO. See “Timing Diagram” on page 6 for the definition of dead-time delay. See Figure 10 on page 7 for the programmed dead time vs resistor value.

While the voltage of the PWM signal is within the boundaries of the mid-level logic (1.6V to 3.4V typical), the HO and LO pins are driven low (with respect to VSS for LO pin and with respect to HS for HO pin). The actual delay time, as programmed by the $R_{RDT}$ resistor value, begins when the high or low logic threshold levels at the PWM input are crossed. The time when the PWM input is in the mid-level range is added to the programmed dead time. This should be a consideration when selecting the $R_{RDT}$ value for a specific dead time.



NOTE: The PWM signal from the controller must be inverted for this active clamp forward topology.

FIGURE 24. TYPICAL ACTIVE CLAMP FORWARD APPLICATION

# Typical Application Circuit

Depending on the application, the switching speed of the bridge FETs can be reduced by adding series connected resistors between the HO output and the FET gate. Gate-to-source resistors are recommended on the low-side FETs to prevent unexpected turn-on of the bridge should the bridge voltage be applied before VDD. Gate-to-source resistors on the high-side FETs are not usually required if low-side gate-to-source resistors are used. If relatively low value gate-to-source resistors are used on the high-side FETs, be aware that a larger value for the boot capacitor may be required.

## Transients on HS Node

An important operating condition that is occasionally overlooked by designers is the negative transient on the HS pin that can occur when the high-side bridge FET turns off. The maximum transient allowed on the HS pin is -5V but it is wise to minimize the amplitude to lower levels. This transient is the result of the parasitic inductance of the low-side drain-source conductor on the PCB. Even the parasitic inductance of the low-side FET contributes to this transient.

When the high-side bridge FET turns off (see Figure 25), because of the load inductive characteristics, the current that was flowing in the high-side FET (blue) must rapidly commutate to flow through the low-side FET (red). The amplitude of the negative transient impressed on the HS node is (L*di/dt) where L is the total parasitic inductance of the low-side FET drain-to-source path and di/dt is the rate at which the high-side FET is turned off. With the increasing power levels of power supplies and motors, clamping this transient becomes significant for the proper operation of the ISL78420.

In the event that the negative transient exceeds -5V, there are several ways of reducing the negative amplitude of this transient. If the bridge FETs are turned off more slowly to reduce di/dt, the amplitude will be reduced but at the expense of more switching losses in the FETs. Careful PCB design will also reduce the value of the parasitic inductance. However, in extreme cases, these two solutions by themselves may not be sufficient. Figure 25 illustrates a simple method for clamping the negative transient. Two series connected, fast 1 amp PN junction diodes are connected between HS and VSS as shown. It is important that these diodes be placed as close as possible to the HS and VSS pins to minimize the parasitic inductance of this current path between the two pins. Two diodes in series are required because they are in parallel with the body diode of the low-side FET. If only one diode is used for the clamp, it will conduct some of the negative load current that is flowing in the body diode of the low-side FET.

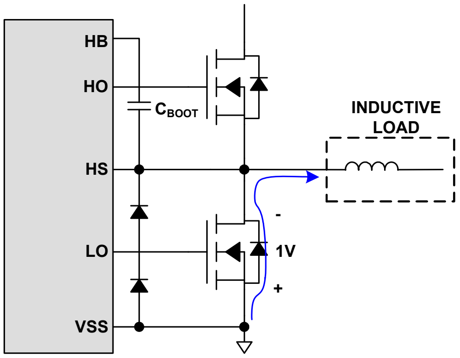


FIGURE 25. TWO CLAMPING DIODES TO SUPPRESS NEGATIVE TRANSIENTS

An alternative to the two series connected diodes is one diode and a resistor, (see Figure 26). In this case, it is necessary to limit the current in the diode with a small value resistor, $R_{HS}$, connected between the phase node of the 1/2 bridge and the HS pin. Observe that $R_{HS}$ is effectively in series with the HO output and serves as a peak current limiting gate resistor on HO.

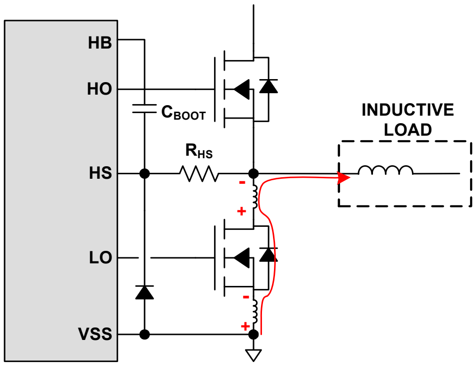


FIGURE 26. RESISTOR AND DIODE NEGATIVE TRANSIENT CLAMP

The value of $R_{HS}$ is determined by how much average current in the clamping diode is acceptable. Current in the low-side FET flows through the body diode during dead time resulting with a negative voltage on HS that is typically about -1.5V. When the low-side FET is turned on, the current through the body diode is shunted away into the channel and the conduction voltage from source-to-drain is typically much less than the conduction voltage through the body diode. Consequently, significant current will flow in the clamping diode only during the dead time. Because the dead time is much less than the on time of the low-side FET, the resulting average current in the clamping diode is very low. The value of $R_{HS}$ is then chosen to limit the peak current in the clamping diode and usually just a few ohms is necessary.

Please note that a similar transient with a positive polarity occurs when the low-side FET turns off. This is less frequently a problem because the HS node is floating up toward the bridge bias voltage. The Absolute Max voltage rating for the HS node does need to be observed when the positive transient occurs.

The maximum rating for $V_{HB} - V_{HS}$ = 14V must also not be overlooked. When a negative transient, Vneg, is present on the HS pin, the voltage differential across HB and HS will approach VDD + Vneg. If the transient duration is short compared to the charging time constant of the boot diode and boot capacitor, the voltage across HB and HS is not significantly affected. However, another source of negative voltage on the HS pin may increase the boot capacitor voltage for a longer duration. During dead time, current is flowing from the source-to-drain of the low-side FET body diode. Depending on the size of the FET and the amplitude of the reverse current, the voltage across the diode can be as high as -1.5V and much higher during a load fault. Because this negative voltage has little impedance, the boot capacitor can charge to a voltage greater than VDD (for example VDD + 1.5V). It may be necessary to either clamp the voltage as described in Figures 25 and 26 and/or keep the dead time as short as possible.

## Power Dissipation

The power dissipation of the ISL78420 is dominated by the gate charge required by the driven bridge FETs and the switching frequency. The internal bias and boot diode also contribute to the total dissipation but these losses are usually less significant compared to the gate charge losses.

The calculation of the power dissipation of the ISL78420 is approximated by the following equations:

### GATE POWER (FOR THE HO AND LO OUTPUTS)

$$P_{gate} = (Q_{gateH} + Q_{gateL}) \times Freq \times VDD \qquad \text{(EQ. 3)}$$

where $Q_{gateH}$ and $Q_{gateL}$ is the total gate charge of the high-side and low-side bridge FET respectively. VDD is the bias to the ISL78420 and Freq is the switching frequency.

### BOOT DIODE DISSIPATION

$$I_{diode\_avg} = Q_{gate} \times Freq \qquad \text{(EQ. 4)}$$

$$P_{diode} = I_{diode\_avg} \times 0.7V \qquad \text{(EQ. 5)}$$

where 0.7V is the diode conduction voltage. Equations 4 and 5 represent the boot diode conduction loss from recharging the boot capacitor during the refresh cycle. The average current is proportional to the total charge delivered to the high-side NFET and the switching frequency.

### BIAS CURRENT

$$P_{bias} = I_{bias} \times VDD \qquad \text{(EQ. 6)}$$

where $I_{bias}$ is the internal bias current of the ISL78420 at the switching frequency (see Figures 5 and 6).

### TOTAL POWER DISSIPATION

$P_{total} = P_{gate} + P_{diode} + P_{bias}$

### JUNCTION OPERATING TEMPERATURE

$T_J = P_{total} \times \theta_{JA} + T_A$

where $T_J$ is the junction temperature at the operating ambient temperature, $T_A$, in the vicinity of the part.

$T_J = P_{total} \times \theta_{JC} + T_{PCB}$

where $T_J$ is the junction temperature with the operating temperature of the PCB, $T_{PCB}$, as measured where the EPAD is soldered.

## High Voltage Conductor Spacing

The HTSSOP package adheres to IPC-2221 guidelines for high voltage conductor spacing of external component leads. The required pin-to-pin spacing for 100V conductors is 0.5mm for nonconformal coat PCB boards. For the ISL78420 14 Ld HTSSOP package, the high voltage pins are separated from the low voltage pins across the 4.4mm wide package. While the HB, HO, and HS pins are grouped together and can swing from 0V to 114V, under normal operation the maximum differential voltage across these pins is limited by the VDD supply (14V Max Operating).

# PC Board Layout

The AC performance of the ISL78420 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance from the ISL78420:

- Understand how power currents flow. The high amplitude di/dt currents of the bridge FETs will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Avoid paralleling high di/dt traces with low level signal lines. High di/dt will induce currents in the low level signal lines.
- When practical, minimize impedances in low level signal circuits; the noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Core gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines.
- The use of low inductance components such as chip resistors and chip capacitors is recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, it may be necessary to add series gate resistors on the bridge FETs to dampen the oscillations.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for the PWM control circuits.
- Avoid having a signal ground plane under a high dv/dt circuit. This will inject high di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Most PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic capacitors, power resistors, etc.) will have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components.

# EPAD Design Considerations

The thermal pad of the ISL78420 is electrically isolated. Its primary function is to provide heat sinking for the IC. It is recommended to tie the EPAD to VSS (GND).

Figure 27 is an example of how to use vias to remove heat from the IC substrate. Depending on the amount of power dissipated by the ISL78420, it may be necessary to connect the EPAD to one or more ground plane layers. A via array, within the area of the EPAD, will conduct heat from the EPAD to the ground plane on the bottom layer. If inner PCB layers are available, it would also be desirable to connect these additional layers with the plated-through vias.

The number of vias and the size of the GND planes required for adequate heat-sinking is determined by the power dissipated by the ISL78420, the air flow, and the maximum temperature of the air around the IC.

It is important that the vias have a low thermal resistance for efficient heat transfer. Do not use “thermal relief” patterns to connect the vias.

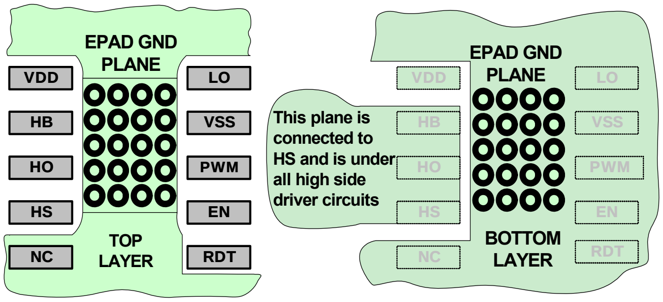


FIGURE 27. RECOMMENDED PCB HEATSINK

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| September 29, 2016 | FN8296.4 | Updated POD to latest revision with updated tiebar note. Updated page 1 description, features, applications and Figure 1 as well as “Functional Overview” on page 10 to incorporate newly released ISL78226 part. |
| November 6, 2014 | FN8296.3 | Removed all references to 9 Ld TDFN (ISL78420ARTBZ) part as it is EOL.<br>Page 1<br>1.Updated Figure 1 with new block diagram for focused applications.<br>Page 2<br>1.Updated Block Diagram on page 2.  Changed internal reference from 5.0V to 6.1V.  Changed PWM pin pull-up resistor from 100kΩ to 235kΩ.  Changed PWM pin pull-down resistor from 100kΩ to 165kΩ.  Changed EN pin pull-up 210kΩ resistor to 210kΩ pull-down resistor.  This is to correct previous datasheet revision error.  Not a functional change to the die.<br>2.Added ISL78420AVEZ 14 Ld HTSSOP package pin out diagram.<br>3.ISL78420ARTAZ Pin Configuration watermarked "NOT RECOMMENDED FOR NEW DESIGNS".<br>Page 3<br>1.Pin Description Table updated with 14 Ld HTSSOP package.<br>2.Ordering Information table added ISL78420AVEZ 14 Ld HTSSOP package.<br>3.Ordering Information table: ISL78420ARTAZ part include: "NOT RECOMMENDED FOR NEW DESIGNS"<br>4.Updated Note 4 from ““B” package option has alternate pin assignments for compliance with 100V Conductor Spacing Guidelines per IPC-2221. Note that Pin 2 is omitted for additional spacing between pins 1 and 3.” to “These packages meet compliance with 100V Conductor Spacing Guidelines per IPC-2221.”<br>Page 4<br>1.Maximum Recommended Operating Condition update section:<br>a.On Voltage on HB removed the line VDD-1V to VDD+100V.  This verbiage is clarified with Note 6.<br>2.Thermal Information section:<br>a.Added 14 Ld HTSSOP data to Thermal Resistance table<br>b.Added 14 Ld HTSSOP data to Max Power Dissipation at +25°C table<br>3.ESD Ratings section update:<br>a.Changed Human Body Model from 3000V to 2000V<br>b.Removed Machine Model ESD rating specification<br>4.Notes section for Abs Max Section update:<br>a.Removed note 5 "The ISL78420 is capable of derated operation at supply voltages exceeding 14V.  Figure 17 shows the high-side voltage derating curve for this mode of operation".  Added new Note 6 "The operating voltage from HB to GND is the sum of VDD and the HS voltage.  The maximum operating voltage from HB to GND is recommended to be under 114V.<br>b.Added Note 9: "Specified at published junction to ambient thermal resistance for a junction temperature of 150°C." to reference Max Power Dissipation at +25°C.<br>5.Electrical Specifications Test Conditions:<br>a.Added test condition: EN = 12V<br>b.Removed test condition RDT = 0k<br>c.Removed test condition PWM = 0V<br>6.VDD Quiescent Current<br>a.Added in under Test Condition PWM = 12V<br>7.Total HB Quiescent Current<br>a.Changed LI = HI = 0V to PWM = EN = 0V<br>8.HB to VSS Current, Quiescent<br>a.Changed from LI = HI = 0V; VHB = VHS = 114V to PWM = EN = 0V; VHB = VHS = 100V<br>9.HB to VSS Current, Operating<br>a.Change from VHB = VHS = 114V to VHB = VHS = 100V<br>10.Tri-Level PWM Input: High Level Threshold Full Temperature limit changed from MAX = 4.3V to MAX = 4.1V.<br>11.Added in verbiage to Middle Level Range for clarity<br>12.Updated PWM Tri-Level pull-up Resistors<br>a.Split into two rows: pull-up resistor 235kΩ.  Pull-down resistor 165kΩ. |

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

| DATE | REVISION | CHANGE |
|---|---|---|
| November 6, 2014<br>(continued) | FN8296.3<br>(continued) | Page 5 and Page 6<br>1.EN Input Low Level Threshold<br>a.T = 25C specifications changed from MIN = 1.4; TYP = 1.8 to MIN = 1.8; TYP = 2.5<br>b.Full Temperature specifications changed from MIN = 1.2 to MIN = 1.8<br>2.EN Input High Level Threshold<br>a.T = 25C specifications changed from TYP = 1.8; MAX = 2.2 to TYP = 2.8; MAX = 4.<br>b.Full Temperature specification change from MAX = 2.4 to MAX = 4.1<br>3.EN Pull-Up Resistance changed to EN Pull-Down Resistor. Resistance value unchanged. This is to correct previous datasheet revision error. Not a functional change to the die.<br>4.Under Voltage Protection VDD Rising Threshold<br>a.MAX limit changed from 8.1V to 8.0V<br>5.Bootstrap Diode<br>a.Low Current Forward Voltage: Changed test condition from 100mA to 100µA. This is to correct previous datasheet revision error. Not a functional change to the test.<br>b.Dynamic Resistance: Test condition clarified. Added formula to calculate dynamic resistance at 50mA and 100mA diode current. This is to correct previous datasheet revision error. Not a functional change to the test.<br>6.Switching Specification Test Condition: Changed RDT = 0kΩ to RDT = 8kΩ or 80kΩ.<br>7.Added Dead Time Delay Matching Specifications for RDT at 8kΩ and 80kΩ.<br>Page 7 to Page 9<br>1.Updated Figures Figures 5 through 8 for clarity.<br>2. Figure 7 (High Level Output Voltage vs Temp) and Figure 8 (Low Level Output Voltage vs Temp) moved to Figures 13 and 14 and updated for clarity.<br>3. Figure 11 (UVLO Rising Threshold) and Figure 12 (UVLO Hysteresis) moved to Figures 17 and 18 and revised for clarity.<br>4. Figure 11 (Propagation Delay vs Temp) moved to Figure 9 and updated for clarity.<br>5. Figure 12 (Delay Matching vs Temp) removed.<br>6. Figure 15 (Peak Pull-up Current) and Figure 16 (Peak Pull-down Current) updated for clarity.<br>7. Figure 15 (Quiescent Current vs Voltage) moved to Figures 21 and 22 and updated for clarity.<br>8.Figure 16 moved to Figure 12 and updated for clarity.<br>9.Removed Figure 17 (VHS Voltage to VDD Voltage Derating)<br>10.Added additional Typical Performance Curves for Output Impedance vs Temp and PWM Threshold Voltages<br>Page 10 to Page 12<br>1.Added to Applications Section: Gate Drive for NMOS Half Bridge<br>2.Added to Applications Section: Input Capacitor<br>3.Added to Application Section: Dead Time Delay<br>4.Added to Application Section: High Voltage Conductor Spacing<br>5.Application Section: Transient On HS Node updated with new content<br>6. Equation 1 updated to fix format error.<br>7. Equation 3 updated to fix error. |
| January 24, 2014 | FN8296.2 | Page 14<br>- 2nd line of the disclaimer changed from:<br>"Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted"<br>to:<br>"Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted"<br>Updated "Products" verbiage to "About Intersil" verbiage |
| September 24, 2012 | FN8296.1 | Initial Release |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

For additional products, see www.intersil.com/en/products.html

Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

For information regarding Intersil Corporation and its products, see www.intersil.com

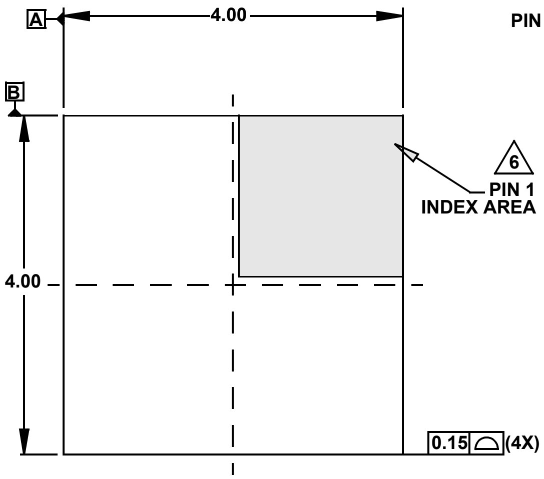
# Package Outline Drawing

For the most recent package outline drawing, see L10.4x4

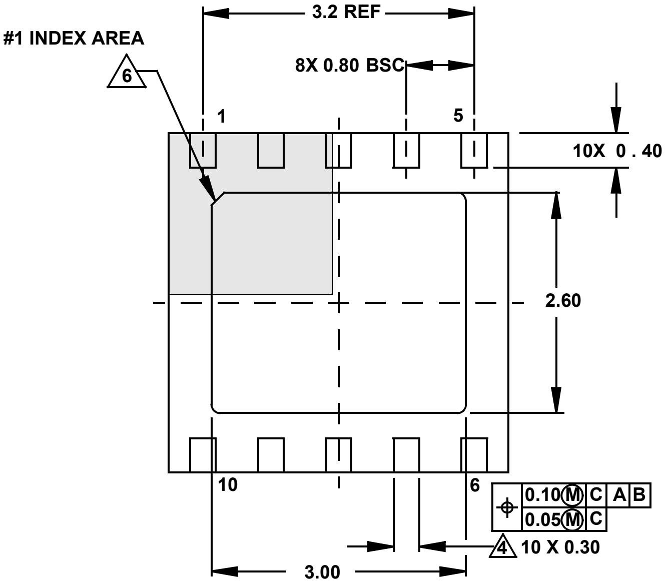
## L10.4x4

**10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE**

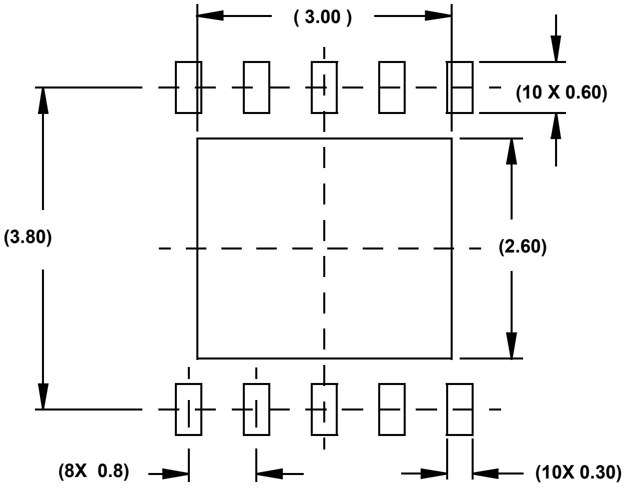
**Rev 2, 4/15**



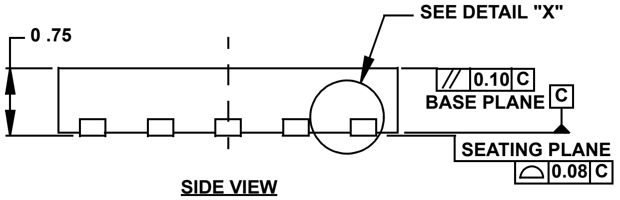
TOP VIEW



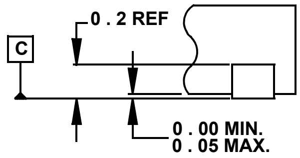
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.