ISL8013A

3A Low Quiescent Current 1MHz High Efficiency Synchronous Buck Regulator

FN7526
Rev 2.01
Dec 3, 2021

The ISL8013A is a high efficiency, monolithic, synchronous step-down DC/DC converter that can deliver up to 3A continuous output current from a 2.8V to 5.5V input supply. It uses a current control architecture to deliver very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL8013A integrates a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 300mV dropout voltage at 3A output current. High 1MHz pulse-width modulation (PWM) switching frequency allows for the use of small external components and the SYNC input enables multiple ICs to synchronize out-of-phase to reduce ripple and eliminate beat frequencies.

The ISL8013A can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference while discontinuous mode provides high efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short circuit and overcurrent conditions, an output overvoltage comparator and over-temperature monitor circuit. A power-good output voltage monitor indicates when the output is in regulation.

The ISL8013A is offered in a space saving 4mmx4mm, Pb-free QFN package with exposed pad leadframes for low thermal resistance.

The ISL8013A includes a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 300mV dropout voltage at 3A.

The ISL8013A offers a 1ms Power-Good (PG) timer at power-up. When shut down, ISL8013A discharges the output capacitor. Other features include internal soft-start, internal compensation, overcurrent protection, and thermal shutdown.

The ISL8013A is offered in a 4mmx4mm 16 Ld QFN package with 1mm maximum height. The complete converter occupies less than 0.4in^2 area.

Features

- High efficiency synchronous buck regulator with up to 97% efficiency
- Power-good (PG) output with a 1ms delay
- 2.8V to 5.5V supply voltage
- 3% output accuracy over temperature, load, line
- 3A output current
- Start-up with prebiased output
- Internal soft-start - 1ms
- Soft-stop output discharge during disable
- 35µA quiescent supply current in PFM mode
- Selectable forced PWM mode and PFM mode
- External synchronization up to 4MHz
- Less than 1µA logic controlled shutdown current
- 100% maximum duty cycle
- Internal current mode compensation
- Peak current limiting and hiccup mode short-circuit protection
- Over-temperature protection
- Small 16 Ld 4mmx4mm QFN
- Pb-Free (RoHS compliant)

Applications

- DC/DC POL modules
- µC/µP, FPGA and DSP power
- Plug-in DC/DC modules for routers and switchers
- Portable instruments
- Test and measurement systems
- Li-ion battery powered devices
- Small form factor (SFP) modules
- Barcode readers

Table of Contents

Ordering Information

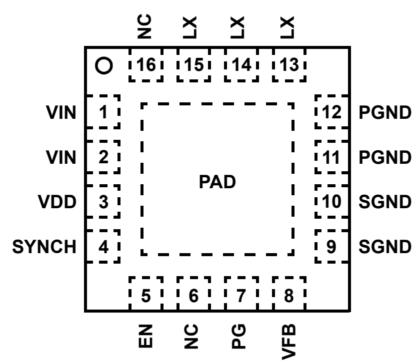
PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE
ISL8013AIRZ	80 13AIRZ	16 Ld 4x4 QFN	L16.4x4	Tube	-40 to +85°C
ISL8013AIRZ-T				Reel, 6k	
ISL8013AIRZ-T7A				Reel, 250	
ISL8013AEVAL2Z	Evaluation Board				

NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL8013A device information page. For more information about MSL, see TB363.

Pin Configuration

ISL8013A
(16 LD QFN)
TOP VIEW



REFER TO AN1365 FOR MORE LAYOUT SUGGESTIONS.

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2	VIN	Input supply voltage. Connect a 10µF ceramic capacitor to power ground.
3	VDD	Input supply voltage for the analog circuitry. Connect to VIN pin.
5	EN	Regulator enable pin. Enable the output when driven to high. Shut down the chip and discharge output capacitor when driven to low. Do not leave this pin floating.
7	PG	1ms timer output. At power-up or EN HI, this output is a 1ms delayed power-good signal for the output voltage.
4	SYNCH	Mode Selection pin. Connect to logic high or input voltage VDD for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the negative edge trigger. Do not leave this pin floating.
13, 14, 15	LX	Switching node connection. Connect to one terminal of the inductor.
11, 12	PGND	Power ground
9, 10	SGND	Signal ground
8	VFB	Buck regulator output feedback. Connect to the output through a resistor divider for adjustable output voltage. For 0.8V output voltage, connect this pin to the output.
6	NC	Pin 6 is used for ISL8013A production test only. It can be connected to GND for noise immunity in applications.
16		No connect pins.
-	Exposed Pad	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to SGND plane for optimal thermal performance.

Typical Application

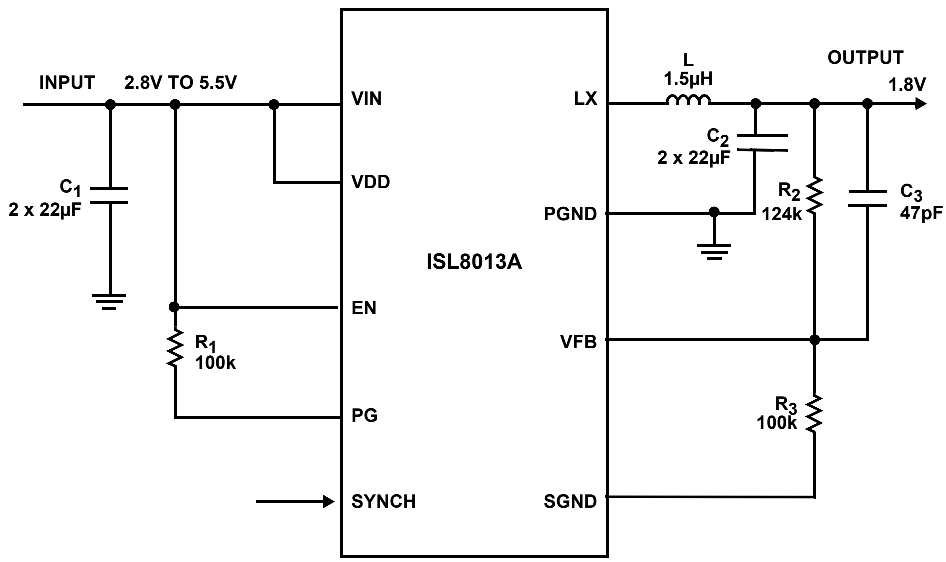


FIGURE 1. TYPICAL APPLICATION DIAGRAM

Block Diagram

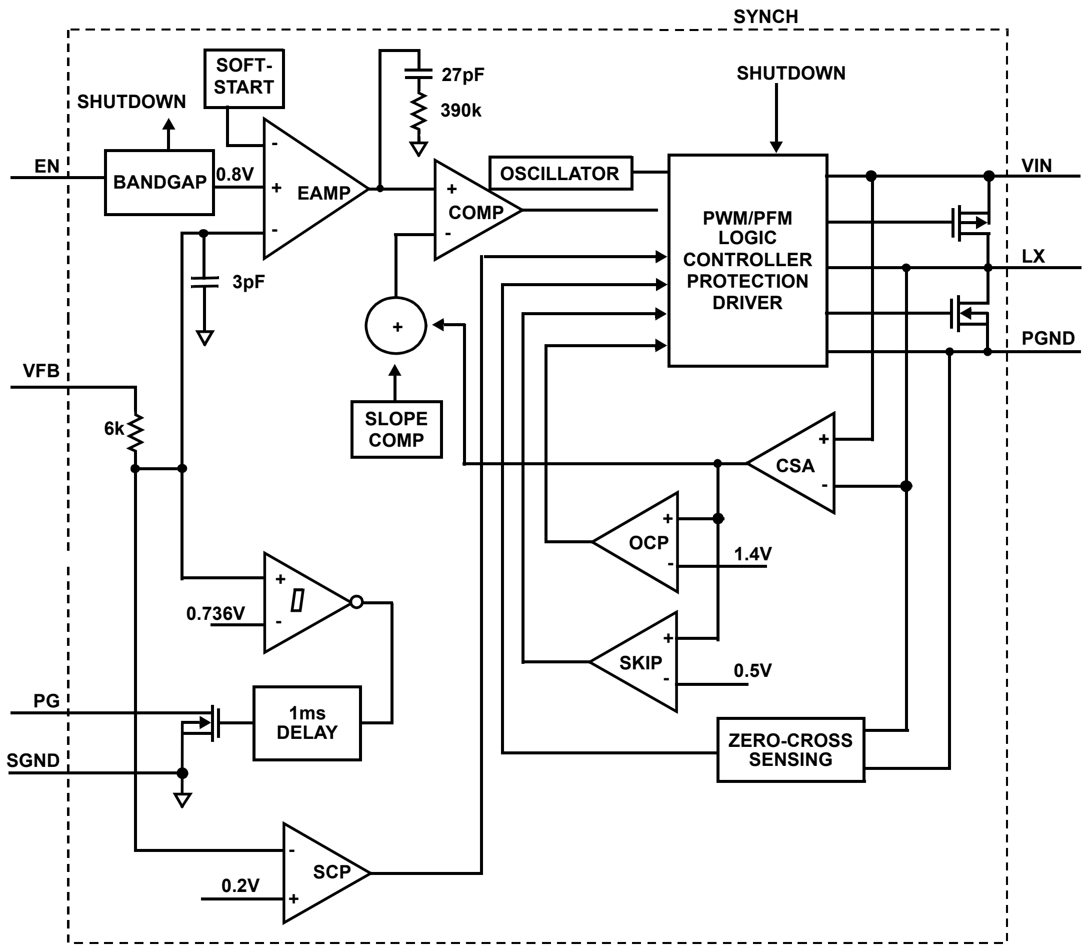


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings (Reference to GND)

VIN, VDD. . . . . -0.3V to 6V (DC) or 7V (20ms)
EN, SYNCH, PG . . . . -0.3V to VIN + 0.3V
LX . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
VFB . . . . -0.3V to 2.8V

Recommended Operating Conditions

VIN Supply Voltage Range. . . . . 2.8V to 5.5V
Load Current Range . . . . 0A to 3A
Ambient Temperature Range . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld 4x4 QFN Package	39	3

Junction Temperature Range . . . . -55°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
5. θ_{JC}, case temperature location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions unless otherwise noted: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = V_{DD}. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load	-	2.6	**2.8**	V
		Falling, no load	**2.15**	2.35	-	V
Quiescent Supply Current	I_{VIN}	SYNCH = GND, no load at the output	-	35	-	µA
		SYNCH = GND, no load at the output and no switches switching	-	30	**45**	µA
		SYNCH = VDD, F_S = 1MHz, no load at the output	-	6.5	**10**	mA
Shut Down Supply Current	I_{SD}	V_{IN} = 5.5V, EN = low	-	0.1	**2**	µA
OUTPUT REGULATION						
Reference Voltage	V_{REF}		**0.790**	0.8	**0.810**	V
VFB Bias Current	I_{VFB}	VFB = 0.75V	-	0.1	-	µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.8V)	-	0.2	-	%/V
Soft-Start Ramp Time Cycle			-	1	-	ms
OVERCURRENT PROTECTION						
Current Limit Blanking Time	t_{OCON}		-	17	-	Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}		-	4	-	SS cycle
Switch Current Limit	I_{LIMIT}	(Note 6)	**4.0**	4.8	**5.9**	A
Peak Skip Limit	I_{SKIP}	(Note 6)	-	1.2	-	A
COMPENSATION						
Error Amplifier Transconductance			-	20	-	µA/V
Trans-Resistance	RT		**0.213**	0.25	**0.287**	Ω
LX						
P-Channel MOSFET ON-resistance		V_{IN} = 5V, I_O = 200mA	-	50	**75**	mΩ
		V_{IN} = 2.8V, I_O = 200mA	-	70	**100**	mΩ

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions unless otherwise noted: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = V_{DD}. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA	-	50	**75**	mΩ
		V_{IN} = 2.8V, I_O = 200mA	-	70	**100**	mΩ
LX Maximum Duty Cycle			-	100	-	%
PWM Switching Frequency	f_S		**0.80**	1.00	**1.20**	MHz
LX Minimum On-Time		SYNCH = High	-	-	**140**	ns
PG						
Output Low Voltage		Sinking 1mA	-	-	**0.3**	V
Delay Time (Rising Edge)			**0.65**	1	**1.35**	ms
PG Pin Leakage Current		PG = VIN = 3.6V	-	0.01	**0.1**	µA
PGOOD Rising Threshold		Percentage of regulation voltage	**89**	92	**95**	%
PGOOD Falling Threshold		Percentage of regulation voltage	**85**	88	**91.5**	%
PGOOD Delay Time (Falling Edge)			-	15	-	µs
EN, SYNCH						
Logic Input Low			-	-	**0.4**	V
Logic Input High			**1.4**	-	-	V
Synch Logic Input Leakage Current	I_{SYNCH}	Pulled up to 5.5V	-	0.1	**1**	µA
Enable Logic Input Leakage Current	I_{EN}		-	0.1	**1**	µA
Thermal Shutdown			-	140	-	°C
Thermal Shutdown Hysteresis			-	25	-	°C

NOTES:

6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A.

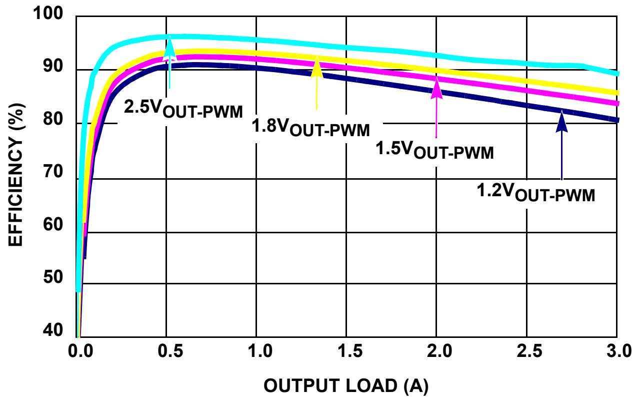


FIGURE 3. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PWM)

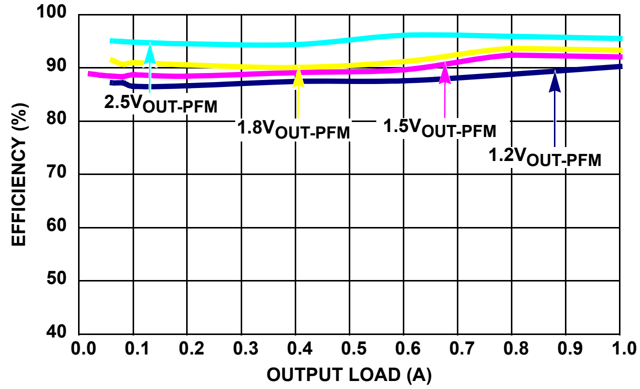


FIGURE 4. EFFICIENCY vs LOAD (1MHz 3.3 V_{IN} PFM)

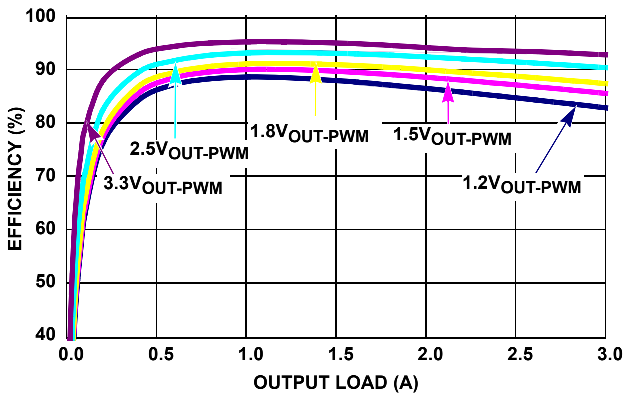


FIGURE 5. EFFICIENCY vs LOAD (1MHz 5V_{IN} PWM)

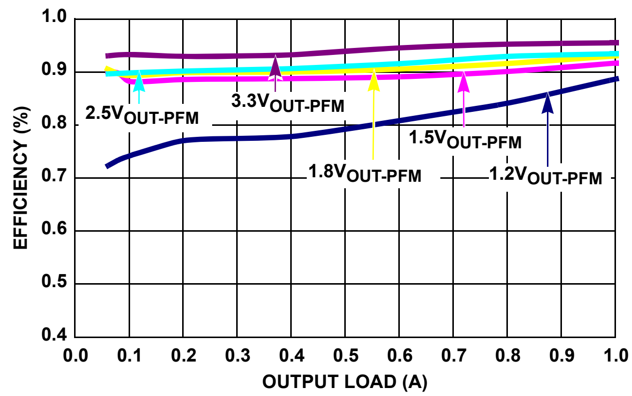


FIGURE 6. EFFICIENCY vs LOAD (1MHz 5V_{IN} PFM)

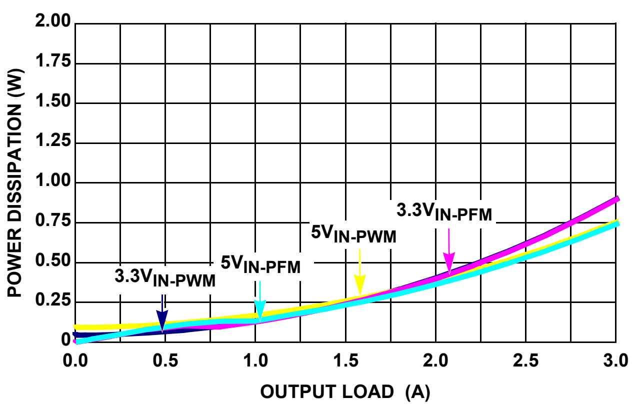


FIGURE 7. POWER DISSIPATION vs LOAD (1MHz, V_{OUT} = 1.8V)

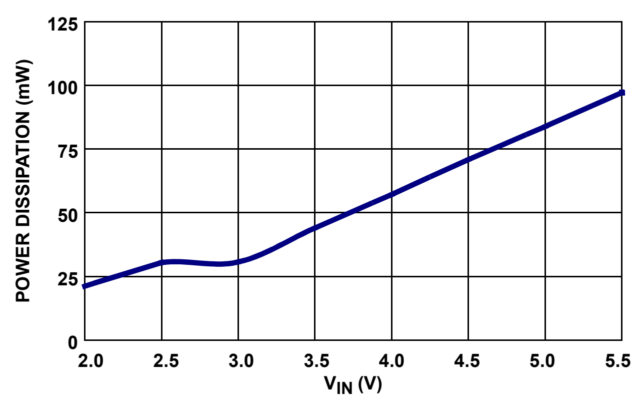


FIGURE 8. POWER DISSIPATION WITH NO LOAD vs V_{IN} (PWM V_{OUT} = 1.8V)

Typical Operating Performance Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A. **(Continued)**

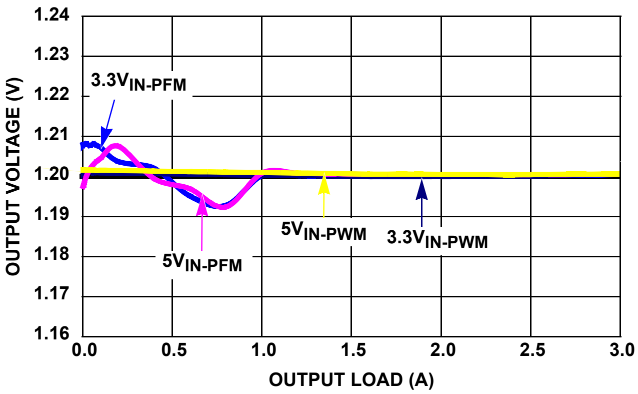


FIGURE 9. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.2V)

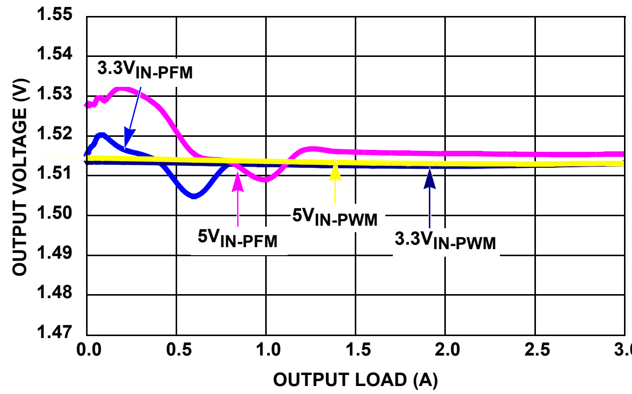


FIGURE 10. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.5V)

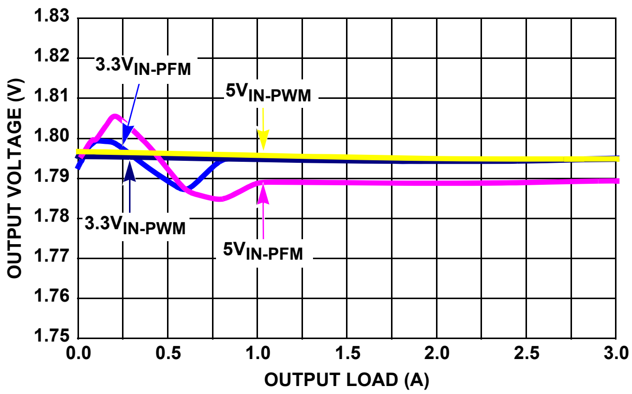


FIGURE 11. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.8V)

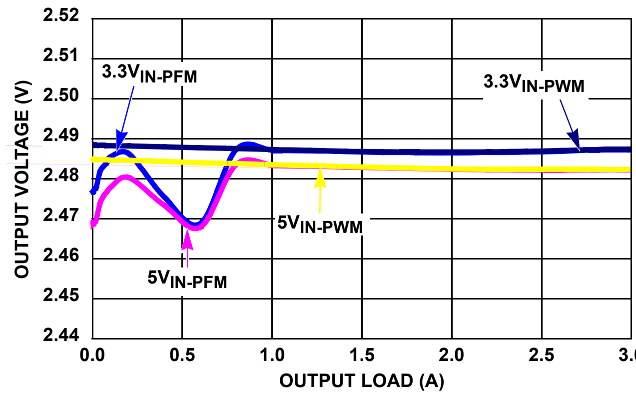


FIGURE 12. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 2.5V)

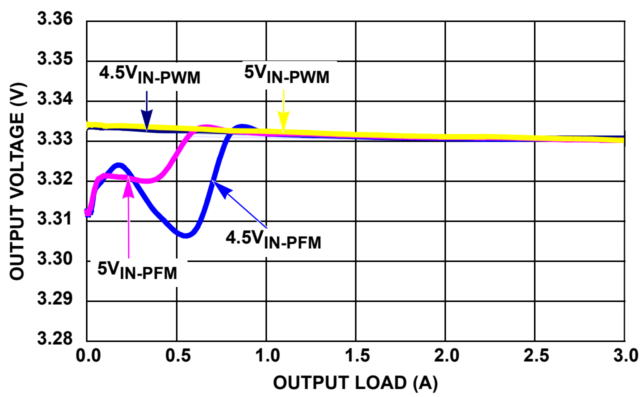


FIGURE 13. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 3.3V)

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A. **(Continued)**

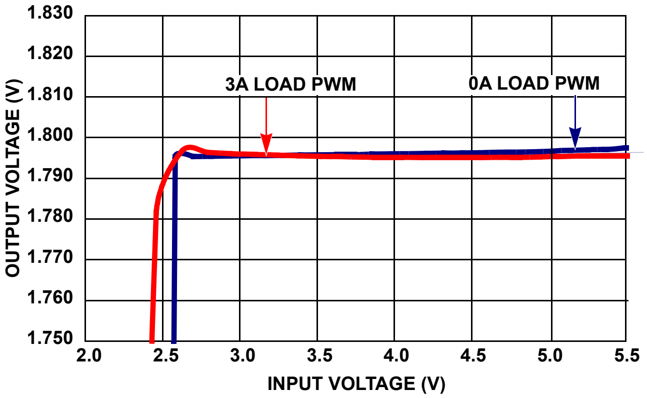


FIGURE 14. OUTPUT VOLTAGE REGULATION vs VIN (PWM V_{OUT} = 1.8)

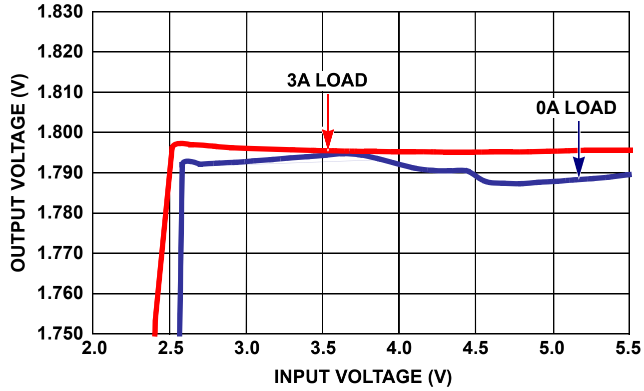


FIGURE 15. OUTPUT VOLTAGE REGULATION vs VIN (PFM V_{OUT} = 1.8V)

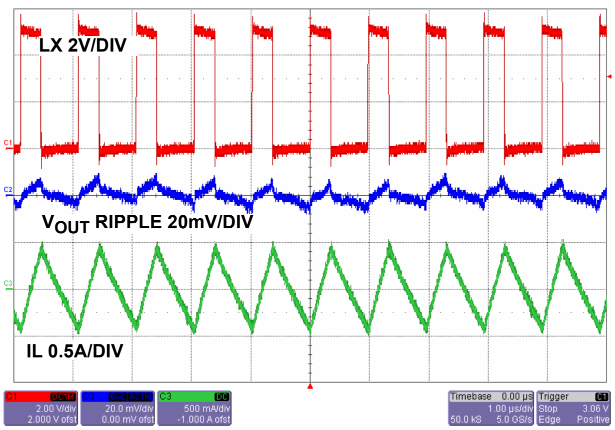


FIGURE 16. STEADY STATE OPERATION AT NO LOAD (PWM)

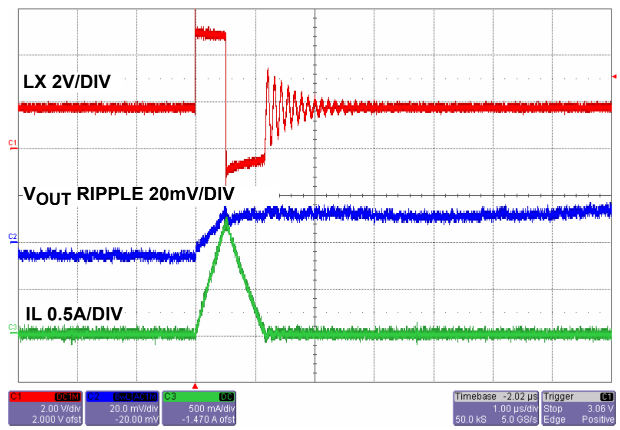


FIGURE 17. STEADY STATE OPERATION AT NO LOAD (PFM)

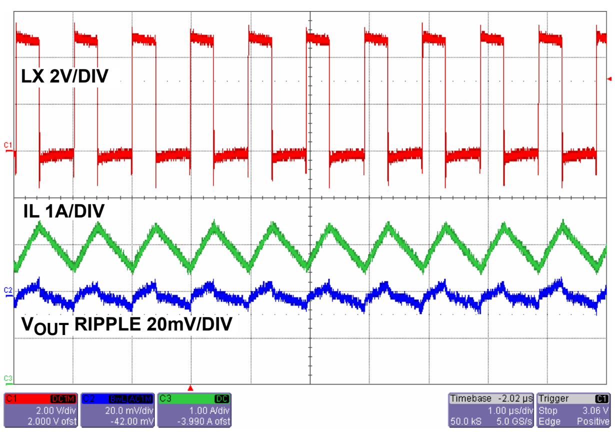


FIGURE 18. STEADY STATE OPERATION WITH FULL LOAD

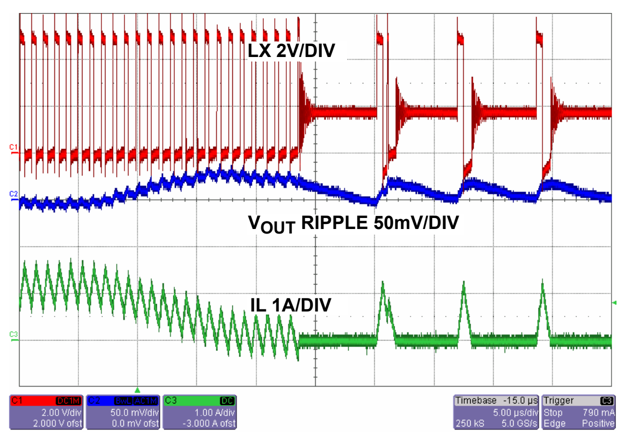


FIGURE 19. MODE TRANSITION CCM TO DCM

Typical Operating Performance Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A. (Continued)

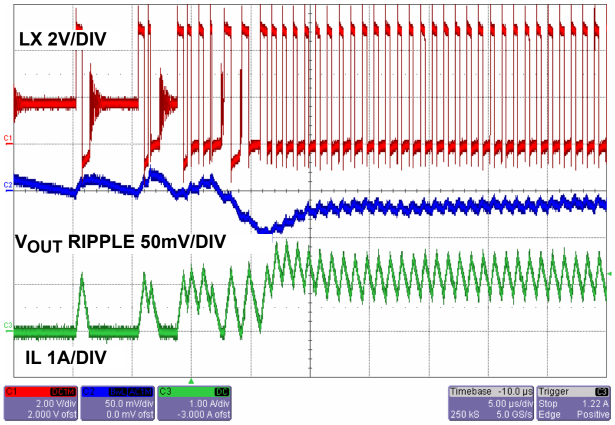


FIGURE 20. MODE TRANSITION DCM TO CCM

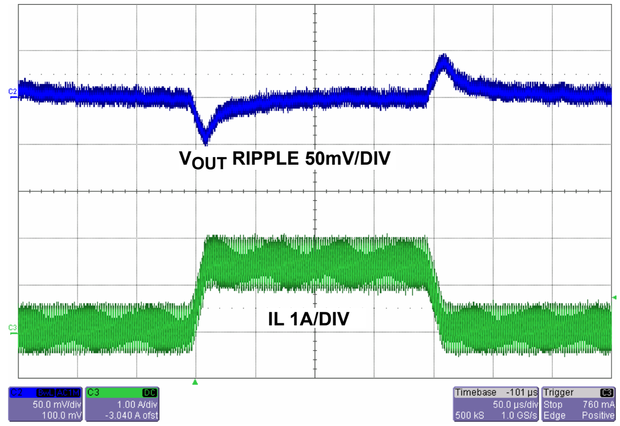


FIGURE 21. LOAD TRANSIENT (PWM)

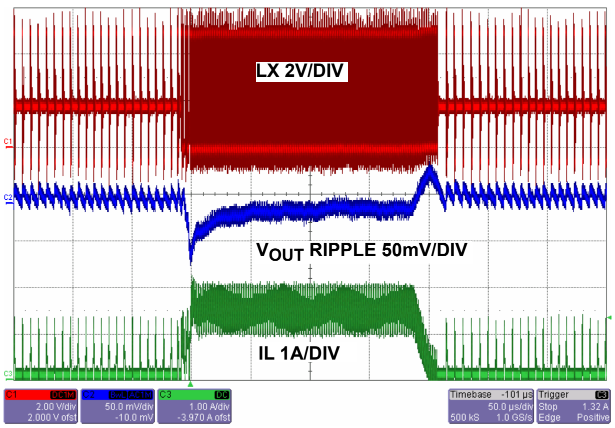


FIGURE 22. LOAD TRANSIENT (PFM)

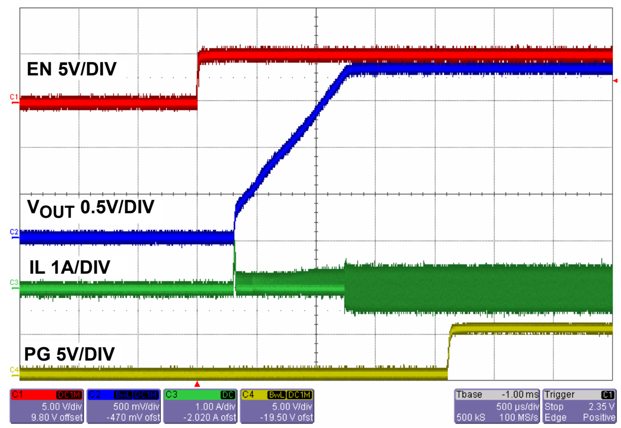


FIGURE 23. SOFT-START WITH NO LOAD (PWM)

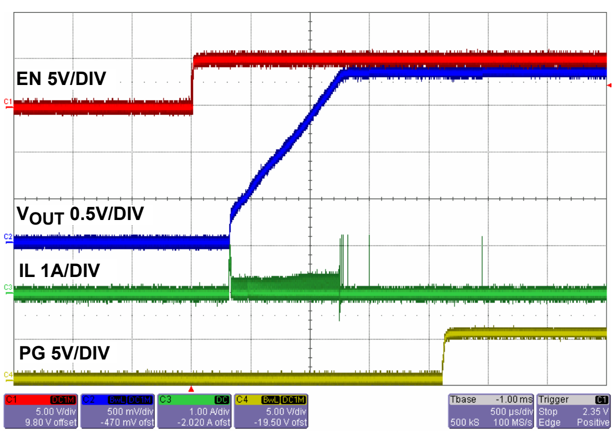


FIGURE 24. SOFT-START AT NO LOAD (PFM)

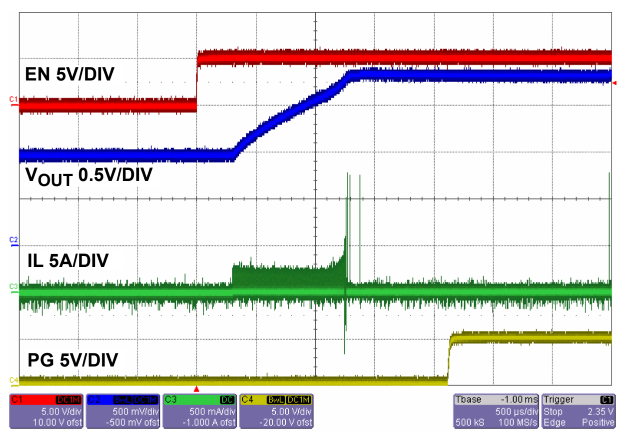


FIGURE 25. SOFT-START WITH PREBIASED 1V

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A. **(Continued)**

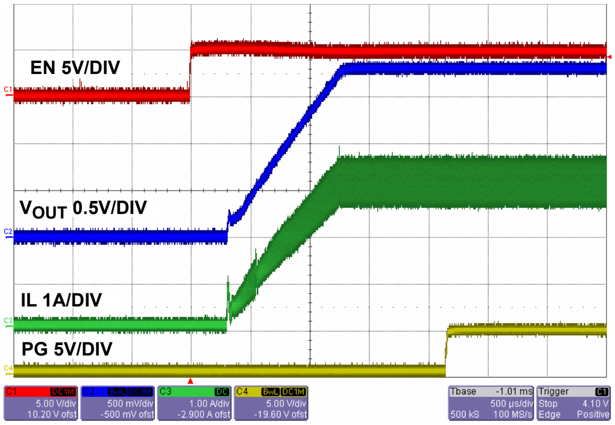


FIGURE 26. SOFT-START AT FULL LOAD

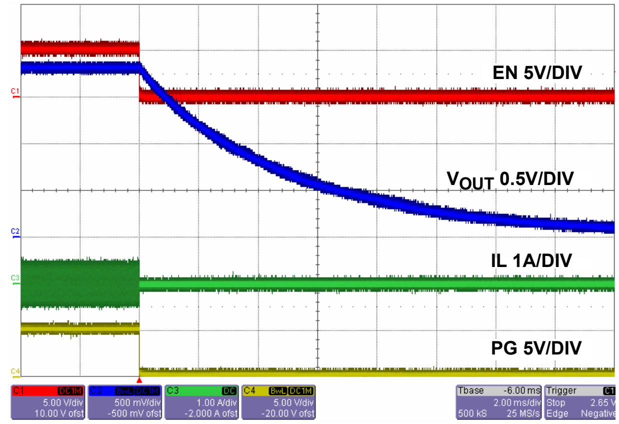


FIGURE 27. SOFT-DISCHARGE SHUTDOWN

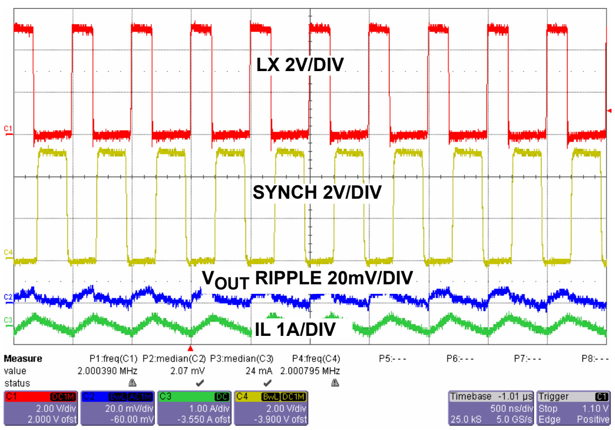


FIGURE 28. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 2MHz

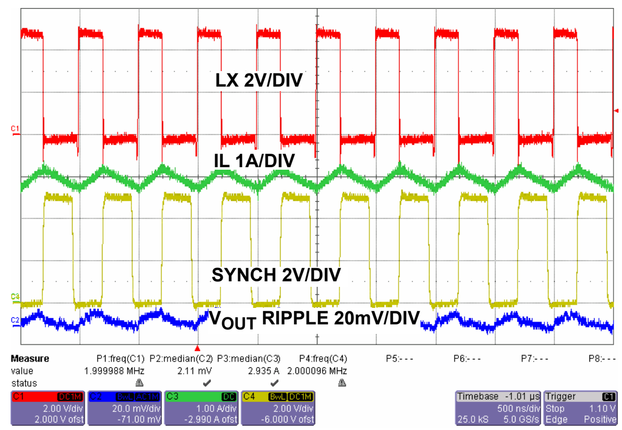


FIGURE 29. STEADY STATE OPERATION AT FULL LOAD WITH FREQUENCY = 2MHz

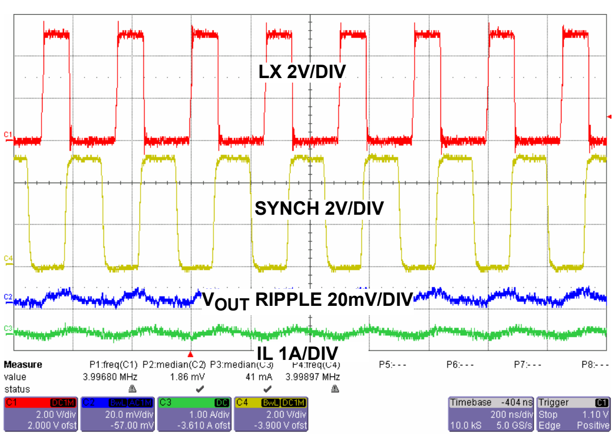


FIGURE 30. STEADY STATE OPERATION AT NO LOAD WITH FREQUENCY = 4MHz

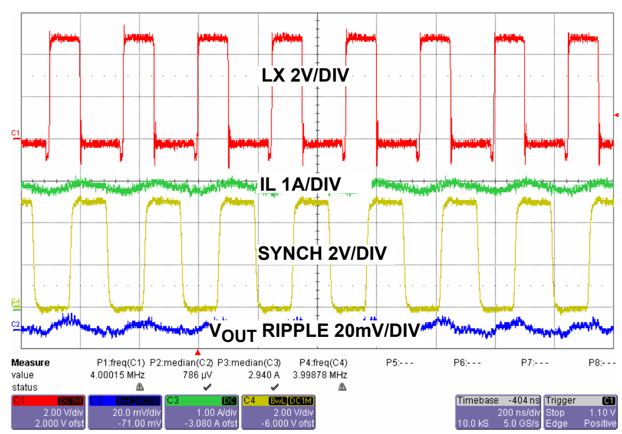


FIGURE 31. STEADY STATE OPERATION AT FULL LOAD (PWM) WITH FREQUENCY = 4MHz

Typical Operating Performance Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 2.5V to 5.5V, EN = V_{IN}, SYNCH = 0V, L = 1.5µH, C_1 = 2x22µF, C_2 = 2x22µF, I_{OUT} = 0A to 3A. **(Continued)**

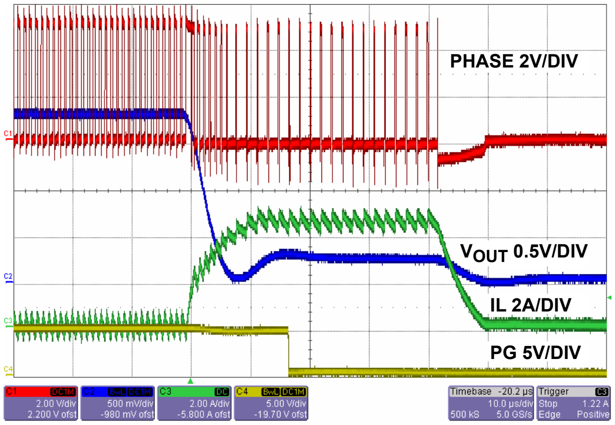


FIGURE 32. OUTPUT SHORT-CIRCUIT

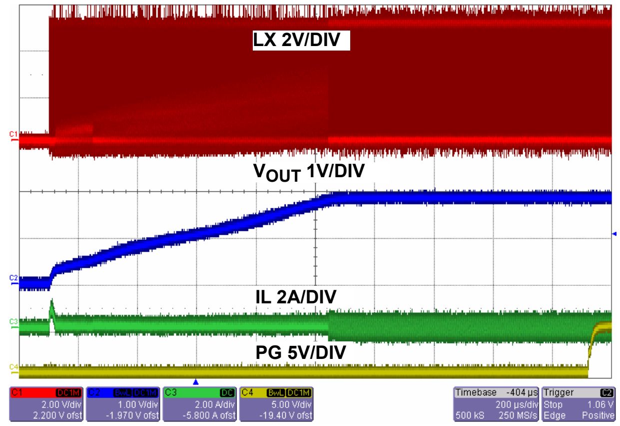


FIGURE 33. OUTPUT SHORT-CIRCUIT RECOVERY

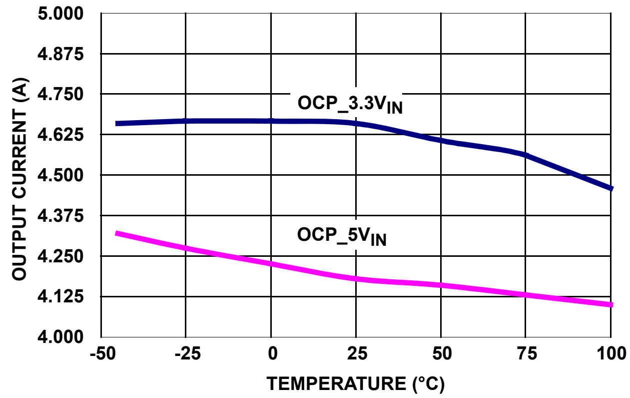


FIGURE 34. OUTPUT CURRENT LIMIT vs TEMPERATURE

Theory of Operation

The ISL8013A is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1MHz fixed switching frequency under heavy load conditions to allow smaller external inductors and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current, when the output is not loaded, is typically only 35µA. The supply current is typically only 0.1µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNCH pin HI (>2.5V) forces the converter into PWM mode, regardless of output current. The ISL8013A employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 2 shows the block diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The gain for the current sensing circuit is typically 250mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation (237mV/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and turn on the N-Channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 35 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 390kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

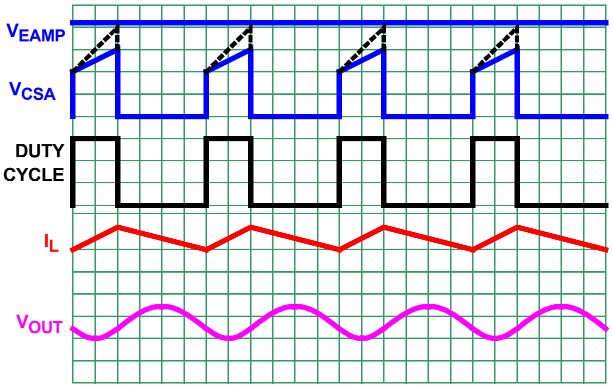


FIGURE 35. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the SYNCH pin LO (<0.4V) forces the converter into PFM mode. The ISL8013A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 36 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 2 monitors the N-MOSFET current for zero crossing. When 8 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the skip mode. During the eight detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 2. Each pulse cycle is still synchronized by the PWM clock. The P-MOSFET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak skip current limit value. Then the inductor current is discharging to 0A and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-MOSFET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Synchronization Control

The frequency of operation can be synchronized up to 4MHz by an external signal applied to the SYNCH pin. The falling edge on the SYNCH triggers the rising edge of the LX pulse. Make sure that the minimum on time of the LX node is greater than 140ns.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 2. The current sensing circuit has a gain of 250mV/A, from the P-MOSFET current to the CSA output. When the CSA output reaches 1.4V, which is equivalent to 4.8A for the switch current, the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of four soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of four soft-start periods, the output will resume back into regulation point after hiccup mode expires.

Short-Circuit Protection

The short-circuit protection SCP comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

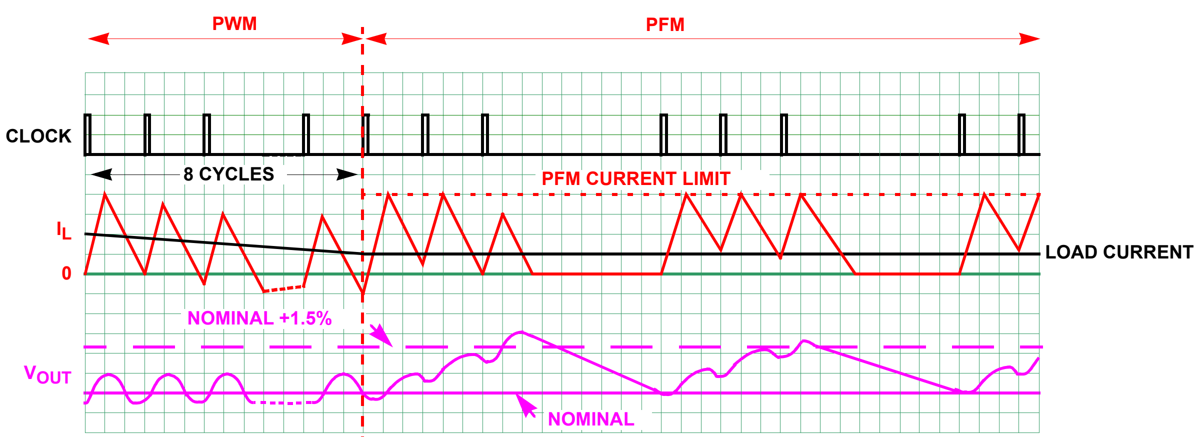


FIGURE 36. SKIP MODE OPERATION WAVEFORMS

PG

During power-up, the open-drain power-good output holds low for about 1ms after V_{OUT} reaches the regulation voltage. The PG output also serves as a 1ms delayed the power-good signal when the pull-up resistor R_1 is installed.

UVLO

When the input voltage is below the undervoltage lockout (UVLO) threshold, the regulator is disabled. To adjust the voltage level of power on and UVLO, use a resistive divider across EN. The input voltage programming resistor R_4 will depend on the bottom resistor R_5, as referred to in Figure 37. The value of R_5 is typically between 10kΩ and 100kΩ.

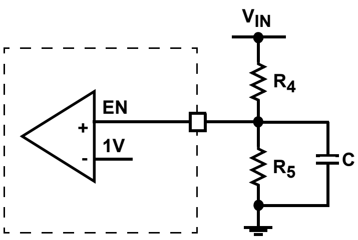


FIGURE 37. EXTERNAL RESISTOR DIVIDER

Soft Start-up

The soft start-up reduces the in-rush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed so that the output voltage rises in a controlled fashion. When VFB is less than 0.2V at the beginning of the soft-start, the switching frequency is reduced to 1/3 of the nominal value so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the SKIP mode to support prebiased output conditions.

Enable

The enable (EN) input allows the user to control the turning on or off the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft-start-up begins. It is recommended that the EN voltage should be kept logic low (less than 400mV), until V_{IN} reaches 2.5V. Refer to Figures 37 and 38 for suggested circuit implementation with V_{IN} slew rate.

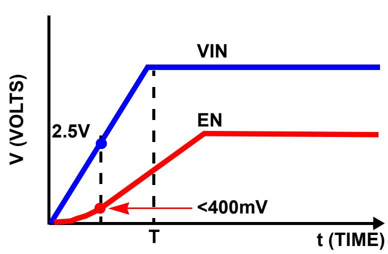


FIGURE 38. CIRCUIT IMPLEMENTATION WITH V_{IN} SLEW RATE

Let T equal the rise time of V_{IN}. Select the ratio of R_5 and R_4 such that the voltage is 1.4V (minimum enable logic high threshold) when V_{IN} is equal to or greater than 2.5V. Set R_5 between 10kΩ to 100kΩ, and use Equation 1 to determine R_4:

$$R_4 = \frac{R_5 \cdot (V_{IN} - 1.4V)}{1.4V} \quad \text{(EQ. 1)}$$

Where V_{IN} is greater than or equal to 2.5V.

Then select C such that the equivalent time constant is at least 2x the rise time, T. This will delay the EN voltage enough so that the overall EN voltage is less than 400mV by the time V_{IN} reaches 2.5V. Use Equation 2 to get C:

$$C \geq \frac{2 \bullet T}{R_4 \| R_5} \quad \text{(EQ. 2)}$$

Where T is the rise time of V_{IN}

As an example, let V_{IN} = 5V with rise time, T = 10ms. Then R_4 = 56.2kΩ, R_5 = 71.5kΩ, and C = 0.68µF are used to insure that V_{IN} was >2.5V and the EN voltage was <400mV.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the V_{IN} UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-MOSFET is typically 50mΩ and the ON-resistance for the N-MOSFET is typically 50mΩ.

100% Duty Cycle

The ISL8013A features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8013A can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shutdown

The ISL8013A has built-in thermal protection. When the internal temperature reaches +140°C, the regulator is completely shut down. As the temperature drops to +115°C, the ISL8013A resumes operation by stepping through the soft-start.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, ISL8013A typically uses a 1.5µH output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 3:

$$\Delta I = \frac{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_S} \quad \text{(EQ. 3)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8013A protects the typical peak current 4.8A. The saturation current needs be over 5.5A for maximum output current applications.

ISL8013A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 1. In Table 1, the minimum output capacitor value is given for the different output voltage to make sure that the whole converter system is stable. Additional output capacitance should be added for better performances in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

TABLE 1. OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT} (V)	C_{OUT} (µF)	L (µH)
0.8	2 x 22	1.0~2.2
1.2	2 x 22	1.0~2.2
1.5	2 x 22	1.5~3.3
1.8	2 x 22	1.5~3.3
2.5	2 x 22	1.5~3.3
3.3	2 x 22	2.2~4.7
3.6	2 x 22	2.2~4.7

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier (see Figure 1).

The output voltage programming resistor, R_3, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 4.

$$R_3 = \frac{R_2 \cdot 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 4)}$$

If the output voltage desired is 0.8V, then R_3 is left unpopulated and R_2 is shorted. There is a leakage current from VIN to LX. It is recommended to preload the output with 10µA minimum. For better performance, add 47pF in parallel with R_2 (100kΩ).

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. Two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Revision History

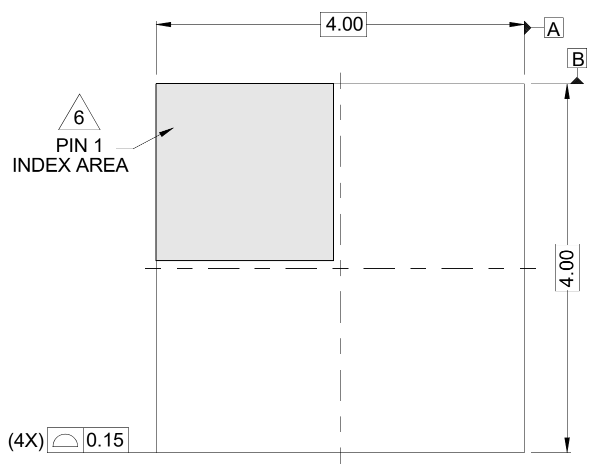
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Dec 3, 2021	2.01	Removed About Intersil section. Updated Ordering Information table format and notes. Updated Pin 6 description.
Nov 17, 2014	2.00	Added more information to section “Enable” on page 14. Added more information to section “UVLO” on page 14.
Jul 24, 2014	1.00	Converted to new datasheet template. Updated Tape & Reel note in “Ordering Information” table from "Add “-T” suffix for tape and reel." to new standard "Add “-T*” suffix for tape and reel." The "*" covers all possible tape and reel options. Added Evaluation board information to the Ordering Information table. Replaced Figure 6 on page 7, Figure 7 on page 7 and Figure 11 on page 8 with the new data curves. Removed Figure 9 (POWER DISSIPATION WITH NO LOAD vs VIN (PFM VOUT = 1.8V).
Nov 25, 2009	0.00	Initial Release.

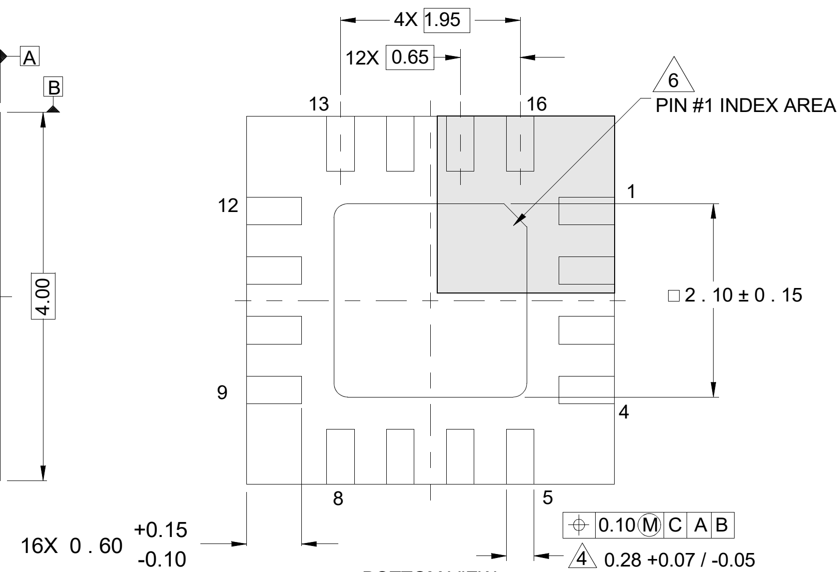
Package Outline Drawing

For the most recent package outline drawing, see L16.4x4.

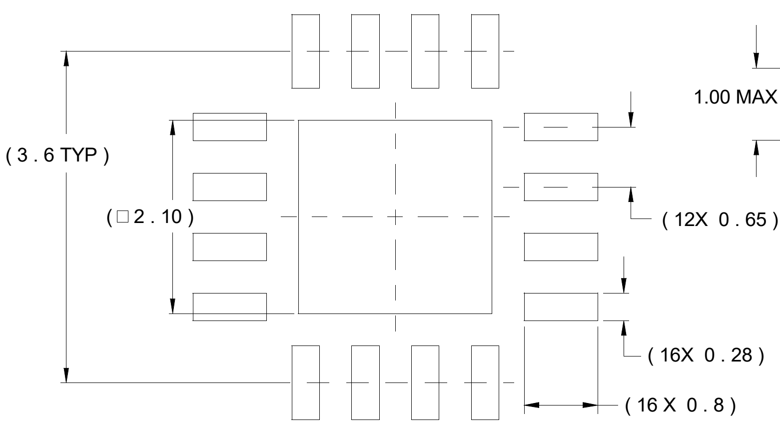
L16.4x4
16 Lead Quad Flat No-Lead Plastic Package
Rev 6, 02/08



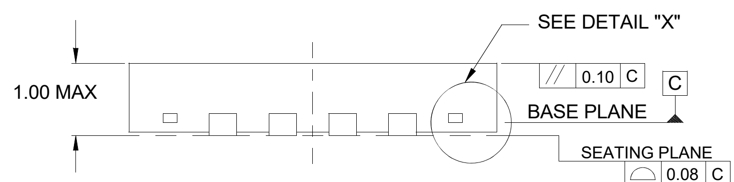
TOP VIEW



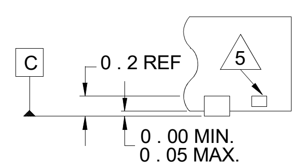
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.